

# NCP5104

## High Voltage, Half Bridge Driver

The NCP5104 is a High Voltage Power gate Driver providing two outputs for direct drive of 2 N-channel power MOSFETs or IGBTs arranged in a half-bridge configuration. It uses the bootstrap technique to insure a proper drive of the High-side power switch.

### Features

- High Voltage Range: up to 600 V
- $dV/dt$  Immunity  $\pm 50$  V/nsec
- Gate Drive Supply Range from 10 V to 20 V
- High and Low Drive Outputs
- Output Source / Sink Current Capability 250 mA / 500 mA
- 3.3 V and 5 V Input Logic Compatible
- Up to  $V_{CC}$  Swing on Input Pins
- Extended Allowable Negative Bridge Pin Voltage Swing to  $-10$  V for Signal Propagation
- Matched Propagation Delays between Both Channels
- 1 Input with Internal Fixed Dead Time (520 ns)
- Under  $V_{CC}$  LockOut (UVLO) for Both Channels
- Pin to Pin Compatible with Industry Standards
- These are Pb-Free Devices

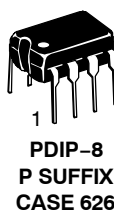
### Typical Applications

- Half-Bridge Power Converters

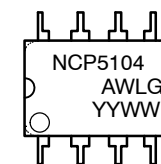
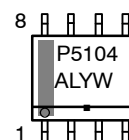


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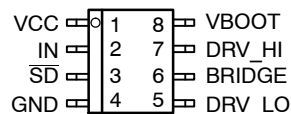


### MARKING DIAGRAMS



NCP5104 = Specific Device Code  
A = Assembly Location  
L or WL = Wafer Lot  
Y or YY = Year  
W or WW = Work Week  
G or ■ = Pb-Free Package

### PINOUT INFORMATION



8 Pin Package

### ORDERING INFORMATION

| Device      | Package             | Shipping†          |
|-------------|---------------------|--------------------|
| NCP5104PG   | PDIP-8<br>(Pb-Free) | 50 Units / Rail    |
| NCP5104DR2G | SOIC-8<br>(Pb-Free) | 2500 / Tape & Reel |

† For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

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The schematic diagram illustrates the UV protection circuit for the DRV8833 motor driver. It features two input pins: IN and SD. The IN pin is connected to a pull-up resistor to VCC and a pull-down resistor to GND. The SD pin is connected to a pull-up resistor to VCC and a pull-down resistor to GND. The circuit includes a UV DETECT block, a DEAD TIME GENERATION block, a PULSE TRIGGER block, a LEVEL SHIFTER block, a DELAY block, and an S-Q-R-Q flip-flop. The UV DETECT block is connected to VCC and GND. The DEAD TIME GENERATION block is connected to the IN pin and the SD pin. The PULSE TRIGGER block is connected to the output of the DEAD TIME GENERATION block. The LEVEL SHIFTER block is connected to the output of the PULSE TRIGGER block and GND. The DELAY block is connected to the output of the LEVEL SHIFTER block. The S-Q-R-Q flip-flop is connected to the output of the DELAY block and the output of the UV DETECT block. The output of the flip-flop is connected to the DRV\_HI pin. The output of the DELAY block is connected to the DRV\_LO pin. The circuit also includes a VBOOT pin, a BRIDGE pin, and a GND pin.

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# NCP5104

## PIN DESCRIPTION

| Pin Name               | Description                                          |
|------------------------|------------------------------------------------------|
| V <sub>CC</sub>        | Low Side and Main Power Supply                       |
| IN                     | Logic Input                                          |
| $\overline{\text{SD}}$ | Logic Input for Shutdown                             |
| GND                    | Ground                                               |
| DRV_LO                 | Low Side Gate Drive Output                           |
| V <sub>BOOT</sub>      | Bootstrap Power Supply                               |
| DRV_HI                 | High Side Gate Drive Output                          |
| BRIDGE                 | Bootstrap Return or High Side Floating Supply Return |

## MAXIMUM RATINGS

| Rating                               | Symbol                                                                                                                                    | Value                                                   | Unit    |
|--------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------|---------|
| V <sub>CC</sub>                      | Main power supply voltage                                                                                                                 | –0.3 to 20                                              | V       |
| V <sub>CC_transient</sub>            | Main transient power supply voltage:<br>I <sub>V<sub>CC_max</sub></sub> = 5 mA during 10 ms                                               | 23                                                      | V       |
| V <sub>BOOT</sub>                    | VHV: High Voltage BOOT Pin                                                                                                                | –1 to 620                                               | V       |
| V <sub>BRIDGE</sub>                  | VHV: High Voltage BRIDGE pin                                                                                                              | –1 to 600                                               | V       |
| V <sub>BRIDGE</sub>                  | Allowable Negative Bridge Pin Voltage for IN Signal Propagation to DRV_LO                                                                 | –10                                                     | V       |
| V <sub>BOOT-V<sub>BRIDGE</sub></sub> | VHV: Floating supply voltage                                                                                                              | –0.3 to 20                                              | V       |
| V <sub>DRV_HI</sub>                  | VHV: High side output voltage                                                                                                             | V <sub>BRIDGE</sub> – 0.3 to<br>V <sub>BOOT</sub> + 0.3 | V       |
| V <sub>DRV_LO</sub>                  | Low side output voltage                                                                                                                   | –0.3 to V <sub>CC</sub> + 0.3                           | V       |
| dV <sub>BRIDGE</sub> /dt             | Allowable output slew rate                                                                                                                | 50                                                      | V/ns    |
| V <sub>IN</sub> , V <sub>SD</sub>    | Inputs IN & SD                                                                                                                            | –1.0 to V <sub>CC</sub> + 0.3                           | V       |
|                                      | ESD Capability:<br>– HBM model (all pins except pins 6–7–8 in 8)<br>– Machine model (all pins except pins 6–7–8)                          | 2<br>200                                                | kV<br>V |
|                                      | Latch up capability per JEDEC JESD78                                                                                                      |                                                         |         |
| R <sub>θJA</sub>                     | Power dissipation and Thermal characteristics<br>PDIP–8: Thermal Resistance, Junction–to–Air<br>SO–8: Thermal Resistance, Junction–to–Air | 100<br>178                                              | °C/W    |
| T <sub>ST</sub>                      | Storage Temperature Range                                                                                                                 | –55 to +150                                             | °C      |
| T <sub>J_max</sub>                   | Maximum Operating Junction Temperature                                                                                                    | +150                                                    | °C      |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

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**ELECTRICAL CHARACTERISTIC** ( $V_{CC} = V_{boot} = 15\text{ V}$ ,  $V_{GND} = V_{bridge}$ ,  $-40^{\circ}\text{C} < T_J < 125^{\circ}\text{C}$ , Outputs loaded with 1 nF)

| Rating | Symbol | $T_J -40^{\circ}\text{C to } 125^{\circ}\text{C}$ |     |     | Units |
|--------|--------|---------------------------------------------------|-----|-----|-------|
|        |        | Min                                               | Typ | Max |       |

## OUTPUT SECTION

|                                                                                                            |                 |   |     |     |          |
|------------------------------------------------------------------------------------------------------------|-----------------|---|-----|-----|----------|
| Output high short circuit pulsed current $V_{DRV} = 0\text{ V}$ , $PW \leq 10\text{ }\mu\text{s}$ (Note 1) | $I_{DRVsource}$ | – | 250 | –   | mA       |
| Output low short circuit pulsed current $V_{DRV} = V_{CC}$ , $PW \leq 10\text{ }\mu\text{s}$ (Note 1)      | $I_{DRVsink}$   | – | 500 | –   | mA       |
| Output resistor (Typical value @ $25^{\circ}\text{C}$ ) Source                                             | $R_{OH}$        | – | 30  | 60  | $\Omega$ |
| Output resistor (Typical value @ $25^{\circ}\text{C}$ ) Sink                                               | $R_{OL}$        | – | 10  | 20  | $\Omega$ |
| High level output voltage, $V_{BIAS} - V_{DRV\_XX}$ @ $I_{DRV\_XX} = 20\text{ mA}$                         | $V_{DRV\_H}$    | – | 0.7 | 1.6 | V        |
| Low level output voltage $V_{DRV\_XX}$ @ $I_{DRV\_XX} = 20\text{ mA}$                                      | $V_{DRV\_L}$    | – | 0.2 | 0.6 | V        |

## DYNAMIC OUTPUT SECTION

|                                                                                                   |               |     |     |     |    |
|---------------------------------------------------------------------------------------------------|---------------|-----|-----|-----|----|
| Turn-on propagation delay ( $V_{bridge} = 0\text{ V}$ ) (Note 2)                                  | $t_{ON}$      | –   | 620 | 800 | ns |
| Turn-off propagation delay ( $V_{bridge} = 0\text{ V}$ or $50\text{ V}$ ) (Note 3)                | $t_{OFF}$     | –   | 100 | 170 | ns |
| Shutdown propagation delay, when Shutdown is enabled                                              | $t_{sd\_en}$  | –   | 100 | 170 | ns |
| Shutdown propagation delay, when Shutdown is disabled                                             | $t_{sd\_dis}$ | –   | 620 | 800 | ns |
| Output voltage rise time (from 10% to 90% @ $V_{CC} = 15\text{ V}$ ) with 1 nF load               | $t_r$         | –   | 85  | 160 | ns |
| Output voltage fall time (from 90% to 10% @ $V_{CC} = 15\text{ V}$ ) with 1 nF load               | $t_f$         | –   | 35  | 75  | ns |
| Propagation delay matching between the High side and the Low side @ $25^{\circ}\text{C}$ (Note 4) | $\Delta t$    | –   | 10  | 45  | ns |
| Internal fixed dead time (Note 5)                                                                 | DT            | 400 | 520 | 650 | ns |

## INPUT SECTION

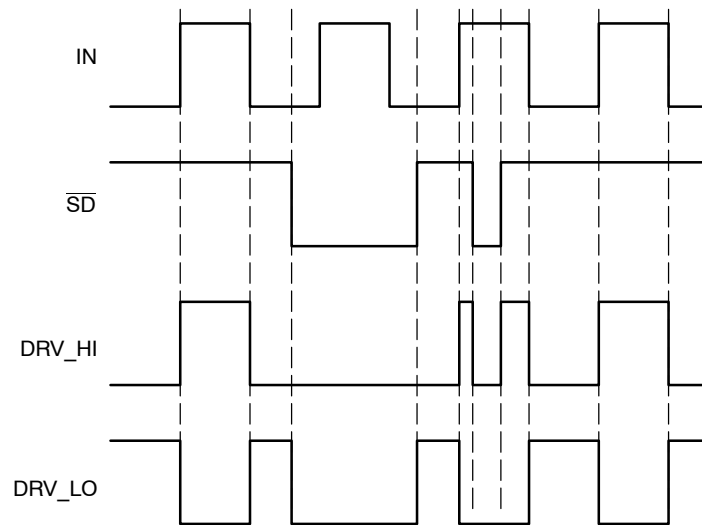
|                                                                             |           |     |     |     |               |
|-----------------------------------------------------------------------------|-----------|-----|-----|-----|---------------|
| Low level input voltage threshold                                           | $V_{IN}$  | –   | –   | 0.8 | V             |
| Input pull-down resistor ( $V_{IN} < 0.5\text{ V}$ )                        | $R_{IN}$  | –   | 200 | –   | k $\Omega$    |
| High level input voltage threshold                                          | $V_{IN}$  | 2.3 | –   | –   | V             |
| Logic “1” input bias current @ $V_{IN} = 5\text{ V}$ @ $25^{\circ}\text{C}$ | $I_{IN+}$ | –   | 5   | 25  | $\mu\text{A}$ |
| Logic “0” input bias current @ $V_{IN} = 0\text{ V}$ @ $25^{\circ}\text{C}$ | $I_{IN-}$ | –   | –   | 2.0 | $\mu\text{A}$ |

## SUPPLY SECTION

|                                                                                                                    |                    |     |     |     |               |
|--------------------------------------------------------------------------------------------------------------------|--------------------|-----|-----|-----|---------------|
| Vcc UV Start-up voltage threshold                                                                                  | $V_{cc\_stup}$     | 8.0 | 8.9 | 9.8 | V             |
| Vcc UV Shut-down voltage threshold                                                                                 | $V_{cc\_shtdwn}$   | 7.3 | 8.2 | 9.0 | V             |
| Hysteresis on Vcc                                                                                                  | $V_{cc\_hyst}$     | 0.3 | 0.7 | –   | V             |
| Vboot Start-up voltage threshold reference to bridge pin ( $V_{boot\_stup} = V_{boot} - V_{bridge}$ )              | $V_{boot\_stup}$   | 8.0 | 8.9 | 9.8 | V             |
| Vboot UV Shut-down voltage threshold                                                                               | $V_{boot\_shtdwn}$ | 7.3 | 8.2 | 9.0 | V             |
| Hysteresis on Vboot                                                                                                | $V_{boot\_shtdwn}$ | 0.3 | 0.7 | –   | V             |
| Leakage current on high voltage pins to GND ( $V_{BOOT} = V_{BRIDGE} = DRV\_HI = 600\text{ V}$ )                   | $I_{HV\_LEAK}$     | –   | 5   | 40  | $\mu\text{A}$ |
| Consumption in active mode ( $V_{cc} = V_{boot}$ , $f_{sw} = 100\text{ kHz}$ and 1 nF load on both driver outputs) | ICC1               | –   | 4   | 5   | mA            |
| Consumption in inhibition mode ( $V_{cc} = V_{boot}$ )                                                             | ICC2               | –   | 250 | 400 | $\mu\text{A}$ |
| Vcc current consumption in inhibition mode                                                                         | ICC3               | –   | 200 | –   | $\mu\text{A}$ |
| Vboot current consumption in inhibition mode                                                                       | ICC4               | –   | 50  | –   | $\mu\text{A}$ |

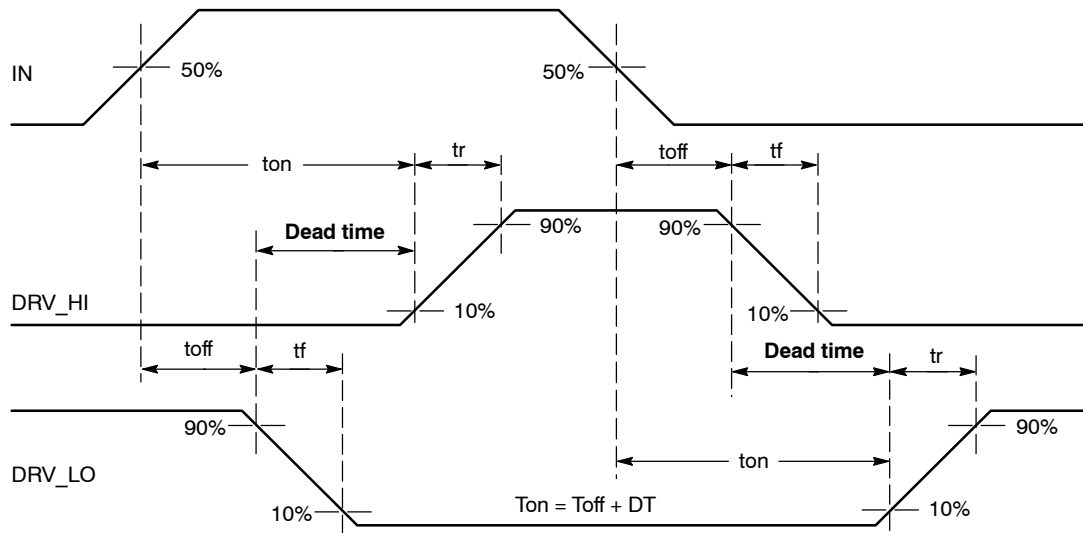
1. Parameter guaranteed by design.
2.  $T_{ON} = T_{OFF} + DT$
3. Turn-off propagation delay @  $V_{bridge} = 600\text{ V}$  is guaranteed by design.
4. See characterization curve for  $\Delta t$  parameters variation on the full range temperature.
5. Timing diagram definition see: Figure 4, Figure 5 and Figure 6.

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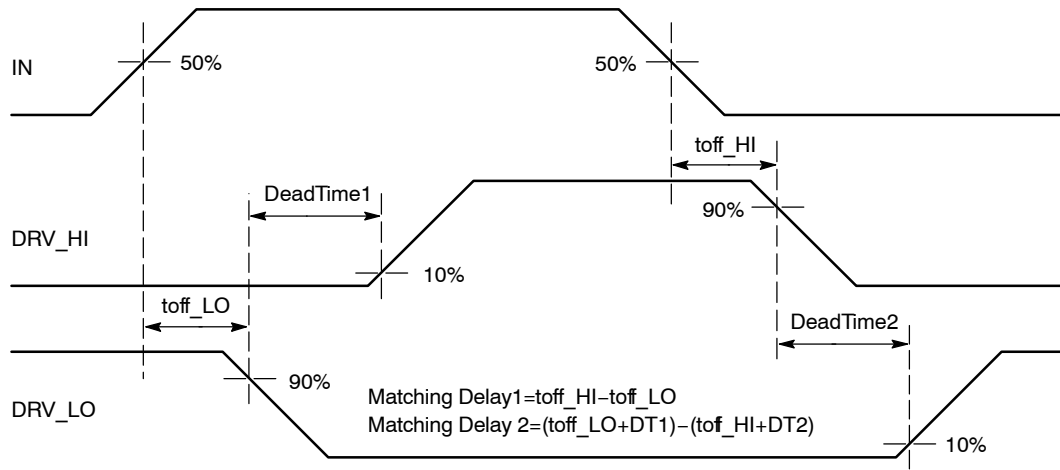
**Figure 4. Input/Output Timing Diagram**

Note: DRV\_HI output is in phase with the input

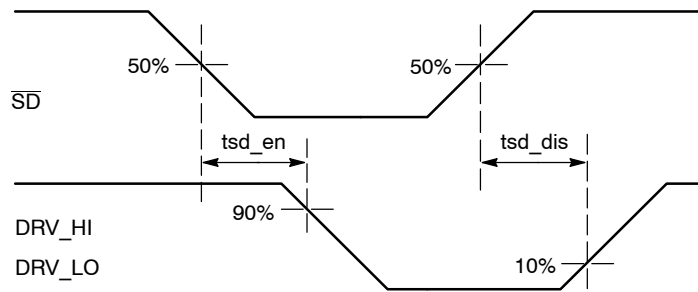


**Figure 5. Timing Definitions**

# NCP5104



**Figure 6. Matching Propagation Delay Definition**



**Figure 7. Shutdown Waveform Definition**

CHARACTERIZATION CURVES

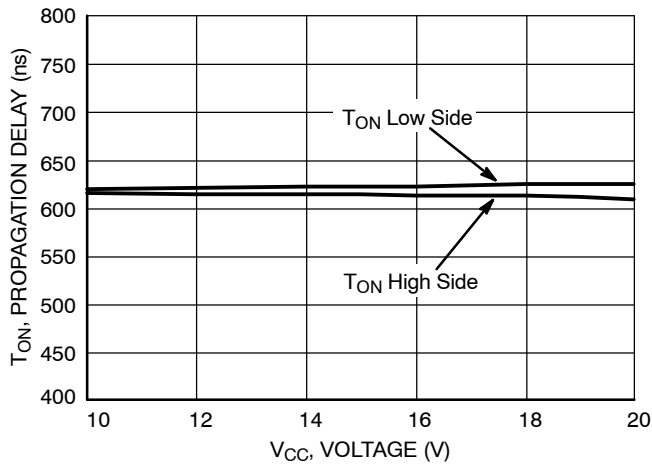


Figure 8. Turn ON Propagation Delay vs. Supply Voltage ( $V_{CC} = V_{BOOT}$ )

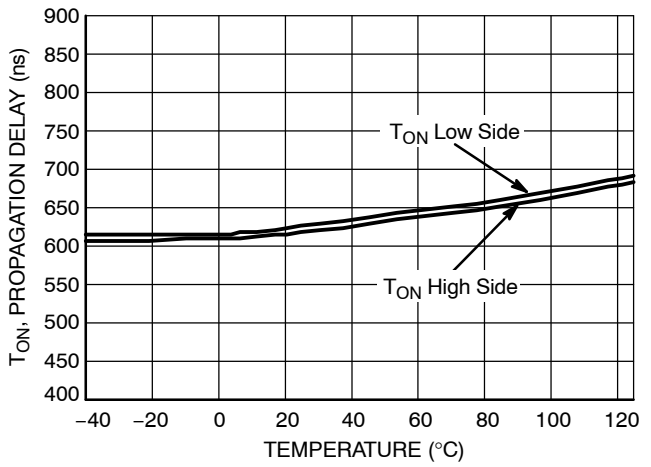


Figure 9. Turn ON Propagation Delay vs. Temperature

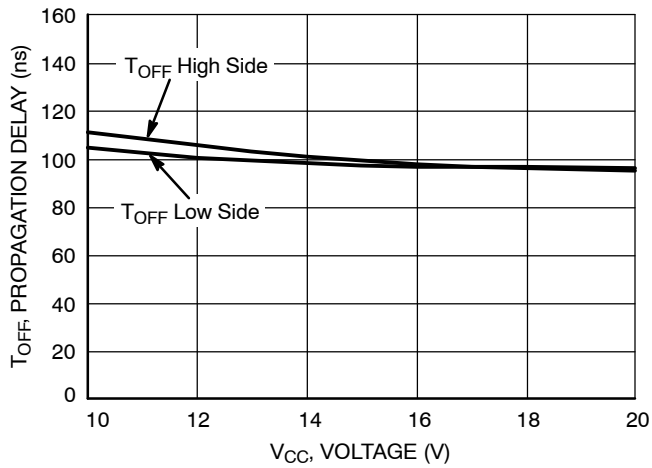


Figure 10. Turn OFF Propagation Delay vs. Supply Voltage ( $V_{CC} = V_{BOOT}$ )

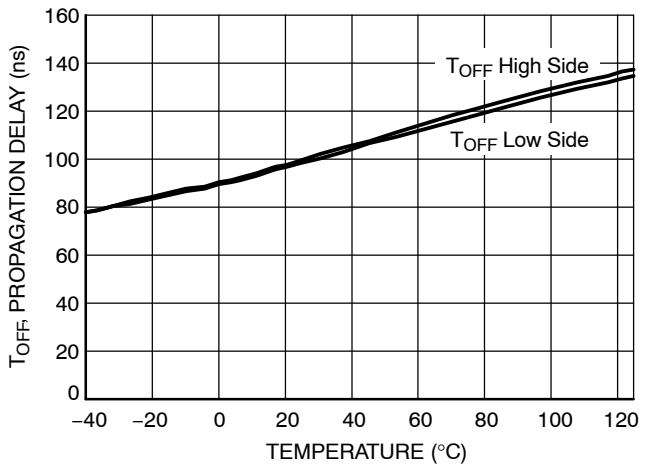


Figure 11. Turn OFF Propagation Delay vs. Temperature

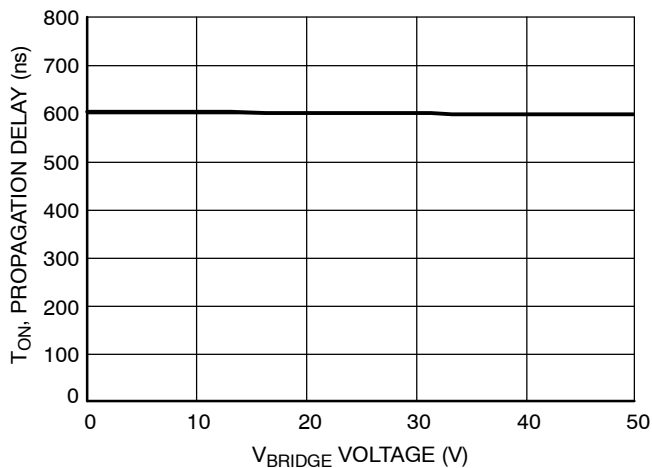


Figure 12. High Side Turn ON Propagation Delay vs.  $V_{BRIDGE}$  Voltage ( $V_{CC} = V_{BOOT}$ )

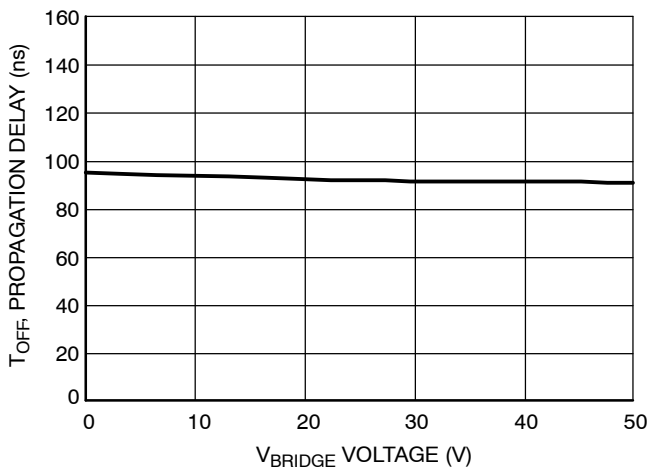


Figure 13. High Side Turn OFF Propagation Delay vs.  $V_{BRIDGE}$  Voltage ( $V_{CC} = V_{BOOT}$ )

## CHARACTERIZATION CURVES

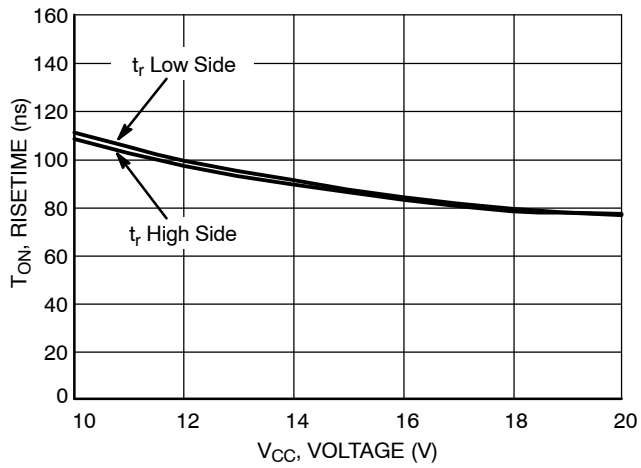


Figure 14. Turn ON Risettime vs. Supply Voltage ( $V_{CC} = V_{BOOT}$ )

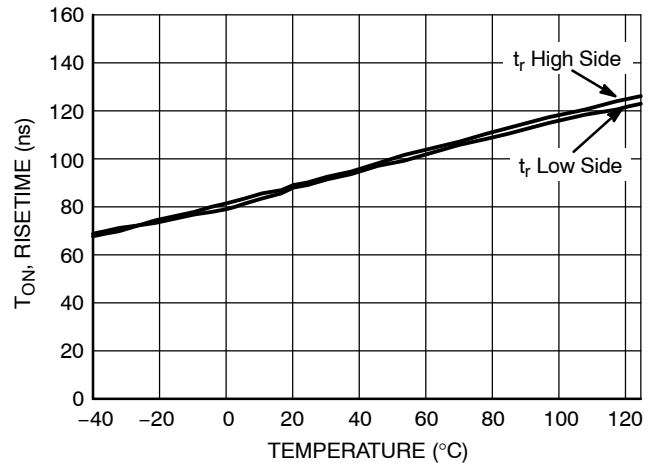


Figure 15. Turn ON Risettime vs. Temperature

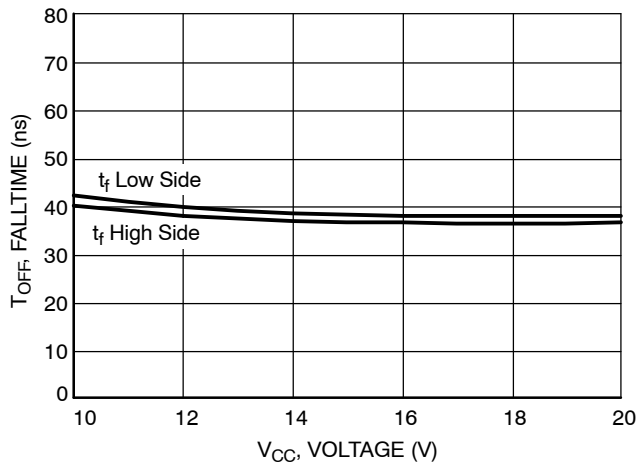


Figure 16. Turn OFF Falltime vs. Supply Voltage ( $V_{CC} = V_{BOOT}$ )

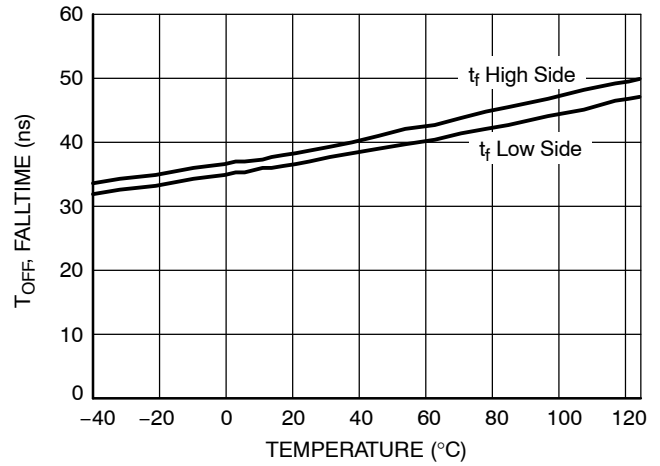


Figure 17. Turn OFF Falltime vs. Temperature

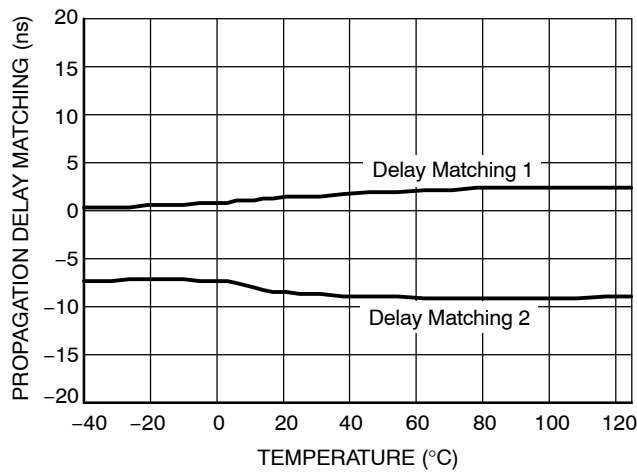


Figure 18. Propagation Delay Matching Between High Side and Low Side Driver vs. Temperature

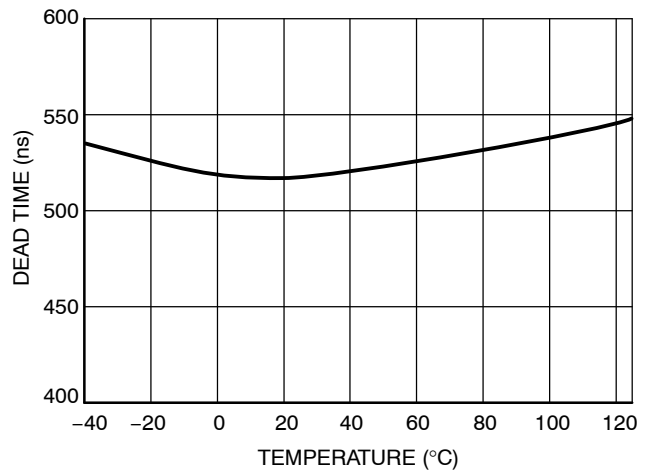


Figure 19. Dead Time vs. Temperature



CHARACTERIZATION CURVES

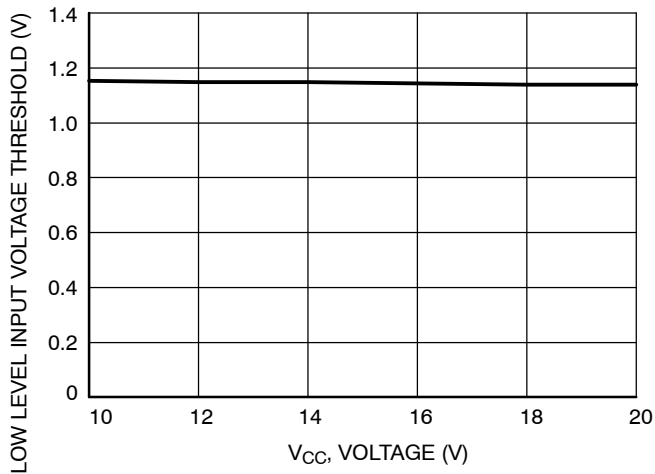


Figure 20. Low Level Input Voltage Threshold vs. Supply Voltage ( $V_{CC} = V_{BOOT}$ )

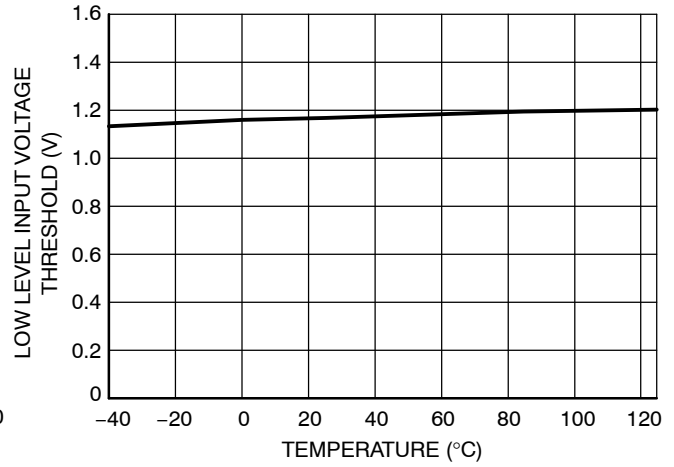


Figure 21. Low Level Input Voltage Threshold vs. Temperature

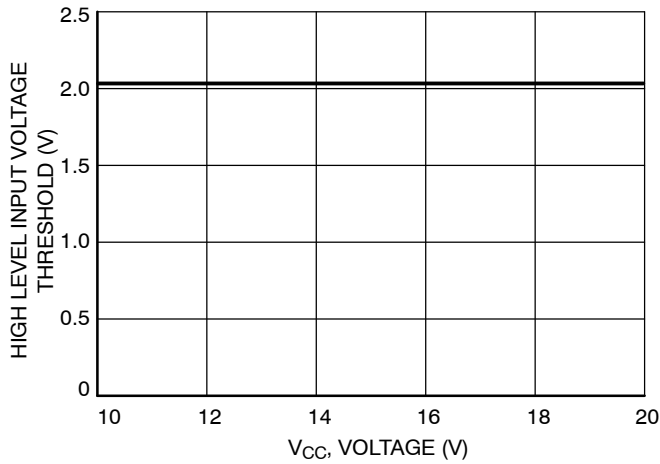


Figure 22. High Level Input Voltage Threshold vs. Supply Voltage ( $V_{CC} = V_{BOOT}$ )

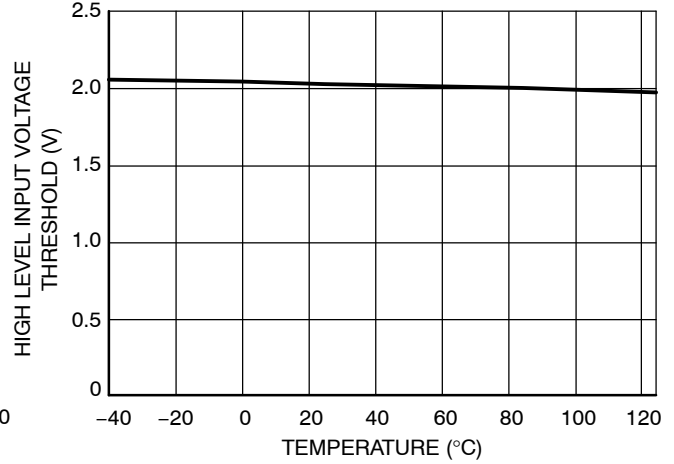


Figure 23. High Level Input Voltage Threshold vs. Temperature

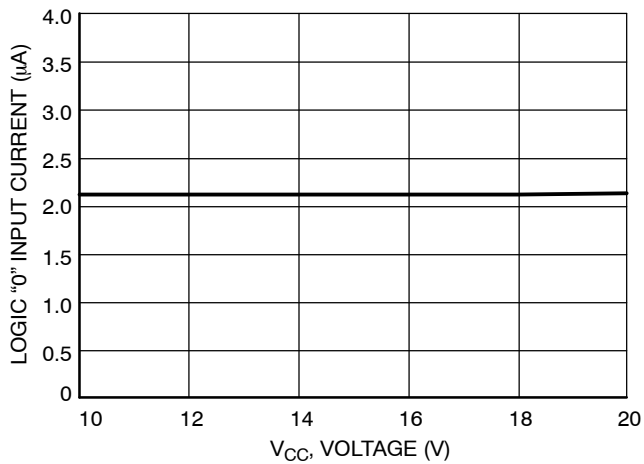


Figure 24. Logic "0" Input Current vs. Supply Voltage ( $V_{CC} = V_{BOOT}$ )

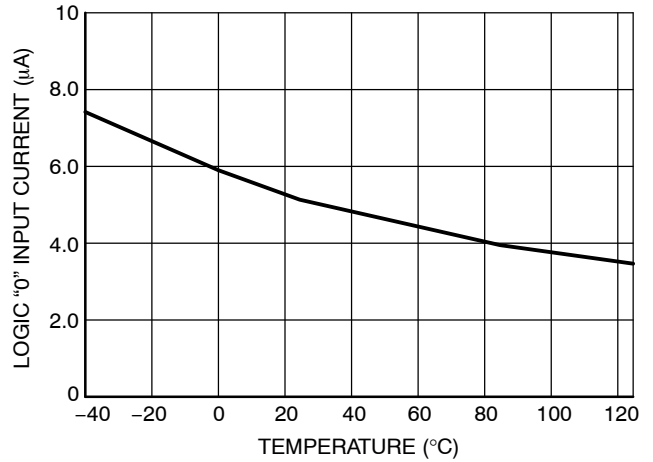


Figure 25. Logic "0" Input Current vs. Temperature

CHARACTERIZATION CURVES

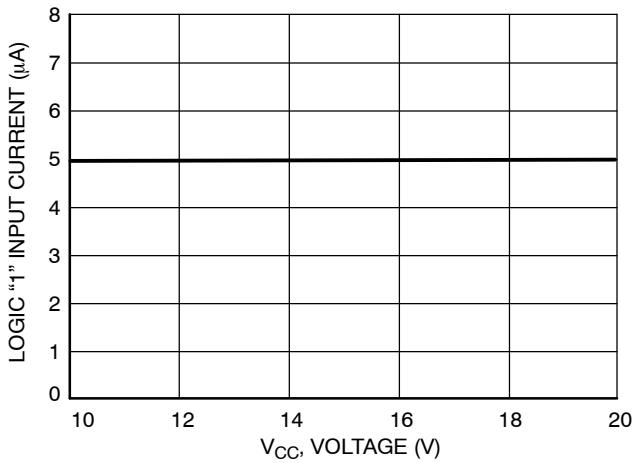


Figure 26. Logic "1" Input Current vs. Supply Voltage ( $V_{CC} = V_{BOOT}$ )

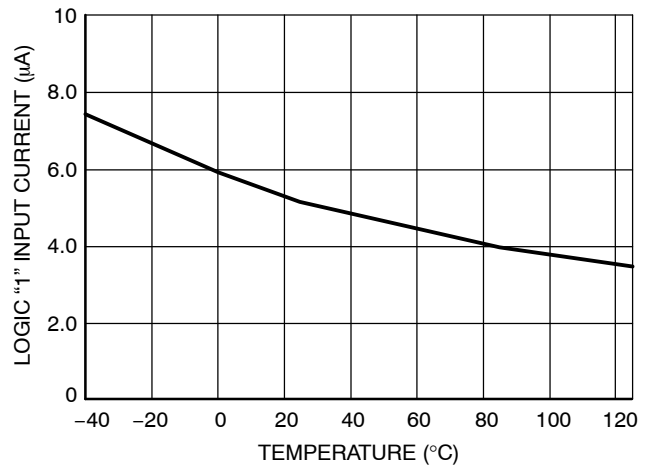


Figure 27. Logic "1" Input Current vs. Temperature

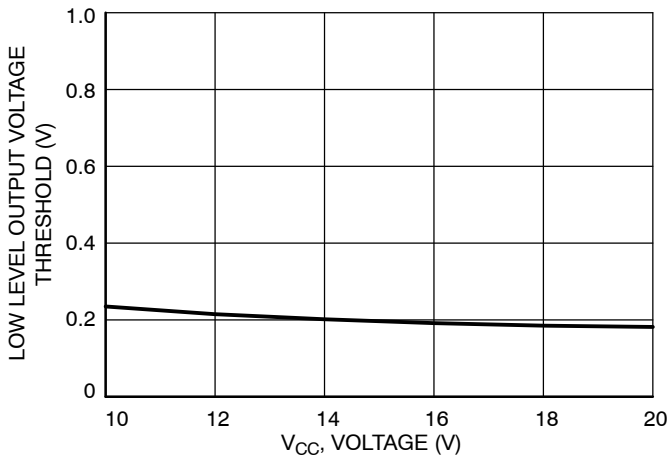


Figure 28. Low Level Output Voltage vs. Supply Voltage ( $V_{CC} = V_{BOOT}$ )

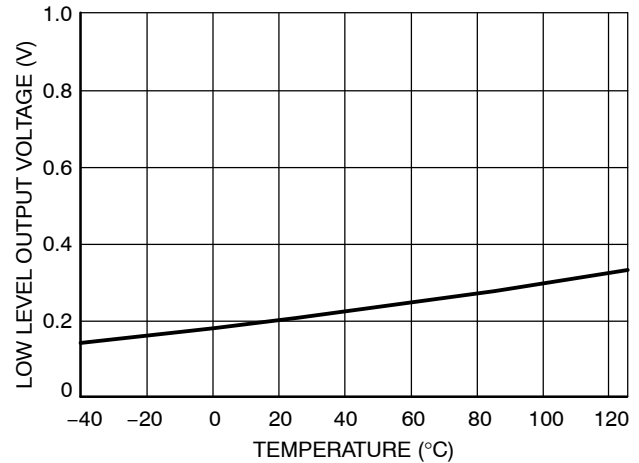


Figure 29. Low Level Output Voltage vs. Temperature

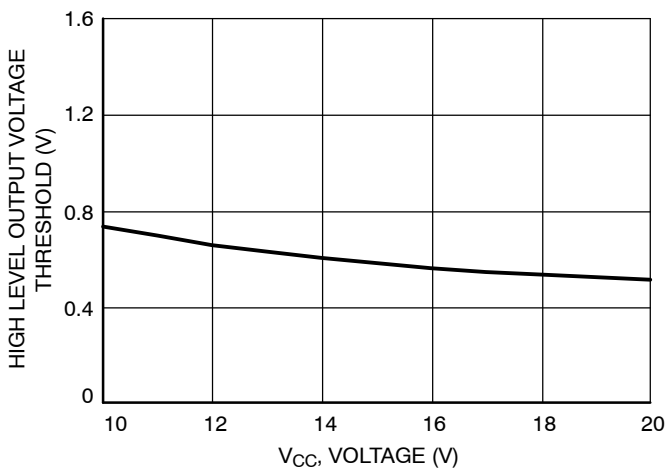


Figure 30. High Level Output Voltage vs. Supply Voltage ( $V_{CC} = V_{BOOT}$ )

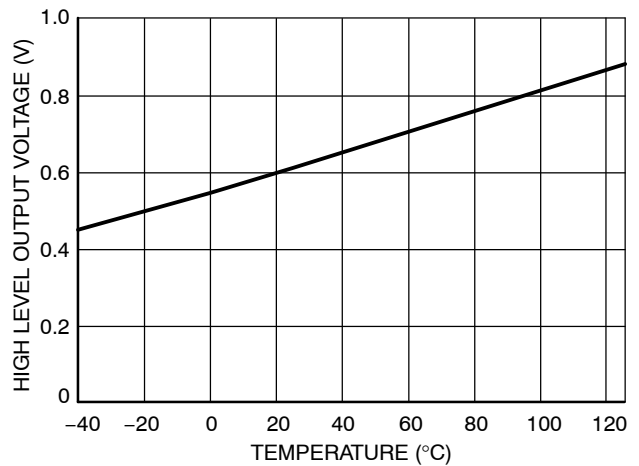


Figure 31. High Level Output Voltage vs. Temperature

CHARACTERIZATION CURVES

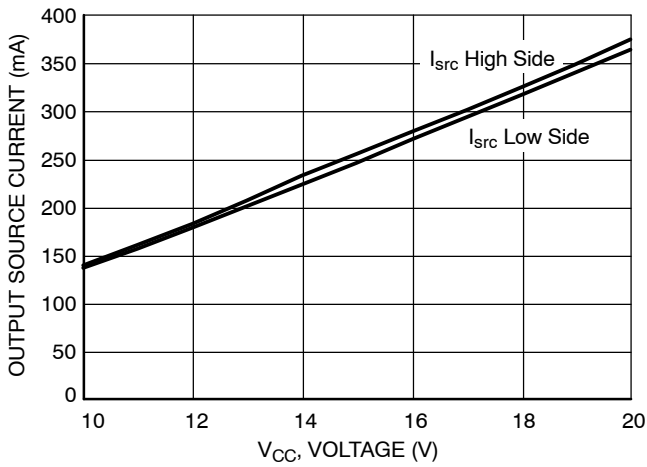


Figure 32. Output Source Current vs. Supply Voltage ( $V_{CC} = V_{BOOT}$ )

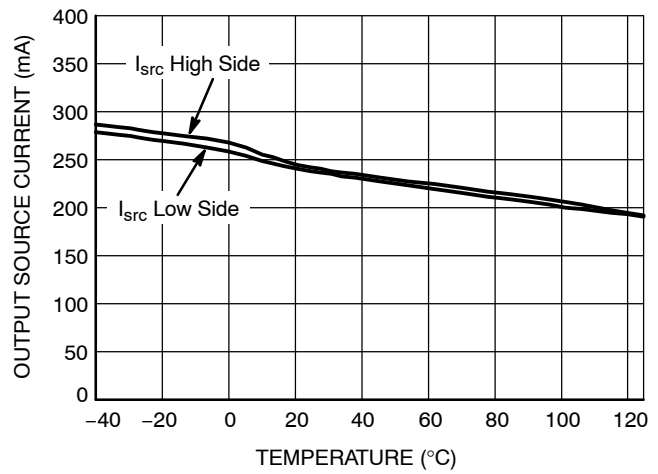


Figure 33. Output Source Current vs. Temperature

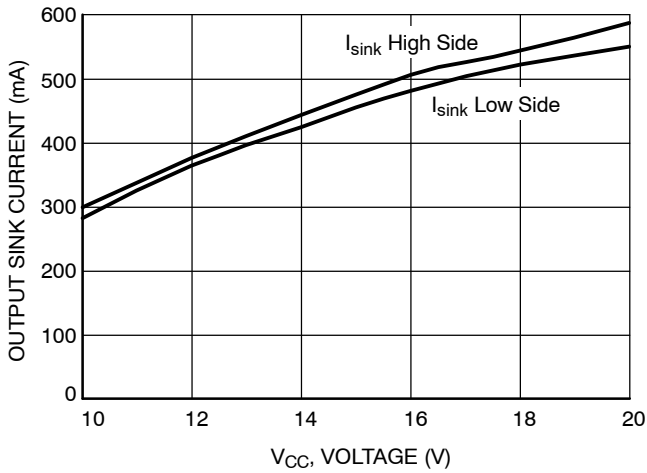


Figure 34. Output Sink Current vs. Supply Voltage ( $V_{CC} = V_{BOOT}$ )

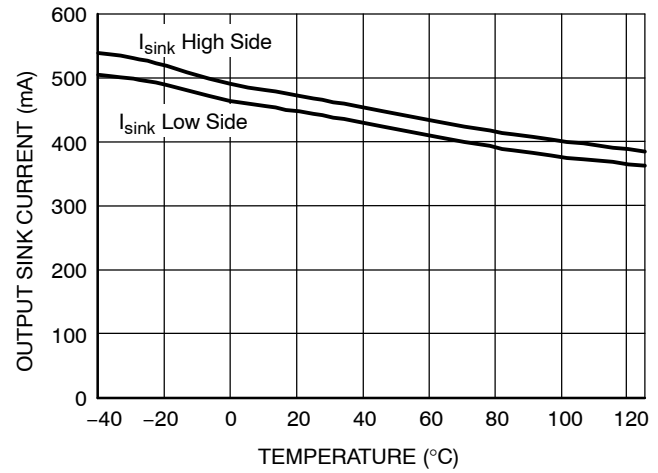


Figure 35. Output Sink Current vs. Temperature

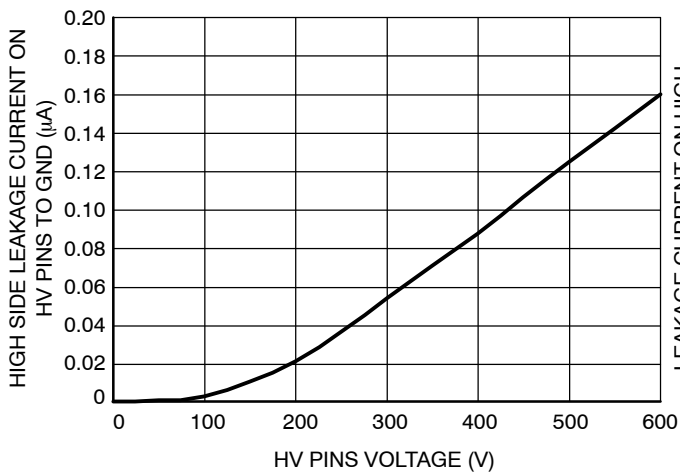


Figure 36. Leakage Current on High Voltage Pins (600 V) to Ground vs.  $V_{BRIDGE}$  Voltage ( $V_{BRIDGE} = V_{BOOT} = V_{DRV\_HI}$ )

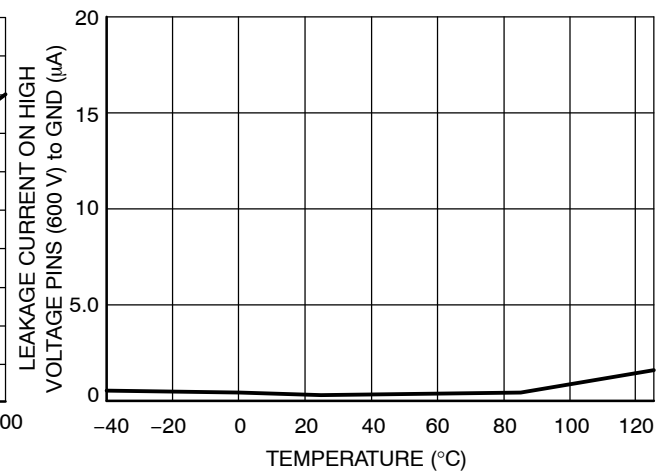


Figure 37. Leakage Current on High Voltage Pins (600 V) to Ground vs. Temperature ( $V_{BRIDGE} = V_{BOOT} = V_{DRV\_HI} = 600$  V)

CHARACTERIZATION CURVES

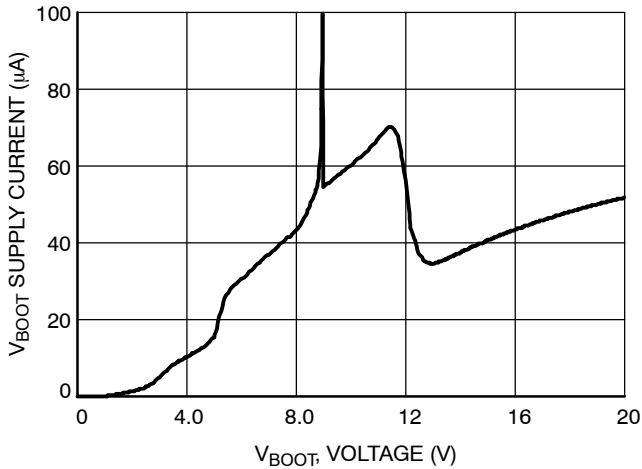


Figure 38.  $V_{BOOT}$  Supply Current vs. Bootstrap Supply Voltage ( $V_{CC} = V_{BOOT}$ )

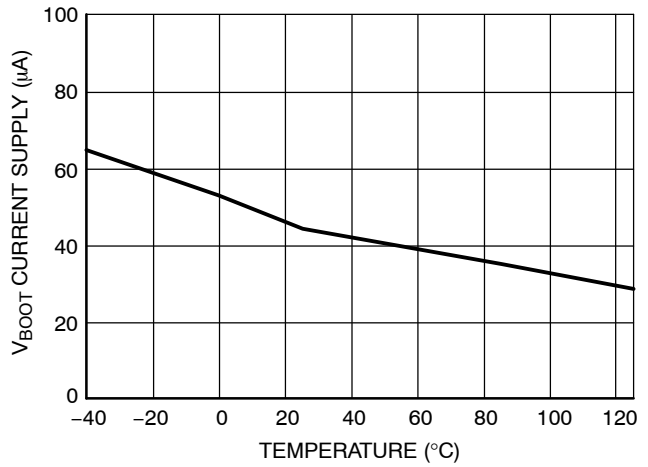


Figure 39.  $V_{BOOT}$  Supply Current vs. Temperature

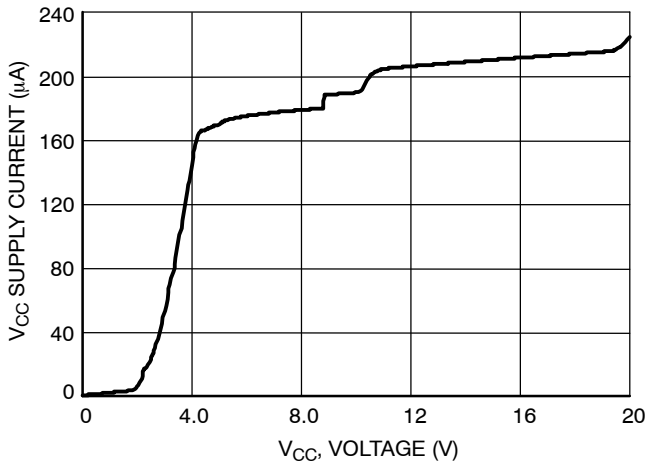


Figure 40.  $V_{CC}$  Supply Current vs.  $V_{CC}$  Supply Voltage ( $V_{CC} = V_{BOOT}$ )

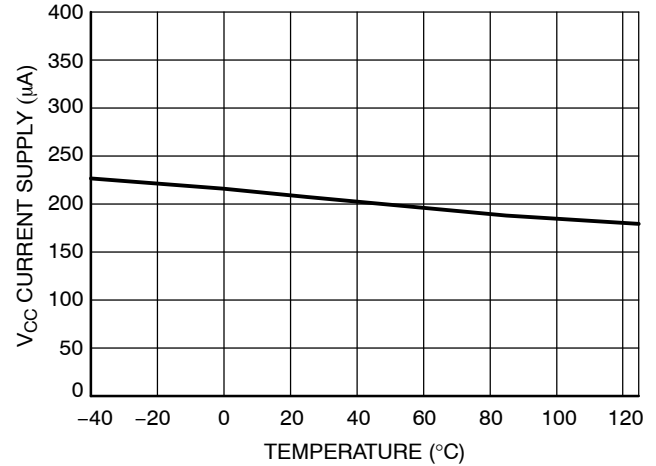


Figure 41.  $V_{CC}$  Supply Current vs. Temperature

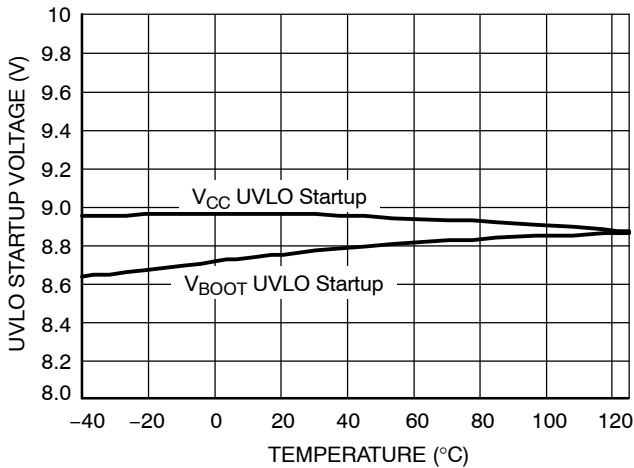


Figure 42. UVLO Startup Voltage vs. Temperature

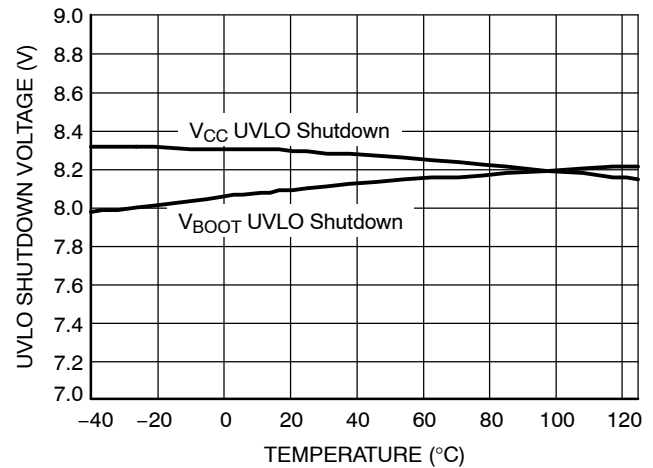
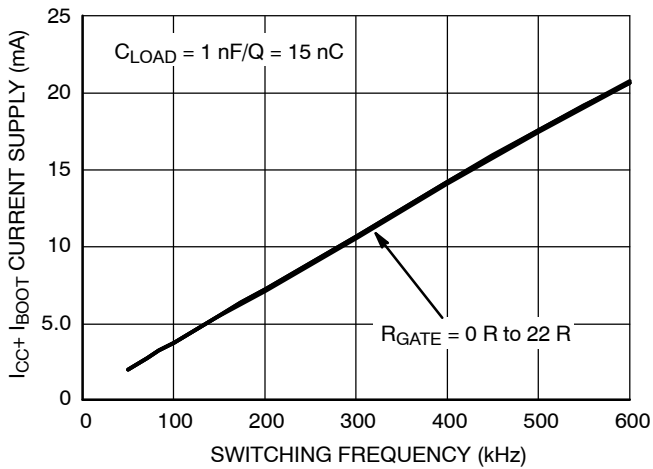
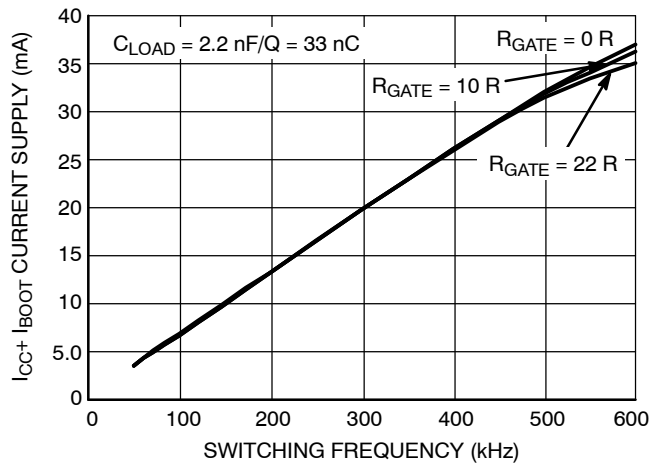


Figure 43. UVLO Shutdown Voltage vs. Temperature

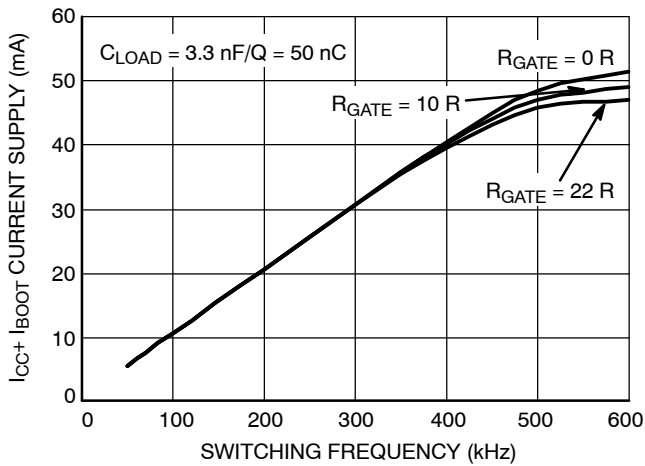
## CHARACTERIZATION CURVES



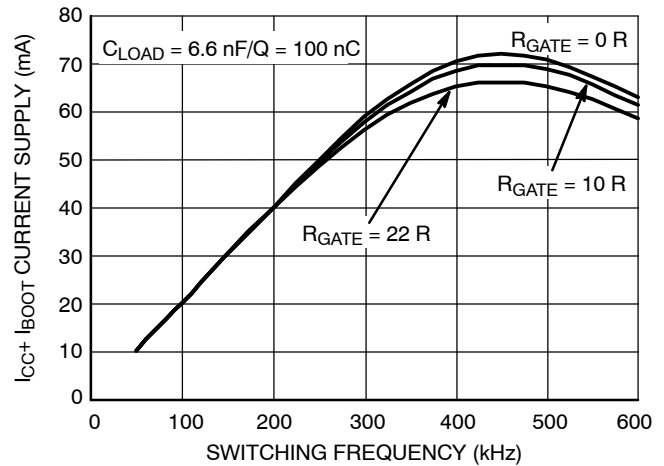
**Figure 44.  $I_{CC1}$  Consumption vs. Switching Frequency with 15 nC Load on Each Driver @  $V_{CC} = 15 \text{ V}$**



**Figure 45.  $I_{CC1}$  Consumption vs. Switching Frequency with 33 nC Load on Each Driver @  $V_{CC} = 15 \text{ V}$**



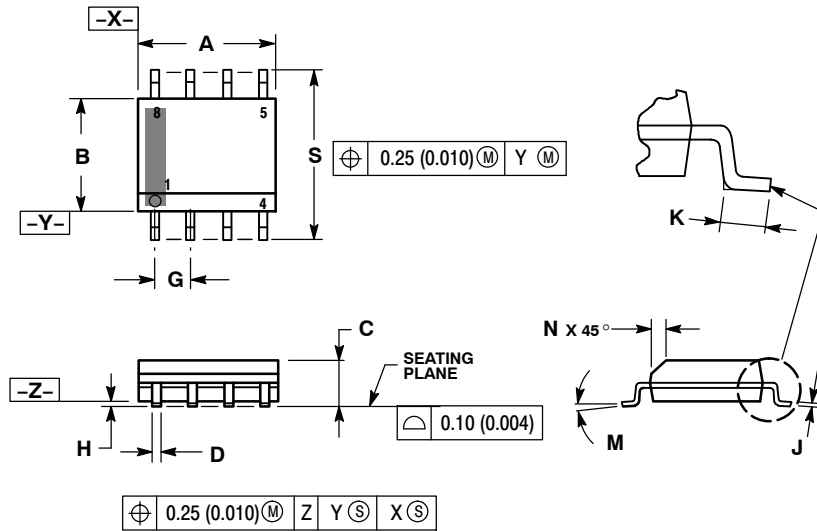
**Figure 46.  $I_{CC1}$  Consumption vs. Switching Frequency with 50 nC Load on Each Driver @  $V_{CC} = 15 \text{ V}$**



**Figure 47.  $I_{CC1}$  Consumption vs. Switching Frequency with 100 nC Load on Each Driver @  $V_{CC} = 15 \text{ V}$**

PACKAGE DIMENSIONS

SOIC-8 NB  
CASE 751-07  
ISSUE AJ

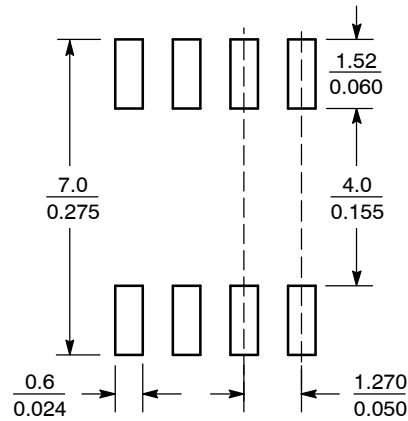


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

| DIM | MILLIMETERS |      | INCHES    |       |
|-----|-------------|------|-----------|-------|
|     | MIN         | MAX  | MIN       | MAX   |
| A   | 4.80        | 5.00 | 0.189     | 0.197 |
| B   | 3.80        | 4.00 | 0.150     | 0.157 |
| C   | 1.35        | 1.75 | 0.053     | 0.069 |
| D   | 0.33        | 0.51 | 0.013     | 0.020 |
| G   | 1.27 BSC    |      | 0.050 BSC |       |
| H   | 0.10        | 0.25 | 0.004     | 0.010 |
| J   | 0.19        | 0.25 | 0.007     | 0.010 |
| K   | 0.40        | 1.27 | 0.016     | 0.050 |
| M   | 0°          | 8°   | 0°        | 8°    |
| N   | 0.25        | 0.50 | 0.010     | 0.020 |
| S   | 5.80        | 6.20 | 0.228     | 0.244 |

SOLDERING FOOTPRINT\*



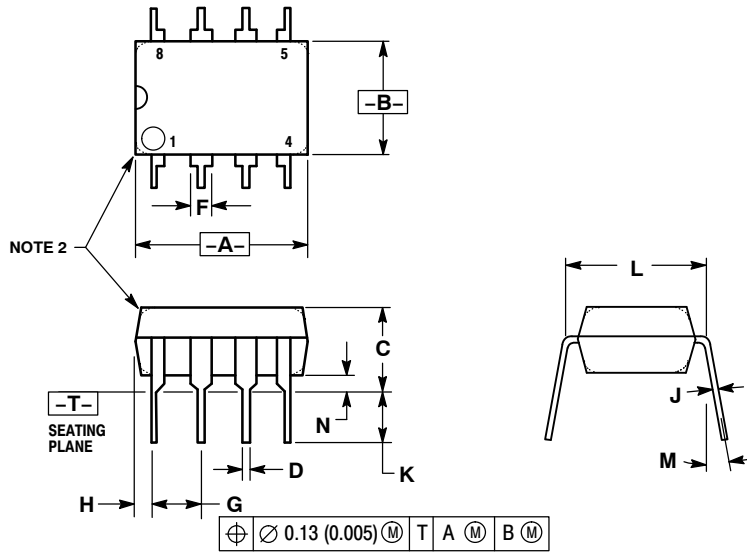
SCALE 6:1 (mm/inches)

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

# NCP5104

## PACKAGE DIMENSIONS

8 LEAD PDIP  
CASE 626-05  
ISSUE L



### NOTES:

1. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
2. PACKAGE CONTOUR OPTIONAL (ROUND OR SQUARE CORNERS).
3. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.

| DIM | MILLIMETERS |       | INCHES    |       |
|-----|-------------|-------|-----------|-------|
|     | MIN         | MAX   | MIN       | MAX   |
| A   | 9.40        | 10.16 | 0.370     | 0.400 |
| B   | 6.10        | 6.60  | 0.240     | 0.260 |
| C   | 3.94        | 4.45  | 0.155     | 0.175 |
| D   | 0.38        | 0.51  | 0.015     | 0.020 |
| F   | 1.02        | 1.78  | 0.040     | 0.070 |
| G   | 2.54 BSC    |       | 0.100 BSC |       |
| H   | 0.76        | 1.27  | 0.030     | 0.050 |
| J   | 0.20        | 0.30  | 0.008     | 0.012 |
| K   | 2.92        | 3.43  | 0.115     | 0.135 |
| L   | 7.62 BSC    |       | 0.300 BSC |       |
| M   | ---         | 10°   | ---       | 10°   |
| N   | 0.76        | 1.01  | 0.030     | 0.040 |

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