CY7B991
CY7B992

Programmable Skew Clock Buffer

Features

- All output pair skew <100 ps typical (250 ps maximum)
- 3.75 MHz to 80 MHz output operation
- User selectable output functions
  - Selectable skew to 18 ns
  - Inverted and non-inverted
  - Operation at 1⁄2 and 1⁄4 input frequency
  - Operation at 2 × and 4 × input frequency (input as low as 3.75 MHz)
- Zero input to output delay
- 50% duty cycle outputs
- Outputs drive 50 Ω terminated lines
- Low operating current
- 32-pin PLCC package
- Jitter < 200 ps peak-to-peak (< 25 ps RMS)

Functional Description

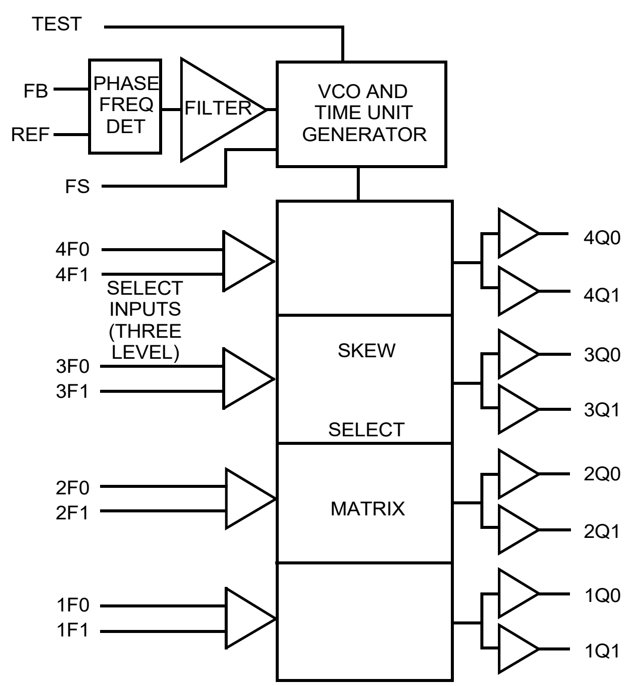
The CY7B991 and CY7B992 Programmable Skew Clock Buffers (PSCB) offer user selectable control over system clock functions. These multiple output clock drivers provide the system integrator with functions necessary to optimize the timing of high performance computer systems. Each of the eight individual drivers, arranged in four pairs of user controllable outputs, can drive terminated transmission lines with impedances as low as 50Ω. They can deliver minimal and specified output skews and full swing logic levels (CY7B991 TTL or CY7B992 CMOS).

Each output is hardwired to one of the nine delay or function configurations. Delay increments of 0.7 to 1.5 ns are determined by the operating frequency with outputs that skew up to ±6 time units from their nominal "zero" skew position. The completely integrated PLL allows cancellation of external load and transmission line delay effects. When this "zero delay" capability of the PSCB is combined with the selectable output skew functions, you can create output-to-output delays of up to ±12 time units.

Divide-by-two and divide-by-four output functions are provided for additional flexibility in designing complex clock systems. When combined with the internal PLL, these divide functions enable distribution of a low frequency clock that are multiplied by two or four at the clock destination. This facility minimizes clock distribution difficulty, allowing maximum system clock speed and flexibility.

For a complete list of related documentation, click here.

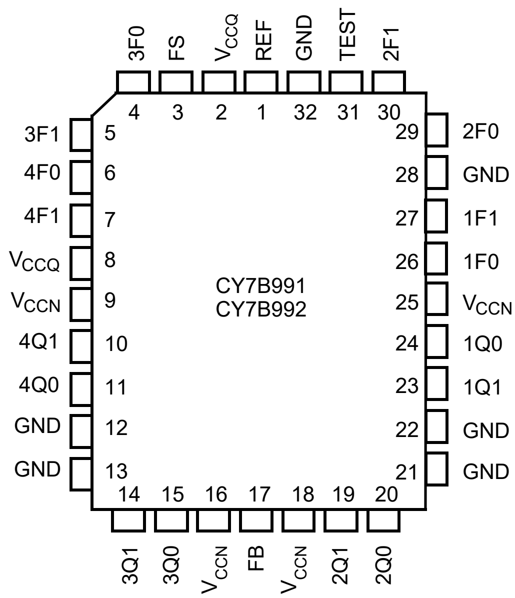
Logic Block Diagram



Contents

Pinouts

Figure 1. 32-pin PLCC pinout



Pin Definitions

Signal Name	I/O	Description
REF	I	Reference frequency input. This input supplies the frequency and timing against which all functional variations are measured.
FB	I	PLL feedback input (typically connected to one of the eight outputs).
FS	I	Three level frequency range select. See Table 1 on page 4.
1F0, 1F1	I	Three level function select inputs for output pair 1 (1Q0, 1Q1). See Table 2 on page 4.
2F0, 2F1	I	Three level function select inputs for output pair 2 (2Q0, 2Q1). See Table 2 on page 4.
3F0, 3F1	I	Three level function select inputs for output pair 3 (3Q0, 3Q1). See Table 2 on page 4.
4F0, 4F1	I	Three level function select inputs for output pair 4 (4Q0, 4Q1). See Table 2 on page 4.
TEST	I	Three level select. See Test Mode on page 5 under the Block Diagram Description on page 4.
1Q0, 1Q1	O	Output pair 1. See Table 2 on page 4.
2Q0, 2Q1	O	Output pair 2. See Table 2 on page 4.
3Q0, 3Q1	O	Output pair 3. See Table 2 on page 4.
4Q0, 4Q1	O	Output pair 4. See Table 2 on page 4.
V_{CCN}	PWR	Power supply for output drivers.
V_{CCQ}	PWR	Power supply for internal circuitry.
GND	PWR	Ground.

Block Diagram Description

Phase Frequency Detector and Filter

The Phase Frequency Detector and Filter blocks accept inputs from the reference frequency (REF) input and the feedback (FB) input and generate correction information to control the frequency of the Voltage Controlled Oscillator (VCO). These blocks, along with the VCO, form a Phase Locked Loop (PLL) that tracks the incoming REF signal.

VCO and Time Unit Generator

The VCO accepts analog control inputs from the PLL filter block. It generates a frequency used by the time unit generator to create discrete time units that are selected in the skew select matrix. The operational range of the VCO is determined by the FS control pin. The time unit (t_U) is determined by the operating frequency of the device and the level of the FS pin as shown in Table 1.

Table 1. Frequency Range Select and t_U Calculation [1]

FS [2, 3]	f_{NOM} (MHz)		$t_U = \frac{1}{f_{NOM} \times N}$ where N =	Approximate Frequency (MHz) at which t_U = 1.0 ns
	Min	Max		
LOW	15	30	44	22.7
MID	25	50	26	38.5
HIGH	40	80	16	62.5

Skew Select Matrix

The skew select matrix contains four independent sections. Each section has two low skew, high fanout drivers (× Q0, × Q1), and two corresponding three level function select (× F0, × F1) inputs. Table 2 shows the nine possible output functions for each section as determined by the function select inputs. All times are measured with respect to the REF input assuming that the output connected to the FB input has $0t_U$ selected.

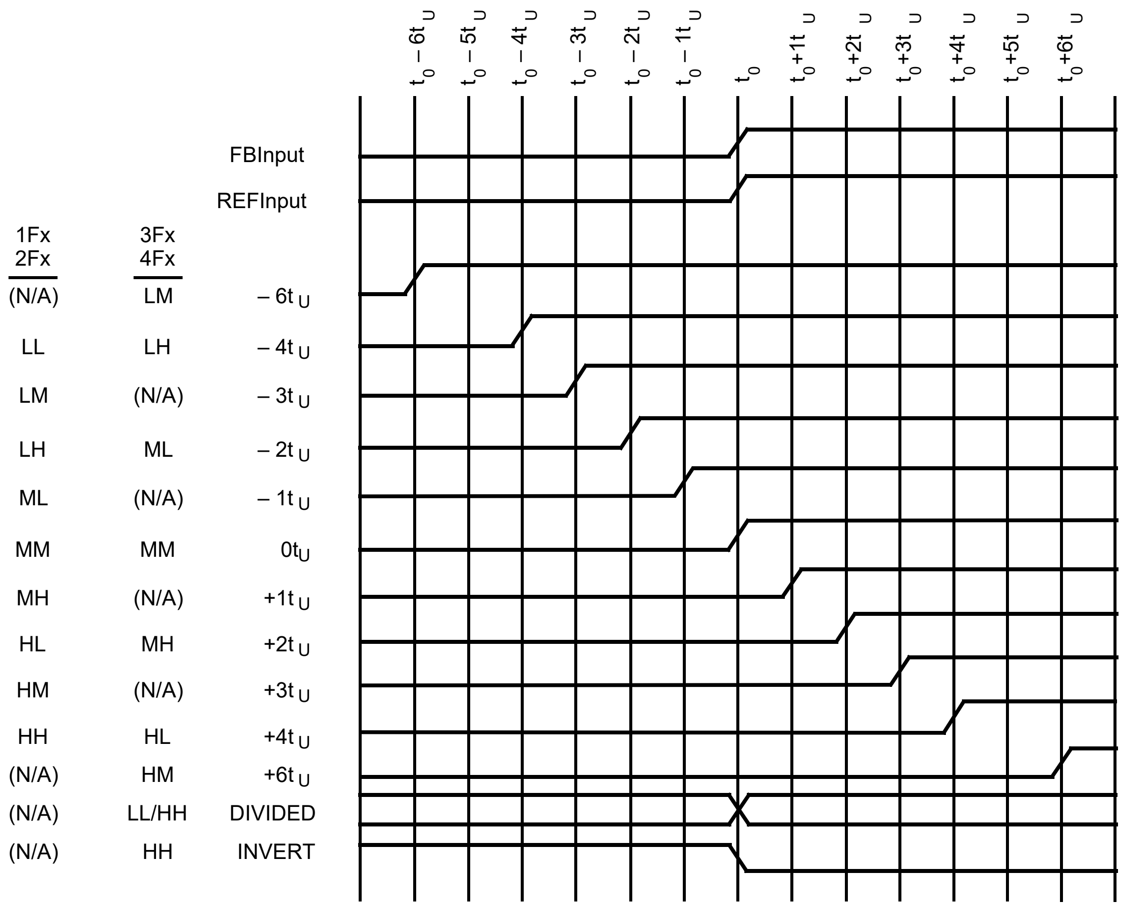
Table 2. Programmable Skew Configurations [1]

Function Selects		Output Functions		
1F1, 2F1, 3F1, 4F1	1F0, 2F0, 3F0, 4F0	1Q0, 1Q1, 2Q0, 2Q1	3Q0, 3Q1	4Q0, 4Q1
LOW	LOW	$-4t_U$	Divide by 2	Divide by 2
LOW	MID	$-3t_U$	$-6t_U$	$-6t_U$
LOW	HIGH	$-2t_U$	$-4t_U$	$-4t_U$
MID	LOW	$-1t_U$	$-2t_U$	$-2t_U$
MID	MID	$0t_U$	$0t_U$	$0t_U$
MID	HIGH	$+1t_U$	$+2t_U$	$+2t_U$
HIGH	LOW	$+2t_U$	$+4t_U$	$+4t_U$
HIGH	MID	$+3t_U$	$+6t_U$	$+6t_U$
HIGH	HIGH	$+4t_U$	Divide by 4	Inverted

Notes
1. For all tristate inputs, HIGH indicates a connection to V_{CC}, LOW indicates a connection to GND, and MID indicates an open connection. Internal termination circuitry holds an unconnected input to $V_{CC}/2$.
2. The level is set on FS is determined by the "normal" operating frequency (fNOM) of the VCO and Time Unit Generator (see Logic Block Diagram on page 1). Nominal frequency (fNOM) always appears at 1Q0 and the other outputs when they are operated in their undivided modes (see Table 2). The frequency appearing at the REF and FB inputs are fNOM when the output connected to FB is undivided. The frequency of the REF and FB inputs are fNOM/2 or fNOM/4 when the part is configured for a frequency multiplication by using a divided output as the FB input.
3. When the FS pin is selected HIGH, the REF input must not transition upon power up until V_{CC} has reached 4.3 V.

Figure 2 shows the typical outputs with FB connected to a zero skew output. [4]

Figure 2. Typical Outputs with FB Connected to a Zero-Skew Output



Test Mode

The TEST input is a three level input. In normal system operation, this pin is connected to ground, enabling the CY7B991 or CY7B992 to operate as explained in Skew Select Matrix on page 4. For testing purposes, any of the three level inputs can have a removable jumper to ground, or be tied LOW through a 100 Ω resistor. This enables an external tester to change the state of these pins.

If the TEST input is forced to its MID or HIGH state, the device operates with its internal phase locked loop disconnected, and input levels supplied to REF directly controls all outputs. Relative output to output functions are the same as in normal mode.

In contrast with normal operation (TEST tied LOW), all outputs function based only on the connection of their own function selects inputs (× F0 and × F1) and the waveform characteristics of the REF input.

Note

4. FB connected to an output selected for “zero” skew (i.e., × F1 = × F0 = MID).

Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Storage Temperature .... –65 °C to +150 °C

Ambient Temperature
with Power Applied .... –55 °C to +125 °C

Supply Voltage to Ground Potential ....–0.5 V to +7.0 V

DC Input Voltage ....–0.5 V to +7.0 V

Output Current into Outputs (LOW) .... 64 mA

Static Discharge Voltage
(MIL-STD-883, Method 3015) .... > 2001 V

Latch-Up Current .... > 200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0 °C to +70 °C	5 V ± 10%
Industrial	–40 °C to +85 °C	5 V ± 10%

Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions	CY7B991		CY7B992		Unit
			Min	Max	Min	Max	
V_{OH}	Output HIGH Voltage	V_{CC} = Min I_{OH} = –16 mA	2.4	–	–	–	V
		V_{CC} = Min, I_{OH} = –40 mA	–	–	V_{CC}– 0.75	–	
V_{OL}	Output LOW Voltage	V_{CC} = Min, I_{OL} = 46 mA	–	0.45	–	–	V
		V_{CC} = Min, I_{OL} = 46 mA	–	–	–	0.45	
V_{IH}	Input HIGH Voltage (REF and FB inputs only)		2.0	V_{CC}	V_{CC} – 1.35	V_{CC}	V
V_{IL}	Input LOW Voltage (REF and FB inputs only)		–0.5	0.8	–0.5	1.35	V

Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions	CY7B991		CY7B992		Unit
			Min	Max	Min	Max	
V_{IHH}	Three Level Input HIGH Voltage (Test, FS, × Fn) [5]	Min ≤ V_{CC} ≤ Max	V_{CC} – 0.85	V_{CC}	V_{CC} – 0.85	V_{CC}	V
V_{IMM}	Three Level Input MID Voltage (Test, FS, × Fn) [5]	Min ≤ V_{CC} ≤ Max	V_{CC}/2 – 500 mV	V_{CC}/2 + 500 mV	V_{CC}/2 – 500 mV	V_{CC}/2 + 500 mV	V
V_{ILL}	Three Level Input LOW Voltage (Test, FS, × Fn) [5]	Min ≤ V_{CC} ≤ Maximum	0.0	0.85	0.0	0.85	V
I_{IH}	Input HIGH Leakage Current (REF and FB inputs only)	V_{CC} = Max, V_{IN} = Max.	–	10	–	10	µA
I_{IL}	Input LOW Leakage Current (REF and FB inputs only)	V_{CC} = Max, V_{IN} = 0.4 V	–500	–	–500	–	µA
I_{IHH}	Input HIGH Current (Test, FS, × Fn)	V_{IN} = V_{CC}	–	200	–	200	µA
I_{IMM}	Input MID Current (Test, FS, × Fn)	V_{IN} = V_{CC}/2	–50	50	–50	50	µA
I_{ILL}	Input LOW Current (Test, FS, × Fn)	V_{IN} = GND	–	–200	–	–200	µA
I_{OS}	Output Short Circuit Current [6]	V_{CC} = Max, V_{OUT} = GND (25 °C only)	–	–250	–	N/A	mA
I_{CCQ}	Operating Current Used by Internal Circuitry	V_{CCN} = V_{CCQ} = Max, All Input Selects Open — Commercial	–	85	–	85	mA
		Industrial	–	90	–	90	
I_{CCN}	Output Buffer Current per Output Pair [7]	V_{CCN} = V_{CCQ} = Max, I_{OUT} = 0 mA Input Selects Open, f_{MAX}	–	14	–	19	mA
PD	Power Dissipation per Output Pair [5]	V_{CCN} = V_{CCQ} = Max, I_{OUT} = 0 mA, Input Selects Open, f_{MAX}	–	78	–	104 [8]	mW

Notes

5. Total power dissipation per output pair can be approximated by the following expression that includes device power dissipation plus power dissipation due to the load circuit:
   CY7B991:PD = [(22 + 0.61F) + [((1550 – 2.7F)/Z) + (.0125FC)]N] × 1.1
   CY7B992:PD = [(19.25+ 0.94F) + [((700 + 6F)/Z) + (.017FC)]N] × 1.1
   See note 7 for variable definition.
6. CY7B991 must be tested one output at a time, output shorted for less than one second, less than 10% duty cycle. Room temperature only. CY7B992 outputs must not be shorted to GND. Doing so may cause permanent damage.
7. Total output current per output pair is approximated by the following expression that includes device current plus load current:
   CY7B991: I_{CCN} = [(4 + 0.11F) + [((835 – 3F)/Z) + (.0022FC)]N] × 1.1
   CY7B992: I_{CCN} = [(3.5 + 0.17F) + [((1160 – 2.8F)/Z) + (.0025FC)]N] × 1.1
   Where
   F = frequency in MHz; C = capacitive load in pF; Z = line impedance in ohms; N = number of loaded outputs; 0, 1, or 2; FC = F × C.
8. Applies to REF and FB inputs only. Tested initially and after any design or process changes that may affect these parameters.

Capacitance

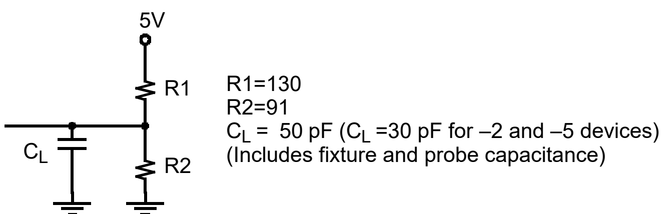
Parameter [9, 10]	Description	Test Conditions	Max	Unit
C_{IN}	Input Capacitance	$T_A = 25\,°C$, f = 1 MHz, $V_{CC} = 5.0\,V$	10	pF

Thermal Resistance

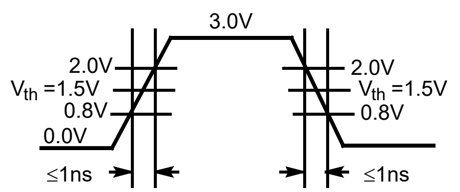
Parameter [10]	Description	Test Conditions	32-pin PLCC Package	Unit
Θ_{JA}	Thermal resistance (junction to ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, according to EIA/JESD51.	44	°C/W
Θ_{JC}	Thermal resistance (junction to case)		26	°C/W

AC Test Loads and Waveforms

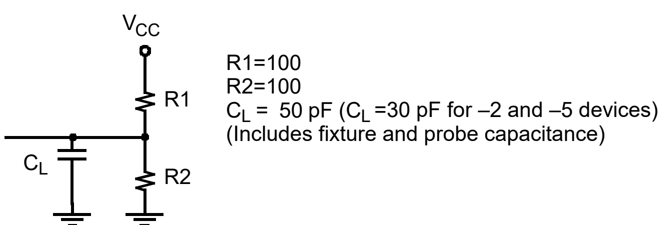
Figure 3. AC Test Loads and Waveforms



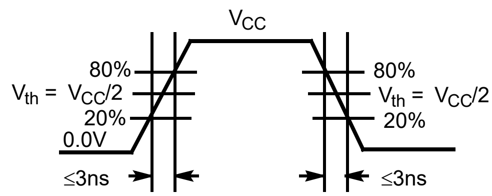
TTL AC Test Load (CY7B991)



TTL Input Test Waveform (CY7B991)



CMOS AC Test Load (CY7B992)



CMOS Input Test Waveform (CY7B992)

Notes
9. CMOS output buffer current and power dissipation specified at 50 MHz reference frequency.
10. Tested initially and after any design or process change that may affect these parameters.

Switching Characteristics

Over the Operating Range

Parameter [11, 12]	Description		CY7B991-2 [13] Min	CY7B991-2 [13] Typ	CY7B991-2 [13] Max	CY7B992-2 [13] Min	CY7B992-2 [13] Typ	CY7B992-2 [13] Max	Unit
f_{NOM}	Operating Clock Frequency in MHz	FS = LOW [11, 14]	15	–	30	15	–	30	MHz
		FS = MID [11, 14]	25	–	50	25	–	50	
		FS = HIGH [11, 14, 15]	40	–	80	40	–	80 [16]	
t_{RPWH}	REF Pulse Width HIGH		5.0	–	–	5.0	–	–	ns
t_{RPWL}	REF Pulse Width LOW		5.0	–	–	5.0	–	–	ns
t_U	Programmable Skew Unit		See Table 1 on page 4						
t_{SKEWPR}	Zero Output Matched-Pair Skew (XQ0, XQ1) [17, 18]		–	0.05	0.20	–	0.05	0.20	ns
t_{SKEW0}	Zero Output Skew (All Outputs) [17, 19, 20]		–	0.1	0.25	–	0.1	0.25	ns
t_{SKEW1}	Output Skew (Rise-Rise, Fall-Fall, Same Class Outputs) [17, 20]		–	0.25	0.5	–	0.25	0.5	ns
t_{SKEW2}	Output Skew (Rise-Fall, Nominal-Inverted, Divided-Divided) [17, 20]		–	0.3	0.5	–	0.3	0.5	ns
t_{SKEW3}	Output Skew (Rise-Rise, Fall-Fall, Different Class Outputs) [17, 20]		–	0.25	0.5	–	0.25	0.5	ns
t_{SKEW4}	Output Skew (Rise-Fall, Nominal-Divided, Divided-Inverted) [17, 20]		–	0.5	0.9	–	0.5	0.7	ns
t_{DEV}	Device-to-Device Skew [13, 21]		–	–	0.75	–	–	0.75	ns
t_{PD}	Propagation Delay, REF Rise to FB Rise		–0.25	0.0	+0.25	–0.25	0.0	+0.25	ns
t_{ODCV}	Output Duty Cycle Variation [22]		–0.65	0.0	+0.65	–0.5	0.0	+0.5	ns
t_{PWH}	Output HIGH Time Deviation from 50% [23, 24]		–	–	2.0	–	–	3.0	ns
t_{PWL}	Output LOW Time Deviation from 50% [23, 24]		–	–	1.5	–	–	3.0	ns
t_{ORISE}	Output Rise Time [23, 25]		0.15	1.0	1.2	0.5	2.0	2.5	ns
t_{OFALL}	Output Fall Time [23, 25]		0.15	1.0	1.2	0.5	2.0	2.5	ns
t_{LOCK}	PLL Lock Time [26]		–	–	0.5	–	–	0.5	ms
t_{JR}	Cycle-to-Cycle Output Jitter	RMS [13]	–	–	25	–	–	25	ps
		Peak-to-Peak [13]	–	–	200	–	–	200	ps

Notes

11. The level is set on FS is determined by the "normal" operating frequency (fNOM) of the VCO and Time Unit Generator (see Logic Block Diagram on page 1). Nominal frequency (f_{NOM}) always appears at 1Q0 and the other outputs when they are operated in their undivided modes (see Table 2). The frequency appearing at the REF and FB inputs are f_{NOM} when the output connected to FB is undivided. The frequency of the REF and FB inputs are fNOM/2 or fNOM/4 when the part is configured for a frequency multiplication by using a divided output as the FB input.
12. Test measurement levels for the CY7B991 are TTL levels (1.5 V to 1.5 V). Test measurement levels for the CY7B992 are CMOS levels (V_{CC}/2 to V_{CC}/2). Test conditions assume signal transition times of 2 ns or less and output loading as shown in the Figure 3 on page 8 unless otherwise specified.
13. Guaranteed by statistical correlation. Tested initially and after any design or process changes that affect these parameters.
14. For all tristate inputs, HIGH indicates a connection to V_{CC}, LOW indicates a connection to GND, and MID indicates an open connection. Internal termination circuitry holds an unconnected input to V_{CC}/2.
15. When the FS pin is selected HIGH, the REF input must not transition upon power up until V_{CC} has reached 4.3 V.
16. Except as noted, all CY7B992-2 and -5 timing parameters are specified to 80 MHz with a 30 pF load.
17. SKEW is defined as the time between the earliest and the latest output transition among all outputs for which the same t_U delay is selected when all are loaded with 50 pF and terminated with 50Ω to 2.06 V (CY7B991) or V_{CC}/2 (CY7B992).
18. t_{SKEWPR} is defined as the skew between a pair of outputs (XQ0 and XQ1) when all eight outputs are selected for 0t_U.
19. t_{SKEW0} is defined as the skew between outputs when they are selected for 0t_U. Other outputs are divided or inverted but not shifted.
20. C_L = 0 pF. For C_L = 30 pF, t_{SKEW0} = 0.35 ns.
21. t_{DEV} is the output-to-output skew between any two devices operating under the same conditions (V_{CC} ambient temperature, air flow, and so on.)
22. t_{ODCV} is the deviation of the output from a 50% duty cycle. Output pulse width variations are included in t_{SKEW2} and t_{SKEW4} specifications.
23. Specified with outputs loaded with 30 pF for the CY7B99X-2 and -5 devices and 50 pF for the CY7B99X-7 devices. Devices are terminated through 50 Ω to 2.06 V (CY7B991) or V_{CC}/2 (CY7B992).
24. tPWH is measured at 2.0 V for the CY7B991 and 0.8 V_{CC} for the CY7B992. tPWL is measured at 0.8V for the CY7B991 and 0.2 V_{CC} for the CY7B992.
25. t_{ORISE} and t_{OFALL} measured between 0.8V and 2.0V for the CY7B991 or 0.8 V_{CC} and 0.2 V_{CC} for the CY7B992.
26. t_{LOCK} is the time that is required before synchronization is achieved. This specification is valid only after V_{CC} is stable and within normal operating limits. This parameter is measured from the application of a new signal or frequency at REF or FB until t_{PD} is within specified limits.

Switching Characteristics

Over the Operating Range

Parameter [27, 28]	Description		CY7B991-5			CY7B992-5			Unit
			Min	Typ	Max	Min	Typ	Max	
f_{NOM}	Operating Clock Frequency in MHz	FS = LOW [27, 29]	15	–	30	15	–	30	MHz
		FS = MID [27, 29]	25	–	50	25	–	50	
		FS = HIGH [27, 29, 30]	40	–	80	40	–	80 [31]	
t_{RPWH}	REF Pulse Width HIGH		5.0	–	–	5.0	–	–	ns
t_{RPWL}	REF Pulse Width LOW		5.0	–	–	5.0	–	–	ns
t_U	Programmable Skew Unit		See Table 1 on page 4						
t_{SKEWPR}	Zero Output Matched-Pair Skew (XQ0, XQ1) [32, 33]		–	0.1	0.25	–	0.1	0.25	ns
t_{SKEW0}	Zero Output Skew (All Outputs) [32, 34]		–	0.25	0.5	–	0.25	0.5	ns
t_{SKEW1}	Output Skew (Rise-Rise, Fall-Fall, Same Class Outputs) [32, 35]		–	0.6	0.7	–	0.6	0.7	ns
t_{SKEW2}	Output Skew (Rise-Fall, Nominal-Inverted, Divided-Divided) [32, 35]		–	0.5	1.0	–	0.6	1.5	ns
t_{SKEW3}	Output Skew (Rise-Rise, Fall-Fall, Different Class Outputs)[32, 35]		–	0.5	0.7	–	0.5	0.7	ns
t_{SKEW4}	Output Skew (Rise-Fall, Nominal-Divided, Divided-Inverted) [32, 35]		–	0.5	1.0	–	0.6	1.7	ns
t_{DEV}	Device-to-Device Skew [36, 37]		–	–	1.25	–	–	1.25	ns
t_{PD}	Propagation Delay, REF Rise to FB Rise		–0.5	0.0	+0.5	–0.5	0.0	+0.5	ns
t_{ODCV}	Output Duty Cycle Variation [22]		–1.0	0.0	+1.0	–1.2	0.0	+1.2	ns
t_{PWH}	Output HIGH Time Deviation from 50% [39, 40]		–	–	2.5	–	–	4.0	ns
t_{PWL}	Output LOW Time Deviation from 50% [39, 40]		–	–	3	–	–	4.0	ns
t_{ORISE}	Output Rise Time [39, 41]		0.15	1.0	1.5	0.5	2.0	3.5	ns
t_{OFALL}	Output Fall Time [39, 41]		0.15	1.0	1.5	0.5	2.0	3.5	ns
t_{LOCK}	PLL Lock Time [42]		–	–	0.5	–	–	0.5	ms
t_{JR}	Cycle-to-Cycle Output Jitter	RMS [36]	–	–	25	–	–	25	ps
		Peak-to-Peak [36]	–	–	200	–	–	200	ps

Notes

27. The level is set on FS is determined by the “normal” operating frequency (fNOM) of the VCO and Time Unit Generator (see Logic Block Diagram on page 1). Nominal frequency (f_{NOM}) always appears at 1Q0 and the other outputs when they are operated in their undivided modes (see Table 2). The frequency appearing at the REF and FB inputs are f_{NOM} when the output connected to FB is undivided. The frequency of the REF and FB inputs are fNOM/2 or fNOM/4 when the part is configured for a frequency multiplication by using a divided output as the FB input.
28. Test measurement levels for the CY7B991 are TTL levels (1.5 V to 1.5 V). Test measurement levels for the CY7B992 are CMOS levels (V_{CC}/2 to V_{CC}/2). Test conditions assume signal transition times of 2 ns or less and output loading as shown in the Figure 3 on page 8 unless otherwise specified.
29. For all tristate inputs, HIGH indicates a connection to V_{CC}, LOW indicates a connection to GND, and MID indicates an open connection. Internal termination circuitry holds an unconnected input to V_{CC}/2.
30. When the FS pin is selected HIGH, the REF input must not transition upon power up until V_{CC} has reached 4.3 V.
31. Except as noted, all CY7B992-2 and -5 timing parameters are specified to 80 MHz with a 30 pF load.
32. SKEW is defined as the time between the earliest and the latest output transition among all outputs for which the same t_U delay is selected when all are loaded with 50 pF and terminated with 50Ω to 2.06 V (CY7B991) or V_{CC}/2 (CY7B992).
33. t_{SKEWPR} is defined as the skew between a pair of outputs (XQ0 and XQ1) when all eight outputs are selected for $0t_U$.
34. t_{SKEW0} is defined as the skew between outputs when they are selected for $0t_U$. Other outputs are divided or inverted but not shifted.
35. C_L = 0 pF. For C_L = 30 pF, t_{SKEW0} = 0.35 ns.
36. Guaranteed by statistical correlation. Tested initially and after any design or process changes that affect these parameters.
37. t_{DEV} is the output-to-output skew between any two devices operating under the same conditions (V_{CC} ambient temperature, air flow, and so on.)
38. t_{ODCV} is the deviation of the output from a 50% duty cycle. Output pulse width variations are included in t_{SKEW2} and t_{SKEW4} specifications.
39. Specified with outputs loaded with 30 pF for the CY7B99X-2 and -5 devices and 50 pF for the CY7B99X-7 devices. Devices are terminated through 50 Ω to 2.06 V (CY7B991) or V_{CC}/2 (CY7B992).
40. tPWH is measured at 2.0 V for the CY7B991 and 0.8 V_{CC} for the CY7B992. tPWL is measured at 0.8V for the CY7B991 and 0.2 V_{CC} for the CY7B992.
41. t_{ORISE} and t_{OFALL} measured between 0.8V and 2.0V for the CY7B991 or 0.8 V_{CC} and 0.2 V_{CC} for the CY7B992.
42. t_{LOCK} is the time that is required before synchronization is achieved. This specification is valid only after V_{CC} is stable and within normal operating limits. This parameter is measured from the application of a new signal or frequency at REF or FB until t_{PD} is within specified limits.

Switching Characteristics

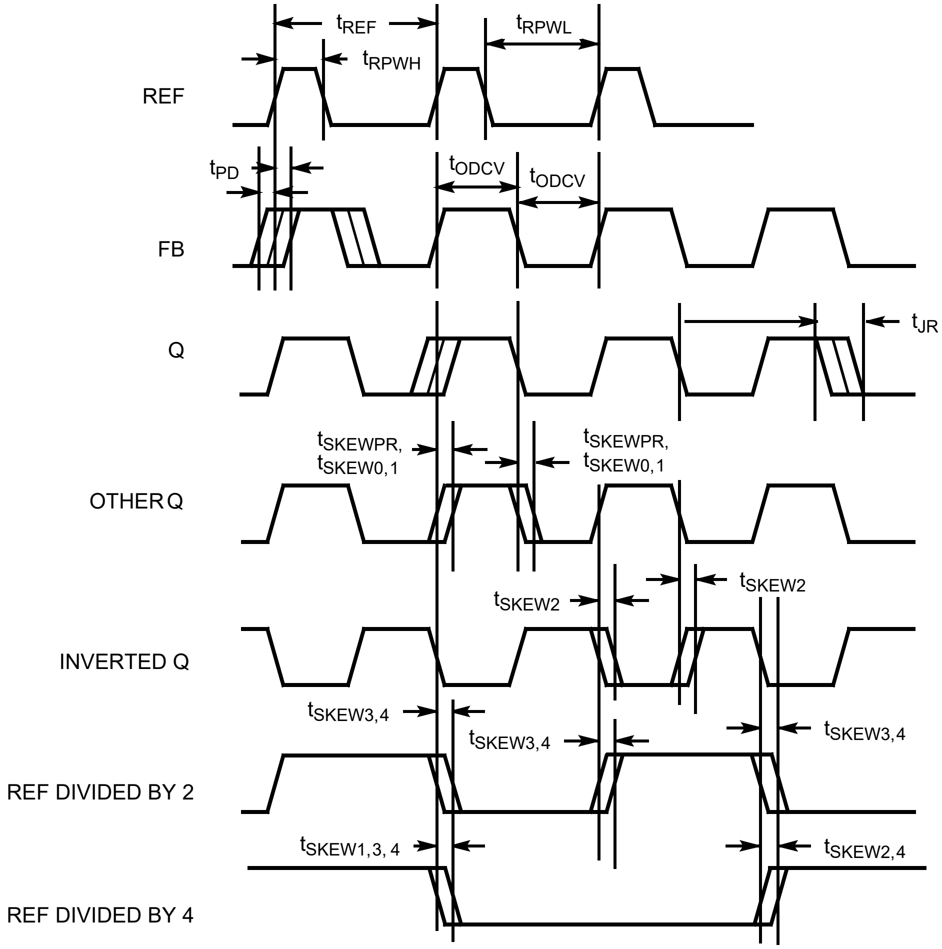
Over the Operating Range

Parameter [43, 44]	Description		CY7B991-7			CY7B992-7			Unit
			Min	Typ	Max	Min	Typ	Max	
f_{NOM}	Operating Clock Frequency in MHz	FS = LOW [43, 45]	15	–	30	15	–	30	MHz
		FS = MID [43, 45]	25	–	50	25	–	50	
		FS = HIGH [43, 45]	40	–	80	40	–	80 [46]	
t_{RPWH}	REF Pulse Width HIGH		5.0	–	–	5.0	–	–	ns
t_{RPWL}	REF Pulse Width LOW		5.0	–	–	5.0	–	–	ns
t_U	Programmable Skew Unit		See Table 1 on page 4						
t_{SKEWPR}	Zero Output Matched-Pair Skew (XQ0, XQ1) [47, 48]		–	0.1	0.25	–	0.1	0.25	ns
t_{SKEW0}	Zero Output Skew (All Outputs) [47, 49]		–	0.3	0.75	–	0.3	0.75	ns
t_{SKEW1}	Output Skew (Rise-Rise, Fall-Fall, Same Class Outputs) [47, 50]		–	0.6	1.0	–	0.6	1.0	ns
t_{SKEW2}	Output Skew (Rise-Fall, Nominal-Inverted, Divided-Divided) [47, 50]		–	1.0	1.5	–	1.0	1.5	ns
t_{SKEW3}	Output Skew (Rise-Rise, Fall-Fall, Different Class Outputs) [47, 50]		–	0.7	1.2	–	0.7	1.2	ns
t_{SKEW4}	Output Skew (Rise-Fall, Nominal-Divided, Divided-Inverted) [17, 20]		–	1.2	1.7	–	1.2	1.7	ns
t_{DEV}	Device-to-Device Skew[51, 52]		–	–	1.65	–	–	1.65	ns
t_{PD}	Propagation Delay, REF Rise to FB Rise		–0.7	0.0	+0.7	–0.7	0.0	+0.7	ns
t_{ODCV}	Output Duty Cycle Variation[53]		–1.2	0.0	+1.2	–1.5	0.0	+1.5	ns
t_{PWH}	Output HIGH Time Deviation from 50%[54, 55]		–	–	3	–	–	5.5	ns
t_{PWL}	Output LOW Time Deviation from 50%[54, 55]		–	–	3.5	–	–	5.5	ns
t_{ORISE}	Output Rise Time [54, 56]		0.15	1.5	2.5	0.5	3.0	5.0	ns
t_{OFALL}	Output Fall Time [54, 56]		0.15	1.5	2.5	0.5	3.0	5.0	ns
t_{LOCK}	PLL Lock Time [57]		–	–	0.5	–	–	0.5	ms
t_{JR}	Cycle-to-Cycle Output Jitter	RMS[51]	–	–	25	–	–	25	ps
		Peak-to-Peak [51]	–	–	200	–	–	200	ps

Notes

43. The level is set on FS is determined by the "normal" operating frequency (fNOM) of the VCO and Time Unit Generator (see Logic Block Diagram on page 1). Nominal frequency (f_{NOM}) always appears at 1Q0 and the other outputs when they are operated in their undivided modes (see Table 2). The frequency appearing at the REF and FB inputs are f_{NOM} when the output connected to FB is undivided. The frequency of the REF and FB inputs are fNOM/2 or fNOM/4 when the part is configured for a frequency multiplication by using a divided output as the FB input.
44. Test measurement levels for the CY7B991 are TTL levels (1.5 V to 1.5 V). Test measurement levels for the CY7B992 are CMOS levels (V_{CC}/2 to V_{CC}/2). Test conditions assume signal transition times of 2 ns or less and output loading as shown in the Figure 3 on page 8 unless otherwise specified.
45. For all tristate inputs, HIGH indicates a connection to V_{CC}, LOW indicates a connection to GND, and MID indicates an open connection. Internal termination circuitry holds an unconnected input to V_{CC}/2.
46. Except as noted, all CY7B992-2 and -5 timing parameters are specified to 80 MHz with a 30 pF load.
47. SKEW is defined as the time between the earliest and the latest output transition among all outputs for which the same t_U delay is selected when all are loaded with 50 pF and terminated with 50Ω to 2.06 V (CY7B991) or V_{CC}/2 (CY7B992).
48. t_{SKEWPR} is defined as the skew between a pair of outputs (XQ0 and XQ1) when all eight outputs are selected for 0t_U.
49. t_{SKEW0} is defined as the skew between outputs when they are selected for 0t_U. Other outputs are divided or inverted but not shifted.
50. C_L = 0 pF. For C_L = 30 pF, t_{SKEW0} = 0.35 ns.
51. Guaranteed by statistical correlation. Tested initially and after any design or process changes that affect these parameters.
52. t_{DEV} is the output-to-output skew between any two devices operating under the same conditions (V_{CC} ambient temperature, air flow, and so on.)
53. t_{ODCV} is the deviation of the output from a 50% duty cycle. Output pulse width variations are included in t_{SKEW2} and t_{SKEW4} specifications.
54. Specified with outputs loaded with 30 pF for the CY7B99X-2 and -5 devices and 50 pF for the CY7B99X-7 devices. Devices are terminated through 50 Ω to 2.06 V (CY7B991) or V_{CC}/2 (CY7B992).
55. tPWH is measured at 2.0 V for the CY7B991 and 0.8 V_{CC} for the CY7B992. tPWL is measured at 0.8V for the CY7B991 and 0.2 V_{CC} for the CY7B992.
56. t_{ORISE} and t_{OFALL} measured between 0.8V and 2.0V for the CY7B991 or 0.8 V_{CC} and 0.2 V_{CC} for the CY7B992.
57. t_{LOCK} is the time that is required before synchronization is achieved. This specification is valid only after V_{CC} is stable and within normal operating limits. This parameter is measured from the application of a new signal or frequency at REF or FB until t_{PD} is within specified limits.

AC Timing Diagrams



Operational Mode Descriptions

Figure 4. Zero Skew and Zero Delay Clock Driver

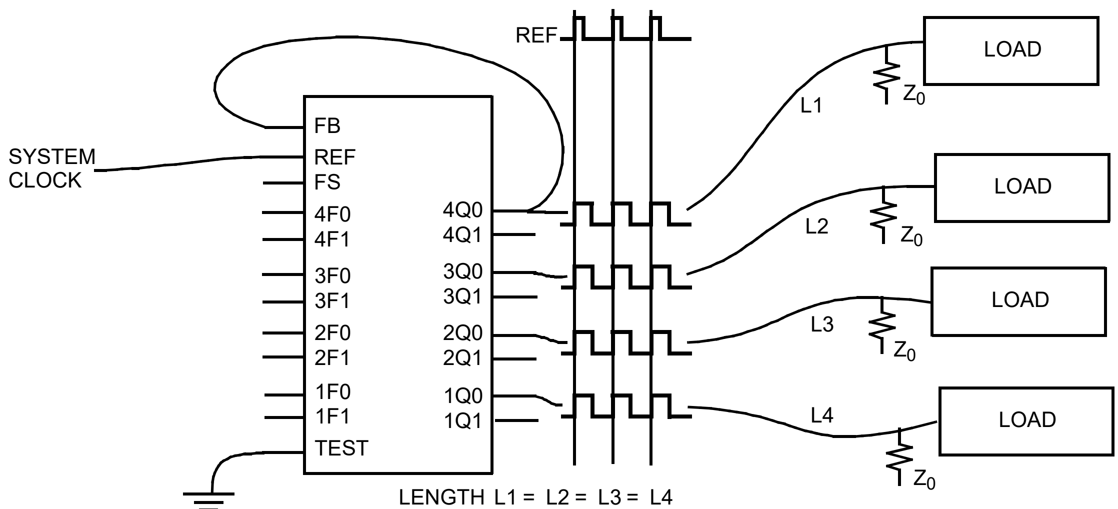


Figure 4 shows the PSCB configured as a zero skew clock buffer. In this mode the 7B991/992 is used as the basis for a low-skew clock distribution tree. When all of the function select inputs (× F0, × F1) are left open, the outputs are aligned and each drives a terminated transmission line to an independent load. The FB input is tied to any output in this configuration and the operating frequency range is selected with the FS pin. The low-skew specification, coupled with the ability to drive terminated transmission lines (with impedances as low as 50 ohms), enables efficient printed circuit board design.

Figure 5. Programmable Skew Clock Driver

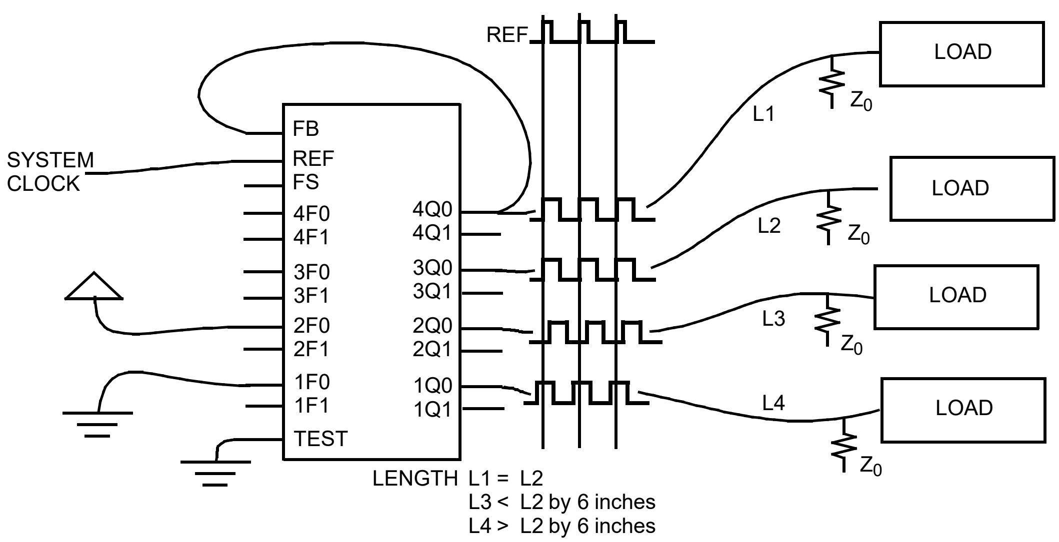


Figure 5 shows a configuration to equalize skew between metal traces of different lengths. In addition to low skew between outputs, the PSCB is programmed to stagger the timing of its outputs. Each of the four groups of output pairs are programmed to different output timing. Skew timing is adjusted over a wide range in small increments with the appropriate strapping of the function select pins. In this configuration the 4Q0 output is fed back to FB and configured for zero skew. The other three pairs of outputs are programmed to yield different skews relative to the feedback. By advancing the clock signal on the longer traces or retarding the clock signal on shorter traces, all loads can receive the clock pulse at the same time.

In this illustration the FB input is connected to an output with 0 ns skew (× F1, × F0 = MID) selected. The internal PLL synchronizes the FB and REF inputs and aligns their rising edges to ensure that all outputs have precise phase alignment.

Clock skews are advanced by ±6 time units (t_U) when using an output selected for zero skew as the feedback. A wider range of delays is possible if the output connected to FB is also skewed. Since "Zero Skew", $+t_U$, and $-t_U$ are defined relative to output groups, and since the PLL aligns the rising edges of REF and FB, you can create wider output skews by proper selection of the × Fn inputs. For example, a +10 t_U between REF and 3Qx is achieved by connecting 1Q0 to FB and setting 1F0 = 1F1 = GND, 3F0 = MID, and 3F1 = High. (Since FB aligns at $-4t_U$ and 3Qx skews to $+6t_U$, a total of $+10t_U$ skew is realized.) Many other configurations are realized by skewing both the outputs used as the FB input and skewing the other outputs.

Figure 6. Inverted Output Connections

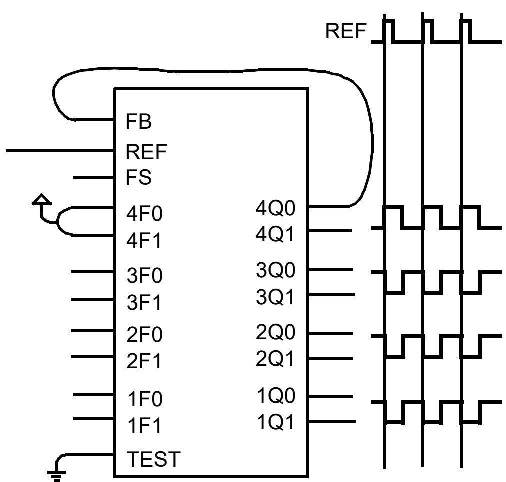


Figure 6 shows an example of the invert function of the PSCB. In this example the 4Q0 output used as the FB input is programmed for invert (4F0 = 4F1 = HIGH) while the other three pairs of outputs are programmed for zero skew. When 4F0 and 4F1 are tied high, 4Q0 and 4Q1 become inverted zero phase outputs. The PLL aligns the rising edge of the FB input with the rising edge of the REF. This causes the 1Q, 2Q, and 3Q outputs to become the "inverted" outputs with respect to the REF input. It is possible to have 2 inverted and 6 non-inverted outputs or 6 inverted and 2 non-inverted outputs by selecting the output connected to FB. The correct configuration is determined by the need for more (or fewer) inverted outputs. 1Q, 2Q, and 3Q outputs can also be skewed to compensate for varying trace delays independent of inversion on 4Q.

Figure 7. Frequency Multiplier with Skew Connections

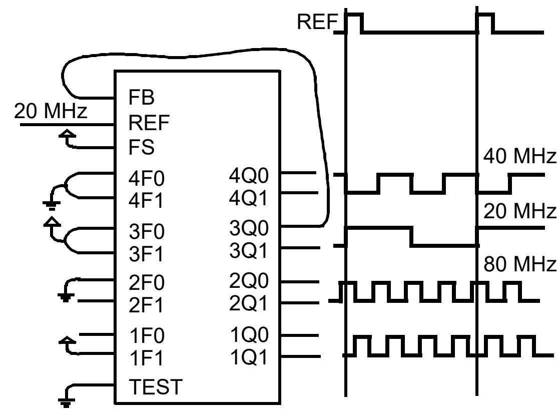


Figure 7 shows the PSCB configured as a clock multiplier. The 3Q0 output is programmed to divide by four and is sent to FB. This causes the PLL to increase its frequency until the 3Q0 and 3Q1 outputs are locked at 20 MHz while the 1Qx and 2Qx outputs run at 80 MHz. The 4Q0 and 4Q1 outputs are programmed to divide by two, that results in a 40 MHz waveform at these outputs. Note that the 20 and 40 MHz clocks fall simultaneously and are out of phase on their rising edge. This enables the designer to use the rising edges of the $\frac{1}{2}$ frequency and $\frac{1}{4}$ frequency outputs without concern for rising edge skew. The 2Q0, 2Q1, 1Q0, and 1Q1 outputs run at 80 MHz and are skewed by programming their select inputs accordingly. Note that the FS pin is wired for 80 MHz operation because that is the frequency of the fastest output.

Figure 8. Frequency Divider Connections

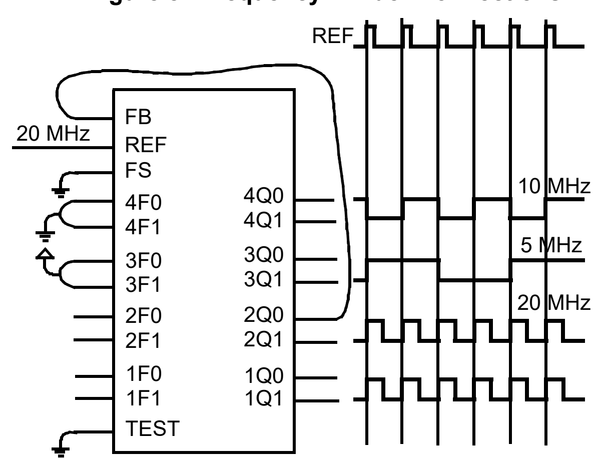
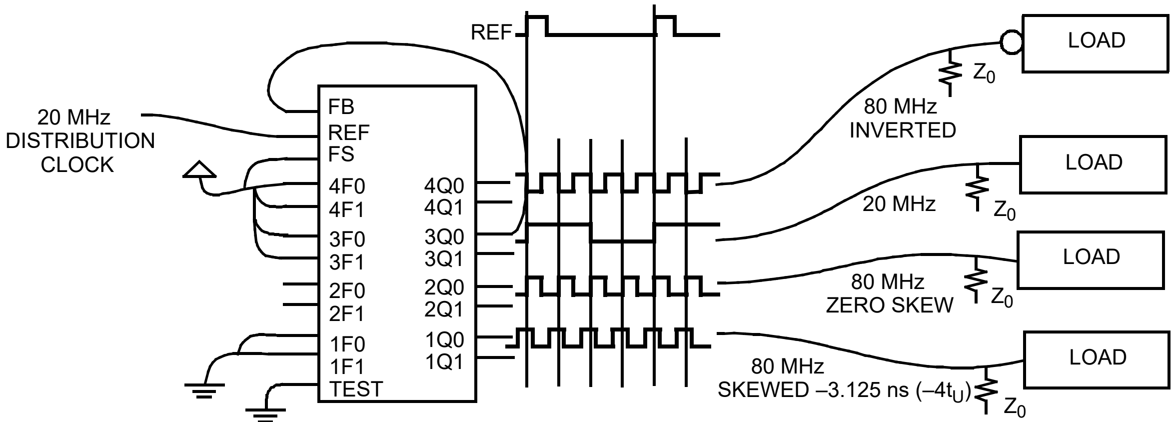


Figure 8 demonstrates the PSCB in a clock divider application. 2Q0 is fed back to the FB input and programmed for zero skew. 3Qx is programmed to divide by four. 4Qx is programmed to divide by two. Note that the falling edges of the 4Qx and 3Qx outputs are aligned. This enables the use of rising edges of the $\frac{1}{2}$ frequency and $\frac{1}{4}$ frequency without concern for skew mismatch. The 1Qx outputs are programmed to zero skew and are aligned with the 2Qx outputs. In this example, the FS input is grounded to configure the device in the 15 MHz to 30 MHz range since the highest frequency output is running at 20 MHz. Figure 9 shows some of the functions that are selectable on the 3Qx and 4Qx outputs. These include inverted outputs and outputs that offer divide-by-2 and divide-by-4 timing. An inverted output enables the system designer to clock different subsystems on opposite edges, without suffering from the pulse asymmetry typical of non-ideal loading. This function enables each of the two subsystems to clock 180 degrees out of phase and align within the skew specifications.

The divided outputs offer a zero delay divider for portions of the system that need the clock divided by either two or four, and still remain within a narrow skew of the “1X” clock. Without this feature, an external divider is added, and the propagation delay of the divider adds to the skew between the different clock signals.

These divided outputs, coupled with the Phase Locked Loop, enables the PSCB to multiply the clock rate at the REF input by either two or four. This mode enables the designer to distribute a low frequency clock between various portions of the system, and then locally multiply the clock rate to a more suitable frequency, still maintaining the low skew characteristics of the clock driver. The PSCB performs all of the functions described in this section at the same time. It multiplies by two and four or divides by two (and four) at the same time. In other words, it is shifting its outputs over a wide range or maintaining zero skew between selected outputs.

Figure 9. Multi-Function Clock Driver



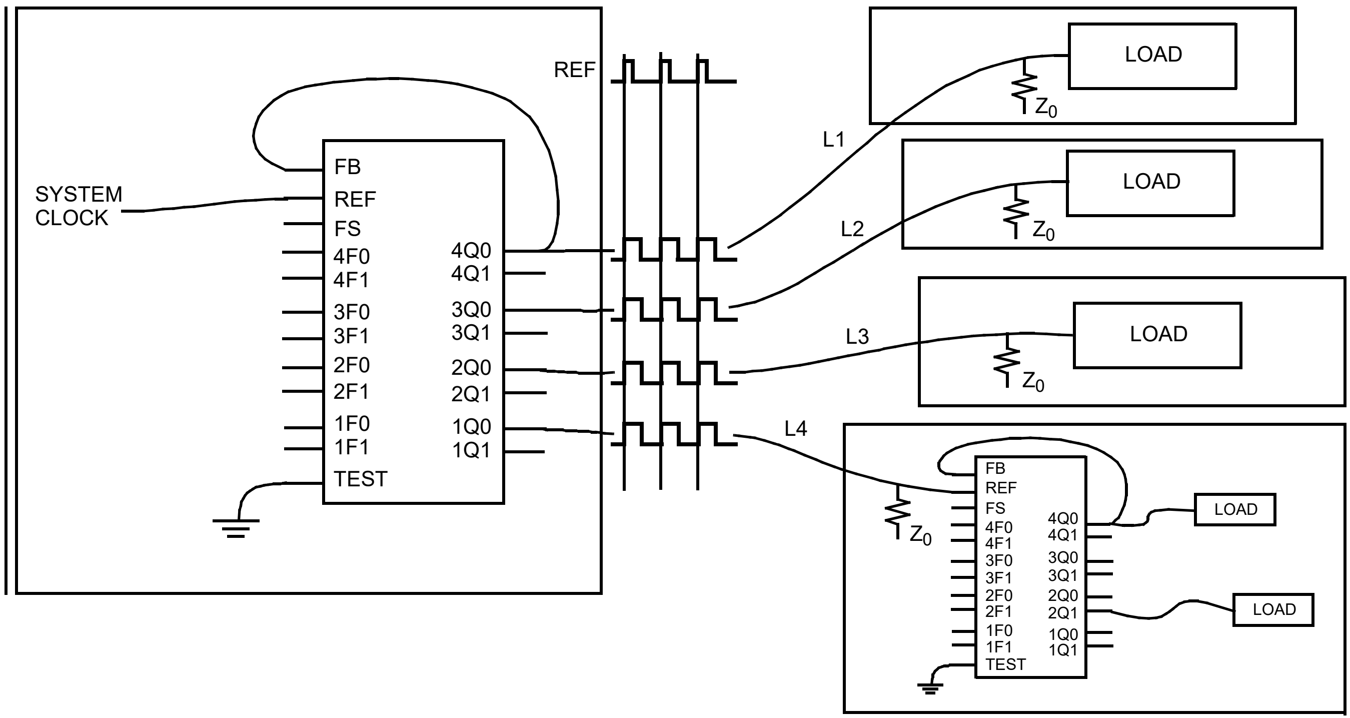


Figure 10. Board-to-Board Clock Distribution

Figure 10 shows the CY7B991 and 992 connected in series to construct a zero skew clock distribution tree between boards. Delays of the downstream clock buffers are programmed to compensate for the wire length (that is, select negative skew equal to the wire delay) necessary to connect them to the master clock source, approximating a zero delay clock tree. Cascaded clock buffers accumulates low frequency jitter because of the non-ideal filtering characteristics of the PLL filter. Do not connect more than two clock buffers in series.

Ordering Information

Accuracy (ps)	Ordering Code	Package Type	Operating Range
500	CY7B991-5JI	32-pin PLCC	Industrial
	CY7B991-5JIT	32-pin PLCC - Tape and Reel	Industrial
750	CY7B991-7JI	32-pin PLCC	Industrial
750	CY7B992-7JI	32-pin PLCC	Industrial
Pb-free			
250	CY7B991-2JXC	32-pin PLCC	Commercial
	CY7B991-2JXCT	32-pin PLCC - Tape and Reel	Commercial
500	CY7B991-5JXC	32-pin PLCC	Commercial
	CY7B991-5JXCT	32-pin PLCC - Tape and Reel	Commercial
	CY7B991-5JXI	32-pin PLCC	Industrial
	CY7B991-5JXIT	32-pin PLCC - Tape and Reel	Industrial
750	CY7B991-7JXC	32-pin PLCC	Commercial
	CY7B991-7JXCT	32-pin PLCC - Tape and Reel	Commercial
	CY7B991-7JXI	32-pin PLCC	Industrial
500	CY7B992-5JXI (Not Recommended for New Designs)	32-pin PLCC	Industrial
	CY7B992-5JXIT	32-pin PLCC - Tape and Reel	Industrial

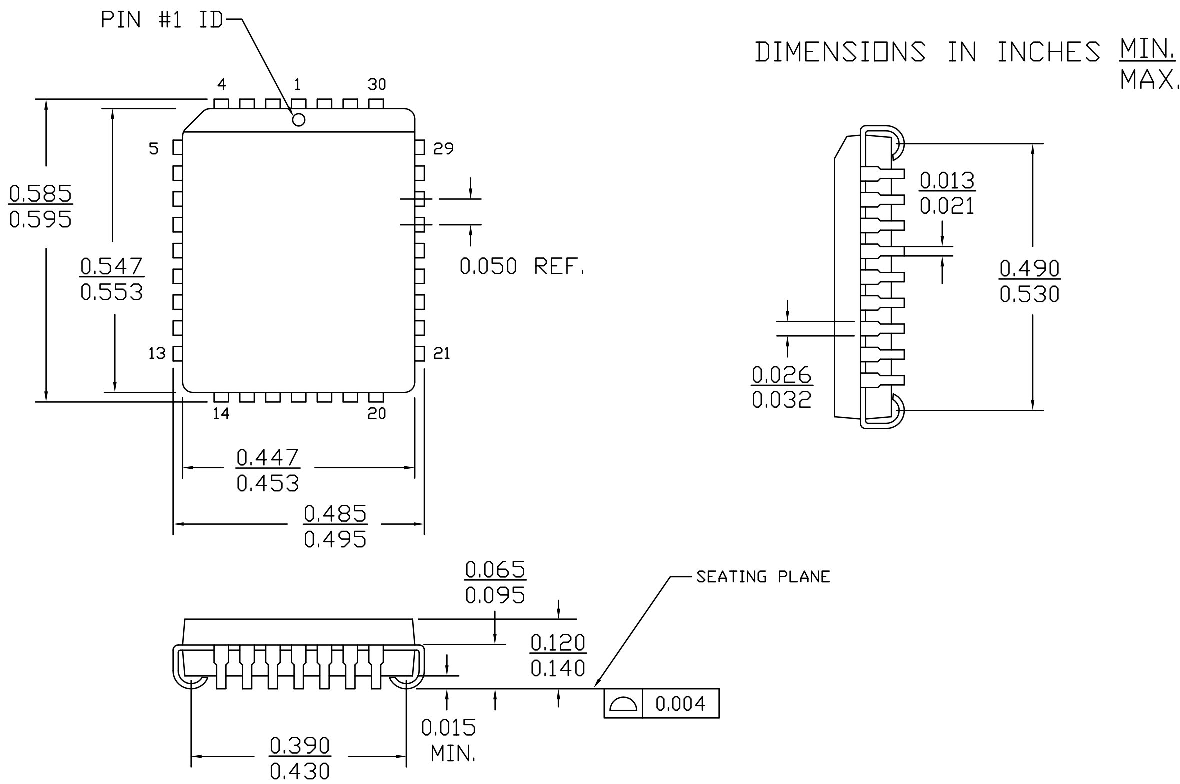
Ordering Code Definitions

CY 7B99X - X J X X X

- X = blank or T
  blank = Tube; T = Tape and Reel
- Temperature: X = C or I
  C = Commercial; I = Industrial
- X = Pb-free; blank = not Pb-free
- Package Type: J = 32-pin PLCC package
- Speed grade: X = 2 ps or 5 ps or 7 ps, based on propagation delay
- Base part number: 7B99X = 7B991 or 7B992
  7B991 = Clock buffer with TTL outputs
  7B992 = Clock buffer with CMOS outputs
- Company ID: CY = Cypress

Package Diagram

Figure 11. 32-pin PLCC (0.453 × 0.553 inches) J32 Package Outline, 51-85002



51-85002 *E

Acronyms

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
FB	Feedback
PLCC	Plastic Leaded Chip Carrier
PLL	Phase-Locked Loop
PSCB	Programmable Skew Clock Buffers
TTL	Transistor-Transistor Logic
VCO	Voltage Controlled Oscillator

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
µA	microampere
mA	milliampere
ms	millisecond
mW	milliwatt
ns	nanosecond
Ω	ohm
%	percent
pF	picofarad
ps	picosecond
V	volt

Document History Page

Rev.	ECN	Orig. of Change	Submission Date	Description of Change
Document Title: CY7B991/CY7B992, Programmable Skew Clock Buffer Document Number: 38-07138				
**	110247	SZV	12/19/2001	Changed specification number from 38-00513 to 38-07138.
*A	1199925	KVM / AESA	06/29/2007	Updated Features: Removed “Compatible with a Pentium™-based processor”. Updated Ordering Information: Removed “Package Name” column. Replaced “Lead” with “Pb” in “Package Type” column. Updated part numbers. Added Note “Not recommended for the new design.” and referred the same note in CY7B991-7LMB, CY7B992-5JI and CY7B992-7LMB. Updated to new template.
*B	1286064	AESA	07/18/2007	Changed status from Preliminary to Final.
*C	2750166	TSAI	08/10/2009	Minor change: Post to external web.
*D	2761988	CXQ	09/10/2009	Updated Ordering Information: No change in part numbers. Fixed typo error (Replaced “Pb” with “Pin” in “Package Type” column).
*E	2894960	KVM	03/18/2010	Updated Ordering Information: Updated part numbers. Removed Note “Not recommended for the new design.” and its reference. Updated Package Diagram: spec 51-85002 – Changed revision from *B to *C. Updated to new template.
*F	2905889	KVM	04/06/2010	Updated Ordering Information: Updated part numbers.
*G	2950368	KVM	06/11/2010	Updated Operating Range: Removed Military Temperature Range. Updated Ordering Information: Updated part numbers. Removed “Military Specifications”. Removed “DC Characteristics”.
*H	3045340	BASH	10/07/2010	Updated Ordering Information: Updated part numbers. Added Ordering Code Definitions.
*I	3201434	BASH	03/21/2011	Added Acronyms and Units of Measure. Completing Sunset Review.
*J	3560698	PURU	03/24/2012	Updated Ordering Information: Updated part numbers. Updated Package Diagram: spec 51-85002 – Changed revision from *C to *D.
*K	4334627	CINM	04/06/2014	Updated to new template. Completing Sunset Review.
*L	4403827	AJU	06/10/2014	Updated Ordering Information: No change in part numbers. Added “(Not Recommended for New Designs)” next to the MPN “CY7B992-5JXI” in “Ordering Code” column.
*M	4570101	AJU	11/14/2014	Updated Functional Description: Added “For a complete list of related documentation, click here.” at the end. Updated Ordering Information: Updated part numbers.

Document History Page (continued)

Document Title: CY7B991/CY7B992, Programmable Skew Clock Buffer Document Number: 38-07138				
Rev.	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
*N	5259008	PSR	05/04/2016	Updated Features: Replaced “32-pin PLCC/LCC package” with “32-pin PLCC package”. Updated Electrical Characteristics: Updated Note 7 (Replaced “FC = F < C” with “FC = F × C”). Added Thermal Resistance. Updated Package Diagram: spec 51-85002 – Changed revision from *D to *E. Updated to new template.
*O	6143627	XHT	04/18/2018	Updated to new template. Completing Sunset Review.

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