

Features

- Powerful Harvard-architecture processor
 - M8C processor speeds up to 24 MHz
 - Two 8 × 8 multiply, 32-bit accumulate
 - 3.15 to 5.25-V operating voltage
 - USB 2.0 USB-IF certified. TID# 40000110
 - Commercial operating temperature range: 0 °C to +70 °C
 - Industrial operating temperature range: -40 °C to +85 °C
- Advanced peripherals (enCoRe™ III blocks)
 - Six analog enCoRe III blocks provide:
 - Up to 14-bit incremental and delta sigma analog-to-digital converters (ADCs)
 - Programmable threshold comparator
 - Four digital enCoRe III blocks provide:
 - 8-bit and 16-bit pulse width modulators (PWMs), timers, and counters
 - I²C master
 - SPI master or slave
 - Full-duplex universal asynchronous receiver-transmitter (UART)
 - CYFISNP modules to talk to Cypress CYFI™ radio
- Complex peripherals by combining blocks
- Full-speed USB (12 Mbps)
 - Four unidirectional endpoints
 - One bidirectional control endpoint
 - Dedicated 256-byte buffer
 - No external crystal required
 - Operational at 3.15 V to 3.5 V or 4.35 V to 5.25 V
- Flexible on-chip memory
 - 16 KB flash program storage 50,000 erase/write cycles
 - 1 KB SRAM data storage
 - In-system serial programming (ISSP)
 - Partial flash updates
 - Flexible protection modes
 - EEPROM emulation in flash
- Programmable pin configurations
 - 25 mA sink on all general purpose I/Os (GPIOs)
 - Pull-up, Pull-down, high Z, strong, or open drain drive modes on all GPIOs
 - Configurable interrupt on all GPIOs
- Precision, programmable clocking
 - Internal ±4% 24- and 48-MHz oscillator with support for external clock oscillator
 - Internal oscillator for watchdog and sleep
 - .25% accuracy for USB with no external components
- Additional system resources
 - Inter-integrated circuit (I²C) slave, master, and multimaster to 400 kHz
 - Watchdog and sleep timers
 - User-configurable low-voltage detection (LVD)
 - Integrated supervisory circuit
 - On-chip precision voltage reference
- Complete development tools
 - Free development software (PSoC® Designer™)
 - Full-featured, in-circuit emulator and programmer
 - Full-speed emulation
 - Complex breakpoint structure
 - 128 KB trace memory

Block Diagram



Errata: For information on silicon errata, see "Errata" on page 40. Details include trigger conditions, devices affected, and proposed workaround.

Contents

| | | | |
|--|-----------|--|-----------|
| Applications | 3 | Operating Temperature | 13 |
| enCoRe III Functional Overview | 3 | DC Electrical Characteristics | 14 |
| enCoRe III Core | 3 | AC Electrical Characteristics | 24 |
| The Digital System | 3 | Packaging Information | 30 |
| The Analog System | 4 | Package Diagrams | 30 |
| Additional System Resources | 4 | Thermal Impedance | 32 |
| enCoRe III Device Characteristics | 4 | Solder Reflow Peak Temperature | 32 |
| Getting Started | 5 | Ordering Information | 33 |
| Application Notes | 5 | Ordering Code Definitions | 33 |
| Development Kits | 5 | Acronyms | 34 |
| Training | 5 | Acronyms Used | 34 |
| CYPros Consultants | 5 | Reference Documents | 34 |
| Solutions Library | 5 | Document Conventions | 35 |
| Technical Support | 5 | Units of Measure | 35 |
| Development Tools | 5 | Numeric Conventions | 35 |
| PSoC Designer Software Subsystems | 5 | Glossary | 35 |
| Designing with PSoC Designer | 6 | Errata | 40 |
| Select Components | 6 | Part Numbers Affected | 40 |
| Configure Components | 6 | CY7C64215 Qualification Status | 40 |
| Organize and Connect | 6 | CY7C64215 Errata Summary | 40 |
| Generate, Verify, and Debug | 6 | Document History Page | 43 |
| Pin Information | 7 | Sales, Solutions, and Legal Information | 45 |
| 56-Pin Part Pinout | 7 | Worldwide Sales and Design Support | 45 |
| 28-Pin Part Pinout | 8 | Products | 45 |
| Register Reference | 9 | PSoC® Solutions | 45 |
| Register Mapping Tables | 9 | Cypress Developer Community | 45 |
| Register Map Bank 0 Table: User Space | 10 | Technical Support | 45 |
| Register Map Bank 1 Table: Configuration Space | 11 | | |
| Electrical Specifications | 12 | | |
| Absolute Maximum Ratings | 13 | | |

Applications

- PC human interface devices
 - Mouse (optomechanical, optical, trackball)
 - Keyboards
 - Joysticks
- Gaming
 - Game pads
 - Console keyboards
- General purpose
 - Barcode scanners
 - POS terminal
 - Consumer electronics
 - Toys
 - Remote controls
 - USB to serial

enCoRe III Functional Overview

The enCoRe III is based on the flexible PSoC architecture and is a full-featured, full-speed (12-Mbps) USB part. Configurable analog, digital, and interconnect circuitry enable a high level of integration in a host of consumer, and communication applications.

This architecture enables the user to create customized peripheral configurations that match the requirements of each individual application. Additionally, a fast CPU, flash program memory, SRAM data memory, and configurable I/O are included in both 28-pin SSOP and 56-pin QFN packages.

enCoRe III architecture, as illustrated in the “Block Diagram” on page 1, is comprised of four main areas: enCoRe III core, digital system, analog system, and system resources including a full-speed USB port. Configurable global busing enables all the device resources to combine into a complete custom system. The enCoRe III CY7C64215 can have up to seven I/O ports that connect to the global digital and analog interconnects, providing access to four digital blocks and six analog blocks.

enCoRe III Core

The enCoRe III Core is a powerful engine that supports a rich feature set. The core includes a CPU, memory, clocks, and configurable GPIOs.

The M8C CPU core is a powerful processor with speeds up to 24 MHz, providing a four-million instructions per second (MIPS) 8-bit Harvard-architecture microprocessor. The CPU uses an interrupt controller with up to 20 vectors, to simplify programming of real-time embedded events. Program execution is timed and protected using the included sleep and watchdog timers (WDT).

Memory encompasses 16 KB of flash for program storage, 1 KB of SRAM for data storage, and up to 2 KB of EEPROM emulated using the flash. Program flash uses four protection levels on blocks of 64 bytes, enabling customized software IP protection.

enCoRe III incorporates flexible internal clock generators, including a 24-MHz internal main oscillator (IMO) accurate to 8% over temperature and voltage as well as an option for an external clock oscillator (ECO). USB operation requires the OSC LOCK bit of the USB_CR0 register to be set to obtain IMO accuracy to.25%.

The 24-MHz IMO is doubled to 48 MHz for use by the digital system, if needed. The 48-MHz clock is required to clock the USB block and must be enabled for communication. A low-power 32-kHz internal low-speed oscillator (ILO) is provided for the sleep timer and WDT. The clocks, together with programmable clock dividers (system resource), provide flexibility to integrate almost any timing requirement into enCoRe III. In USB systems, the IMO self-tunes to ±0.25% accuracy for USB communication.

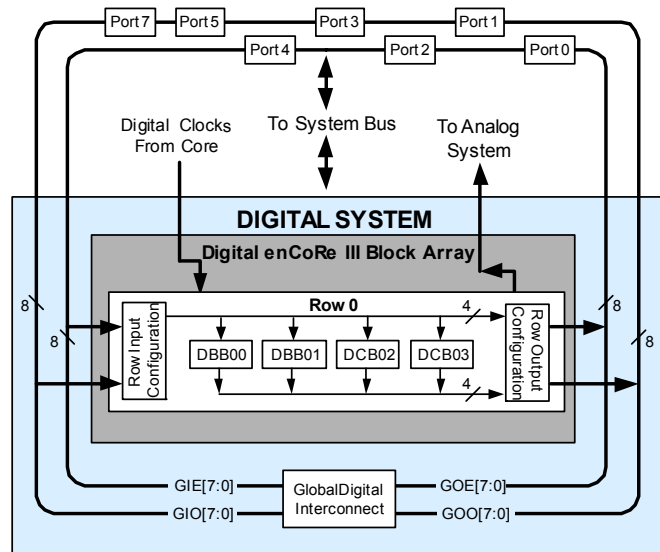
The extended temperature range for the industrial operating range (–40 °C to +85 °C) requires the use of an ECO, which is only available on the 56-pin QFN package.

enCoRe III GPIOs provide connection to the CPU, digital and analog resources of the device. Each pin’s drive mode may be selected from eight options, enabling great flexibility in external interfacing. Every pin also has capability to generate a system interrupt on high-level, low-level, and change from last read.

The Digital System

The digital system is composed of four digital enCoRe III blocks. Each block is an 8-bit resource that is used alone or combined with other blocks to form 8-, 16-, 24-, and 32-bit peripherals, which are called user module references.

Figure 1. Digital System Block Diagram



The following digital configurations can be built from the blocks:

- PWMs, timers, and counters (8-bit and 16-bit)
- UART 8-bit with selectable parity
- SPI master and slave
- I²C master
- RF interface: Interface to Cypress CYFI radio

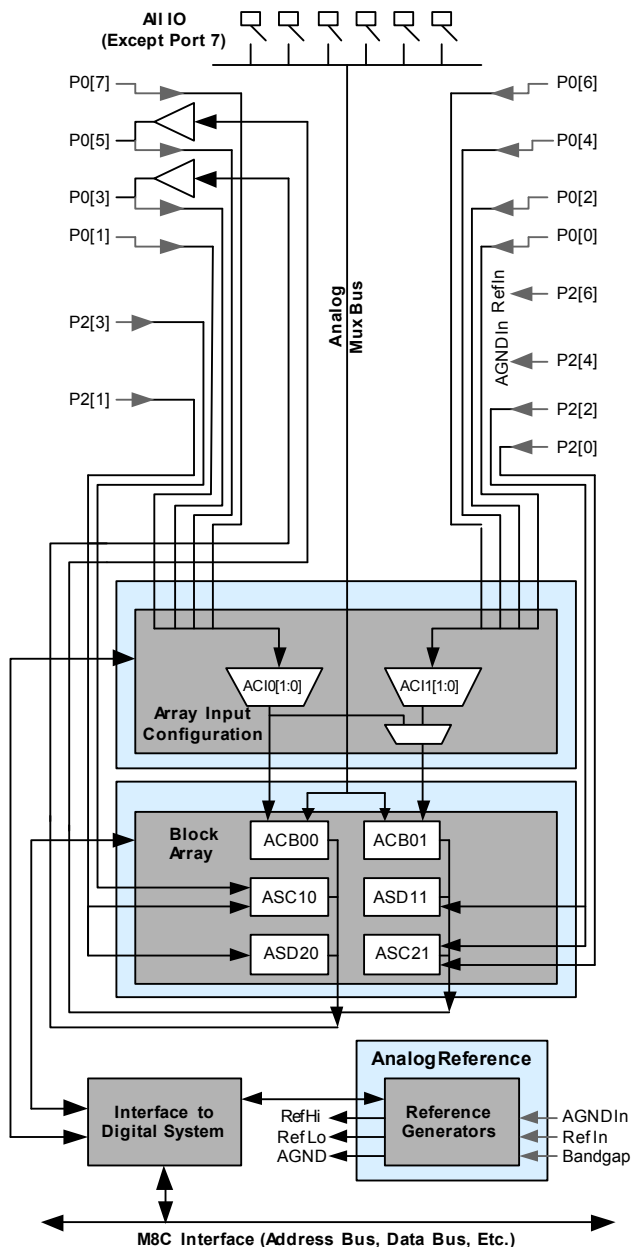
The digital blocks are connected to any GPIO through a series of global buses that can route any signal to any pin. The buses also enable signal multiplexing and performing logic operations. This configurability frees your designs from the constraints of a fixed peripheral controller.

The Analog System

The analog system is composed of six configurable blocks, comprised of an opamp circuit enabling the creation of complex analog signal flows. Analog peripherals are very flexible and are customized to support specific application requirements. enCoRe III analog function supports the Analog-to-digital converters (with 6- to 14-bit resolution, selectable as incremental, and delta-sigma) and programmable threshold comparator).

Analog blocks are arranged in two columns of three, with each column comprising one continuous time (CT) - AC B00 or AC B01 - and two switched capacitor (SC) - ASC10 and ASD20 or ASD11 and ASC21 - blocks, as shown in Figure 2.

Figure 2. Analog System Block Diagram



The Analog Multiplexer System

The analog mux bus can connect to every GPIO pin in ports 0 to 5. Pins are connected to the bus individually or in any combination. The bus also connects to the analog system for analysis with comparators and analog-to-digital converters. It is split into two sections for simultaneous dual-channel processing. An additional 8:1 analog input multiplexer provides a second path to bring Port 0 pins to the analog array.

Additional System Resources

System resources provide additional capability useful to complete systems. Additional resources include a multiplier, decimator, low voltage detection, and power-on reset. Brief statements describing the merits of each resource follow.

- Full-speed USB (12 Mbps) with five configurable endpoints and 256 bytes of RAM. No external components required except two series resistors. Industrial temperature operating range for USB requires an external clock oscillator.
- Two multiply accumulates (MACs) provide fast 8-bit multipliers with 32-bit accumulate, to assist in both general math and digital filters.
- The decimator provides a custom hardware filter for digital signal processing applications including the creation of delta-sigma ADCs.
- Digital clock dividers provide three customizable clock frequencies for use in applications. The clocks are routed to both the digital and analog systems.
- The I²C module provides 100- and 400-kHz communication over two wires. Slave, master, and multimaster modes are all supported.
- LVD interrupts can signal the application of falling voltage levels, while the advanced power-on reset (POR) circuit eliminates the need for a system supervisor.

enCoRe III Device Characteristics

enCoRe III devices have four digital blocks and six analog blocks. The following table lists the resources available for specific enCoRe III devices.

Table 1. enCoRe III Device Characteristics

| Part Number | Digital I/O | Digital Rows | Digital Blocks | Analog Inputs | Analog Outputs | Analog Columns | Analog Blocks | SRAM Size | Flash Size |
|------------------|-------------|--------------|----------------|---------------|----------------|----------------|---------------|-----------|------------|
| CY7C64215 28 Pin | up to 22 | 1 | 4 | 22 | 2 | 2 | 6 | 1K | 16K |
| CY7C64215 56 Pin | up to 50 | 1 | 4 | 48 | 2 | 2 | 6 | 1K | 16K |

Getting Started

The quickest path to understanding the enCoRe III silicon is by reading this datasheet and using the PSoC Designer Integrated Development Environment (IDE). This datasheet is an overview of the enCoRe V integrated circuit and presents specific pin, register, and electrical specifications.

For in-depth information, along with detailed programming details, see the PSoC® [Technical Reference Manual](#).

For up-to-date ordering, packaging, and electrical specification information, see the latest [PSoC device datasheets](#) on the web.

Application Notes

[Cypress application notes](#) are an excellent introduction to the wide variety of possible PSoC designs.

Development Kits

[PSoC Development Kits](#) are available online from and through a growing number of regional and global distributors, which include Arrow, Avnet, Digi-Key, Farnell, Future Electronics, and Newark.

Training

[Free PSoC technical training](#) (on demand, webinars, and workshops), which is available online via www.cypress.com, covers a wide variety of topics and skill levels to assist you in your designs.

CYPros Consultants

Certified PSoC consultants offer everything from technical assistance to completed PSoC designs. To contact or become a PSoC consultant go to the [CYPros Consultants](#) web site.

Solutions Library

Visit our growing [library of solution focused designs](#). Here you can find various application designs that include firmware and hardware design files that enable you to complete your designs quickly.

Technical Support

[Technical support](#) – including a searchable Knowledge Base articles and technical forums – is also available online. If you cannot find an answer to your question, call our Technical Support hotline at 1-800-541-4736.

Development Tools

PSoC Designer™ is the revolutionary integrated design environment (IDE) that you can use to customize PSoC to meet your specific application requirements. PSoC Designer software accelerates system design and time to market. Develop your applications using a library of precharacterized analog and digital peripherals (called user modules) in a drag-and-drop design environment. Then, customize your design by leveraging the dynamically generated application programming interface (API) libraries of code. Finally, debug and test your designs with the integrated debug environment, including in-circuit emulation and standard software debug features. PSoC Designer includes:

- Application editor graphical user interface (GUI) for device and user module configuration and dynamic reconfiguration
- Extensive user module catalog
- Integrated source-code editor (C and assembly)
- Free C compiler with no size restrictions or time limits
- Built-in debugger
- In-circuit emulation
- Built-in support for communication interfaces:
 - Hardware and software I²C slaves and masters
 - Full-speed USB 2.0
 - Up to four full-duplex universal asynchronous receiver/transmitters (UARTs), SPI master and slave, and wireless

PSoC Designer supports the entire library of PSoC 1 devices and runs on Windows XP, Windows Vista, and Windows 7.

PSoC Designer Software Subsystems

Design Entry

In the chip-level view, choose a base device to work with. Then select different onboard analog and digital components that use the PSoC blocks, which are called user modules. Examples of user modules are ADCs, DACs, amplifiers, and filters. Configure the user modules for your chosen application and connect them to each other and to the proper pins. Then generate your project. This prepopulates your project with APIs and libraries that you can use to program your application.

The tool also supports easy development of multiple configurations and dynamic reconfiguration. Dynamic reconfiguration makes it possible to change configurations at run time. In essence, this allows you to use more than 100 percent of PSoC's resources for an application.

Code Generation Tools

The code generation tools work seamlessly within the PSoC Designer interface and have been tested with a full range of debugging tools. You can develop your design in C, assembly, or a combination of the two.

Assemblers. The assemblers allow you to merge assembly code seamlessly with C code. Link libraries automatically use absolute addressing or are compiled in relative mode, and are linked with other software modules to get absolute addressing.

C Language Compilers. C language compilers are available that support the PSoC family of devices. The products allow you to create complete C programs for the PSoC family devices. The optimizing C compilers provide all of the features of C, tailored to the PSoC architecture. They come complete with embedded libraries providing port and bus operations, standard keypad and display support, and extended math functionality.

Debugger

PSoC Designer has a debug environment that provides hardware in-circuit emulation, allowing you to test the program in a physical system while providing an internal view of the PSoC device. Debugger commands allow you to read and program and read and write data memory, and read and write I/O registers. You can read and write CPU registers, set and clear breakpoints,

and provide program run, halt, and step control. The debugger also allows you to create a trace buffer of registers and memory locations of interest.

Online Help System

The online help system displays online, context-sensitive help. Designed for procedural and quick reference, each functional subsystem has its own context-sensitive help. This system also provides tutorials and links to FAQs and an online support Forum to aid the designer.

In-Circuit Emulator

A low-cost, high-functionality in-circuit emulator (ICE) is available for development support. This hardware can program single devices.

The emulator consists of a base unit that connects to the PC using a USB port. The base unit is universal and operates with all PSoC devices. Emulation pods for each device family are available separately. The emulation pod takes the place of the PSoC device in the target board and performs full-speed (24 MHz) operation.

Designing with PSoC Designer

The development process for the PSoC device differs from that of a traditional fixed function microprocessor. The configurable analog and digital hardware blocks give the PSoC architecture a unique flexibility that pays dividends in managing specification change during development and by lowering inventory costs. These configurable resources, called PSoC Blocks, have the ability to implement a wide variety of user-selectable functions.

The PSoC development process can be summarized in the following four steps:

1. Select [User Modules](#)
2. Configure User Modules
3. Organize and Connect
4. Generate, Verify, and Debug

Select Components

PSoC Designer provides a library of pre-built, pre-tested hardware peripheral components called “user modules”. User modules make selecting and implementing peripheral devices, both analog and digital, simple.

Configure Components

Each of the User Modules you select establishes the basic register settings that implement the selected function. They also provide parameters and properties that allow you to tailor their

precise configuration to your particular application. For example, a PWM User Module configures one or more

digital PSoC blocks, one for each 8 bits of resolution. The user module parameters permit you to establish the pulse width and duty cycle. Configure the parameters and properties to correspond to your chosen application. Enter values directly or by selecting values from drop-down menus. All the user modules are documented in datasheets that may be viewed directly in PSoC Designer or on the Cypress website. These [user module datasheets](#) explain the internal operation of the User Module and provide performance specifications. Each datasheet describes the use of each user module parameter, and other information you may need to successfully implement your design.

Organize and Connect

You build signal chains at the chip level by interconnecting user modules to each other and the I/O pins. You perform the selection, configuration, and routing so that you have complete control over all on-chip resources.

Generate, Verify, and Debug

When you are ready to test the hardware configuration or move on to developing code for the project, you perform the “Generate Configuration Files” step. This causes PSoC Designer to generate source code that automatically configures the device to your specification and provides the software for the system. The generated code provides application programming interfaces (APIs) with high-level functions to control and respond to hardware events at run time and interrupt service routines that you can adapt as needed.

A complete code development environment allows you to develop and customize your applications in C, assembly language, or both.

The last step in the development process takes place inside PSoC Designer's Debugger (access by clicking the Connect icon). PSoC Designer downloads the HEX image to the ICE where it runs at full speed. PSoC Designer debugging capabilities rival those of systems costing many times more. In addition

to traditional single-step, run-to-breakpoint and watch-variable features, the debug interface provides a large trace buffer and allows you to define complex breakpoint events that include monitoring address and data bus values, memory locations and external signals.

Pin Information

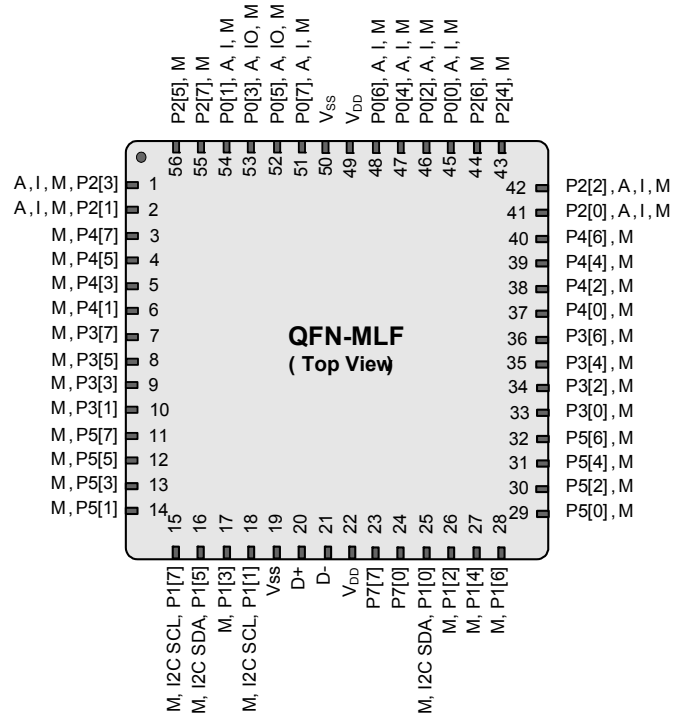
56-Pin Part Pinout

The CY7C64215 enCoRe III device is available in a 56-pin package which is listed and illustrated in the following table. Every port pin (labeled “P”) is capable of digital I/O. However, V_{SS} and V_{DD} are not capable of digital I/O.

Table 2. 56-Pin Part Pinout (QFN-MLF SAWN)^[1]

| Pin No. | Type | | Name | Description |
|---------|---------|--------|-----------------|--|
| | Digital | Analog | | |
| 1 | I/O | I, M | P2[3] | Direct switched capacitor block input. |
| 2 | I/O | I, M | P2[1] | Direct switched capacitor block input. |
| 3 | I/O | M | P4[7] | |
| 4 | I/O | M | P4[5] | |
| 5 | I/O | M | P4[3] | |
| 6 | I/O | M | P4[1] | |
| 7 | I/O | M | P3[7] | |
| 8 | I/O | M | P3[5] | |
| 9 | I/O | M | P3[3] | |
| 10 | I/O | M | P3[1] | |
| 11 | I/O | M | P5[7] | |
| 12 | I/O | M | P5[5] | |
| 13 | I/O | M | P5[3] | |
| 14 | I/O | M | P5[1] | |
| 15 | I/O | M | P1[7] | I ² C serial clock (SCL). |
| 16 | I/O | M | P1[5] | I ² C serial data (SDA). |
| 17 | I/O | M | P1[3] | |
| 18 | I/O | M | P1[1] | I ² C SCL, ISSP-SCLK. |
| 19 | Power | | V _{SS} | Ground connection. |
| 20 | USB | | D+ | |
| 21 | USB | | D- | |
| 22 | Power | | V _{DD} | Supply voltage. |
| 23 | I/O | | P7[7] | |
| 24 | I/O | | P7[0] | |
| 25 | I/O | M | P1[0] | I ² C SDA, ISSP-SDATA. |
| 26 | I/O | M | P1[2] | |
| 27 | I/O | M | P1[4] | Optional external clock input EXTCLK. |
| 28 | I/O | M | P1[6] | |
| 29 | I/O | M | P5[0] | |
| 30 | I/O | M | P5[2] | |
| 31 | I/O | M | P5[4] | |
| 32 | I/O | M | P5[6] | |
| 33 | I/O | M | P3[0] | |
| 34 | I/O | M | P3[2] | |
| 35 | I/O | M | P3[4] | |
| 36 | I/O | M | P3[6] | |
| 37 | I/O | M | P4[0] | |
| 38 | I/O | M | P4[2] | |
| 39 | I/O | M | P4[4] | |
| 40 | I/O | M | P4[6] | |
| 41 | I/O | I, M | P2[0] | Direct switched capacitor block input. |
| 42 | I/O | I, M | P2[2] | Direct switched capacitor block input. |
| 43 | I/O | M | P2[4] | External analog ground (AGND) input. |
| 44 | I/O | M | P2[6] | External voltage reference (VREF) input. |
| 45 | I/O | I, M | P0[0] | Analog column mux input. |
| 46 | I/O | I, M | P0[2] | Analog column mux input and column output. |
| 47 | I/O | I, M | P0[4] | Analog column mux input and column output. |
| 48 | I/O | I, M | P0[6] | Analog column mux input. |
| 49 | Power | | V _{DD} | Supply voltage. |
| 50 | Power | | V _{SS} | Ground connection. |
| 51 | I/O | I, M | P0[7] | Analog column mux input. |
| 52 | I/O | I/O, M | P0[5] | Analog column mux input and column output |
| 53 | I/O | I/O, M | P0[3] | Analog column mux input and column output. |
| 54 | I/O | I, M | P0[1] | Analog column mux input. |
| 55 | I/O | M | P2[7] | |
| 56 | I/O | M | P2[5] | |

Figure 3. CY7C64215 56-Pin enCoRe III Device



| Pin No. | Type | | Name | Description |
|---------|---------|--------|-----------------|--|
| | Digital | Analog | | |
| 44 | I/O | M | P2[6] | External voltage reference (VREF) input. |
| 45 | I/O | I, M | P0[0] | Analog column mux input. |
| 46 | I/O | I, M | P0[2] | Analog column mux input and column output. |
| 47 | I/O | I, M | P0[4] | Analog column mux input and column output. |
| 48 | I/O | I, M | P0[6] | Analog column mux input. |
| 49 | Power | | V _{DD} | Supply voltage. |
| 50 | Power | | V _{SS} | Ground connection. |
| 51 | I/O | I, M | P0[7] | Analog column mux input. |
| 52 | I/O | I/O, M | P0[5] | Analog column mux input and column output |
| 53 | I/O | I/O, M | P0[3] | Analog column mux input and column output. |
| 54 | I/O | I, M | P0[1] | Analog column mux input. |
| 55 | I/O | M | P2[7] | |
| 56 | I/O | M | P2[5] | |

LEGEND A = Analog, I = Input, O = Output, and M = Analog Mux Input.

Note

1. The center pad on the QFN-MLF package should be connected to ground (V_{SS}) for best mechanical, thermal, and electrical performance. If not connected to ground, it should be electrically floated and not connected to any other signal.

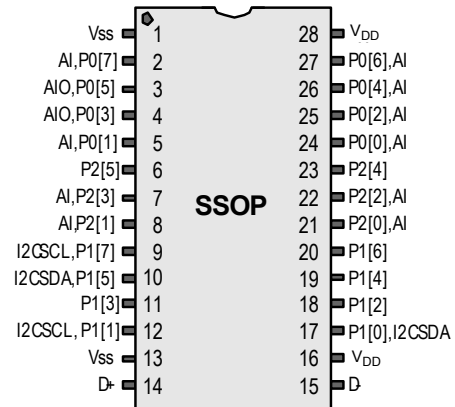
28-Pin Part Pinout

The CY7C64215 enCoRe III device is available in a 28-pin package which is listed and illustrated in the following table. Every port pin (labeled with a “P”) is capable of digital I/O. However, V_{SS} and V_{DD} are not capable of digital I/O.

Table 3. 28-Pin Part Pinout (SSOP)

| Pin No. | Type | | Name | Description |
|---------|---------|--------|-----------------|--|
| | Digital | Analog | | |
| 1 | Power | | GND | Ground connection. |
| 2 | I/O | I, M | P0[7] | Analog column mux input. |
| 3 | I/O | I/O,M | P0[5] | Analog column mux input and column output. |
| 4 | I/O | I/O,M | P0[3] | Analog column mux input and column output. |
| 5 | I/O | I,M | P0[1] | Analog column mux input. |
| 6 | I/O | M | P2[5] | |
| 7 | I/O | M | P2[3] | Direct switched capacitor block input. |
| 8 | I/O | M | P2[1] | Direct switched capacitor block input. |
| 9 | I/O | M | P1[7] | I ² C SCL |
| 10 | I/O | M | P1[5] | I ² C SDA |
| 11 | I/O | M | P1[3] | |
| 12 | I/O | M | P1[1] | I ² C SCL, ISSP-SCLK. |
| 13 | Power | | GND | Ground connection. |
| 14 | USB | | D+ | |
| 15 | USB | | D- | |
| 16 | Power | | V _{DD} | Supply voltage. |
| 17 | I/O | M | P1[0] | I ² C SCL, ISSP-SDATA. |
| 18 | I/O | M | P1[2] | |
| 19 | I/O | M | P1[4] | |
| 20 | I/O | M | P1[6] | |
| 21 | I/O | M | P2[0] | Direct switched capacitor block input. |
| 22 | I/O | M | P2[2] | Direct switched capacitor block input. |
| 23 | I/O | M | P2[4] | External analog ground (AGND) input. |
| 24 | I/O | M | P0[0] | Analog column mux input. |
| 25 | I/O | M | P0[2] | Analog column mux input and column output. |
| 26 | I/O | M | P0[4] | Analog column mux input and column output. |
| 27 | I/O | M | P0[6] | Analog column mux input. |
| 28 | Power | | V _{DD} | Supply voltage. |

Figure 4. CY7C64215 28-Pin enCoRe III Device



LEGEND A = Analog, I = Input, O = Output, and M = Analog Mux Input.

Register Reference

The register conventions specific to this section are listed in the following table.

Table 4. Register Conventions

| Convention | Description |
|------------|------------------------------|
| R | Read register or bit(s) |
| W | Write register or bit(s) |
| L | Logical register or bit(s) |
| C | Clearable register or bit(s) |
| # | Access is bit specific |

Register Mapping Tables

The enCoRe III device has a total register address space of 512 bytes. The register space is referred to as I/O space and is divided into two banks, bank 0 and bank 1. The XO1 bit in the Flag register (CPU_F) determines which bank the user is currently in. When the XO1 bit is set to '1', the user is in bank 1.

Note In the following register mapping tables, blank fields are reserved and should not be accessed.

Register Map Bank 0 Table: User Space

| Name | Addr (0,Hex) | Access | Name | Addr (0,Hex) | Access | Name | Addr (0,Hex) | Access | Name | Addr (0,Hex) | Access |
|----------|--------------|--------|-----------|--------------|--------|----------|--------------|--------|----------|--------------|--------|
| PRT0DR | 00 | RW | PMA0_DR | 40 | RW | ASC10CR0 | 80 | RW | | C0 | |
| PRT0IE | 01 | RW | PMA1_DR | 41 | RW | ASC10CR1 | 81 | RW | | C1 | |
| PRT0GS | 02 | RW | PMA2_DR | 42 | RW | ASC10CR2 | 82 | RW | | C2 | |
| PRT0DM2 | 03 | RW | PMA3_DR | 43 | RW | ASC10CR3 | 83 | RW | | C3 | |
| PRT1DR | 04 | RW | PMA4_DR | 44 | RW | ASD11CR0 | 84 | RW | | C4 | |
| PRT1IE | 05 | RW | PMA5_DR | 45 | RW | ASD11CR1 | 85 | RW | | C5 | |
| PRT1GS | 06 | RW | PMA6_DR | 46 | RW | ASD11CR2 | 86 | RW | | C6 | |
| PRT1DM2 | 07 | RW | PMA7_DR | 47 | RW | ASD11CR3 | 87 | RW | | C7 | |
| PRT2DR | 08 | RW | USB_SOF0 | 48 | R | | 88 | | | C8 | |
| PRT2IE | 09 | RW | USB_SOF1 | 49 | R | | 89 | | | C9 | |
| PRT2GS | 0A | RW | USB_CR0 | 4A | RW | | 8A | | | CA | |
| PRT2DM2 | 0B | RW | USBIO_CR0 | 4B | # | | 8B | | | CB | |
| PRT3DR | 0C | RW | USBIO_CR1 | 4C | RW | | 8C | | | CC | |
| PRT3IE | 0D | RW | | 4D | | | 8D | | | CD | |
| PRT3GS | 0E | RW | EP1_CNT1 | 4E | # | | 8E | | | CE | |
| PRT3DM2 | 0F | RW | EP1_CNT | 4F | RW | | 8F | | | CF | |
| PRT4DR | 10 | RW | EP2_CNT1 | 50 | # | ASD20CR0 | 90 | RW | CUR_PP | D0 | RW |
| PRT4IE | 11 | RW | EP2_CNT | 51 | RW | ASD20CR1 | 91 | RW | STK_PP | D1 | RW |
| PRT4GS | 12 | RW | EP3_CNT1 | 52 | # | ASD20CR2 | 92 | RW | | D2 | |
| PRT4DM2 | 13 | RW | EP3_CNT | 53 | RW | ASD20CR3 | 93 | RW | IDX_PP | D3 | RW |
| PRT5DR | 14 | RW | EP4_CNT1 | 54 | # | ASC21CR0 | 94 | RW | MVR_PP | D4 | RW |
| PRT5IE | 15 | RW | EP4_CNT | 55 | RW | ASC21CR1 | 95 | RW | MVW_PP | D5 | RW |
| PRT5GS | 16 | RW | EP0_CR | 56 | # | ASC21CR2 | 96 | RW | I2C_CFG | D6 | RW |
| PRT5DM2 | 17 | RW | EP0_CNT | 57 | # | ASC21CR3 | 97 | RW | I2C_SCR | D7 | # |
| | 18 | | EP0_DR0 | 58 | RW | | 98 | | I2C_DR | D8 | RW |
| | 19 | | EP0_DR1 | 59 | RW | | 99 | | I2C_MSCR | D9 | # |
| | 1A | | EP0_DR2 | 5A | RW | | 9A | | INT_CLR0 | DA | RW |
| | 1B | | EP0_DR3 | 5B | RW | | 9B | | INT_CLR1 | DB | RW |
| PRT7DR | 1C | RW | EP0_DR4 | 5C | RW | | 9C | | INT_CLR2 | DC | RW |
| PRT7IE | 1D | RW | EP0_DR5 | 5D | RW | | 9D | | INT_CLR3 | DD | RW |
| PRT7GS | 1E | RW | EP0_DR6 | 5E | RW | | 9E | | INT_MSK3 | DE | RW |
| PRT7DM2 | 1F | RW | EP0_DR7 | 5F | RW | | 9F | | INT_MSK2 | DF | RW |
| DBB00DR0 | 20 | # | AMX_IN | 60 | RW | | A0 | | INT_MSK0 | E0 | RW |
| DBB00DR1 | 21 | W | AMUXCFG | 61 | RW | | A1 | | INT_MSK1 | E1 | RW |
| DBB00DR2 | 22 | RW | | 62 | | | A2 | | INT_VC | E2 | RC |
| DBB00CR0 | 23 | # | ARF_CR | 63 | RW | | A3 | | RES_WDT | E3 | W |
| DBB01DR0 | 24 | # | CMP_CR0 | 64 | # | | A4 | | DEC_DH | E4 | RC |
| DBB01DR1 | 25 | W | ASY_CR | 65 | # | | A5 | | DEC_DL | E5 | RC |
| DBB01DR2 | 26 | RW | CMP_CR1 | 66 | RW | | A6 | | DEC_CR0 | E6 | RW |
| DBB01CR0 | 27 | # | | 67 | | | A7 | | DEC_CR1 | E7 | RW |
| DCB02DR0 | 28 | # | | 68 | | MUL1_X | A8 | W | MUL0_X | E8 | W |
| DCB02DR1 | 29 | W | | 69 | | MUL1_Y | A9 | W | MUL0_Y | E9 | W |
| DCB02DR2 | 2A | RW | | 6A | | MUL1_DH | AA | R | MUL0_DH | EA | R |
| DCB02CR0 | 2B | # | | 6B | | MUL1_DL | AB | R | MUL0_DL | EB | R |
| DCB03DR0 | 2C | # | TMP_DR0 | 6C | RW | ACC1_DR1 | AC | RW | ACC0_DR1 | EC | RW |
| DCB03DR1 | 2D | W | TMP_DR1 | 6D | RW | ACC1_DR0 | AD | RW | ACC0_DR0 | ED | RW |
| DCB03DR2 | 2E | RW | TMP_DR2 | 6E | RW | ACC1_DR3 | AE | RW | ACC0_DR3 | EE | RW |
| DCB03CR0 | 2F | # | TMP_DR3 | 6F | RW | ACC1_DR2 | AF | RW | ACC0_DR2 | EF | RW |
| | 30 | | ACB00CR3 | 70 | RW | RDI0RI | B0 | RW | | F0 | |
| | 31 | | ACB00CR0 | 71 | RW | RDI0SYN | B1 | RW | | F1 | |
| | 32 | | ACB00CR1 | 72 | RW | RDI0IS | B2 | RW | | F2 | |
| | 33 | | ACB00CR2 | 73 | RW | RDI0LT0 | B3 | RW | | F3 | |
| | 34 | | ACB01CR3 | 74 | RW | RDI0LT1 | B4 | RW | | F4 | |
| | 35 | | ACB01CR0 | 75 | RW | RDI0RO0 | B5 | RW | | F5 | |
| | 36 | | ACB01CR1 | 76 | RW | RDI0RO1 | B6 | RW | | F6 | |
| | 37 | | ACB01CR2 | 77 | RW | | B7 | | CPU_F | F7 | RL |
| | 38 | | | 78 | | | B8 | | | F8 | |
| | 39 | | | 79 | | | B9 | | | F9 | |
| | 3A | | | 7A | | | BA | | | FA | |
| | 3B | | | 7B | | | BB | | | FB | |
| | 3C | | | 7C | | | BC | | | FC | |
| | 3D | | | 7D | | | BD | | DAC_D | FD | RW |
| | 3E | | | 7E | | | BE | | CPU_SCR1 | FE | # |
| | 3F | | | 7F | | | BF | | CPU_SCR0 | FF | # |

Blank fields are Reserved and should not be accessed.

Access is bit specific.

Register Map Bank 1 Table: Configuration Space

| Name | Addr (1,Hex) | Access | Name | Addr (1,Hex) | Access | Name | Addr (1,Hex) | Access | Name | Addr (1,Hex) | Access |
|---------|--------------|--------|-----------|--------------|--------|----------|--------------|--------|-----------|--------------|--------|
| PRT0DM0 | 00 | RW | PMA0_WA | 40 | RW | ASC10CR0 | 80 | RW | USBIO_CR2 | C0 | RW |
| PRT0DM1 | 01 | RW | PMA1_WA | 41 | RW | ASC10CR1 | 81 | RW | USB_CR1 | C1 | # |
| PRT0IC0 | 02 | RW | PMA2_WA | 42 | RW | ASC10CR2 | 82 | RW | | | |
| PRT0IC1 | 03 | RW | PMA3_WA | 43 | RW | ASC10CR3 | 83 | RW | | | |
| PRT1DM0 | 04 | RW | PMA4_WA | 44 | RW | ASD11CR0 | 84 | RW | EP1_CR0 | C4 | # |
| PRT1DM1 | 05 | RW | PMA5_WA | 45 | RW | ASD11CR1 | 85 | RW | EP2_CR0 | C5 | # |
| PRT1IC0 | 06 | RW | PMA6_WA | 46 | RW | ASD11CR2 | 86 | RW | EP3_CR0 | C6 | # |
| PRT1IC1 | 07 | RW | PMA7_WA | 47 | RW | ASD11CR3 | 87 | RW | EP4_CR0 | C7 | # |
| PRT2DM0 | 08 | RW | | 48 | | | 88 | | | C8 | |
| PRT2DM1 | 09 | RW | | 49 | | | 89 | | | C9 | |
| PRT2IC0 | 0A | RW | | 4A | | | 8A | | | CA | |
| PRT2IC1 | 0B | RW | | 4B | | | 8B | | | CB | |
| PRT3DM0 | 0C | RW | | 4C | | | 8C | | | CC | |
| PRT3DM1 | 0D | RW | | 4D | | | 8D | | | CD | |
| PRT3IC0 | 0E | RW | | 4E | | | 8E | | | CE | |
| PRT3IC1 | 0F | RW | | 4F | | | 8F | | | CF | |
| PRT4DM0 | 10 | RW | PMA0_RA | 50 | RW | | 90 | | GDI_O_IN | D0 | RW |
| PRT4DM1 | 11 | RW | PMA1_RA | 51 | RW | ASD20CR1 | 91 | RW | GDI_E_IN | D1 | RW |
| PRT4IC0 | 12 | RW | PMA2_RA | 52 | RW | ASD20CR2 | 92 | RW | GDI_O_OU | D2 | RW |
| PRT4IC1 | 13 | RW | PMA3_RA | 53 | RW | ASD20CR3 | 93 | RW | GDI_E_OU | D3 | RW |
| PRT5DM0 | 14 | RW | PMA4_RA | 54 | RW | ASC21CR0 | 94 | RW | | D4 | |
| PRT5DM1 | 15 | RW | PMA5_RA | 55 | RW | ASC21CR1 | 95 | RW | | D5 | |
| PRT5IC0 | 16 | RW | PMA6_RA | 56 | RW | ASC21CR2 | 96 | RW | | D6 | |
| PRT5IC1 | 17 | RW | PMA7_RA | 57 | RW | ASC21CR3 | 97 | RW | | D7 | |
| | 18 | | | 58 | | | 98 | | MUX_CR0 | D8 | RW |
| | 19 | | | 59 | | | 99 | | MUX_CR1 | D9 | RW |
| | 1A | | | 5A | | | 9A | | MUX_CR2 | DA | RW |
| | 1B | | | 5B | | | 9B | | MUX_CR3 | DB | RW |
| PRT7DM0 | 1C | RW | | 5C | | | 9C | | | DC | |
| PRT7DM1 | 1D | RW | | 5D | | | 9D | | OSC_GO_EN | DD | RW |
| PRT7IC0 | 1E | RW | | 5E | | | 9E | | OSC_CR4 | DE | RW |
| PRT7IC1 | 1F | RW | | 5F | | | 9F | | OSC_CR3 | DF | RW |
| DBB00FN | 20 | RW | CLK_CR0 | 60 | RW | | A0 | | OSC_CR0 | E0 | RW |
| DBB00IN | 21 | RW | CLK_CR1 | 61 | RW | | A1 | | OSC_CR1 | E1 | RW |
| DBB00OU | 22 | RW | ABF_CR0 | 62 | RW | | A2 | | OSC_CR2 | E2 | RW |
| | 23 | | AMD_CR0 | 63 | RW | | A3 | | VLT_CR | E3 | RW |
| DBB01FN | 24 | RW | CMP_GO_EN | 64 | RW | | A4 | | VLT_CMP | E4 | R |
| DBB01IN | 25 | RW | | 65 | RW | | A5 | | | E5 | |
| DBB01OU | 26 | RW | AMD_CR1 | 66 | RW | | A6 | | | E6 | |
| | 27 | | ALT_CR0 | 67 | RW | | A7 | | | E7 | |
| DCB02FN | 28 | RW | | 68 | | | A8 | | IMO_TR | E8 | W |
| DCB02IN | 29 | RW | | 69 | | | A9 | | ILO_TR | E9 | W |
| DCB02OU | 2A | RW | | 6A | | | AA | | BDG_TR | EA | RW |
| | 2B | | | 6B | | | AB | | ECO_TR | EB | W |
| DCB03FN | 2C | RW | TMP_DR0 | 6C | RW | | AC | | MUX_CR4 | EC | RW |
| DCB03IN | 2D | RW | TMP_DR1 | 6D | RW | | AD | | MUX_CR5 | ED | RW |
| DCB03OU | 2E | RW | TMP_DR2 | 6E | RW | | AE | | | EE | |
| | 2F | | TMP_DR3 | 6F | RW | | AF | | | EF | |
| | 30 | | ACB00CR3 | 70 | RW | RDI0RI | B0 | RW | | F0 | |
| | 31 | | ACB00CR0 | 71 | RW | RDI0SYN | B1 | RW | | F1 | |
| | 32 | | ACB00CR1 | 72 | RW | RDI0IS | B2 | RW | | F2 | |
| | 33 | | ACB00CR2 | 73 | RW | RDI0LT0 | B3 | RW | | F3 | |
| | 34 | | ACB01CR3 | 74 | RW | RDI0LT1 | B4 | RW | | F4 | |
| | 35 | | ACB01CR0 | 75 | RW | RDI0RO0 | B5 | RW | | F5 | |
| | 36 | | ACB01CR1 | 76 | RW | RDI0RO1 | B6 | RW | | F6 | |
| | 37 | | ACB01CR2 | 77 | RW | | B7 | | CPU_F | F7 | RL |
| | 38 | | | 78 | | | B8 | | | F8 | |
| | 39 | | | 79 | | | B9 | | | F9 | |
| | 3A | | | 7A | | | BA | | | FA | |
| | 3B | | | 7B | | | BB | | | FB | |
| | 3C | | | 7C | | | BC | | | FC | |
| | 3D | | | 7D | | | BD | | DAC_CR | FD | RW |
| | 3E | | | 7E | | | BE | | CPU_SCR1 | FE | # |
| | 3F | | | 7F | | | BF | | CPU_SCR0 | FF | # |

Blank fields are Reserved and should not be accessed.

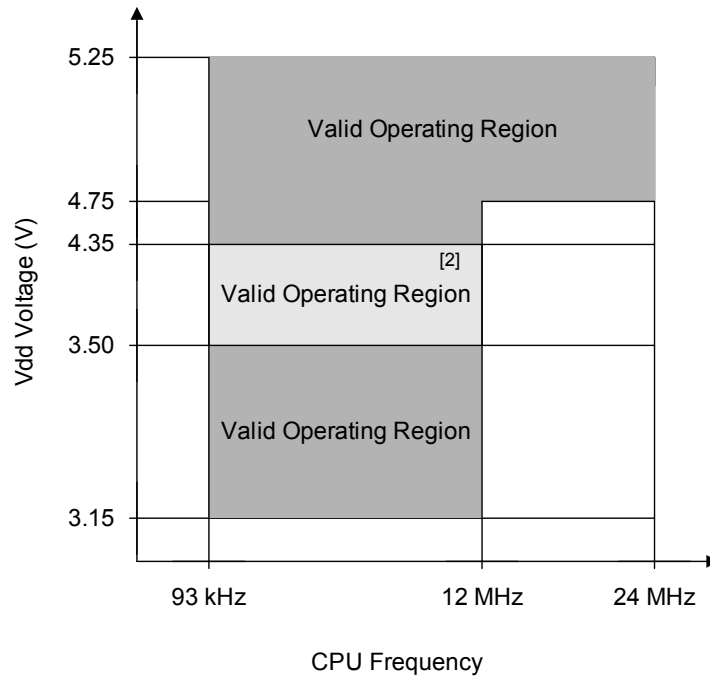
Access is bit specific.

Electrical Specifications

This section presents the DC and AC electrical specifications of the CY7C64215 enCoRe III. For the most up-to-date electrical specifications, confirm that you have the most recent datasheet by going to the web at <http://www.cypress.com/go/usb>.

Specifications are valid for $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$ and $T_J \leq 100\text{ }^{\circ}\text{C}$, except where noted. Specifications for devices running at greater than 12 MHz are valid for $-40\text{ }^{\circ}\text{C} \leq T_A \leq 70\text{ }^{\circ}\text{C}$ and $T_J \leq 82\text{ }^{\circ}\text{C}$.

Figure 5. Voltage versus CPU Frequency



Note

2. This is a valid operating region for the CPU, but USB hardware is non functional in the voltage range from 3.50 V to 4.35 V.

Absolute Maximum Ratings
Table 5. Absolute Maximum Ratings

| Parameter | Description | Min | Typ | Max | Unit | Notes |
|-----------------------|--|-----------------------|-----|-----------------------|-------|--|
| T _{STG} | Storage temperature | -55 | - | +100 | °C | Higher storage temperatures reduces data retention time. |
| T _{BAKETEMP} | Bake temperature | - | 125 | See package label | °C | - |
| T _{BAKETIME} | Bake time | See package label | - | 72 | Hours | - |
| T _A | Ambient temperature with power applied | 0 | - | +70 | °C | - |
| V _{DD} | Supply voltage on V _{DD} relative to V _{SS} | -0.5 | - | +6.0 | V | - |
| V _{IO} | DC input voltage | V _{SS} - 0.5 | - | V _{DD} + 0.5 | V | - |
| V _{IO2} | DC voltage applied to tristate | V _{SS} - 0.5 | - | V _{DD} + 0.5 | V | - |
| I _{MIO} | Maximum current into any port pin | -25 | - | +50 | mA | - |
| I _{MAIO} | Maximum current into any port pin configured as an analog driver | -50 | - | +50 | mA | - |
| ESD | Electrostatic discharge voltage | 2000 | - | - | V | Human body model ESD. |
| LU | Latch up current | - | - | 200 | mA | - |

Operating Temperature
Table 6. Operating Temperature

| Parameter | Description | Min | Typ | Max | Unit | Notes |
|-----------------|--------------------------------|-----|-----|------|------|---|
| T _{AC} | Commercial ambient temperature | 0 | - | +70 | °C | - |
| T _{AI} | Industrial ambient temperature | -40 | - | +85 | °C | USB operation requires the use of an external clock oscillator and the 56-pin QFN package. |
| T _J | Junction temperature | -40 | - | +100 | °C | The temperature rise from ambient to junction is package specific. See "Thermal Impedance" on page 32. The user must limit the power consumption to comply with this requirement. |

DC Electrical Characteristics

DC Chip-Level Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, or 3.15 V to 3.5 V and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 7. DC Chip-Level Specifications

| Parameter | Description | Min | Typ | Max | Unit | Notes |
|------------------|---|-----|-----|------|------|--|
| V _{DD} | Supply voltage | 3.0 | – | 5.25 | V | See DC POR and LVD specifications, Table 15 on page 22 . USB hardware is not functional when V _{DD} is between 3.5 V to 4.35 V. |
| I _{DD5} | Supply current, IMO = 24 MHz (5 V) | – | 14 | 27 | mA | Conditions are V _{DD} = 5.0 V, T _A = 25 °C, CPU = 3 MHz, SYSCLK doubler disabled, VC1 = 1.5 MHz, VC2 = 93.75 kHz, VC3 = 93.75 kHz, analog power = off. |
| I _{DD3} | Supply current, IMO = 24 MHz (3.3 V) | – | 8 | 14 | mA | Conditions are V _{DD} = 3.3 V, T _A = 25 °C, CPU = 3 MHz, SYSCLK doubler disabled, VC1 = 1.5 MHz, VC2 = 93.75 kHz, VC3 = 0.367 kHz, analog power = off. |
| I _{SB} | Sleep ^[3] (mode) current with POR, LVD, sleep timer, and WDT ^[4] . | – | 3 | 6.5 | μA | Conditions are with internal slow speed oscillator, V _{DD} = 3.3 V, 0 °C ≤ T _A ≤ 55 °C, analog power = off. |
| I _{SBH} | Sleep (mode) current with POR, LVD, sleep timer, and WDT at high temperature ^[4] . | – | 4 | 25 | μA | Conditions are with internal slow speed oscillator, V _{DD} = 3.3 V, 55 °C < T _A ≤ 70 °C, analog power = off. |

Notes

- Errata:** When the device operates at 4.75 V to 5.25 V and the 3.3-V regulator is enabled, a short low pulse may be created on the DP signal line during device wakeup. The 15- to 20-μs low pulse of the DP line may be interpreted by the host computer as a deattach or the beginning of a wakeup. For more details refer to [Errata on page 40](#).
- Standby current includes all functions (POR, LVD, WDT, sleep time) needed for reliable system operation. This should be compared with devices that have similar functions enabled.

DC GPIO Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, or 3.15 V to 3.5 V and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 8. DC GPIO Specifications

| Parameter | Description | Min | Typ | Max | Unit | Notes |
|------------------|-----------------------------------|-----------------------|-----|------|------|---|
| R _{PU} | Pull-up resistor | 4 | 5.6 | 8 | kΩ | – |
| R _{PD} | Pull-down resistor | 4 | 5.6 | 8 | kΩ | – |
| V _{OH} | High output level | V _{DD} – 1.0 | – | – | V | I _{OH} = 10 mA, V _{DD} = 4.75 to 5.25 V (8 total loads, 4 on even port pins (for example, P0[2], P1[4]), 4 on odd port pins (for example, P0[3], P1[5])). 80 mA maximum combined I _{OH} budget. |
| V _{OL} | Low output level | – | – | 0.75 | V | I _{OL} = 25 mA, V _{DD} = 4.75 to 5.25 V (8 total loads, 4 on even port pins (for example, P0[2], P1[4]), 4 on odd port pins (for example, P0[3], P1[5])). 150 mA maximum combined I _{OL} budget. |
| I _{OH} | High-level source current | 10 | – | – | mA | – |
| I _{OL} | Low-level sink current | 25 | – | – | mA | – |
| V _{IL} | Input low level | – | – | 0.8 | V | V _{DD} = 3.15 to 5.25. |
| V _{IH} | Input high level | 2.1 | – | – | V | V _{DD} = 3.15 to 5.25. |
| V _H | Input hysteresis | – | 60 | – | mV | – |
| I _{IL} | Input leakage (absolute value) | – | 1 | – | nA | Gross tested to 1 μA. |
| C _{IN} | Capacitive load on pins as input | – | 3.5 | 10 | pF | Package and pin dependent. Temp = 25 °C. |
| C _{OUT} | Capacitive load on pins as output | – | 3.5 | 10 | pF | Package and pin dependent. Temp = 25 °C. |

DC Full-Speed USB Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges when the IMO is selected as system clock: 4.75 V to 5.25 V and $0\text{ }^{\circ}\text{C} \leq T_A \leq 70\text{ }^{\circ}\text{C}$, or 3.15 V to 3.5 V and $0\text{ }^{\circ}\text{C} \leq T_A \leq 70\text{ }^{\circ}\text{C}$, respectively.

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges when an external clock is selected as the system clock: 4.75 V to 5.25 V and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, or 3.15 V to 3.5 V and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$.

Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 9. DC Full Speed (12 Mbps) USB Specifications

| Parameter | Description | Min | Typ | Max | Unit | Notes |
|----------------------|--------------------------------------|-----|-----|-----|------|---|
| USB Interface | | | | | | |
| V _{DI} | Differential input sensitivity | 0.2 | – | – | V | (D+) – (D–) |
| V _{CM} | Differential input common mode range | 0.8 | – | 2.5 | V | – |
| V _{SE} | Single-ended receiver threshold | 0.8 | – | 2.0 | V | – |
| C _{IN} | Transceiver capacitance | – | – | 20 | pF | – |
| I _{IO} | High Z state data line leakage | –10 | – | 10 | μA | 0 V < V _{IN} < 3.3 V. |
| R _{EXT} | External USB series resistor | 23 | – | 25 | Ω | In series with each USB pin. |
| V _{UOH} | Static output high, driven | 2.8 | – | 3.6 | V | 15 kΩ ± 5% to ground. Internal pull-up enabled. |
| V _{UOHI} | Static output high, idle | 2.7 | – | 3.6 | V | 15 kΩ ± 5% to ground. Internal pull-up enabled. |
| V _{UOL} | Static output low | – | – | 0.3 | V | 15 kΩ ± 5% to ground. Internal pull-up enabled. |
| Z _O | USB driver output impedance | 28 | – | 44 | Ω | Including R _{EXT} resistor. |
| V _{CRS} | D+/D– crossover voltage | 1.3 | – | 2.0 | V | – |

DC Analog Output Buffer Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, or 3.15 V to 3.5 V and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 10. 5 V DC Analog Output Buffer Specifications

| Parameter | Description | Min | Typ | Max | Unit | Notes |
|---------------|---|--|------------|--|--------------------------------|--|
| C_L | Load Capacitance | – | – | 200 | pF | This specification applies to the external circuit that is being driven by the analog output buffer. |
| V_{OSOB} | Input offset voltage (absolute value) | – | 3 | 12 | mV | – |
| TCV_{OSOB} | Average input offset voltage drift | – | +6 | – | $\mu\text{V}/^{\circ}\text{C}$ | – |
| V_{CMOB} | Common mode input voltage range | 0.5 | – | $V_{DD} - 1.0$ | V | – |
| R_{OUTOB} | Output resistance Power = low Power = high | – – | 0.6 0.6 | – – | W W | – |
| $V_{OHIGHOB}$ | High output voltage swing (Load = 32 ohms to $V_{DD}/2$) Power = low Power = high | $0.5 \times V_{DD} + 1.1$ $0.5 \times V_{DD} + 1.1$ | – – | – – | V V | – |
| V_{OLOWOB} | Low output voltage swing (Load = 32 ohms to $V_{DD}/2$) Power = low Power = high | – – | – – | $0.5 \times V_{DD} - 1.3$ $0.5 \times V_{DD} - 1.3$ | V V | – |
| I_{SOB} | Supply current including bias cell (no load) Power = low Power = high | – – | 1.1 2.6 | 5.1 8.8 | mA mA | – |
| $PSRR_{OB}$ | Supply voltage rejection ratio | 53 | 64 | – | dB | $(0.5 \times V_{DD} - 1.3) \leq V_{OUT} \leq (V_{DD} - 2.3)$. |

Table 11. 3.3 V DC Analog Output Buffer Specifications

| Parameter | Description | Min | Typ | Max | Unit | Notes |
|---------------|--|--|------------|--|--------------------------------|--|
| C_L | Load Capacitance | – | – | 200 | pF | This specification applies to the external circuit that is being driven by the analog output buffer. |
| V_{OSOB} | Input offset voltage (absolute value) | – | 3 | 12 | mV | – |
| TCV_{OSOB} | Average input offset voltage drift | – | +6 | – | $\mu\text{V}/^{\circ}\text{C}$ | – |
| V_{CMOB} | Common mode input voltage range | 0.5 | – | $V_{DD} - 1.0$ | V | – |
| R_{OUTOB} | Output resistance Power = low Power = high | – – | 1 1 | – – | W W | – |
| $V_{OHIGHOB}$ | High output voltage swing (Load = 1 K Ω to $V_{DD}/2$) Power = low Power = high | $0.5 \times V_{DD} + 1.0$ $0.5 \times V_{DD} + 1.0$ | – – | – – | V V | – |
| V_{OLOWOB} | Low output voltage swing (Load = 1 K Ω to $V_{DD}/2$) Power = low Power = high | – – | – – | $0.5 \times V_{DD} - 1.0$ $0.5 \times V_{DD} - 1.0$ | V V | – |
| I_{SOB} | Supply current including bias cell (no load) Power = low Power = high | – – | 0.8 2.0 | 2.0 4.3 | mA mA | – |
| $PSRR_{OB}$ | Supply voltage rejection ratio | 34 | 64 | – | dB | $(0.5 \times V_{DD} - 1.0) \leq V_{OUT} \leq (0.5 \times V_{DD} + 0.9)$. |

DC Analog Reference Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, or 3.15 V to 3.5 V and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

The guaranteed specifications are measured through the analog continuous time PSoC blocks. The power levels for AGND refer to the power of the Analog Continuous Time PSoC block. The power levels for RefHi and RefLo refer to the Analog Reference Control register. The limits stated for AGND include the offset error of the AGND buffer local to the Analog Continuous Time PSoC block. Reference control power is high.

Table 12. 5-V DC Analog Reference Specifications

| Reference ARF_CR [5:3] | Reference Power Settings | Symbol | Reference | Description | Min | Typ | Max | Units |
|------------------------|--|--------------------|-----------|---|----------------------------|----------------------------|----------------------------|-------|
| 0b000 | RefPower = high Opamp bias = high | V _{REFHI} | Ref High | V _{DD} /2 + Bandgap | V _{DD} /2 + 1.229 | V _{DD} /2 + 1.290 | V _{DD} /2 + 1.346 | V |
| | | V _{AGND} | AGND | V _{DD} /2 | V _{DD} /2 - 0.038 | V _{DD} /2 | V _{DD} /2 + 0.040 | V |
| | | V _{REFLO} | Ref Low | V _{DD} /2 - Bandgap | V _{DD} /2 - 1.356 | V _{DD} /2 - 1.295 | V _{DD} /2 - 1.218 | V |
| | RefPower = high Opamp bias = low | V _{REFHI} | Ref High | V _{DD} /2 + Bandgap | V _{DD} /2 + 1.220 | V _{DD} /2 + 1.292 | V _{DD} /2 + 1.348 | V |
| | | V _{AGND} | AGND | V _{DD} /2 | V _{DD} /2 - 0.036 | V _{DD} /2 | V _{DD} /2 + 0.036 | V |
| | | V _{REFLO} | Ref Low | V _{DD} /2 - Bandgap | V _{DD} /2 - 1.357 | V _{DD} /2 - 1.297 | V _{DD} /2 - 1.225 | V |
| | RefPower = medium Opamp bias = high | V _{REFHI} | Ref High | V _{DD} /2 + Bandgap | V _{DD} /2 + 1.221 | V _{DD} /2 + 1.293 | V _{DD} /2 + 1.351 | V |
| | | V _{AGND} | AGND | V _{DD} /2 | V _{DD} /2 - 0.036 | V _{DD} /2 | V _{DD} /2 + 0.036 | V |
| | | V _{REFLO} | Ref Low | V _{DD} /2 - Bandgap | V _{DD} /2 - 1.357 | V _{DD} /2 - 1.298 | V _{DD} /2 - 1.228 | V |
| | RefPower = medium Opamp bias = low | V _{REFHI} | Ref High | V _{DD} /2 + Bandgap | V _{DD} /2 + 1.219 | V _{DD} /2 + 1.293 | V _{DD} /2 + 1.353 | V |
| | | V _{AGND} | AGND | V _{DD} /2 | V _{DD} /2 - 0.037 | V _{DD} /2 - 0.001 | V _{DD} /2 + 0.036 | V |
| | | V _{REFLO} | Ref Low | V _{DD} /2 - Bandgap | V _{DD} /2 - 1.359 | V _{DD} /2 - 1.299 | V _{DD} /2 - 1.229 | V |
| 0b001 | RefPower = high Opamp bias = high | V _{REFHI} | Ref High | P2[4]+P2[6] (P2[4] = V _{DD} /2, P2[6] = 1.3 V) | P2[4] + P2[6] - 0.092 | P2[4] + P2[6] - 0.011 | P2[4] + P2[6] + 0.064 | V |
| | | V _{AGND} | AGND | P2[4] | P2[4] | P2[4] | P2[4] | - |
| | | V _{REFLO} | Ref Low | P2[4]-P2[6] (P2[4] = V _{DD} /2, P2[6] = 1.3 V) | P2[4] - P2[6] - 0.031 | P2[4] - P2[6] + 0.007 | P2[4] - P2[6] + 0.056 | V |
| | RefPower = high Opamp bias = low | V _{REFHI} | Ref High | P2[4]+P2[6] (P2[4] = V _{DD} /2, P2[6] = 1.3 V) | P2[4] + P2[6] - 0.078 | P2[4] + P2[6] - 0.008 | P2[4] + P2[6] + 0.063 | V |
| | | V _{AGND} | AGND | P2[4] | P2[4] | P2[4] | P2[4] | - |
| | | V _{REFLO} | Ref Low | P2[4]-P2[6] (P2[4] = V _{DD} /2, P2[6] = 1.3 V) | P2[4] - P2[6] - 0.031 | P2[4] - P2[6] + 0.004 | P2[4] - P2[6] + 0.043 | V |
| | RefPower = medium Opamp bias = high | V _{REFHI} | Ref High | P2[4]+P2[6] (P2[4] = V _{DD} /2, P2[6] = 1.3 V) | P2[4] + P2[6] - 0.073 | P2[4] + P2[6] - 0.006 | P2[4] + P2[6] + 0.062 | V |
| | | V _{AGND} | AGND | P2[4] | P2[4] | P2[4] | P2[4] | - |
| | | V _{REFLO} | Ref Low | P2[4]-P2[6] (P2[4] = V _{DD} /2, P2[6] = 1.3 V) | P2[4] - P2[6] - 0.032 | P2[4] - P2[6] + 0.003 | P2[4] - P2[6] + 0.038 | V |
| | RefPower = medium Opamp bias = low | V _{REFHI} | Ref High | P2[4]+P2[6] (P2[4] = V _{DD} /2, P2[6] = 1.3 V) | P2[4] + P2[6] - 0.073 | P2[4] + P2[6] - 0.006 | P2[4] + P2[6] + 0.062 | V |
| | | V _{AGND} | AGND | P2[4] | P2[4] | P2[4] | P2[4] | - |
| | | V _{REFLO} | Ref Low | P2[4]-P2[6] (P2[4] = V _{DD} /2, P2[6] = 1.3 V) | P2[4] - P2[6] - 0.034 | P2[4] - P2[6] + 0.002 | P2[4] - P2[6] + 0.037 | V |

Table 12. 5-V DC Analog Reference Specifications (continued)

| Reference ARF_CR [5:3] | Reference Power Settings | Symbol | Reference | Description | Min | Typ | Max | Units |
|------------------------|--|--------------------|-----------|--|----------------------------|----------------------------|----------------------------|-------|
| 0b010 | RefPower = high Opamp bias = high | V _{REFHI} | Ref High | V _{DD} | V _{DD} - 0.037 | V _{DD} - 0.007 | V _{DD} | V |
| | | V _{AGND} | AGND | V _{DD} /2 | V _{DD} /2 - 0.036 | V _{DD} /2 - 0.001 | V _{DD} /2 + 0.036 | V |
| | | V _{REFLO} | Ref Low | V _{SS} | V _{SS} | V _{SS} + 0.005 | V _{SS} + 0.029 | V |
| | RefPower = high Opamp bias = low | V _{REFHI} | Ref High | V _{DD} | V _{DD} - 0.034 | V _{DD} - 0.006 | V _{DD} | V |
| | | V _{AGND} | AGND | V _{DD} /2 | V _{DD} /2 - 0.036 | V _{DD} /2 - 0.001 | V _{DD} /2 + 0.035 | V |
| | | V _{REFLO} | Ref Low | V _{SS} | V _{SS} | V _{SS} + 0.004 | V _{SS} + 0.024 | V |
| | RefPower = medium Opamp bias = high | V _{REFHI} | Ref High | V _{DD} | V _{DD} - 0.032 | V _{DD} - 0.005 | V _{DD} | V |
| | | V _{AGND} | AGND | V _{DD} /2 | V _{DD} /2 - 0.036 | V _{DD} /2 - 0.001 | V _{DD} /2 + 0.035 | V |
| | | V _{REFLO} | Ref Low | V _{SS} | V _{SS} | V _{SS} + 0.003 | V _{SS} + 0.022 | V |
| | RefPower = medium Opamp bias = low | V _{REFHI} | Ref High | V _{DD} | V _{DD} - 0.031 | V _{DD} - 0.005 | V _{DD} | V |
| | | V _{AGND} | AGND | V _{DD} /2 | V _{DD} /2 - 0.037 | V _{DD} /2 - 0.001 | V _{DD} /2 + 0.035 | V |
| | | V _{REFLO} | Ref Low | V _{SS} | V _{SS} | V _{SS} + 0.003 | V _{SS} + 0.020 | V |
| 0b011 | RefPower = high Opamp bias = high | V _{REFHI} | Ref High | 3 × Bandgap | 3.760 | 3.884 | 4.006 | V |
| | | V _{AGND} | AGND | 2 × Bandgap | 2.522 | 2.593 | 2.669 | V |
| | | V _{REFLO} | Ref Low | Bandgap | 1.252 | 1.299 | 1.342 | V |
| | RefPower = high Opamp bias = low | V _{REFHI} | Ref High | 3 × Bandgap | 3.766 | 3.887 | 4.010 | V |
| | | V _{AGND} | AGND | 2 × Bandgap | 2.523 | 2.594 | 2.670 | V |
| | | V _{REFLO} | Ref Low | Bandgap | 1.252 | 1.297 | 1.342 | V |
| | RefPower = medium Opamp bias = high | V _{REFHI} | Ref High | 3 × Bandgap | 3.769 | 3.888 | 4.013 | V |
| | | V _{AGND} | AGND | 2 × Bandgap | 2.523 | 2.594 | 2.671 | V |
| | | V _{REFLO} | Ref Low | Bandgap | 1.251 | 1.296 | 1.343 | V |
| | RefPower = medium Opamp bias = low | V _{REFHI} | Ref High | 3 × Bandgap | 3.769 | 3.889 | 4.015 | V |
| | | V _{AGND} | AGND | 2 × Bandgap | 2.523 | 2.595 | 2.671 | V |
| | | V _{REFLO} | Ref Low | Bandgap | 1.251 | 1.296 | 1.344 | V |
| 0b100 | RefPower = high Opamp bias = high | V _{REFHI} | Ref High | 2 × Bandgap + P2[6] (P2[6] = 1.3 V) | 2.483 - P2[6] | 2.582 - P2[6] | 2.674 - P2[6] | V |
| | | V _{AGND} | AGND | 2 × Bandgap | 2.522 | 2.593 | 2.669 | V |
| | | V _{REFLO} | Ref Low | 2 × Bandgap - P2[6] (P2[6] = 1.3 V) | 2.524 - P2[6] | 2.600 - P2[6] | 2.676 - P2[6] | V |
| | RefPower = high Opamp bias = low | V _{REFHI} | Ref High | 2 × Bandgap + P2[6] (P2[6] = 1.3 V) | 2.490 - P2[6] | 2.586 - P2[6] | 2.679 - P2[6] | V |
| | | V _{AGND} | AGND | 2 × Bandgap | 2.523 | 2.594 | 2.669 | V |
| | | V _{REFLO} | Ref Low | 2 × Bandgap - P2[6] (P2[6] = 1.3 V) | 2.523 - P2[6] | 2.598 - P2[6] | 2.675 - P2[6] | V |
| | RefPower = medium Opamp bias = high | V _{REFHI} | Ref High | 2 × Bandgap + P2[6] (P2[6] = 1.3 V) | 2.493 - P2[6] | 2.588 - P2[6] | 2.682 - P2[6] | V |
| | | V _{AGND} | AGND | 2 × Bandgap | 2.523 | 2.594 | 2.670 | V |
| | | V _{REFLO} | Ref Low | 2 × Bandgap - P2[6] (P2[6] = 1.3 V) | 2.523 - P2[6] | 2.597 - P2[6] | 2.675 - P2[6] | V |
| | RefPower = medium Opamp bias = low | V _{REFHI} | Ref High | 2 × Bandgap + P2[6] (P2[6] = 1.3 V) | 2.494 - P2[6] | 2.589 - P2[6] | 2.685 - P2[6] | V |
| | | V _{AGND} | AGND | 2 × Bandgap | 2.523 | 2.595 | 2.671 | V |
| | | V _{REFLO} | Ref Low | 2 × Bandgap - P2[6] (P2[6] = 1.3 V) | 2.522 - P2[6] | 2.596 - P2[6] | 2.676 - P2[6] | V |

Table 12. 5-V DC Analog Reference Specifications (continued)

| Reference ARF_CR [5:3] | Reference Power Settings | Symbol | Reference | Description | Min | Typ | Max | Units |
|------------------------|--|--------------------|-----------|---|-----------------|-------------------------|-------------------------|-------|
| 0b101 | RefPower = high Opamp bias = high | V _{REFHI} | Ref High | P2[4] + Bandgap (P2[4] = V _{DD} /2) | P2[4] + 1.218 | P2[4] + 1.291 | P2[4] + 1.354 | V |
| | | V _{AGND} | AGND | P2[4] | P2[4] | P2[4] | P2[4] | – |
| | | V _{REFLO} | Ref Low | P2[4] – Bandgap (P2[4] = V _{DD} /2) | P2[4] – 1.335 | P2[4] – 1.294 | P2[4] – 1.237 | V |
| | RefPower = high Opamp bias = low | V _{REFHI} | Ref High | P2[4] + Bandgap (P2[4] = V _{DD} /2) | P2[4] + 1.221 | P2[4] + 1.293 | P2[4] + 1.358 | V |
| | | V _{AGND} | AGND | P2[4] | P2[4] | P2[4] | P2[4] | – |
| | | V _{REFLO} | Ref Low | P2[4] – Bandgap (P2[4] = V _{DD} /2) | P2[4] – 1.337 | P2[4] – 1.297 | P2[4] – 1.243 | V |
| | RefPower = medium Opamp bias = high | V _{REFHI} | Ref High | P2[4] + Bandgap (P2[4] = V _{DD} /2) | P2[4] + 1.222 | P2[4] + 1.294 | P2[4] + 1.360 | V |
| | | V _{AGND} | AGND | P2[4] | P2[4] | P2[4] | P2[4] | – |
| | | V _{REFLO} | Ref Low | P2[4] – Bandgap (P2[4] = V _{DD} /2) | P2[4] – 1.338 | P2[4] – 1.298 | P2[4] – 1.245 | V |
| | RefPower = medium Opamp bias = low | V _{REFHI} | Ref High | P2[4] + Bandgap (P2[4] = V _{DD} /2) | P2[4] + 1.221 | P2[4] + 1.294 | P2[4] + 1.362 | V |
| | | V _{AGND} | AGND | P2[4] | P2[4] | P2[4] | P2[4] | – |
| | | V _{REFLO} | Ref Low | P2[4] – Bandgap (P2[4] = V _{DD} /2) | P2[4] – 1.340 | P2[4] – 1.298 | P2[4] – 1.245 | V |
| 0b110 | RefPower = high Opamp bias = high | V _{REFHI} | Ref High | 2 × Bandgap | 2.513 | 2.593 | 2.672 | V |
| | | V _{AGND} | AGND | Bandgap | 1.264 | 1.302 | 1.340 | V |
| | | V _{REFLO} | Ref Low | V _{SS} | V _{SS} | V _{SS} + 0.008 | V _{SS} + 0.038 | V |
| | RefPower = high Opamp bias = low | V _{REFHI} | Ref High | 2 × Bandgap | 2.514 | 2.593 | 2.674 | V |
| | | V _{AGND} | AGND | Bandgap | 1.264 | 1.301 | 1.340 | V |
| | | V _{REFLO} | Ref Low | V _{SS} | V _{SS} | V _{SS} + 0.005 | V _{SS} + 0.028 | V |
| | RefPower = medium Opamp bias = high | V _{REFHI} | Ref High | 2 × Bandgap | 2.514 | 2.593 | 2.676 | V |
| | | V _{AGND} | AGND | Bandgap | 1.264 | 1.301 | 1.340 | V |
| | | V _{REFLO} | Ref Low | V _{SS} | V _{SS} | V _{SS} + 0.004 | V _{SS} + 0.024 | V |
| | RefPower = medium Opamp bias = low | V _{REFHI} | Ref High | 2 × Bandgap | 2.514 | 2.593 | 2.677 | V |
| | | V _{AGND} | AGND | Bandgap | 1.264 | 1.300 | 1.340 | V |
| | | V _{REFLO} | Ref Low | V _{SS} | V _{SS} | V _{SS} + 0.003 | V _{SS} + 0.021 | V |
| 0b111 | RefPower = high Opamp bias = high | V _{REFHI} | Ref High | 3.2 × Bandgap | 4.028 | 4.144 | 4.242 | V |
| | | V _{AGND} | AGND | 1.6 × Bandgap | 2.028 | 2.076 | 2.125 | V |
| | | V _{REFLO} | Ref Low | V _{SS} | V _{SS} | V _{SS} + 0.008 | V _{SS} + 0.034 | V |
| | RefPower = high Opamp bias = low | V _{REFHI} | Ref High | 3.2 × Bandgap | 4.032 | 4.142 | 4.245 | V |
| | | V _{AGND} | AGND | 1.6 × Bandgap | 2.029 | 2.076 | 2.126 | V |
| | | V _{REFLO} | Ref Low | V _{SS} | V _{SS} | V _{SS} + 0.005 | V _{SS} + 0.025 | V |
| | RefPower = medium Opamp bias = high | V _{REFHI} | Ref High | 3.2 × Bandgap | 4.034 | 4.143 | 4.247 | V |
| | | V _{AGND} | AGND | 1.6 × Bandgap | 2.029 | 2.076 | 2.126 | V |
| | | V _{REFLO} | Ref Low | V _{SS} | V _{SS} | V _{SS} + 0.004 | V _{SS} + 0.021 | V |
| | RefPower = medium Opamp bias = low | V _{REFHI} | Ref High | 3.2 × Bandgap | 4.036 | 4.144 | 4.249 | V |
| | | V _{AGND} | AGND | 1.6 × Bandgap | 2.029 | 2.076 | 2.126 | V |
| | | V _{REFLO} | Ref Low | V _{SS} | V _{SS} | V _{SS} + 0.003 | V _{SS} + 0.019 | V |

Table 13. 3.3-V DC Analog Reference Specifications

| Reference ARF_CR [5:3] | Reference Power Settings | Symbol | Reference | Description | Min | Typ | Max | Units |
|------------------------|---|--------------------|-----------|---|----------------------------|----------------------------|----------------------------|-------|
| 0b000 | RefPower = high Opamp bias = high | V _{REFHI} | Ref High | V _{DD} /2 + Bandgap | V _{DD} /2 + 1.200 | V _{DD} /2 + 1.290 | V _{DD} /2 + 1.365 | V |
| | | V _{AGND} | AGND | V _{DD} /2 | V _{DD} /2 – 0.030 | V _{DD} /2 | V _{DD} /2 + 0.034 | V |
| | | V _{REFLO} | Ref Low | V _{DD} /2 – Bandgap | V _{DD} /2 – 1.346 | V _{DD} /2 – 1.292 | V _{DD} /2 – 1.208 | V |
| | RefPower = high Opamp bias = low | V _{REFHI} | Ref High | V _{DD} /2 + Bandgap | V _{DD} /2 + 1.196 | V _{DD} /2 + 1.292 | V _{DD} /2 + 1.374 | V |
| | | V _{AGND} | AGND | V _{DD} /2 | V _{DD} /2 – 0.029 | V _{DD} /2 | V _{DD} /2 + 0.031 | V |
| | | V _{REFLO} | Ref Low | V _{DD} /2 – Bandgap | V _{DD} /2 – 1.349 | V _{DD} /2 – 1.295 | V _{DD} /2 – 1.227 | V |
| | RefPower = medium Opamp bias = high | V _{REFHI} | Ref High | V _{DD} /2 + Bandgap | V _{DD} /2 + 1.204 | V _{DD} /2 + 1.293 | V _{DD} /2 + 1.369 | V |
| | | V _{AGND} | AGND | V _{DD} /2 | V _{DD} /2 – 0.030 | V _{DD} /2 | V _{DD} /2 + 0.030 | V |
| | | V _{REFLO} | Ref Low | V _{DD} /2 – Bandgap | V _{DD} /2 – 1.351 | V _{DD} /2 – 1.297 | V _{DD} /2 – 1.229 | V |
| | RefPower = medium Opamp bias = low | V _{REFHI} | Ref High | V _{DD} /2 + Bandgap | V _{DD} /2 + 1.189 | V _{DD} /2 + 1.294 | V _{DD} /2 + 1.384 | V |
| | | V _{AGND} | AGND | V _{DD} /2 | V _{DD} /2 – 0.032 | V _{DD} /2 | V _{DD} /2 + 0.029 | V |
| | | V _{REFLO} | Ref Low | V _{DD} /2 – Bandgap | V _{DD} /2 – 1.353 | V _{DD} /2 – 1.297 | V _{DD} /2 – 1.230 | V |
| 0b001 | RefPower = high Opamp bias = high | V _{REFHI} | Ref High | P2[4]+P2[6] (P2[4] = V _{DD} /2, P2[6] = 0.5 V) | P2[4] + P2[6] – 0.105 | P2[4] + P2[6] – 0.008 | P2[4] + P2[6] + 0.095 | V |
| | | V _{AGND} | AGND | P2[4] | P2[4] | P2[4] | P2[4] | – |
| | | V _{REFLO} | Ref Low | P2[4]–P2[6] (P2[4] = V _{DD} /2, P2[6] = 0.5 V) | P2[4] – P2[6] – 0.035 | P2[4] – P2[6] + 0.006 | P2[4] – P2[6] + 0.053 | V |
| | RefPower = high Opamp bias = low | V _{REFHI} | Ref High | P2[4]+P2[6] (P2[4] = V _{DD} /2, P2[6] = 0.5 V) | P2[4] + P2[6] – 0.094 | P2[4] + P2[6] – 0.005 | P2[4] + P2[6] + 0.073 | V |
| | | V _{AGND} | AGND | P2[4] | P2[4] | P2[4] | P2[4] | – |
| | | V _{REFLO} | Ref Low | P2[4]–P2[6] (P2[4] = V _{DD} /2, P2[6] = 0.5 V) | P2[4] – P2[6] – 0.033 | P2[4] – P2[6] + 0.002 | P2[4] – P2[6] + 0.042 | V |
| | RefPower = medium Opamp bias = high | V _{REFHI} | Ref High | P2[4]+P2[6] (P2[4] = V _{DD} /2, P2[6] = 0.5 V) | P2[4] + P2[6] – 0.094 | P2[4] + P2[6] – 0.003 | P2[4] + P2[6] + 0.075 | V |
| | | V _{AGND} | AGND | P2[4] | P2[4] | P2[4] | P2[4] | – |
| | | V _{REFLO} | Ref Low | P2[4]–P2[6] (P2[4] = V _{DD} /2, P2[6] = 0.5 V) | P2[4] – P2[6] – 0.035 | P2[4] – P2[6] | P2[4] – P2[6] + 0.038 | V |
| | RefPower = medium Opamp bias = low | V _{REFHI} | Ref High | P2[4]+P2[6] (P2[4] = V _{DD} /2, P2[6] = 0.5 V) | P2[4] + P2[6] – 0.095 | P2[4] + P2[6] – 0.003 | P2[4] + P2[6] + 0.080 | V |
| | | V _{AGND} | AGND | P2[4] | P2[4] | P2[4] | P2[4] | – |
| | | V _{REFLO} | Ref Low | P2[4]–P2[6] (P2[4] = V _{DD} /2, P2[6] = 0.5 V) | P2[4] – P2[6] – 0.038 | P2[4] – P2[6] | P2[4] – P2[6] + 0.038 | V |
| 0b010 | RefPower = high Opamp bias = high | V _{REFHI} | Ref High | V _{DD} | V _{DD} – 0.119 | V _{DD} – 0.005 | V _{DD} | V |
| | | V _{AGND} | AGND | V _{DD} /2 | V _{DD} /2 – 0.028 | V _{DD} /2 | V _{DD} /2 + 0.029 | V |
| | | V _{REFLO} | Ref Low | V _{SS} | V _{SS} | V _{SS} + 0.004 | V _{SS} + 0.022 | V |
| | RefPower = high Opamp bias = low | V _{REFHI} | Ref High | V _{DD} | V _{DD} – 0.131 | V _{DD} – 0.004 | V _{DD} | V |
| | | V _{AGND} | AGND | V _{DD} /2 | V _{DD} /2 – 0.028 | V _{DD} /2 | V _{DD} /2 + 0.028 | V |
| | | V _{REFLO} | Ref Low | V _{SS} | V _{SS} | V _{SS} + 0.003 | V _{SS} + 0.021 | V |
| | RefPower = medium Opamp bias = high | V _{REFHI} | Ref High | V _{DD} | V _{DD} – 0.111 | V _{DD} – 0.003 | V _{DD} | V |
| | | V _{AGND} | AGND | V _{DD} /2 | V _{DD} /2 – 0.029 | V _{DD} /2 | V _{DD} /2 + 0.028 | V |
| | | V _{REFLO} | Ref Low | V _{SS} | V _{SS} | V _{SS} + 0.002 | V _{SS} + 0.017 | V |
| | RefPower = medium Opamp bias = low | V _{REFHI} | Ref High | V _{DD} | V _{DD} – 0.128 | V _{DD} – 0.003 | V _{DD} | V |
| | | V _{AGND} | AGND | V _{DD} /2 | V _{DD} /2 – 0.029 | V _{DD} /2 | V _{DD} /2 + 0.029 | V |
| | | V _{REFLO} | Ref Low | V _{SS} | V _{SS} | V _{SS} + 0.002 | V _{SS} + 0.019 | V |
| 0b011 | All power settings. Not allowed for 3.3 V. | – | – | – | – | – | – | |

Table 13. 3.3-V DC Analog Reference Specifications (continued)

| Reference ARF_CR [5:3] | Reference Power Settings | Symbol | Reference | Description | Min | Typ | Max | Units |
|------------------------|--|--------------------|-----------|---|-----------------|-------------------------|-------------------------|-------|
| 0b100 | All power settings. Not allowed for 3.3 V. | – | – | – | – | – | – | – |
| 0b101 | RefPower = high Opamp bias = high | V _{REFHI} | Ref High | P2[4] + Bandgap (P2[4] = V _{DD} /2) | P2[4] + 1.214 | P2[4] + 1.291 | P2[4] + 1.359 | V |
| | | V _{AGND} | AGND | P2[4] | P2[4] | P2[4] | P2[4] | – |
| | | V _{REFLO} | Ref Low | P2[4] – Bandgap (P2[4] = V _{DD} /2) | P2[4] – 1.335 | P2[4] – 1.292 | P2[4] – 1.200 | V |
| | RefPower = high Opamp bias = low | V _{REFHI} | Ref High | P2[4] + Bandgap (P2[4] = V _{DD} /2) | P2[4] + 1.219 | P2[4] + 1.293 | P2[4] + 1.357 | V |
| | | V _{AGND} | AGND | P2[4] | P2[4] | P2[4] | P2[4] | – |
| | | V _{REFLO} | Ref Low | P2[4] – Bandgap (P2[4] = V _{DD} /2) | P2[4] – 1.335 | P2[4] – 1.295 | P2[4] – 1.243 | V |
| | RefPower = medium Opamp bias = high | V _{REFHI} | Ref High | P2[4] + Bandgap (P2[4] = V _{DD} /2) | P2[4] + 1.222 | P2[4] + 1.294 | P2[4] + 1.356 | V |
| | | V _{AGND} | AGND | P2[4] | P2[4] | P2[4] | P2[4] | – |
| | | V _{REFLO} | Ref Low | P2[4] – Bandgap (P2[4] = V _{DD} /2) | P2[4] – 1.337 | P2[4] – 1.296 | P2[4] – 1.244 | V |
| | RefPower = medium Opamp bias = low | V _{REFHI} | Ref High | P2[4] + Bandgap (P2[4] = V _{DD} /2) | P2[4] + 1.224 | P2[4] + 1.295 | P2[4] + 1.355 | V |
| | | V _{AGND} | AGND | P2[4] | P2[4] | P2[4] | P2[4] | – |
| | | V _{REFLO} | Ref Low | P2[4] – Bandgap (P2[4] = V _{DD} /2) | P2[4] – 1.339 | P2[4] – 1.297 | P2[4] – 1.244 | V |
| 0b110 | RefPower = high Opamp bias = high | V _{REFHI} | Ref High | 2 × Bandgap | 2.510 | 2.595 | 2.655 | V |
| | | V _{AGND} | AGND | Bandgap | 1.276 | 1.301 | 1.332 | V |
| | | V _{REFLO} | Ref Low | V _{SS} | V _{SS} | V _{SS} + 0.006 | V _{SS} + 0.031 | V |
| | RefPower = high Opamp bias = low | V _{REFHI} | Ref High | 2 × Bandgap | 2.513 | 2.594 | 2.656 | V |
| | | V _{AGND} | AGND | Bandgap | 1.275 | 1.301 | 1.331 | V |
| | | V _{REFLO} | Ref Low | V _{SS} | V _{SS} | V _{SS} + 0.004 | V _{SS} + 0.021 | V |
| | RefPower = medium Opamp bias = high | V _{REFHI} | Ref High | 2 × Bandgap | 2.516 | 2.595 | 2.657 | V |
| | | V _{AGND} | AGND | Bandgap | 1.275 | 1.301 | 1.331 | V |
| | | V _{REFLO} | Ref Low | V _{SS} | V _{SS} | V _{SS} + 0.003 | V _{SS} + 0.017 | V |
| | RefPower = medium Opamp bias = low | V _{REFHI} | Ref High | 2 × Bandgap | 2.520 | 2.595 | 2.658 | V |
| | | V _{AGND} | AGND | Bandgap | 1.275 | 1.300 | 1.331 | V |
| | | V _{REFLO} | Ref Low | V _{SS} | V _{SS} | V _{SS} + 0.002 | V _{SS} + 0.015 | V |
| 0b111 | All power settings. Not allowed for 3.3 V. | – | – | – | – | – | – | |

DC Analog enCoRe III Block Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, or 3.15 V to 3.5 V and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 14. DC Analog enCoRe III Block Specifications

| Parameter | Description | Min | Typ | Max | Unit | Notes |
|-----------------|---------------------------|-----|------|-----|------|-------|
| R _{CT} | Resistor unit value (CT) | – | 12.2 | – | kΩ | – |
| C _{SC} | Capacitor unit value (SC) | – | 80 | – | fF | – |

DC POR and LVD Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, or 3.15 V to 3.5 V and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, respectively. Typical parameters apply to 5 V or 3.3 V at 25 °C and are for design guidance only.

Note The bits PORLEV and VM in the following table refer to bits in the VLT_CR register. See the PSoC® *Technical Reference Manual* for more information on the VLT_CR register.

Table 15. DC POR and LVD Specifications

| Parameter | Description | Min | Typ | Max | Unit | Notes |
|------------------|---|------|------|---------------------|------|-------|
| V_{PPOR0R} [5] | V_{DD} value for PPOR trip (positive ramp) PORLEV[1:0] = 00b | – | 2.91 | – | V | – |
| V_{PPOR1R} [5] | | | 4.39 | | V | |
| V_{PPOR2R} [5] | | | 4.55 | | V | |
| V_{PPOR0} | V_{DD} value for PPOR trip (negative ramp) PORLEV[1:0] = 00b | – | 2.82 | – | V | – |
| V_{PPOR1} | | | 4.39 | | V | |
| V_{PPOR2} | | | 4.55 | | V | |
| V_{PH0} | PPOR hysteresis PORLEV[1:0] = 00b | – | 92 | – | mV | – |
| V_{PH1} | | | 0 | | mV | |
| V_{PH2} | | | 0 | | mV | |
| V_{LVD0} | V_{DD} value for LVD trip VM[2:0] = 000b | 2.86 | 2.92 | 2.98 ^[6] | V | – |
| V_{LVD1} | | | 3.02 | 3.08 | V | |
| V_{LVD2} | | | 3.13 | 3.20 | V | |
| V_{LVD3} | | | 4.00 | 4.08 | V | |
| V_{LVD4} | | | 4.48 | 4.57 | V | |
| V_{LVD5} | | | 4.64 | 4.74 ^[7] | V | |
| V_{LVD6} | | | 4.73 | 4.82 | V | |
| V_{LVD7} | | | 4.81 | 4.91 | V | |

Notes

- Errata:** When VDD of the device is pulled below ground just before power on, the first read from each 8K Flash page may be corrupted. This issue does not affect Flash page 0 because it is the selected page upon reset. For more details in [Errata on page 40](#).
- Always greater than 50 mV above PPOR (PORLEV = 00) for falling supply.
- Always greater than 50 mV above PPOR (PORLEV = 10) for falling supply.

DC Programming Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, or 3.15 V to 3.5 V and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 16. DC Programming Specifications

| Parameter | Description | Min | Typ | Max | Unit | Notes |
|-----------------------|---|-----------------------|-----|------------------------|-------|--|
| V _{DDP} | V _{DD} for programming and erase | 4.5 | 5.0 | 5.5 | V | This specification applies to the functional requirements of external programmer tools |
| V _{DDL} | Low V _{DD} for verify | 3.0 | 3.1 | 3.2 | V | This specification applies to the functional requirements of external programmer tools |
| V _{DDH} | High V _{DD} for verify | 5.1 | 5.2 | 5.3 | V | This specification applies to the functional requirements of external programmer tools |
| V _{DDIWRITE} | Supply voltage for flash write operation | 3.15 | – | 5.25 | V | This specification applies to this device when it is executing internal flash writes |
| I _{DDP} | Supply current during programming or verify | – | 15 | 30 | mA | – |
| V _{ILP} | Input low voltage during programming or verify | – | – | 0.8 | V | – |
| V _{IHP} | Input high voltage during programming or Verify | 2.1 | – | – | V | – |
| I _{ILP} | Input current when applying V _{ilp} to P1[0] or P1[1] during programming or verify | – | – | 0.2 | mA | Driving internal pull-down resistor. |
| I _{IHP} | Input current when applying V _{ihp} to P1[0] or P1[1] during programming or verify | – | – | 1.5 | mA | Driving internal pull-down resistor. |
| V _{OLV} | Output low voltage during programming or verify | – | – | V _{SS} + 0.75 | V | – |
| V _{OHV} | Output high voltage during programming or verify | V _{DD} – 1.0 | – | V _{DD} | V | – |
| Flash _{ENPB} | Flash endurance (per block) | 50,000 ^[8] | – | – | – | Erase/write cycles per block. |
| Flash _{ENT} | Flash endurance (total) ^[9] | 1,800,000 | – | – | – | Erase/write cycles. |
| Flash _{DR} | Flash data retention | 10 | – | – | Years | – |

DC I²C Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, or 3.15 V to 3.5 V and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 17. DC I²C Specifications ^[10]

| Symbol | Description | Min | Typ | Max | Units | Notes |
|--------------------|------------------|-----------------------|-----|------------------------|-------|-----------------------------------|
| V _{ILI2C} | Input low level | – | – | 0.3 × V _{DD} | V | 3.15 V ≤ V _{DD} ≤ 3.6 V |
| | | – | – | 0.25 × V _{DD} | V | 4.75 V ≤ V _{DD} ≤ 5.25 V |
| V _{IHI2C} | Input high level | 0.7 × V _{DD} | – | – | V | 3.15 V ≤ V _{DD} ≤ 5.25 V |

Notes

- The 50,000 cycle Flash endurance per block will only be guaranteed if the Flash is operating within one voltage range. Voltage ranges are 3.0V to 3.6V and 4.75V to 5.25V.
- A maximum of 36 × 50,000 block endurance cycles is allowed. This may be balanced between operations on 36x1 blocks of 50,000 maximum cycles each, 36x2 blocks of 25,000 maximum cycles each, or 36x4 blocks of 12,500 maximum cycles each (to limit the total number of cycles to 36x50,000 and that no single block ever sees more than 50,000 cycles).
For the full industrial range, the user must employ a temperature sensor user module (FlashTemp) and feed the result to the temperature argument before writing. Refer to the Flash APIs application note [AN2015](#) for more information.
- All GPIOs meet the DC GPIO V_{IL} and V_{IH} specifications found in the DC GPIO Specifications sections. The I²C GPIO pins also meet the mentioned specifications.

AC Electrical Characteristics

AC Chip-Level Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, or 3.15 V to 3.5 V and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 18. AC Chip-Level Specifications

| Parameter | Description | Min | Typ | Max | Unit | Notes |
|--------------------------------------|--|-------|------|-----------------------------|------|--|
| F _{IMO245V} | IMO frequency for 24 MHz (5 V) | 23.04 | 24 | 24.96 ^[11, 12] | MHz | Trimmed for 5 V operation using factory trim values. |
| F _{IMO243V} | IMO frequency for 24 MHz (3.3 V) | 22.08 | 24 | 25.92 ^[11,13] | MHz | Trimmed for 3.3 V operation using factory trim values. |
| F _{IMOUSB} | IMO frequency with USB frequency locking enabled and USB traffic present | 23.94 | 24 | 24.06 ^[12] | MHz | USB operation for system clock source from the IMO is limited to $0^{\circ}\text{C} \leq T_A \leq 70^{\circ}\text{C}$. |
| F _{CPU1} | CPU frequency (5 V nominal) | 0.090 | 24 | 24.96 ^[11,12] | MHz | SLIMO mode = 0. |
| F _{CPU2} | CPU frequency (3.3 V nominal) | 0.086 | 12 | 12.96 ^[12,13] | MHz | SLIMO mode = 0. |
| F _{BLK5} | Digital PSoC block frequency (5 V nominal) | 0 | 48 | 49.92 ^[11,12,14] | MHz | Refer to the AC Digital Block Specifications on page 26 . |
| F _{BLK3} | Digital PSoC block frequency (3.3 V nominal) | 0 | 24 | 25.92 ^[12,14] | MHz | – |
| F _{32K1} | ILO frequency | 15 | 32 | 64 | kHz | – |
| F _{32K_U} | ILO untrimmed frequency | 5 | – | 100 | kHz | After a reset and before the M8C starts to run, the ILO is not trimmed. See the System Resets section of the PSoC Technical Reference Manual for details on this timing. |
| DC _{ILO} | ILO duty cycle | 20 | 50 | 80 | % | – |
| DC _{24M} | 24-MHz duty cycle | 40 | 50 | 60 | % | – |
| Step24M | 24-MH trim step size | – | 50 | – | kHz | – |
| F _{out48M} | 48-MHz output frequency | 46.08 | 48.0 | 49.92 ^[11,13] | MHz | Trimmed. Utilizing factory trim values. |
| F _{MAX} | Maximum frequency of signal on row input or row output | – | – | 12.96 | MHz | – |
| SR _{POWER_UP} | Power supply slew rate | – | – | 250 | V/ms | – |
| T _{POWERUP} | Time from end of POR to CPU executing code | – | 16 | 100 | ms | – |
| T _{jit_IMO} ^[15] | 24 MHz IMO cycle-to-cycle jitter (RMS) | – | 200 | 1200 | ps | |
| | 24 MHz IMO long term N cycle-to-cycle jitter (RMS) | – | 900 | 6000 | ps | N = 32. |
| | 24 MHz IMO period jitter (RMS) | – | 200 | 900 | ps | |

Notes

- 11. 4.75 V < V_{DD} < 5.25 V.
- 12. Accuracy derived from Internal Main Oscillator with appropriate trim for V_{DD} range.
- 13. 3.0 V < V_{DD} < 3.6 V. See application note [AN2012 "Adjusting PSoC Microcontroller Trims for Dual Voltage-Range Operation"](#) for information on trimming for operation at 3.3 V.
- 14. See the individual user module data sheets for information on maximum frequencies for user modules.
- 15. Refer to Cypress Jitter Specifications application note, [Understanding Datasheet Jitter Specifications for Cypress Timing Products – AN5054](#) for more information.

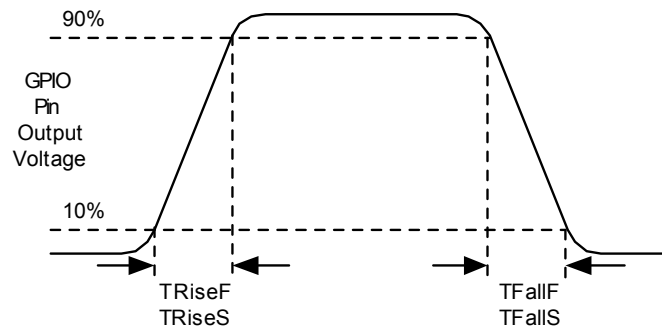
AC GPIO Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, or 3.15 V to 3.5 V and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 19. AC GPIO Specifications

| Parameter | Description | Min | Typ | Max | Unit | Notes |
|-------------|--|-----|-----|-----|------|--|
| F_{GPIO} | GPIO operating frequency | 0 | – | 12 | MHz | Normal Strong Mode |
| T_{RiseF} | Rise time, normal strong mode, $C_{load} = 50\text{ pF}$ | 3 | – | 18 | ns | $V_{DD} = 4.5\text{ to }5.25\text{ V}$, 10%–90% |
| T_{FallF} | Fall time, normal strong mode, $C_{load} = 50\text{ pF}$ | 2 | – | 18 | ns | $V_{DD} = 4.5\text{ to }5.25\text{ V}$, 10%–90% |
| T_{RiseS} | Rise time, slow strong mode, $C_{load} = 50\text{ pF}$ | 10 | 27 | – | ns | $V_{DD} = 3\text{ to }5.25\text{ V}$, 10%–90% |
| T_{FallS} | Fall time, slow strong mode, $C_{load} = 50\text{ pF}$ | 10 | 22 | – | ns | $V_{DD} = 3\text{ to }5.25\text{ V}$, 10%–90% |

Figure 6. GPIO Timing Diagram



AC Full Speed USB Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, or 3.15 V to 3.5 V and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 20. AC Full-Speed (12 Mbps) USB Specifications

| Parameter | Description | Min | Typ | Max | Unit | Notes |
|---------------|--------------------------------------|------------|-----|------------|------|-----------------|
| T_{RFS} | Transition rise time | 4 | – | 20 | ns | For 50-pF load. |
| T_{FSS} | Transition fall time | 4 | – | 20 | ns | For 50-pF load. |
| T_{RFMFS} | Rise/fall time matching: (T_R/T_F) | 90 | – | 111 | % | For 50-pF load. |
| $T_{DRATEFS}$ | Full-speed data rate | 12 – 0.25% | 12 | 12 + 0.25% | Mbps | – |

AC Digital Block Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, or 3.15 V to 3.5 V and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 21. AC Digital Block Specifications

| Function | Description | Min | Typ | Max | Unit | Notes |
|-------------------|--|--------------------|-----|-------|------|---|
| All functions | Block input clock frequency | | | | | |
| | $V_{DD} \geq 4.75\text{ V}$ | – | – | 49.92 | MHz | |
| | $V_{DD} < 4.75\text{ V}$ | – | – | 25.92 | MHz | |
| Timer | Input clock frequency | | | | | |
| | No capture, $V_{DD} \geq 4.75\text{ V}$ | – | – | 49.92 | MHz | |
| | No capture, $V_{DD} < 4.75\text{ V}$ | – | – | 25.92 | MHz | |
| | With capture | – | – | 25.92 | MHz | |
| | Capture pulse width | 50 ^[16] | – | – | ns | |
| Counter | Input clock frequency | | | | | |
| | No enable input, $V_{DD} \geq 4.75\text{ V}$ | – | – | 49.92 | MHz | |
| | No enable input, $V_{DD} < 4.75\text{ V}$ | – | – | 25.92 | MHz | |
| | With enable input | – | – | 25.92 | MHz | |
| | Enable input pulse width | 50 ^[16] | – | – | ns | |
| | Kill pulse width | | | | | |
| | Asynchronous restart mode | 20 | – | – | ns | |
| | Synchronous restart mode | 50 ^[16] | – | – | ns | |
| | Disable mode | 50 ^[16] | – | – | ns | |
| | Input clock frequency | | | | | |
| | $V_{DD} \geq 4.75\text{ V}$ | – | – | 49.92 | MHz | |
| | $V_{DD} < 4.75\text{ V}$ | – | – | 25.92 | MHz | |
| CRCPRS (PRS Mode) | Input clock frequency | | | | | |
| | $V_{DD} \geq 4.75\text{ V}$ | – | – | 49.92 | MHz | |
| | $V_{DD} < 4.75\text{ V}$ | – | – | 25.92 | MHz | |
| CRCPRS (CRC Mode) | Input clock frequency | – | – | 24.6 | MHz | |
| SPIM | Input clock frequency | – | – | 8.2 | MHz | The SPI serial clock (SCLK) frequency is equal to the input clock frequency divided by 2. |
| SPIS | Input clock (SCLK) frequency | – | – | 4.1 | MHz | The input clock is the SPI SCLK in SPIS mode. |
| | Width of SS_negated between transmissions | 50 ^[16] | – | – | ns | |
| Transmitter | Input clock frequency | | | | | The baud rate is equal to the input clock frequency divided by 8. |
| | $V_{DD} \geq 4.75\text{ V}$, 2 stop bits | – | – | 49.92 | MHz | |
| | $V_{DD} \geq 4.75\text{ V}$, 1 stop bit | – | – | 24.6 | MHz | |
| | $V_{DD} < 4.75\text{ V}$ | – | – | 24.6 | MHz | |
| Receiver | Input clock frequency | | | | | The baud rate is equal to the input clock frequency divided by 8. |
| | $V_{DD} \geq 4.75\text{ V}$, 2 stop bits | – | – | 49.92 | MHz | |
| | $V_{DD} \geq 4.75\text{ V}$, 1 stop bit | – | – | 24.6 | MHz | |
| | $V_{DD} < 4.75\text{ V}$ | – | – | 24.6 | MHz | |

Note

16. 50 ns minimum input pulse width is based on the input synchronizers running at 24 MHz (42 ns nominal period).

AC External Clock Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, or 3.15 V to 3.5 V and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 22. AC External Clock Specifications

| Parameter | Description | Min | Typ | Max | Unit | Notes |
|---------------------|--------------------------------|-------|-----|-------|------|--|
| F _{OSCEXT} | Frequency for USB applications | 23.94 | 24 | 24.06 | MHz | USB operation in the extended Industrial temperature range ($-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$) requires that the system clock is sourced from an external clock oscillator. |
| – | Duty cycle | 47 | 50 | 53 | % | – |
| – | Power-up to IMO switch | 150 | – | – | μs | – |

AC Analog Output Buffer Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, or 3.15 V to 3.5 V and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 23. 5 V AC Analog Output Buffer Specifications

| Parameter | Description | Min | Typ | Max | Unit | Notes |
|--------------------|---|--------------|--------|------------|--------------|-------|
| T _{ROB} | Rising settling time to 0.1%, 1 V Step, 100-pF load Power = low Power = high | – – | – – | 2.5 2.5 | μs μs | – |
| T _{SOB} | Falling settling time to 0.1%, 1 V Step, 100-pF load Power = low Power = high | – – | – – | 2.2 2.2 | μs μs | – |
| SR _{ROB} | Rising slew rate (20% to 80%), 1 V Step, 100-pF load Power = low Power = high | 0.65 0.65 | – – | – – | V/μs V/μs | – |
| SR _{FOB} | Falling slew rate (80% to 20%), 1 V Step, 100-pF load Power = low Power = high | 0.65 0.65 | – – | – – | V/μs V/μs | – |
| BW _{OBSS} | Small signal bandwidth, 20 mV _{pp} , 3-dB BW, 100-pF load Power = low Power = high | 0.8 0.8 | – – | – – | MHz MHz | – |
| BW _{OBLs} | Large signal bandwidth, 1 V _{pp} , 3-dB BW, 100-pF load Power = low Power = high | 300 300 | – – | – – | kHz kHz | – |

Table 24. 3.3 V AC Analog Output Buffer Specifications

| Parameter | Description | Min | Typ | Max | Unit | Notes |
|--------------------|--|------------|--------|------------|--------------|-------|
| T _{ROB} | Rising settling time to 0.1%, 1 V Step, 100-pF load Power = low Power = high | – – | – – | 3.8 3.8 | μs μs | – |
| T _{SOB} | Falling settling time to 0.1%, 1 V Step, 100-pF load Power = low Power = high | – – | – – | 2.6 2.6 | μs μs | – |
| SR _{ROB} | Rising slew rate (20% to 80%), 1 V Step, 100-pF load Power = low Power = high | 0.5 0.5 | – – | – – | V/μs V/μs | – |
| SR _{FOB} | Falling slew rate (80% to 20%), 1 V Step, 100-pF load Power = low Power = high | 0.5 0.5 | – – | – – | V/μs V/μs | – |
| BW _{OBSS} | Small signal bandwidth, 20 mV _{pp} , 3dB BW, 100-pF load Power = low Power = high | 0.7 0.7 | – – | – – | MHz MHz | – |
| BW _{OBLs} | Large signal bandwidth, 1 V _{pp} , 3dB BW, 100-pF load Power = low Power = high | 200 200 | – – | – – | kHz kHz | – |

AC Programming Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, or 3.15 V to 3.5 V and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 25. AC Programming Specifications

| Parameter | Description | Min | Typ | Max | Unit | Notes |
|---------------------------|--|-----|-----|-----|------|---|
| T _{RSCLK} | Rise time of SCLK | 1 | – | 20 | ns | – |
| T _{FSCLK} | Fall time of SCLK | 1 | – | 20 | ns | – |
| T _{SSCLK} | Data setup time to falling edge of SCLK | 40 | – | – | ns | – |
| T _{HSCLK} | Data hold time from falling edge of SCLK | 40 | – | – | ns | – |
| F _{SCLK} | Frequency of SCLK | 0 | – | 8 | MHz | – |
| T _{ERASEB} | Flash erase time (block) | – | 10 | – | ms | – |
| T _{WRITE} | Flash block write time | – | 40 | – | ms | – |
| T _{DSCLK} | Data out delay from falling edge of SCLK | – | – | 45 | ns | V _{DD} > 3.6 |
| T _{DSCLK3} | Data out delay from falling edge of SCLK | – | – | 50 | ns | 3.15 ≤ V _{DD} ≤ 3.5 |
| T _{ERASEALL} | Flash erase time (bulk) | – | 40 | – | ms | Erase all blocks and protection fields at once. |
| T _{PROGRAM_HOT} | Flash block erase + flash block write time | – | – | 100 | ms | 0 °C ≤ T _J ≤ 100 °C |
| T _{PROGRAM_COLD} | Flash block erase + flash block write time | – | – | 200 | ms | –40 °C ≤ T _J ≤ 0 °C |

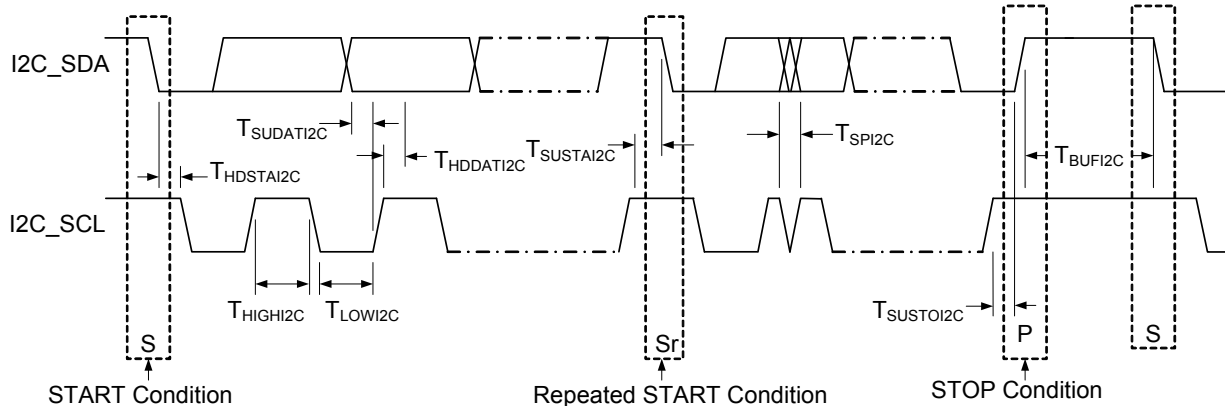
AC I²C Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, or 3.15 V to 3.5 V and $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 26. AC Characteristics of the I²C SDA and SCL Pins for V_{DD}

| Parameter | Description | Standard-Mode | | Fast-Mode | | Unit | Notes |
|-----------------------|--|---------------|-----|---------------------|-----|------|-------|
| | | Min | Max | Min | Max | | |
| F _{SCL I2C} | SCL clock frequency | 0 | 100 | 0 | 400 | kHz | – |
| T _{HDSTAI2C} | Hold time (repeated) START condition. After this period, the first clock pulse is generated. | 4.0 | – | 0.6 | – | μs | – |
| T _{LOWI2C} | LOW period of the SCL clock | 4.7 | – | 1.3 | – | μs | – |
| T _{HIGHI2C} | HIGH period of the SCL clock | 4.0 | – | 0.6 | – | μs | – |
| T _{SUSTAI2C} | Setup time for a repeated START condition | 4.7 | – | 0.6 | – | μs | – |
| T _{HDDATI2C} | Data hold time | 0 | – | 0 | – | μs | – |
| T _{SUDATI2C} | Data setup time | 250 | – | 100 ^[17] | – | ns | – |
| T _{SUSTOI2C} | Setup time for STOP condition | 4.0 | – | 0.6 | – | μs | – |
| T _{BUFI2C} | Bus free time between a STOP and START condition | 4.7 | – | 1.3 | – | μs | – |
| T _{SPI2C} | Pulse width of spikes are suppressed by the input filter. | – | – | 0 | 50 | ns | – |

Figure 7. Definition for Timing for Fast-/Standard-Mode on the I²C Bus



Note

17. A Fast-Mode I²C-bus device can be used in a Standard-Mode I²C-bus system, but the requirement $T_{SUDATI2C} \geq 250\text{ ns}$ must then be met. This automatically is the case if the device does not stretch the LOW period of the SCL signal. If such device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{rmax} + T_{SUDATI2C} = 1000 + 250 = 1250\text{ ns}$ (according to the Standard-Mode I²C-bus specification) before the SCL line is released.

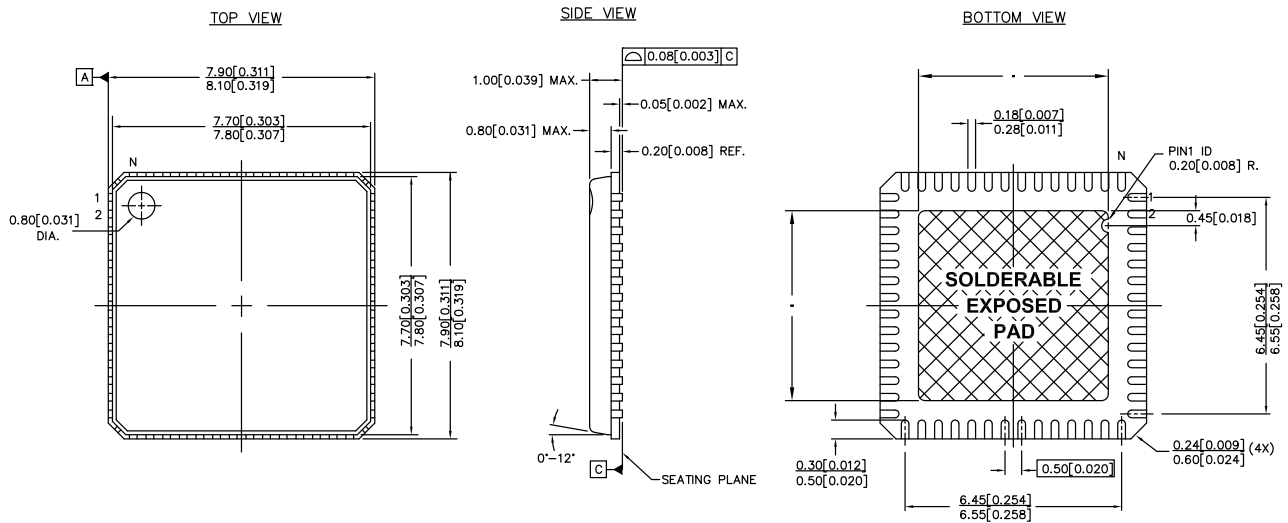
Packaging Information

This section illustrates the package specification for the CY7C64215 enCoRe III, along with the thermal impedance for the package.


Important Note Emulation tools may require a larger area on the target PCB than the chip's footprint. For a detailed description of the emulation tools' dimensions, refer to the emulator pod drawings at <http://www.cypress.com>.

Package Diagrams

Figure 8. 56-pin QFN (8 × 8 × 1.0 mm) 4.5 × 5.21 E-Pad (Subcon Punch Type Package) Package Outline, 001-12921



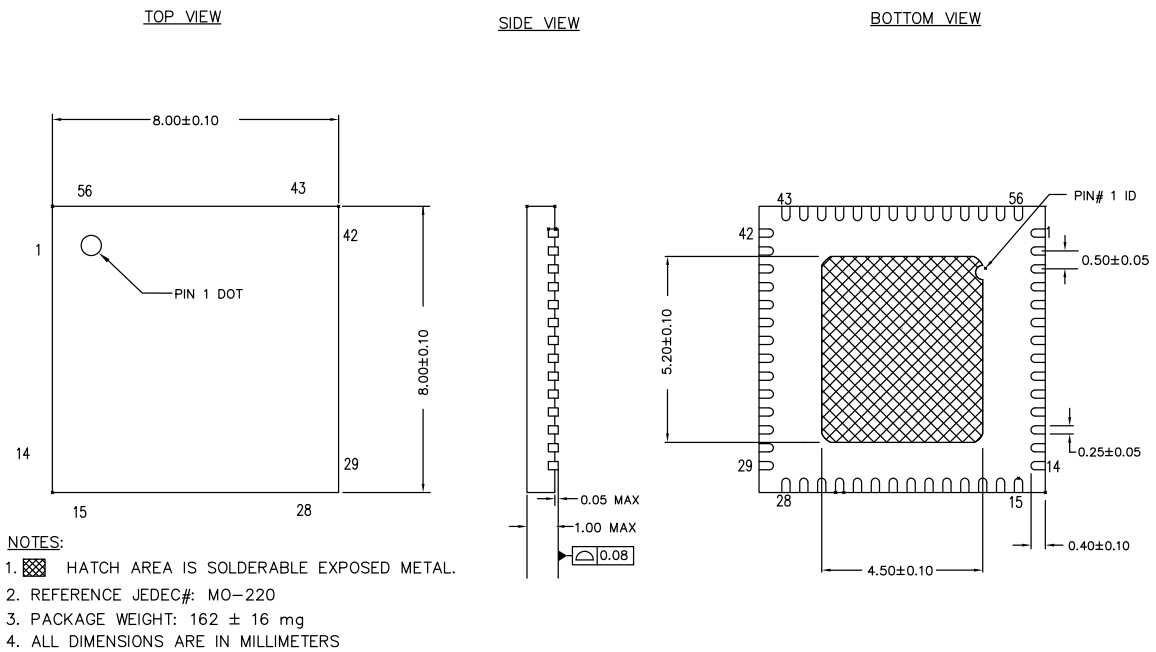
NOTES:

1.  HATCH AREA IS SOLDERABLE EXPOSED METAL.
2. REFERENCE JEDEC#: MO-220
3. PACKAGE WEIGHT: 0.162g
4. ALL DIMENSIONS ARE IN MM [MIN/MAX]
5. PACKAGE CODE

| PART # | DESCRIPTION |
|--------|-------------|
| LF56A | STANDARD |
| LY56A | PB-FREE |

001-12921 *C

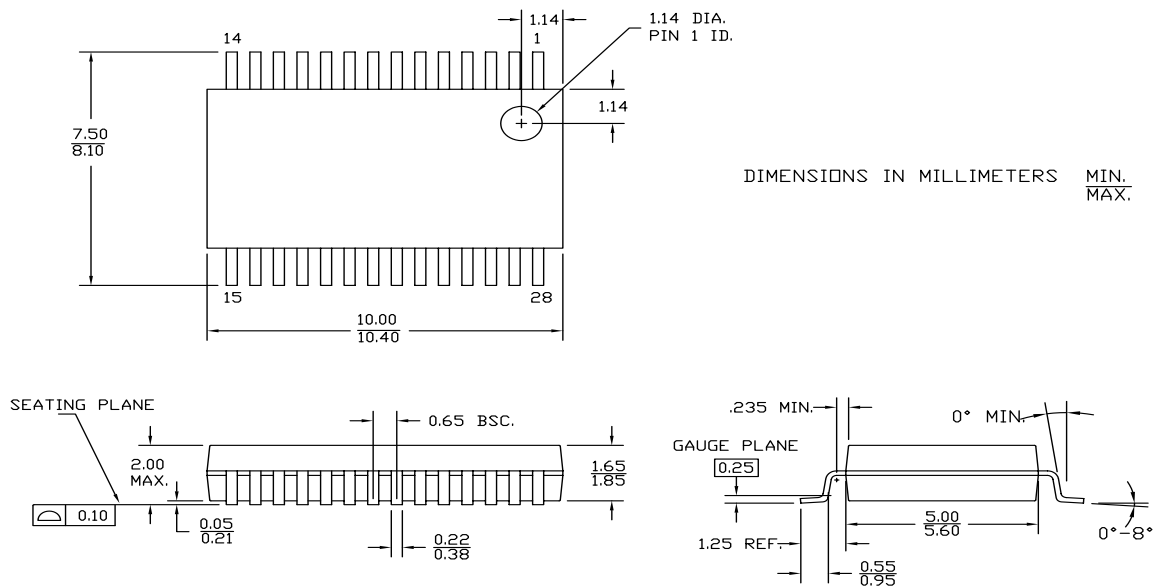
Figure 9. 56-pin QFN (8 × 8 × 1.0 mm) 4.5 × 5.2 E-Pad (Sawn) Package Outline, 001-53450



001-53450 *D

Figure 10. 28-pin SSOP (210 Mils) Package Outline, 51-85079

28 Lead (5.3mm) SSOP



51-85079 *F

Thermal Impedance

Table 27. Thermal Impedance for the Package

| Package | Typical θ_{JA} [18] |
|----------------|----------------------------|
| 56-pin QFN[19] | 20 °C/W |
| 28-pin SSOP | 96 °C/W |

Solder Reflow Peak Temperature

Following is the minimum solder reflow peak temperature to achieve good solderability.

Table 28. Solder Reflow Peak Temperature

| Package | Maximum Peak Temperature | Time at Maximum Peak Temperature |
|-------------|--------------------------|----------------------------------|
| 56-pin QFN | 260 °C | 20 s |
| 28-pin SSOP | 260 °C | 20 s |

Notes

18. $T_J = T_A + \text{POWER} \times \theta_{JA}$

19. To achieve the thermal impedance specified for the QFN package, the center thermal pad should be soldered to the PCB ground plane.

Ordering Information

| Package | Ordering Code | Flash Size | SRAM (Bytes) | Temperature Range |
|-----------------------------------|-------------------|------------|--------------|-----------------------------|
| 28-pin SSOP | CY7C64215-28PVXC | 16K | 1K | Commercial, 0 °C to 70 °C |
| 28-pin SSOP (Tape and Reel) | CY7C64215-28PVXCT | 16K | 1K | Commercial, 0 °C to 70 °C |
| 28-pin SSOP | CY7C64215-28PVXI | 16 K | 1K | Industrial, -40 °C to 85 °C |
| 28-pin SSOP (Tape and Reel) | CY7C64215-28PVXIT | 16 K | 1K | Industrial, -40 °C to 85 °C |
| 56-pin QFN (Sawn) | CY7C64215-56LTXC | 16K | 1K | Commercial, 0 °C to 70 °C |
| 56-pin QFN (Sawn) (Tape and Reel) | CY7C64215-56LTXCT | 16K | 1K | Commercial, 0 °C to 70 °C |
| 56-pin QFN (Sawn) | CY7C64215-56LTXI | 16K | 1K | Industrial, -40 °C to 85 °C |
| 56-pin QFN (Sawn) (Tape and Reel) | CY7C64215-56LTXIT | 16K | 1K | Industrial, -40 °C to 85 °C |

Ordering Code Definitions

CY 7C64 XXX- XX XXX C/I (T)



Acronyms

Acronyms Used

The following table lists the acronyms that are used in this document.

| Acronym | Description | Acronym | Description |
|---------|---|---------|---|
| AC | alternating current | MIPS | million instructions per second |
| ADC | analog-to-digital converter | PCB | printed circuit board |
| API | application programming interface | PGA | programmable gain amplifier |
| CPU | central processing unit | POR | power-on reset |
| CRC | cyclic redundancy check | PPOR | precision power-on reset |
| CT | continuous time | PSoC® | Programmable System-on-Chip™ |
| DAC | digital-to-analog converter | PWM | pulse-width modulator |
| DC | direct current | QFN | quad flat no leads |
| EEPROM | electrically erasable programmable read-only memory | RF | radio frequency |
| GPIO | general purpose I/O | SC | switched capacitor |
| ICE | in-circuit emulator | SLIMO | slow IMO |
| IDE | integrated development environment | SPI™ | serial peripheral interface |
| ILO | internal low speed oscillator | SRAM | static random-access memory |
| IMO | internal main oscillator | SROM | supervisory read-only memory |
| I/O | input/output | SSOP | shrink small-outline package |
| ISSP | In-System Serial Programming | UART | universal asynchronous receiver / transmitter |
| LVD | low voltage detect | USB | universal serial bus |
| MAC | multiply-accumulate | WDT | watchdog timer |

Reference Documents

CY8CPLC20, CY8CLED16P01, CY8C29x66, CY8C27x43, CY8C24x94, CY8C24x23, CY8C24x23A, CY8C22x13, CY8C21x34, CY8C21x23, CY7C64215, CY7C603xx, CY8CNP1xx, and CYWUSB6953 PSoC® Programmable System-on-Chip Technical Reference Manual (TRM) (001-14463)

Design Aids – Reading and Writing PSoC® Flash – AN2015 (001-40459)

Document Conventions

Units of Measure

| Symbol | Unit of Measure | Symbol | Unit of Measure |
|--------|-----------------|--------|-----------------|
| °C | degree Celsius | ms | milli-second |
| dB | decibels | mV | milli-volts |
| fF | femto farad | nA | nanoampere |
| kHz | kilohertz | ns | nanosecond |
| kΩ | kilohm | Ω | ohm |
| MHz | megahertz | pF | picofarad |
| μA | microampere | ps | picosecond |
| μs | microsecond | % | percent |
| μV | microvolts | V | volts |
| mA | milli-ampere | W | watts |
| mm | milli-meter | | |

Numeric Conventions

Hexadecimal numbers are represented with all letters in uppercase with an appended lowercase 'h' (for example, '14h' or '3Ah'). Hexadecimal numbers may also be represented by a '0x' prefix, the C coding convention. Binary numbers have an appended lowercase 'b' (for example, '01010100b' or '01000011b'). Numbers not indicated by an 'h' or 'b' are decimal.

| | |
|---|--|
| active high | <ol style="list-style-type: none"> 5. A logic signal having its asserted state as the logic 1 state. 6. A logic signal having the logic 1 state as the higher voltage of the two states. |
| analog blocks | The basic programmable opamp circuits. These are SC (switched capacitor) and CT (continuous time) blocks. These blocks can be interconnected to provide ADCs, DACs, multi-pole filters, gain stages, and much more. |
| analog-to-digital (ADC) | A device that changes an analog signal to a digital signal of corresponding magnitude. Typically, an ADC converts a voltage to a digital number. The digital-to-analog (DAC) converter performs the reverse operation. |
| API (Application Programming Interface) | A series of software routines that comprise an interface between a computer application and lower level services and functions (for example, user modules and libraries). APIs serve as building blocks for programmers that create software applications. |
| asynchronous | A signal whose data is acknowledged or acted upon immediately, irrespective of any clock signal. |
| Bandgap reference | A stable voltage reference design that matches the positive temperature coefficient of VT with the negative temperature coefficient of VBE, to produce a zero temperature coefficient (ideally) reference. |
| bandwidth | <ol style="list-style-type: none"> 1. The frequency range of a message or information processing system measured in hertz. 2. The width of the spectral region over which an amplifier (or absorber) has substantial gain (or loss); it is sometimes represented more specifically as, for example, full width at half maximum. |
| bias | <ol style="list-style-type: none"> 1. A systematic deviation of a value from a reference value. 2. The amount by which the average of a set of values departs from a reference value. 3. The electrical, mechanical, magnetic, or other force (field) applied to a device to establish a reference level to operate the device. |
| block | <ol style="list-style-type: none"> 1. A functional unit that performs a single function, such as an oscillator. 2. A functional unit that may be configured to perform one of several functions, such as a digital PSoC block or an analog PSoC block. |

| | |
|-------------------------------|--|
| buffer | <ol style="list-style-type: none">1. A storage area for data that is used to compensate for a speed difference, when transferring data from one device to another. Usually refers to an area reserved for IO operations, into which data is read, or from which data is written.2. A portion of memory set aside to store data, often before it is sent to an external device or as it is received from an external device.3. An amplifier used to lower the output impedance of a system. |
| bus | <ol style="list-style-type: none">1. A named connection of nets. Bundling nets together in a bus makes it easier to route nets with similar routing patterns.2. A set of signals performing a common function and carrying similar data. Typically represented using vector notation; for example, address[7:0].3. One or more conductors that serve as a common connection for a group of related devices. |
| clock | The device that generates a periodic signal with a fixed frequency and duty cycle. A clock is sometimes used to synchronize different logic blocks. |
| comparator | An electronic circuit that produces an output voltage or current whenever two input levels simultaneously satisfy predetermined amplitude requirements. |
| compiler | A program that translates a high level language, such as C, into machine language. |
| configuration space | In PSoC devices, the register space accessed when the XIO bit, in the CPU_F register, is set to '1'. |
| crystal oscillator | An oscillator in which the frequency is controlled by a piezoelectric crystal. Typically a piezoelectric crystal is less sensitive to ambient temperature than other circuit components. |
| cyclic redundancy check (CRC) | A calculation used to detect errors in data communications, typically performed using a linear feedback shift register. Similar calculations may be used for a variety of other purposes such as data compression. |
| data bus | A bi-directional set of signals used by a computer to convey information from a memory location to the central processing unit and vice versa. More generally, a set of signals used to convey data between digital functions. |
| debugger | A hardware and software system that allows the user to analyze the operation of the system under development. A debugger usually allows the developer to step through the firmware one step at a time, set break points, and analyze memory. |
| dead band | A period of time when neither of two or more signals are in their active state or in transition. |
| digital blocks | The 8-bit logic blocks that can act as a counter, timer, serial receiver, serial transmitter, CRC generator, pseudo-random number generator, or SPI. |
| digital-to-analog (DAC) | A device that changes a digital signal to an analog signal of corresponding magnitude. The analog-to-digital (ADC) converter performs the reverse operation. |
| duty cycle | The relationship of a clock period high time to its low time, expressed as a percent. |
| emulator | Duplicates (provides an emulation of) the functions of one system with a different system, so that the second system appears to behave like the first system. |
| external reset (XRES) | An active high signal that is driven into the PSoC device. It causes all operation of the CPU and blocks to stop and return to a pre-defined state. |

| | |
|---------------------------------|--|
| flash | An electrically programmable and erasable, non-volatile technology that provides users with the programmability and data storage of EPROMs, plus in-system erasability. Non-volatile means that the data is retained when power is off. |
| Flash block | The smallest amount of Flash ROM space that may be programmed at one time and the smallest amount of Flash space that may be protected. A Flash block holds 64 bytes. |
| frequency | The number of cycles or events per unit of time, for a periodic function. |
| gain | The ratio of output current, voltage, or power to input current, voltage, or power, respectively. Gain is usually expressed in dB. |
| I ² C | A two-wire serial computer bus by Philips Semiconductors (now NXP Semiconductors). I2C is an Inter-Integrated Circuit. It is used to connect low-speed peripherals in an embedded system. The original system was created in the early 1980s as a battery control interface, but it was later used as a simple internal bus system for building control electronics. I2C uses only two bi-directional pins, clock and data, both running at +5V and pulled high with resistors. The bus operates at 100 kbits/second in standard mode and 400 kbits/second in fast mode. |
| ICE | The in-circuit emulator that allows users to test the project in a hardware environment, while viewing the debugging device activity in a software environment (PSoC Designer). |
| input/output (I/O) | A device that introduces data into or extracts data from a system. |
| interrupt | A suspension of a process, such as the execution of a computer program, caused by an event external to that process, and performed in such a way that the process can be resumed. |
| interrupt service routine (ISR) | A block of code that normal code execution is diverted to when the M8C receives a hardware interrupt. Many interrupt sources may each exist with its own priority and individual ISR code block. Each ISR code block ends with the RETI instruction, returning the device to the point in the program where it left normal program execution. |
| jitter | <ol style="list-style-type: none"> 1. A misplacement of the timing of a transition from its ideal position. A typical form of corruption that occurs on serial data streams. 2. The abrupt and unwanted variations of one or more signal characteristics, such as the interval between successive pulses, the amplitude of successive cycles, or the frequency or phase of successive cycles. |
| low-voltage detect (LVD) | A circuit that senses V _{DD} and provides an interrupt to the system when V _{DD} falls lower than a selected threshold. |
| M8C | An 8-bit Harvard-architecture microprocessor. The microprocessor coordinates all activity inside a PSoC by interfacing to the Flash, SRAM, and register space. |
| master device | A device that controls the timing for data exchanges between two devices. Or when devices are cascaded in width, the master device is the one that controls the timing for data exchanges between the cascaded devices and an external interface. The controlled device is called the slave device . |
| microcontroller | An integrated circuit chip that is designed primarily for control systems and products. In addition to a CPU, a microcontroller typically includes memory, timing circuits, and IO circuitry. The reason for this is to permit the realization of a controller with a minimal quantity of chips, thus achieving maximal possible miniaturization. This in turn, reduces the volume and the cost of the controller. The microcontroller is normally not used for general-purpose computation as is a microprocessor. |
| mixed-signal | The reference to a circuit containing both analog and digital techniques and components. |
| modulator | A device that imposes a signal on a carrier. |

| | |
|-----------------------------|---|
| noise | <ol style="list-style-type: none">1. A disturbance that affects a signal and that may distort the information carried by the signal.2. The random variations of one or more characteristics of any entity such as voltage, current, or data. |
| oscillator | A circuit that may be crystal controlled and is used to generate a clock frequency. |
| parity | A technique for testing transmitting data. Typically, a binary digit is added to the data to make the sum of all the digits of the binary data either always even (even parity) or always odd (odd parity). |
| phase-locked loop (PLL) | An electronic circuit that controls an oscillator so that it maintains a constant phase angle relative to a reference signal. |
| pinouts | The pin number assignment: the relation between the logical inputs and outputs of the PSoC device and their physical counterparts in the printed circuit board (PCB) package. Pinouts involve pin numbers as a link between schematic and PCB design (both being computer generated files) and may also involve pin names. |
| port | A group of pins, usually eight. |
| power on reset (POR) | A circuit that forces the PSoC device to reset when the voltage is lower than a pre-set level. This is one type of hardware reset. |
| PSoC® | Cypress Semiconductor's PSoC® is a registered trademark and Programmable System-on-Chip™ is a trademark of Cypress. |
| PSoC Designer™ | The software for Cypress' Programmable System-on-Chip technology. |
| pulse width modulator (PWM) | An output in the form of duty cycle which varies as a function of the applied measurand |
| RAM | An acronym for random access memory. A data-storage device from which data can be read out and new data can be written in. |
| register | A storage device with a specific capacity, such as a bit or byte. |
| reset | A means of bringing a system back to a know state. See hardware reset and software reset. |
| ROM | An acronym for read only memory. A data-storage device from which data can be read out, but new data cannot be written in. |
| serial | <ol style="list-style-type: none">1. Pertaining to a process in which all events occur one after the other.2. Pertaining to the sequential or consecutive occurrence of two or more related activities in a single device or channel. |
| settling time | The time it takes for an output signal or value to stabilize after the input has changed from one value to another. |
| shift register | A memory storage device that sequentially shifts a word either left or right to output a stream of serial data. |
| slave device | A device that allows another device to control the timing for data exchanges between two devices. Or when devices are cascaded in width, the slave device is the one that allows another device to control the timing of data exchanges between the cascaded devices and an external interface. The controlling device is called the master device. |
| SRAM | An acronym for static random access memory. A memory device allowing users to store and retrieve data at a high rate of speed. The term static is used because, after a value has been loaded into an SRAM cell, it remains unchanged until it is explicitly altered or until power is removed from the device. |

| | |
|-----------------|---|
| SROM | An acronym for supervisory read only memory. The SROM holds code that is used to boot the device, calibrate circuitry, and perform Flash operations. The functions of the SROM may be accessed in normal user code, operating from Flash. |
| stop bit | A signal following a character or block that prepares the receiving device to receive the next character or block. |
| synchronous | <ol style="list-style-type: none">1. A signal whose data is not acknowledged or acted upon until the next active edge of a clock signal.2. A system whose operation is synchronized by a clock signal. |
| tri-state | A function whose output can adopt three states: 0, 1, and Z (high-impedance). The function does not drive any value in the Z state and, in many respects, may be considered to be disconnected from the rest of the circuit, allowing another output to drive the same net. |
| UART | A UART or universal asynchronous receiver-transmitter translates between parallel bits of data and serial bits. |
| user modules | Pre-build, pre-tested hardware/firmware peripheral functions that take care of managing and configuring the lower level Analog and Digital PSoC Blocks. User Modules also provide high level API (Application Programming Interface) for the peripheral function. |
| user space | The bank 0 space of the register map. The registers in this bank are more likely to be modified during normal program execution and not just during initialization. Registers in bank 1 are most likely to be modified only during the initialization phase of the program. |
| V _{DD} | A name for a power net meaning “voltage drain.” The most positive power supply signal. Usually 5 V or 3.3 V. |
| V _{SS} | A name for a power net meaning “voltage source.” The most negative power supply signal. |
| watchdog timer | A timer that must be serviced periodically. If it is not serviced, the CPU resets after a specified period of time. |

Errata

This section describes the errata for the enCoRe III CY7C64215 device. The information in this document describes hardware issues associated with Silicon Revision A.

Contact your local Cypress sales representative if you have questions.

Part Numbers Affected

| Part Number | Silicon Revision |
|-------------|------------------|
| CY7C64215 | A |

CY7C64215 Qualification Status

Product Status: In Production

CY7C64215 Errata Summary

This table defines the errata applicability to available enCoRe III CY7C64215 family devices.

| Items | Part Number | Silicon Revision | Fix Status |
|---|-------------|------------------|---|
| USB interface DP line pulses low when the enCoRe III device wakes from sleep. | CY7C64215 | A | No silicon fix planned. Use workaround. |
| Invalid flash reads may occur if V_{DD} is pulled to -0.5 V just before power on. | CY7C64215 | A | |
| PMA Index Register fails to auto-increment with CPU_Clock set to SysClk/1 (24 MHz). | CY7C64215 | A | |

1. USB interface DP line pulses low when the enCoRe III device wakes from sleep

■ Problem Definition

When the device operates at 4.75 V to 5.25 V and the 3.3-V regulator is enabled, a short low pulse may be created on the DP signal line during device wakeup. The 15- to 20- μ s low pulse of the DP line may be interpreted by the host computer as a deattach or the beginning of a wakeup.

■ Parameters Affected

The bandgap reference voltage used by the 3.3-V regulator decreases during sleep due to leakage. Upon device wakeup, the bandgap is re-enabled and, after a delay for settling, the 3.3-V regulator is enabled. On some devices the 3.3-V regulator used to generate the USB DP signal may be enabled before the bandgap is fully stabilized. This can cause a low pulse on the regulator output and DP signal line until the bandgap stabilizes. In applications where V_{DD} is 3.3 V, the regulator is not used and, therefore, the DP low pulse is not generated.

■ Trigger Condition

N/A

■ Scope of Impact

N/A

■ Workaround

To prevent the DP signal from pulsing low, keep the bandgap enabled during sleep. The most efficient method is to set the No Buzz bit in the OSC_CR0 register. The No Buzz bit keeps the bandgap powered and output stable during sleep. Setting the No Buzz bit results in a nominal 100 μ A increase in sleep current. Leaving the analog reference block enabled during sleep also resolves this issue because it forces the bandgap to remain enabled. The following example shows how to disable the No Buzz bit:

Assembly

```
M8C_SetBank1
    or    reg[OSC_CR0], 0x20
M8C_SetBank0
```

C

```
OSC_CR0 |= 0x20;
```


■ Fix Status

There is no planned silicon fix; use workaround.

2. Invalid flash reads may occur if V_{DD} is pulled to -0.5 V just before power on**■ Problem Definition**

When V_{DD} of the device is pulled below ground just before power on, the first read from each 8-KB flash page may be corrupted. This issue does not affect flash page 0 because it is the selected page upon reset.

■ Parameters Affected

When V_{DD} is pulled below ground before power on, an internal flash reference may deviate from its nominal voltage. The reference deviation tends to result in the first flash read from that page returning 0xFF. During the first read from each page, the reference is reset resulting in all future reads returning the correct value. A short delay of 5 μs before the first real read provides time for the reference voltage to stabilize.

■ Trigger Condition

N/A

■ Scope of Impact

N/A

■ Workaround

To prevent an invalid flash read, a dummy read from each flash page must occur before use of the pages. A delay of 5 μs must occur after the dummy read and before a real read. The dummy reads occur as soon as possible and must be located in flash page 0 before a read from any other flash page. An example for reading a byte of memory from each flash page is listed below. Place it in *boot.tpl* and *boot.asm* immediately after the 'start:' label.

```
// dummy read from each 8K Flash page
// page 1
movA, 0x20      // MSB
movX, 0x00      // LSB
romx
// wait at least 5 μs
movX, 14
loop1:
decX
jnzloop1
```

■ Fix Status

There is no planned silicon fix; use workaround.

3. PMA Index Register fails to auto-increment with CPU_Clock set to SysClk/1 (24 MHz)**■ Problem Definition**

When the device operates at 4.75 V to 5.25 V and the CPU_Clock is set to SysClk/1 (24 MHz), the USB PMA Index Register may fail to increment automatically when used in an OUT endpoint configuration at full-speed. When the application program attempts to use the bReadOutEP() function, the first byte in the PMA buffer is always returned.

■ Parameters Affected

An internal flip-flop hold problem is associated with the index register increment function. All reads of the associated RAM originate from the first byte. The hold problem has no impact on other circuits or functions within the device.

■ Trigger Condition

N/A

■ Scope of Impact

N/A

■ WORKAROUND

To make certain that the index register properly increments, set the CPU_Clock to SysClk/2 (12 MHz) during the read of the PMA buffer. An example for the clock adjustment method follows:

PSoC Designer 4.3 User Module workaround: PSoC Designer Release 4.3 and subsequent releases include a revised full-speed USB User Module with the revised firmware workaround included (see the following example).

```
24-Mhz read PMA workaround
;;
M8C_SetBank1
mov A, reg[OSC_CR0]
push A
and A, 0xf8 ;clear the clock bits (briefly chg the cpu_clk to 3Mhz)
or A, 0x02 ;will set clk to 12Mhz

mov reg[OSC_CR0],A ;clk is now set at 12Mhz
M8C_SetBank0
.loop:
    mov A, reg[PMA0_DR] ; Get the data from the PMA space
    mov [X], A ; save it in data array
    inc X ; increment the pointer
    dec [USB_APITemp+1] ; decrement the counter
    jnz .loop ; wait for count to zero out
;;
;; 24Mhz read PMA workaround (back to previous clock speed)
;;
pop A ;recover previous reg[OSC_CR0] value
M8C_SetBank1
mov reg[OSC_CR0],A ;clk is now set at previous value
M8C_SetBank0
;;
;; end 24Mhz read PMA workaround
```

■ Fix Status

There is no planned silicon fix; use workaround.

Document History Page

| Description Title: CY7C64215, enCoRe™ III Full-Speed USB Controller Document Number: 38-08036 | | | | |
|--|---------|-----------------|-----------------|---|
| Rev. | ECN No. | Submission Date | Orig. of Change | Description of Change |
| ** | 131325 | See ECN | XGR | New data sheet. |
| *A | 385256 | See ECN | BHA | Changed status from Advance Information to Preliminary. Added standard data sheet items. Changed Part number from CY7C642xx to CY7C64215. |
| *B | 2547630 | 08/04/2008 | AZIEL / PYRS | Operational voltage range for USB specified under "Full Speed USB (12Mbps)". CMP_GO_EN1 register removed as it has no functionality on Radon. Figure "CPU Frequency" adjusted to show invalid operating region for USB with footnote describing reason. DC electrical characteristic, V _{DD} . Note added describing where USB hardware is non-functional. |
| *C | 2620679 | 12/12/2008 | CMCC / PYRS | Added Package Handling information. Deleted note regarding link to amkor.com for MLF package dimensions. |
| *D | 2717887 | 06/11/2009 | DPT | Added 56 -Pin Sawn QFN (8 X 8 mm) package diagram and added CY7C64215-56LTXC part information in the Ordering Information table. |
| *E | 2852393 | 01/15/2010 | BHA / XUT | <ul style="list-style-type: none"> ■ Added Table of Contents. ■ Added external clock oscillator option and Industrial Temperature information to the Features, Pin Information, Electrical Specifications, Operating Temperature, DC Electrical Characteristics, AC Electrical Characteristics, and Ordering Information sections. ■ Updated DC GPIO, AC Chip, and AC Programming Specifications follows: <ul style="list-style-type: none"> □ Replaced TRAMP (time) with SRPOWER_UP (slew rate) specification. □ Added I_{OH}, I_{OL}, DCILO, F32K_U, TPOWERUP, TERASEALL, TPROGRAM_HOT, and TPROGRAM_COLD specifications. □ Updated V_{DD} ranges on Figure 5 and Table 8. □ Added notes for VM and VDI on Table 10. □ Removed TR/TF from Table 20. ■ Update Ordering Information for: CY7C64215-56LFXCT, CY7C64215-28PVXCT, CY7C64215-56LTXIT Tape and Reel. ■ Updated 28-Pin SSOP and 56-Pin QFN PUNCH and SAWN package diagrams. ■ Updated copyright and Sales, Solutions, and Legal Information URLs. |
| *F | 2892683 | 03/15/2010 | NJF | Updated Cypress website links. Added T _{BAKETEMP} and T _{BAKETIME} parameters in Absolute Maximum Ratings . Updated AC Chip-Level Specifications Removed inactive parts from Ordering Information Updated note in Packaging Information . |
| *G | 3070717 | 10/25/2010 | XUT | Removed reference to CYFISPI in Features . Updated datasheet as per Cypress style guide and new datasheet template. |
| *H | 3090908 | 11/19/10 | CSAI | Updated AC Chip-Level Specifications table. Added DC I ² C Specification. |
| *I | 3143408 | 01/17/11 | NJF | Added DC I ² C Specifications table. Added T _{jit_IMO} specification, removed existing jitter specifications. Updated Analog reference tables. Updated Units of Measure, Acronyms, Glossary, and References sections. Updated solder reflow specifications. No specific changes were made to AC Digital Block Specifications table and I ² C Timing Diagram. They were updated for clearer understanding. |

Document History Page (continued)

| Description Title: CY7C64215, enCoRe™ III Full-Speed USB Controller Document Number: 38-08036 | | | | |
|--|---------|-----------------|-----------------|---|
| Rev. | ECN No. | Submission Date | Orig. of Change | Description of Change |
| *J | 3995635 | 05/09/2013 | CSAI | Updated Packaging Information : spec 001-12921 – Changed revision from *A to *B. spec 001-53450 – Changed revision from *B to *C. spec 51-85079 – Changed revision from *D to *E. Added Errata . |
| *K | 4080167 | 07/29/2013 | CSAI | Added Errata footnotes (Note 3, 5). Updated Electrical Specifications : Updated DC Electrical Characteristics : Updated DC Chip-Level Specifications : Added Note 3 and referred the same note in “Sleep Mode” in description of I _{SB} parameter in Table 7 . Updated DC POR and LVD Specifications : Added Note 5 and referred the same note in V _{PPOR0} , V _{PPOR1} , V _{PPOR2} parameters in Table 15 . Updated Reference Documents : Removed references of spec 001-17397 and spec 001-14503 as these specs are obsolete. Updated in new template. |
| *L | 4247931 | 01/16/2014 | CSAI | Updated Packaging Information : spec 001-53450 – Changed revision from *C to *D. Completing Sunset Review. |
| *M | 4481449 | 08/28/2014 | MVTA | Updated Packaging Information : spec 001-12921 – Changed revision from *B to *C. Updated Ordering Information (Updated part numbers). Updated in new template. |
| *N | 5730242 | 05/10/2017 | MVTA | Updated Packaging Information : spec 51-85079 - Changed revision from *E to *F. Updated Cypress Logo and Copyright. |

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