

IS61/64WV25616EFALL IS61/64WV25616EFBLL

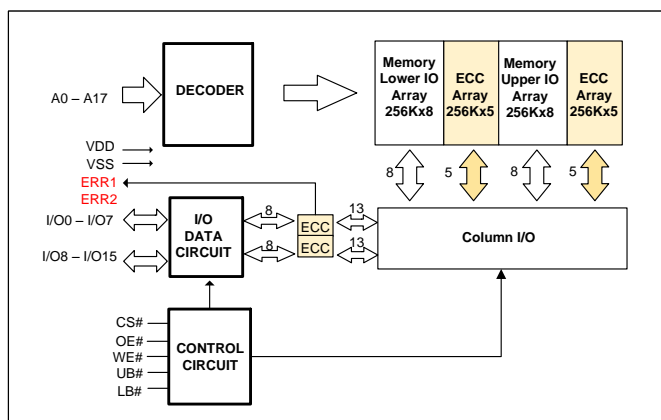
APRIL 2018

256Kx16 HIGH SPEED ASYNCHRONOUS CMOS STATIC RAM with ECC

KEY FEATURES

- High-speed access time: 8, 10ns, 12ns
- Single power supply
 - 1.65V-2.2V V_{DD} (IS61/64WV25616EFALL)
 - 2.4V-3.6V V_{DD} (IS61/64WV25616EFBLL)
- Error Detection and Correction with optional ERR1/ERR2 output pin:
 - ERR1 pin indicates 1-bit error detection and correction.
 - ERR2 pin indicates 2-bit error detection
- Three state outputs
- Industrial and Automotive temperature support
- Lead-free available

FUNCTIONAL BLOCK DIAGRAM



DESCRIPTION

The *ISSI* IS61/64WV25616EFALL/EFBLL are high-speed, low power, 4M bit static RAMs organized as 256K words by 16 bits. It is fabricated using *ISSI*'s high-performance CMOS technology and implemented ECC function to improve reliability.

This highly reliable process coupled with innovative circuit design techniques including ECC (SEC-DED: Single Error Correcting-Double Error Detecting) yield high-performance and highly reliable devices.

When CS# is HIGH (deselected), the device assumes a standby mode at which the power dissipation can be reduced down with CMOS input levels.

Easy memory expansion is provided by using Chip Enable and Output Enable inputs. The active LOW Write Enable (WE#) controls both writing and reading of the memory. A data byte allows Upper Byte (UB#) and Lower Byte (LB#) access.

The IS61/64WV25616EFALL/EFBLL are packaged in the JEDEC standard 48-ball mini BGA (6mm x 8mm), and 44-pin TSOP (TYPE II)

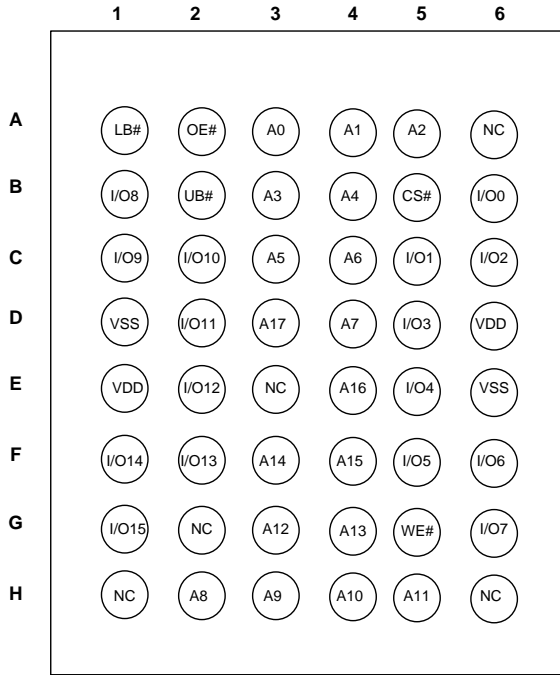
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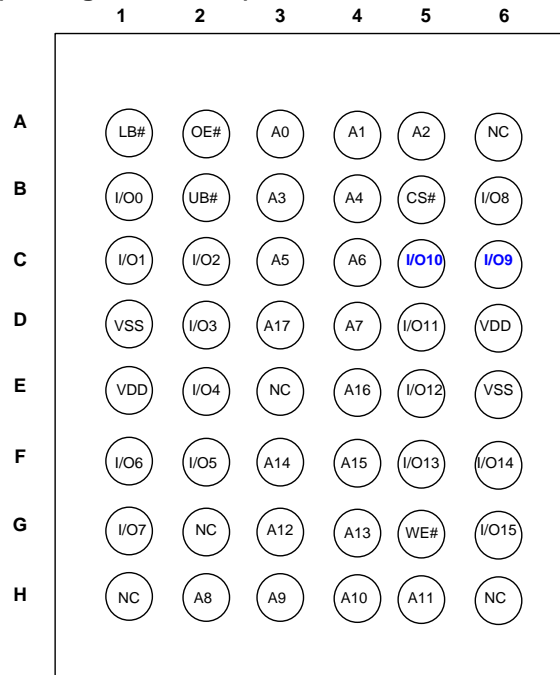
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- b.) the user assume all such risks; and
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PIN CONFIGURATIONS

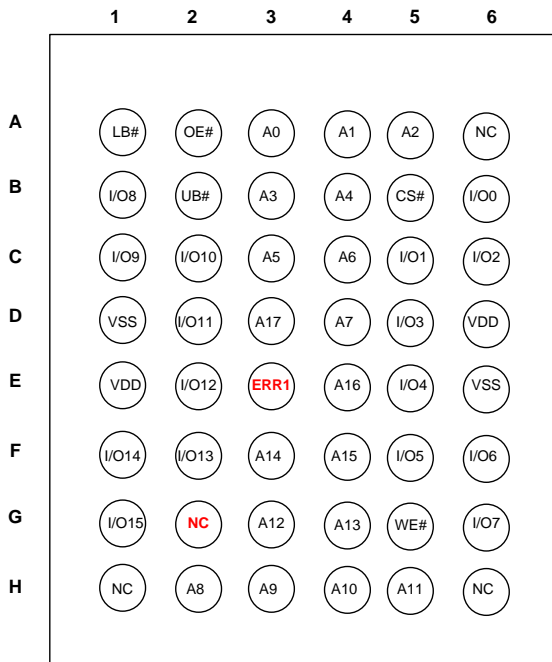
48-Ball mini BGA(6mm x 8mm),
(Package Code : B)



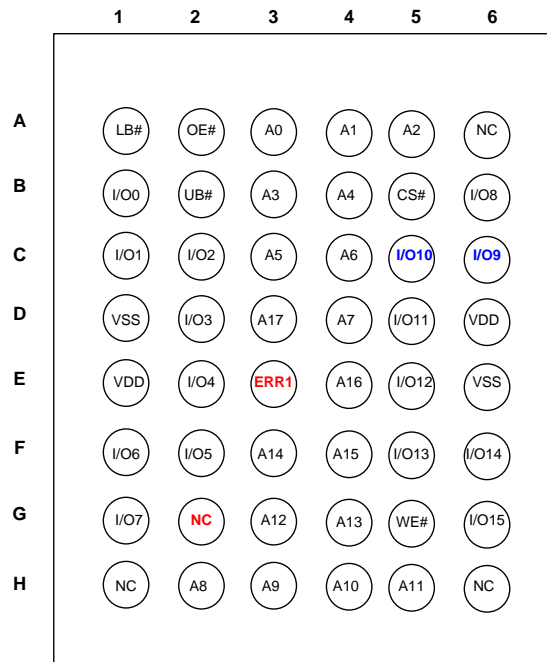
48-Ball mini BGA (6mm x 8mm) , Switched IO
(Package Code : B2)



48-Ball mini BGA(6mm x 8mm), ERR1
(Package Code : B3)



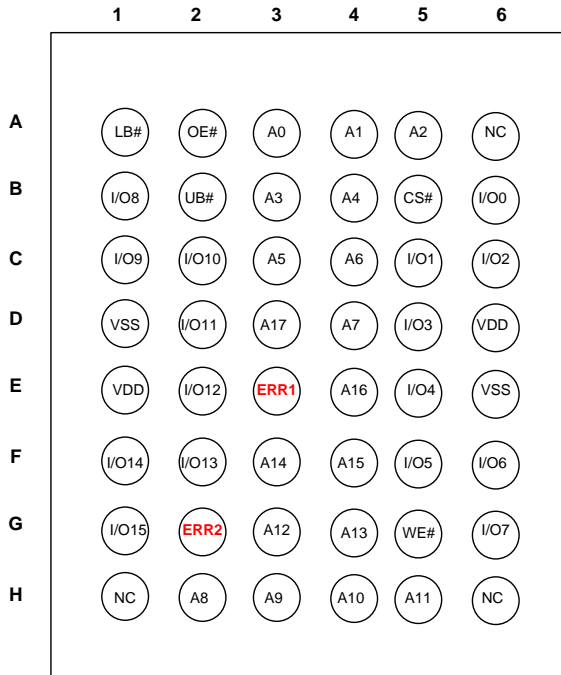
48-Ball mini BGA (6mm x 8mm) , ERR1
(Package Code : B4)



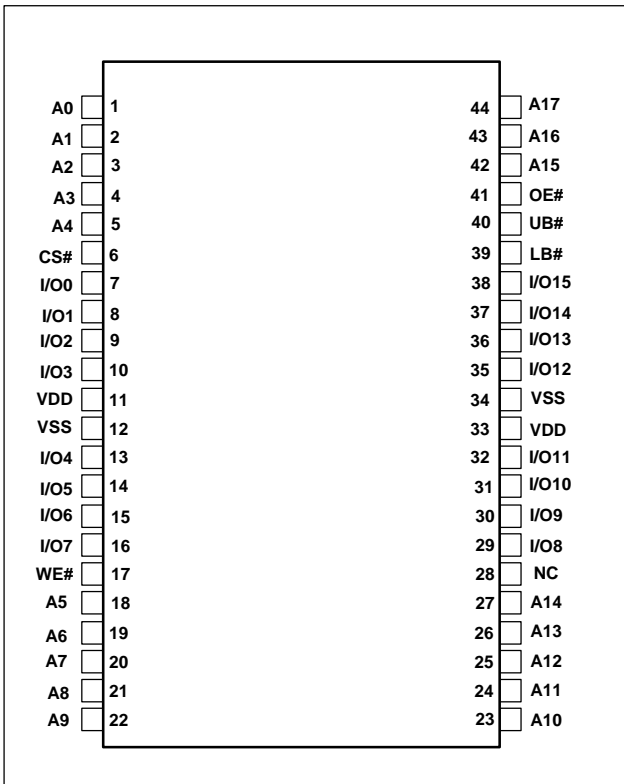
IS61/64WV25616EFALL
IS61/64WV25616EFBLL



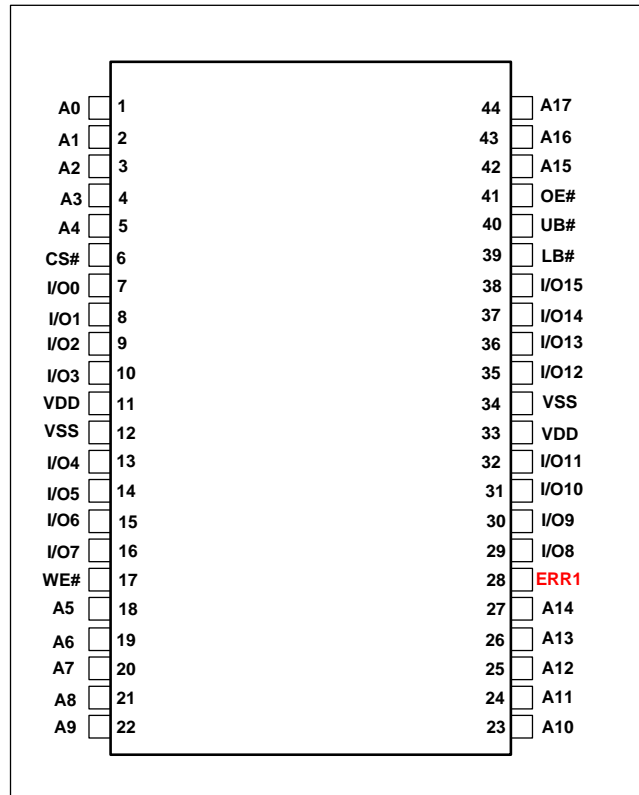
48-Ball BGA (6mm x 8mm) , ERR1/2
(Package Code : B5)



44-Pin TSOP-II, (Package Code : T)



44-Pin TSOP-II with ERR1, (Package Code : T2)



PIN DESCRIPTIONS

| | |
|------------|--|
| A0-A17 | Address Inputs |
| I/O0-I/O15 | Data Inputs/Outputs |
| CS# | Chip Enable Input |
| OE# | Output Enable Input |
| WE# | Write Enable Input |
| LB# | Lower-byte Control (I/O0-I/O7) |
| UB# | Upper-byte Control (I/O8-I/O15) |
| ERR1 | 1-bit Error Detection and Correction Signal |
| ERR2 | 2-bit ERR Detection Signal |
| NC | No Connection |
| VDD | Power |
| VSS | Ground |

FUNCTION DESCRIPTION

SRAM is one of random access memories. Each byte or word has an address and can be accessed randomly. SRAM has three different modes supported. Each function is described below with Truth Table.

STANDBY MODE

Device enters standby mode when deselected (CS# HIGH). The input and output pins (I/O0-15) are placed in a high impedance state. CMOS input in this mode will maximize saving power.

WRITE MODE

Write operation issues with Chip selected (CS#) and Write Enable (WE#) input LOW. The input and output pins (I/O0-15) are in data input mode. Output buffers are closed during this time even if OE# is LOW. UB# and LB# enables a byte write feature. By enabling LB# LOW, data from I/O pins (I/O0 through I/O7) are written into the location specified on the address pins. And with UB# being LOW, data from I/O pins (I/O8 through I/O15) are written into the location.

READ MODE

Read operation issues with Chip selected (CS# LOW) and Write Enable (WE#) input HIGH. When OE# is LOW, output buffer turns on to make data output. Any input to I/O pins during READ mode is not permitted. UB# and LB# enables a byte read feature. By enabling LB# LOW, data from memory appears on I/O0-7. And with UB# being LOW, data from memory appears on I/O8-15.

In the READ mode, output buffers can be turned off by pulling OE# HIGH. In this mode, internal device operates as READ but I/Os are in a high impedance state. Since device is in READ mode, active current is used.

ERROR DETECTION AND ERROR CORRECTION

- Independent ECC per each byte
 - detect and correct one bit error per byte or detect 2-bit error per byte
- Optional ERR1 output signal indicates 1-bit error detection and correction
- Optional ERR2 output signal indicates 2-bit error detection.
- Controller can use either ERR1 or ERR2 to monitor ECC event. Unused pins (ERR1 or ERR2) can be left floating.
- Better reliability than parity code schemes which can only detect an error but not correct an error
- Backward Compatible: Drop in replacement to current in industry standard devices (without ECC)

ERR1, ERR2 OUTPUT SIGNAL BEHAVIOR

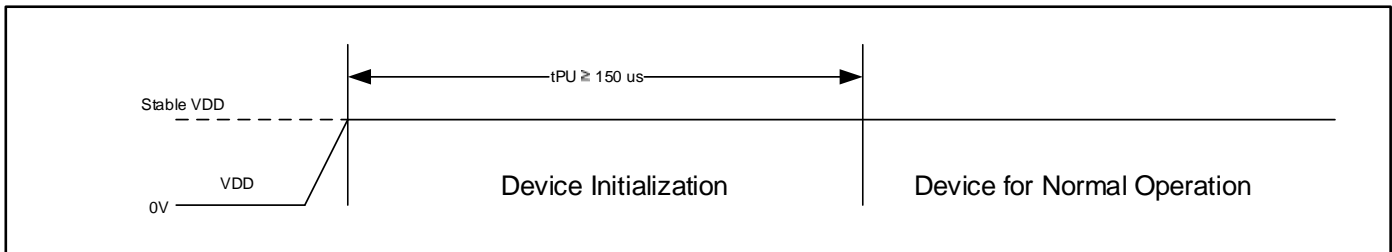
| ERR1 | ERR2 | DQ pin | Status | Remark |
|--------|--------|------------|---------------------|---|
| 0 | 0 | Valid Q | No Error | |
| 1 | 0 | Valid Q | 1-Bit Error only | 1-bit error per byte detected and corrected |
| 0 | 1 | In-Valid Q | 2-Bit Error only | No 1-bit error. 2-bit error per byte detected (out of 2 bytes) |
| 1 | 1 | In-Valid Q | 1-bit & 2-bit error | 1-bit error detected and corrected at one byte, and 2-bit error detected at another byte. |
| High-Z | High-Z | Valid D | Non-Read | Write operation or Output Disabled |

TRUTH TABLE

| Mode | CS# | WE# | OE# | LB# | UB# | I/O0-I/O7 | I/O8-I/O15 | VDD Current |
|-----------------|-----|-----|-----|-----|-----|-----------|------------|-------------------------------------|
| Not Selected | H | X | X | X | X | High-Z | High-Z | I _{SB1} , I _{SB2} |
| Output Disabled | L | H | H | L | L | High-Z | High-Z | ICC |
| | L | H | H | H | L | High-Z | High-Z | |
| Read | L | H | L | L | H | DOUT | High-Z | ICC |
| | L | H | L | H | L | High-Z | DOUT | |
| | L | H | L | L | L | DOUT | DOUT | |
| Write | L | L | X | L | H | DIN | High-Z | ICC |
| | L | L | X | H | L | High-Z | DIN | |
| | L | L | X | L | L | DIN | DIN | |

POWER UP INITIALIZATION

The device includes on-chip voltage sensor used to launch POWER-UP initialization process. When VDD reaches stable level, the device requires 150us of t_{PU} (Power-Up Time) to complete its self-initialization process. When initialization is complete, the device is ready for normal operation.



ABSOLUTE MAXIMUM RATINGS AND OPERATING RANGE

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

| Symbol | Parameter | Value | Unit |
|-------------------|--------------------------------------|--------------------------------|------|
| V _{term} | Terminal Voltage with Respect to VSS | -0.5 to V _{DD} + 0.5V | V |
| V _{DD} | V _{DD} Related to VSS | -0.3 to 4.0 | V |
| t _{Stg} | Storage Temperature | -65 to +150 | °C |
| P _T | Power Dissipation | 1.0 | W |

Note:

1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

PIN CAPACITANCE ⁽¹⁾

| Parameter | Symbol | Test Condition | Max | Units |
|---------------------------|------------------|---|-----|-------|
| Input capacitance | C _{IN} | T _A = 25°C, f = 1 MHz, V _{DD} = V _{DD} (typ) | 6 | pF |
| DQ capacitance (IO0–IO15) | C _{I/O} | | 8 | pF |

Note:

1. These parameters are guaranteed by design and tested by a sample basis only.

OPERATING RANGE⁽¹⁾

| Range | Ambient Temperature | PART NUMBER | VDD | SPEED (MAX) |
|-----------------|---------------------|------------------|--------------|-------------|
| Commercial | 0°C to +70°C | IS61WV25616EFALL | 1.65V – 2.2V | 10 ns |
| | | IS61WV25616EFBLL | 2.4V – 3.6V | |
| | | | | |
| Industrial | -40°C to +85°C | IS61WV25616EFALL | 1.65V – 2.2V | 10 ns |
| | | IS61WV25616EFBLL | 2.4V – 3.6V | |
| | | | | |
| Automotive (A3) | -40°C to +125°C | IS64WV25616EFALL | 1.65V – 2.2V | 10 ns |
| | | IS64WV25616EFBLL | 2.4V – 3.6V | |

AC TEST CONDITIONS (OVER THE OPERATING RANGE)

| Parameter | Unit (1.65V~2.2V) | Unit (2.4V~3.6V) | Unit (3.3V +/-10%) |
|-------------------------------|-------------------------|----------------------|-----------------------|
| Input Pulse Level | 0V to V_{DD} | 0V to V_{DD} | 0V to V_{DD} |
| Input Rise and Fall Time | 1.5 ns | 1.5 ns | 1.5 ns |
| Output Timing Reference Level | $\frac{1}{2} V_{DD}$ | $\frac{1}{2} V_{DD}$ | $\frac{1}{2} V_{DD}$ |
| R1 (ohm) | 13500 | 319 | 319 |
| R2 (ohm) | 10800 | 353 | 353 |
| V_{TM} (V) | V_{DD} | V_{DD} | V_{DD} |
| Output Load Conditions | Refer to Figure 1 and 2 | | |

AC TEST LOADS

FIGURE 1

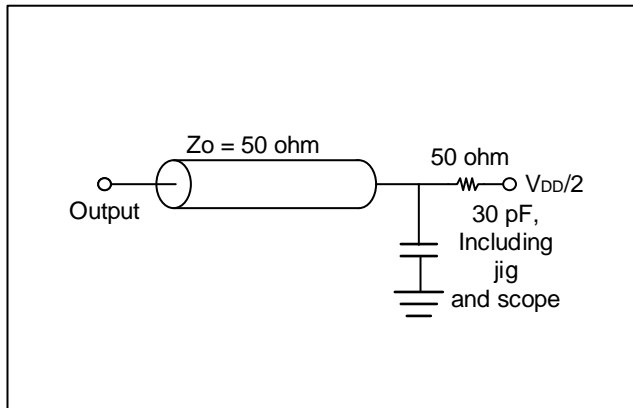
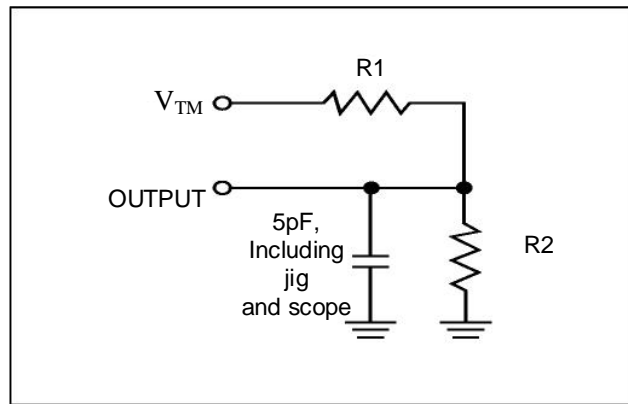


FIGURE 2



DC ELECTRICAL CHARACTERISTICS

DC ELECTRICAL CHARACTERISTICS (OVER THE OPERATING RANGE)

IS61/64WV25616EFALL (VDD = 1.65V – 2.2V)

| Symbol | Parameter | Test Conditions | Min. | Max. | Unit |
|----------------------------------|---------------------|---|------|-----------------------|------|
| V _{OH} | Output HIGH Voltage | I _{OH} = -0.1 mA | 1.4 | — | V |
| V _{OL} | Output LOW Voltage | I _{OL} = 0.1 mA | — | 0.2 | V |
| V _{IH} (¹) | Input HIGH Voltage | | 1.4 | V _{DD} + 0.2 | V |
| V _{IL} (¹) | Input LOW Voltage | | -0.2 | 0.4 | V |
| I _{LI} | Input Leakage | GND < V _{IN} < V _{DD} | -1 | 1 | μA |
| I _{LO} | Output Leakage | GND < V _{IN} < V _{DD} , Output Disabled | -1 | 1 | μA |

Note:

- V_{ILL}(min) = -1.0V AC (pulse width < 10ns). Not 100% tested.
V_{IHH}(max) = V_{DD} + 1.0V AC (pulse width < 10ns). Not 100% tested.

IS61/64WV25616EFBLL (VDD = 2.4V – 3.6V)

| Symbol | Parameter | Test Conditions | Min. | Max. | Unit | |
|----------------------------------|---------------------|---|---|------|-----------------------|---|
| V _{OH} | Output HIGH Voltage | 2.4V ~ 2.7V | V _{DD} = Min., I _{OH} = -1.0 mA | 2.0 | — | V |
| | | 2.7V ~ 3.6V | V _{DD} = Min., I _{OH} = -4.0 mA | 2.2 | | |
| V _{OL} | Output LOW Voltage | 2.4V ~ 2.7V | V _{DD} = Min., I _{OL} = 2.0 mA | — | 0.4 | V |
| | | 2.7V ~ 3.6V | V _{DD} = Min., I _{OL} = 8.0 mA | — | 0.4 | |
| V _{IH} (¹) | Input HIGH Voltage | 2.4V ~ 2.7V | | 2.0 | V _{DD} + 0.3 | V |
| | | 2.7V ~ 3.6V | | 2.0 | | |
| V _{IL} (¹) | Input LOW Voltage | 2.4V ~ 2.7V | | -0.3 | 0.6 | V |
| | | 2.7V ~ 3.6V | | -0.3 | 0.8 | |
| I _{LI} | Input Leakage | V _{SS} < V _{IN} < V _{DD} | -2 | 2 | μA | |
| I _{LO} | Output Leakage | V _{SS} < V _{IN} < V _{DD} , Output Disabled | -2 | 2 | μA | |

Note:

- V_{IL}(min) = -0.3V DC ; V_{IL}(min) = -2.0V AC (pulse width 2.0ns). Not 100% tested.
V_{IH}(max) = V_{DD} + 0.3V DC ; V_{IH}(max) = V_{DD} + 2.0V AC (pulse width 2.0ns). Not 100% tested.

POWER SUPPLY CHARACTERISTICS-II FOR POWER (OVER THE OPERATING RANGE)

| Symbol | Parameter | Test Conditions | Grade | -8 ⁽³⁾ Max. | -10 Max. | -12 Max. | Unit |
|--------|--|--|---------------------|---------------------------|-------------|-------------|------|
| ICC | V _{DD} Dynamic Operating Supply Current | V _{DD} = MAX, I _{OUT} = 0 mA, f = f _{MAX} | Com. | 40 | 30 | 30 | mA |
| | | | Ind. | 45 | 35 | 35 | |
| | | | Auto. | - | 40 | 40 | |
| ICC1 | Operating Supply Current | V _{DD} = MAX, I _{OUT} = 0 mA, f = 0 | Com. | 20 | 20 | 20 | mA |
| | | | Ind. | 25 | 25 | 25 | |
| | | | Auto. | - | 35 | 35 | |
| ISB1 | TTL Standby Current (TTL Inputs) | V _{DD} = MAX, V _{IN} = V _{IH} or V _{IL} CS# ≥ V _{IH} , f = 0 | Com. | 15 | 15 | 15 | mA |
| | | | Ind. | 20 | 20 | 20 | |
| | | | Auto. | - | 30 | 30 | |
| ISB2 | CMOS Standby Current (CMOS Inputs) | V _{DD} = MAX, CS# ≥ V _{DD} - 0.2V V _{IN} ≥ V _{DD} - 0.2V, or V _{IN} ≤ 0.2V , f = 0 | Com. | 8 | 8 | 8 | mA |
| | | | Ind. | 10 | 10 | 10 | |
| | | | Auto. | - | 20 | 20 | |
| | | | Typ. ⁽²⁾ | 3 | | | |

Notes:

1. At f = f_{MAX}, address and data inputs are cycling at the maximum frequency, f = 0 means no input line change.
2. Typical value indicate the value for the center of distribution, measured at V_{DD} = 3.0V/1.8V, T_A = 25 °C, and not 100% tested.
3. 8ns is at V_{DD}=3.3V +/-10%

AC CHARACTERISTICS (OVER OPERATING RANGE)

READ CYCLE AC CHARACTERISTICS⁽¹⁾

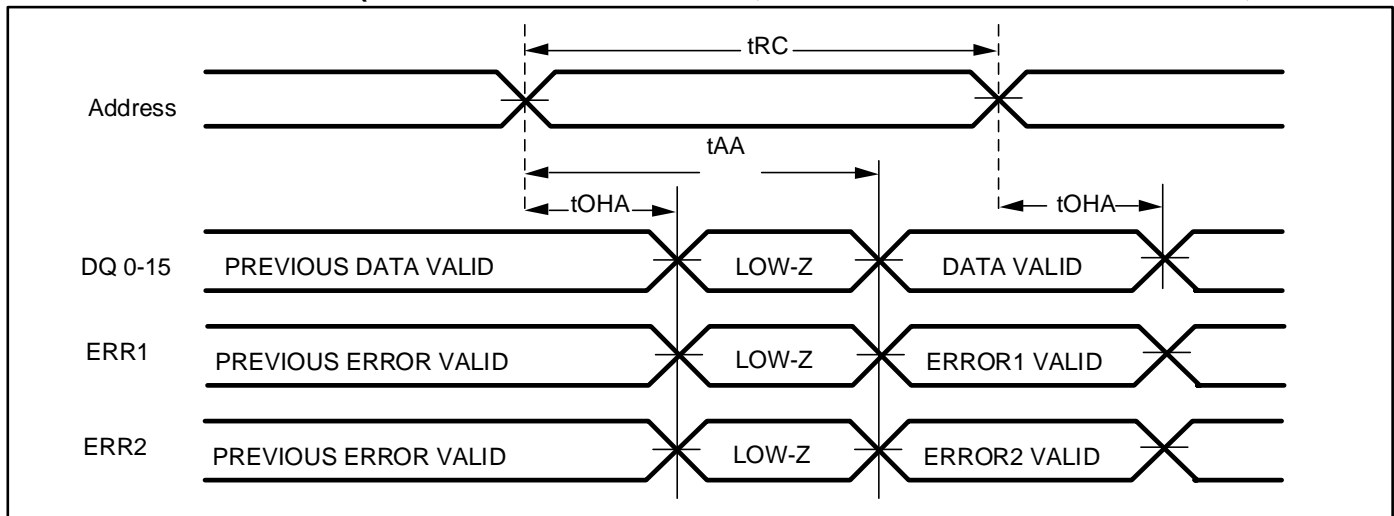
| Parameter | Symbol | -8 ⁽³⁾ | | -10 | | -12 | | unit | notes |
|---------------------------|--------|-------------------|-----|-----|-----|-----|-----|------|-------|
| | | Min | Min | Min | Min | Min | Max | | |
| Read Cycle Time | tRC | 8 | - | 10 | - | 12 | - | ns | |
| Address Access Time | tAA | - | 8 | - | 10 | - | 12 | ns | |
| Output Hold Time | tOHA | 2.0 | - | 2.5 | - | 2.5 | - | ns | |
| CS# Access Time | tACE | - | 8 | - | 10 | - | 12 | ns | |
| OE# Access Time | tDOE | - | 4.5 | - | 6 | - | 7 | ns | |
| OE# to High-Z Output | tHZOE | 0 | 3 | 0 | 5 | 0 | 6 | ns | 2 |
| OE# to Low-Z Output | tLZOE | 0 | - | 0 | - | 0 | - | ns | 2 |
| CS# to High-Z Output | tHZCE | 0 | 3 | 0 | 5 | 0 | 6 | ns | 2 |
| CS# to Low-Z Output | tLZCE | 3 | - | 3 | - | 3 | - | ns | 2 |
| UB#, LB# Access Time | tBA | - | 5.5 | - | 6 | - | 7 | ns | |
| UB#, LB# to High-Z Output | tHZB | 0 | 3 | 0 | 5 | 0 | 6 | ns | 2 |
| UB#, LB# to Low-Z Output | tLZB | 0 | - | 0 | - | 0 | - | ns | 2 |

Notes:

1. Test conditions assume signal transition times of 1.5 ns or less, timing reference levels of $V_{DD}/2$, input pulse levels of 0V to V_{DD} and output loading specified in Figure 1.
2. Tested with the load in Figure 2. Transition is measured ± 500 mV from steady-state voltage. Not 100% tested.
3. 8ns is at $V_{DD}=3.3V \pm 10\%$

AC WAVEFORMS

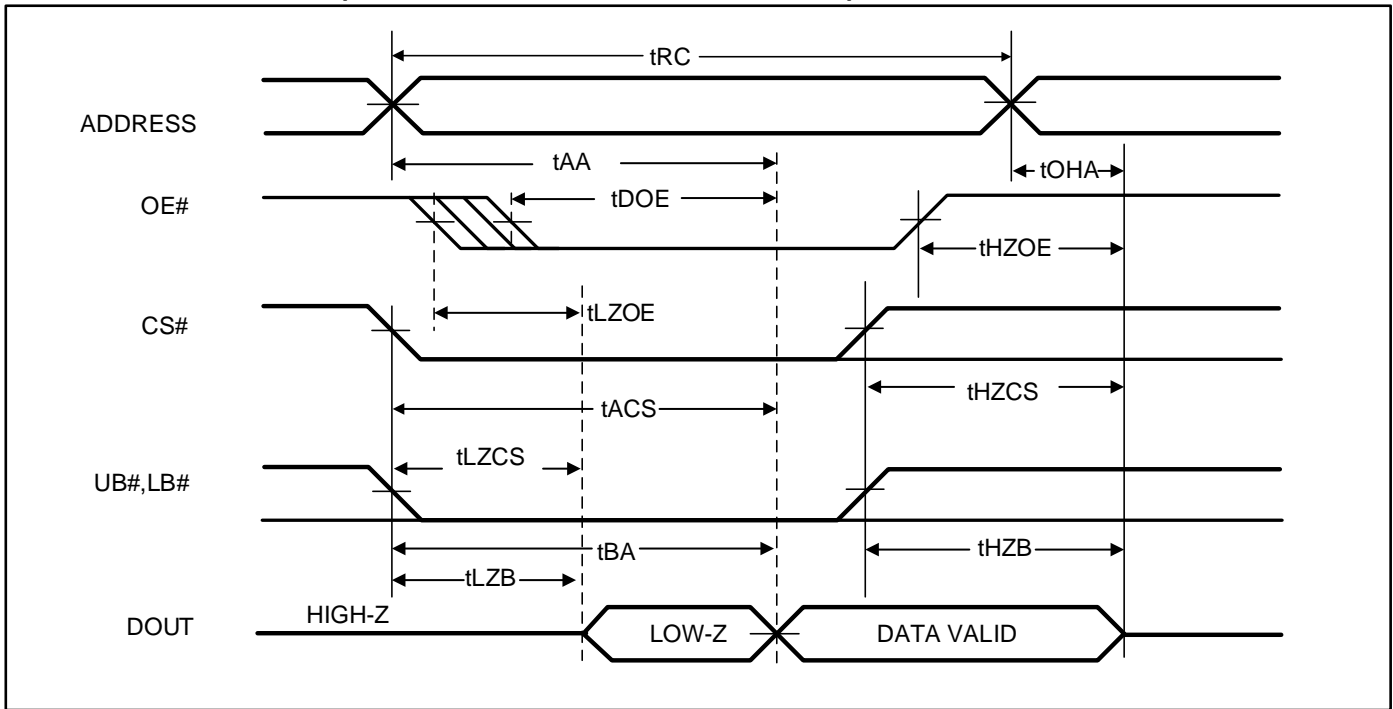
READ CYCLE NO. 1^(1,2) (ADDRESS CONTROLLED, CS# = OE# = UB# = LB# = LOW, WE# = HIGH)



Notes:

1. The device is continuously selected.
2. ERR1, ERR2 signals act like a Read Data Q during Read Operation.

READ CYCLE NO. 2⁽¹⁾ (OE# CONTROLLED, WE# = HIGH)



Note:

1. Address is valid prior to or coincident with CS# LOW transition.

WRITE CYCLE AC CHARACTERISTICS⁽¹⁾

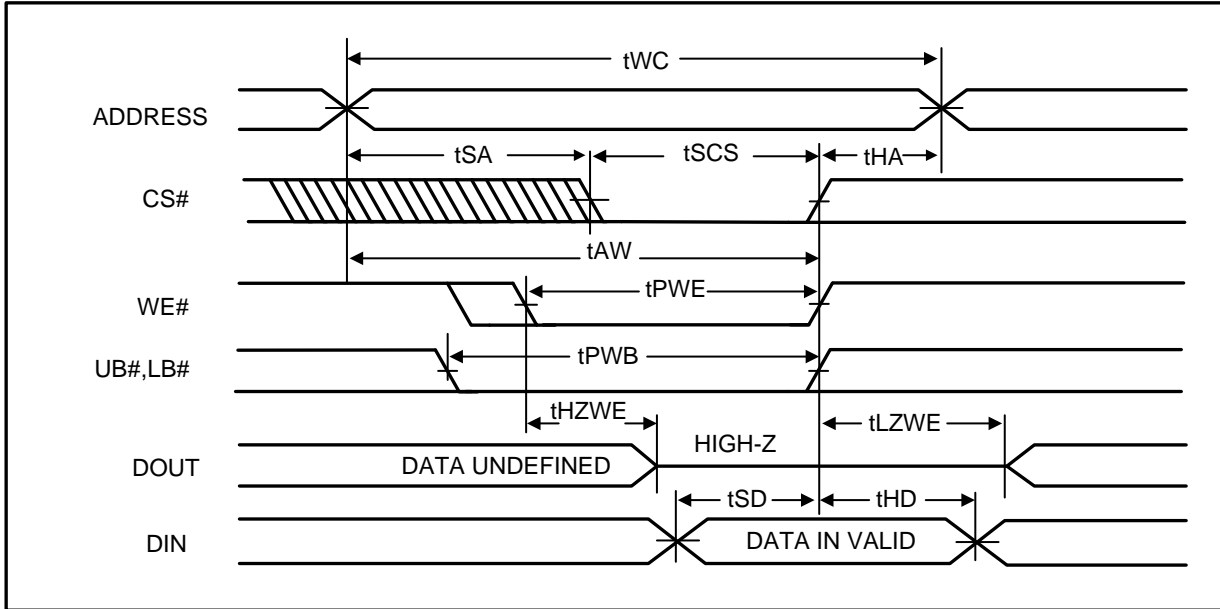
| Parameter | Symbol | -8 ⁽³⁾ | | -10 | | -12 | | unit | notes |
|---------------------------------|--------|-------------------|-----|-----|-----|-----|-----|------|-------|
| | | Min | Max | Min | Max | Min | Max | | |
| Write Cycle Time | tWC | 8 | - | 10 | - | 12 | - | ns | |
| CS# to Write End | tSCS | 6.5 | - | 8 | - | 9 | - | ns | |
| Address Setup Time to Write End | tAW | 6.5 | - | 8 | - | 9 | - | ns | |
| UB#,LB# to Write End | tPWB | 6.5 | - | 8 | - | 9 | - | ns | |
| Address Hold from Write End | tHA | 0 | - | 0 | - | 0 | - | ns | |
| Address Setup Time | tSA | 0 | - | 0 | - | 0 | - | ns | |
| WE# Pulse Width | tPWE1 | 6.5 | - | 8 | - | 9 | - | ns | |
| WE# Pulse Width (OE# = LOW) | tPWE2 | 8 | - | 10 | - | 12 | - | ns | 2 |
| Data Setup to Write End | tSD | 5 | - | 6 | - | 7 | - | ns | |
| Data Hold from Write End | tHD | 0 | - | 0 | - | 0 | - | ns | |
| WE# LOW to High-Z Output | tHZWE | - | 3.5 | - | 4 | - | 5 | ns | |
| WE# HIGH to Low-Z Output | tLZWE | 2 | - | 2 | - | 2 | - | ns | |

Notes:

- 1 The internal write time is defined by the overlap of CS# = LOW, UB# or LB# = LOW, and WE# = LOW. All conditions must be in valid states to initiate a Write, but any condition can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the write.
- 2 tPWE > tHZWE + tSD when OE# is LOW.
- 3 8ns is at VDD=3.3V +/-10%

AC WAVEFORMS

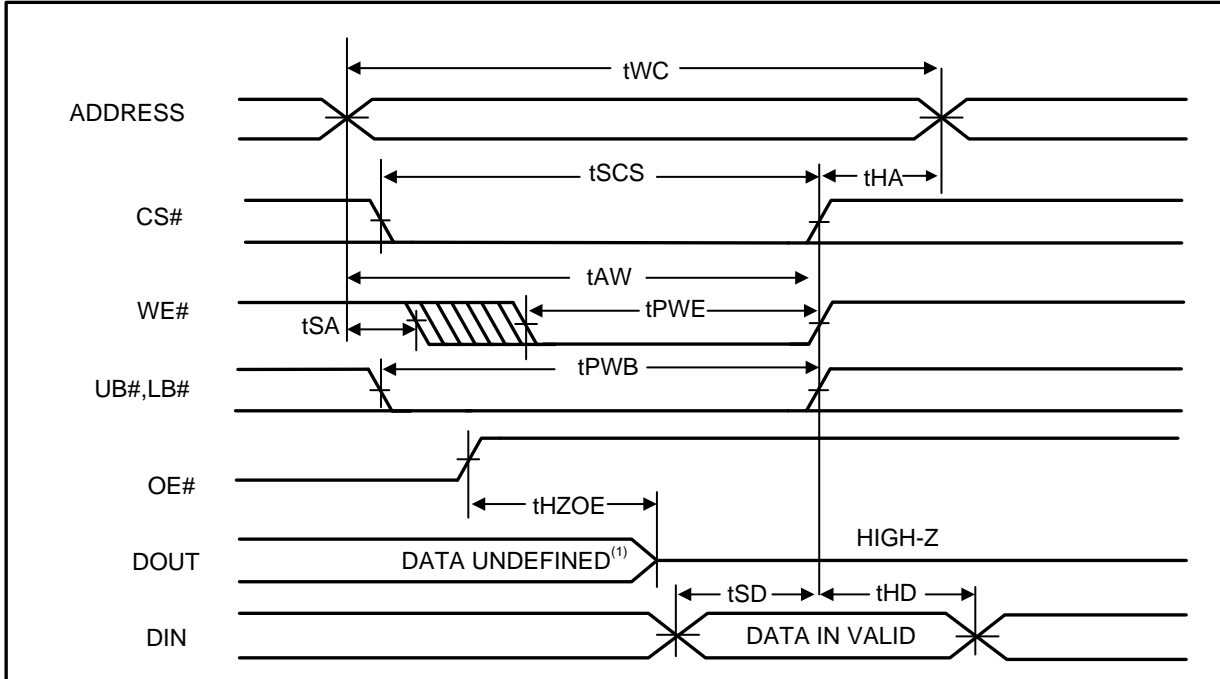
WRITE CYCLE NO. 1⁽¹⁾ (CS# CONTROLLED, OE# = HIGH OR LOW)



Note:

1. I/O will assume the High-Z state if CS# = V_{IH} or OE# = V_{IH} .

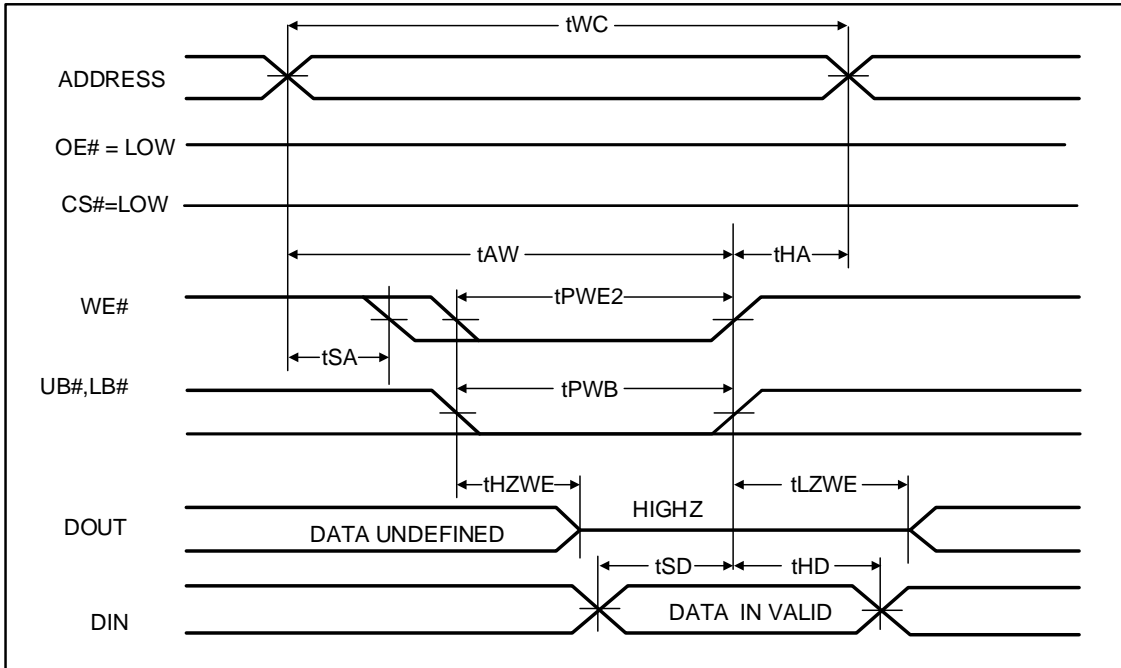
WRITE CYCLE NO. 2⁽¹⁾ (WE# CONTROLLED: OE# IS HIGH DURING WRITE CYCLE)



Note:

1. tHZOE is the time DOUT goes to High-Z after OE# goes high. During this period the I/Os are in output state. Do not apply input signals.

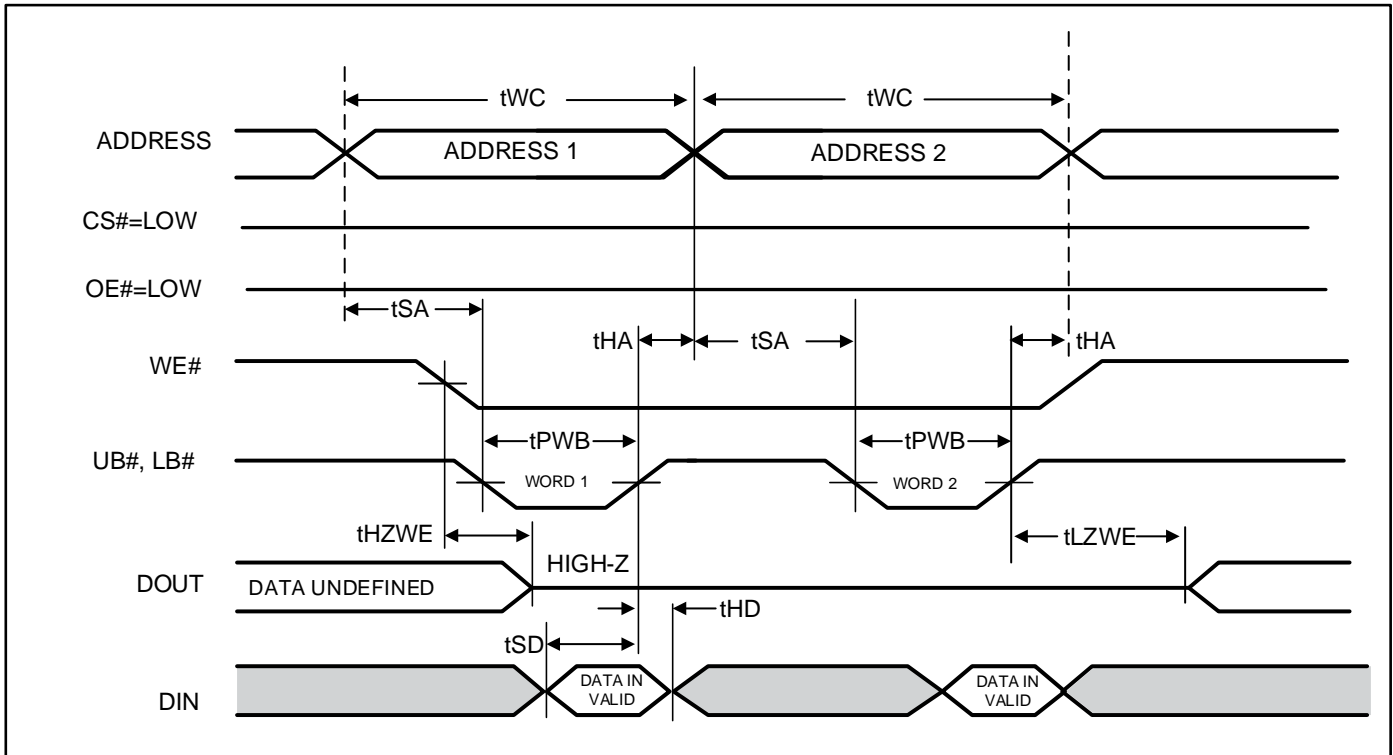
WRITE CYCLE NO. 3⁽¹⁾ (WE# CONTROLLED: OE# IS LOW DURING WRITE CYCLE)



Note:

1. I/O will assume the High-Z state if CS# = V_{IH} or OE# = V_{IH}.

WRITE CYCLE NO. 4^(1, 2, 3) (UB# & LB# Controlled, CS# = OE# = LOW)



Notes:

- 1 If OE# is low during write cycle, t_{HZWE} must be met in the application. Do not apply input signal during this period. Data output from the previous READ operation will drive IO BUS.
- 2 Due to the restriction of note1, OE# is recommended to be HIGH during write period.
- 3 WE# stays LOW in this example. If WE# toggles, t_{PWE} and t_{HZWE} must be considered.

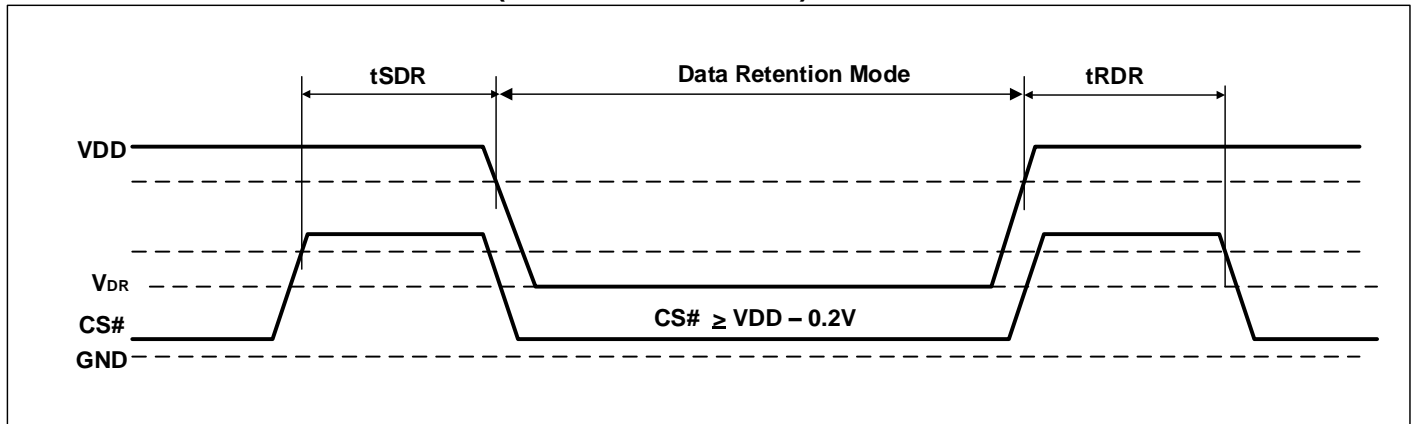
DATA RETENTION CHARACTERISTICS⁽²⁾

| Symbol | Parameter | Test Condition | OPTION | Min. | Typ. | Max. | Unit |
|------------------|------------------------------------|--|---------------------------------|-----------------|------------------|------|------|
| V _{DR} | V _{DD} for Data Retention | See Data Retention Waveform | V _{DD} = 2.4V to 3.6V | 2.0 | | - | V |
| | | | V _{DD} = 1.65V to 2.2V | 1.2 | | - | |
| I _{DR} | Data Retention Current | V _{DD} = V _{DR} (min.), CS# ≥ V _{DD} - 0.2V, VIN ≤ 0.2V or VIN ≥ V _{DD} - 0.2V | Com. | - | 3 ⁽¹⁾ | 8 | mA |
| | | | Ind. | - | - | 10 | |
| | | | Auto | - | - | 20 | |
| t _{SDR} | Data Retention Setup Time | See Data Retention Waveform | | 0 | - | - | ns |
| t _{RDR} | Recovery Time | See Data Retention Waveform | | t _{RC} | - | - | ns |

Notes:

1. Typical value indicates the value for the center of distribution, measured at V_{DD} = V_{DR} (min.), T_A = 25 °C and not 100% tested.
2. VDD power down slope must be longer than 100 us/volt when enter into Data Retention Mode.

DATA RETENTION WAVEFORM (CS# CONTROLLED)



ORDERING INFORMATION

Industrial Range: -40°C to +85°C, Voltage Range: 1.65V to 2.2V

| Speed (ns) | Order Part No. | Package |
|------------|-------------------------|---|
| 10 | IS61WV25616EFALL-10BI | mini BGA (6mm x 8mm) |
| 10 | IS61WV25616EFALL-10BLI | mini BGA (6mm x 8mm), Lead-free |
| 10 | IS61WV25616EFALL-10B2I | mini BGA (6mm x 8mm), Switched IO |
| 10 | IS61WV25616EFALL-10B2LI | mini BGA (6mm x 8mm), Switched IO, Lead-free |
| 10 | IS61WV25616EFALL-10B3I | mini BGA (6mm x 8mm), ERR1 Pin |
| 10 | IS61WV25616EFALL-10B3LI | mini BGA (6mm x 8mm), ERR1 Pin, Lead-free |
| 10 | IS61WV25616EFALL-10B4I | mini BGA (6mm x 8mm), ERR1 Pin, Switched IO |
| 10 | IS61WV25616EFALL-10B4LI | mini BGA (6mm x 8mm), ERR1 Pin, Switched IO Lead-free |
| 10 | IS61WV25616EFALL-10B5I | mini BGA (6mm x 8mm), ERR1/ERR2 Pins |
| 10 | IS61WV25616EFALL-10B5LI | mini BGA (6mm x 8mm), ERR1/ERR2 Pins, Lead-free |
| 10 | IS61WV25616EFALL-10TLI | TSOP (Type II) , Lead-free |
| 10 | IS61WV25616EFALL-10T2LI | TSOP (Type II), ERR1 Pin , Lead-free |

Industrial Range: -40°C to +85°C, Voltage Range: 2.4V to 3.6V

| Speed (ns) ⁽¹⁾ | Order Part No. | Package |
|---------------------------|-------------------------|---|
| 10 (8) | IS61WV25616EFBLL-10BI | mini BGA (6mm x 8mm) |
| 10 (8) | IS61WV25616EFBLL-10BLI | mini BGA (6mm x 8mm), Lead-free |
| 10 (8) | IS61WV25616EFBLL-10B2I | mini BGA (6mm x 8mm), Switched IO |
| 10 (8) | IS61WV25616EFBLL-10B2LI | mini BGA (6mm x 8mm), Switched IO, Lead-free |
| 10 (8) | IS61WV25616EFBLL-10B3I | mini BGA (6mm x 8mm), ERR1 Pin |
| 10 (8) | IS61WV25616EFBLL-10B3LI | mini BGA (6mm x 8mm), ERR1 Pin, Lead-free |
| 10 (8) | IS61WV25616EFBLL-10B4I | mini BGA (6mm x 8mm), ERR1 Pin, Switched IO |
| 10 (8) | IS61WV25616EFBLL-10B4LI | mini BGA (6mm x 8mm), ERR1 Pin, Switched IO Lead-free |
| 10 (8) | IS61WV25616EFBLL-10B5I | mini BGA (6mm x 8mm), ERR1/ERR2 Pins |
| 10 (8) | IS61WV25616EFBLL-10B5LI | mini BGA (6mm x 8mm), ERR1/ERR2 Pins, Lead-free |
| 10 (8) | IS61WV25616EFBLL-10TLI | TSOP (Type II) , Lead-free |
| 10 (8) | IS61WV25616EFBLL-10T2LI | TSOP (Type II), ERR1 Pin , Lead-free |

Note:

1. Speed = 8ns when VDD = 3.3V +/-10%. Speed = 10ns when VDD = 2.4V to 3.6V

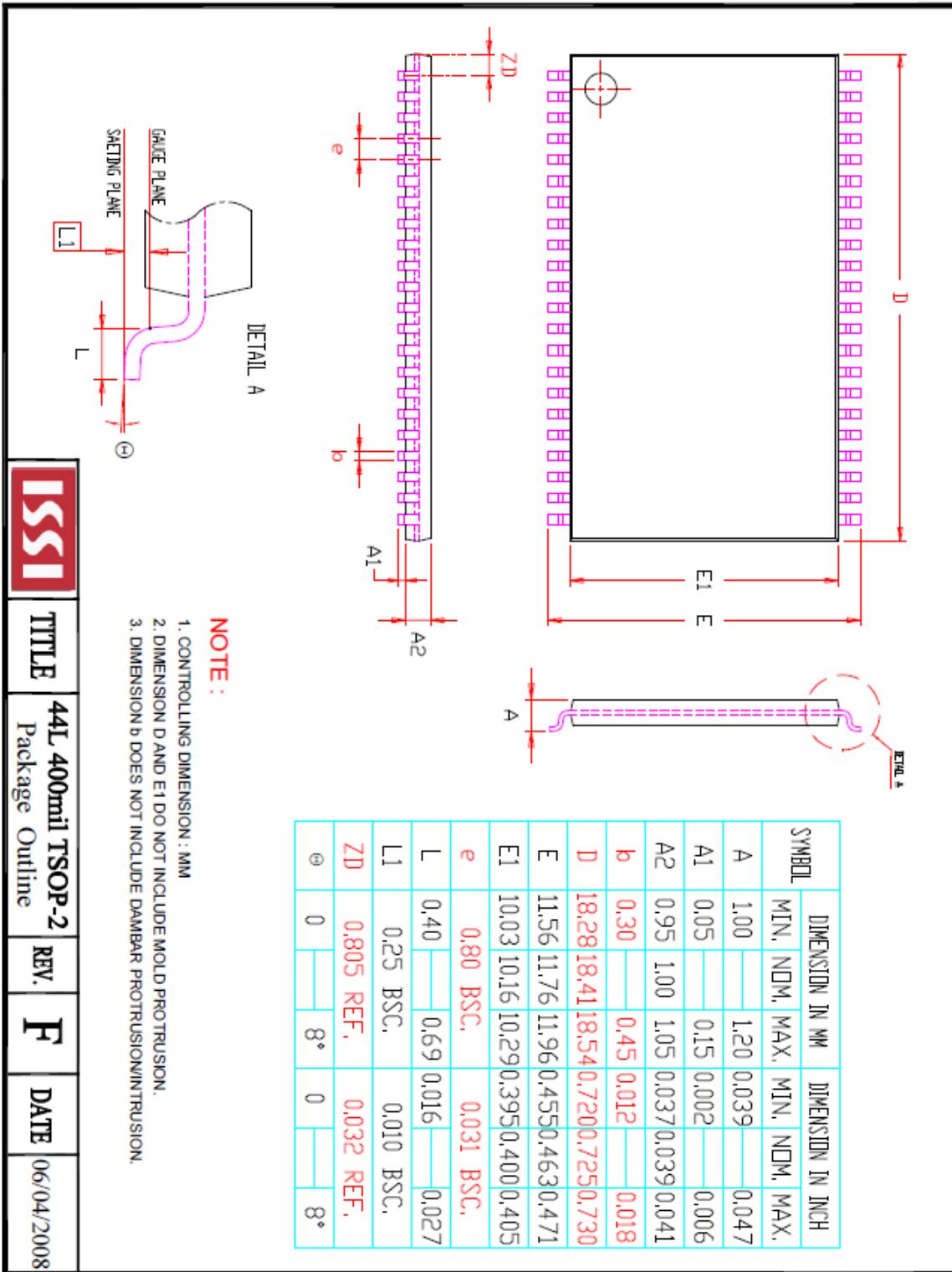
Automotive (A3) Range: -40°C to +125°C, Voltage Range: 1.65V to 2.2V

| Speed (ns) | Order Part No. | Package |
|------------|---------------------------|---|
| 12 | IS64WV25616EFALL-12BA3 | mini BGA (6mm x 8mm) |
| 12 | IS64WV25616EFALL-12BLA3 | mini BGA (6mm x 8mm), Lead-free |
| 12 | IS64WV25616EFALL-12B2A3 | mini BGA (6mm x 8mm), Switched IO |
| 12 | IS64WV25616EFALL-12B2LA3 | mini BGA (6mm x 8mm), Switched IO, Lead-free |
| 12 | IS64WV25616EFALL-12B3A3 | mini BGA (6mm x 8mm), ERR1 Pin |
| 12 | IS64WV25616EFALL-12B3LA3 | mini BGA (6mm x 8mm), ERR1 Pin, Lead-free |
| 12 | IS64WV25616EFALL-12B4A3 | mini BGA (6mm x 8mm), ERR1 Pin, Switched IO |
| 12 | IS64WV25616EFALL-12B4LA3 | mini BGA (6mm x 8mm), ERR1 Pin, Switched IO Lead-free |
| 12 | IS64WV25616EFALL-12B5A3 | mini BGA (6mm x 8mm), ERR1/ERR2 Pins |
| 12 | IS64WV25616EFALL-12B5LA3 | mini BGA (6mm x 8mm), ERR1/ERR2 Pins, Lead-free |
| 12 | IS64WV25616EFALL-12CTLA3 | TSOP (Type II) , Copper Lead-frame, Lead-free |
| 12 | IS64WV25616EFALL-12CT2LA3 | TSOP (Type II), ERR1 Pin , Copper Lead-frame ,Lead-free |

Automotive (A3) Range: -40°C to +125°C, Voltage Range: 2.4V to 3.6V

| Speed (ns) | Order Part No. | Package |
|------------|---------------------------|---|
| 10 | IS64WV25616EFBLL-10BA3 | mini BGA (6mm x 8mm) |
| 10 | IS64WV25616EFBLL-10BLA3 | mini BGA (6mm x 8mm), Lead-free |
| 10 | IS64WV25616EFBLL-10B2A3 | mini BGA (6mm x 8mm), Switched IO |
| 10 | IS64WV25616EFBLL-10B2LA3 | mini BGA (6mm x 8mm), Switched IO, Lead-free |
| 10 | IS64WV25616EFBLL-10B3A3 | mini BGA (6mm x 8mm), ERR1 Pin |
| 10 | IS64WV25616EFBLL-10B3LA3 | mini BGA (6mm x 8mm), ERR1 Pin, Lead-free |
| 10 | IS64WV25616EFBLL-10B4A3 | mini BGA (6mm x 8mm), ERR1 Pin, Switched IO |
| 10 | IS64WV25616EFBLL-10B4LA3 | mini BGA (6mm x 8mm), ERR1 Pin, Switched IO Lead-free |
| 10 | IS64WV25616EFBLL-10B5A3 | mini BGA (6mm x 8mm), ERR1/ERR2 Pins |
| 10 | IS64WV25616EFBLL-10B5LA3 | mini BGA (6mm x 8mm), ERR1/ERR2 Pins, Lead-free |
| 10 | IS64WV25616EFBLL-10CTLA3 | TSOP (Type II) , Copper Lead-frame, Lead-free |
| 10 | IS64WV25616EFBLL-10CT2LA3 | TSOP (Type II), ERR1 Pin , Copper Lead-frame ,Lead-free |

PACKAGE INFORMATION



TITLE

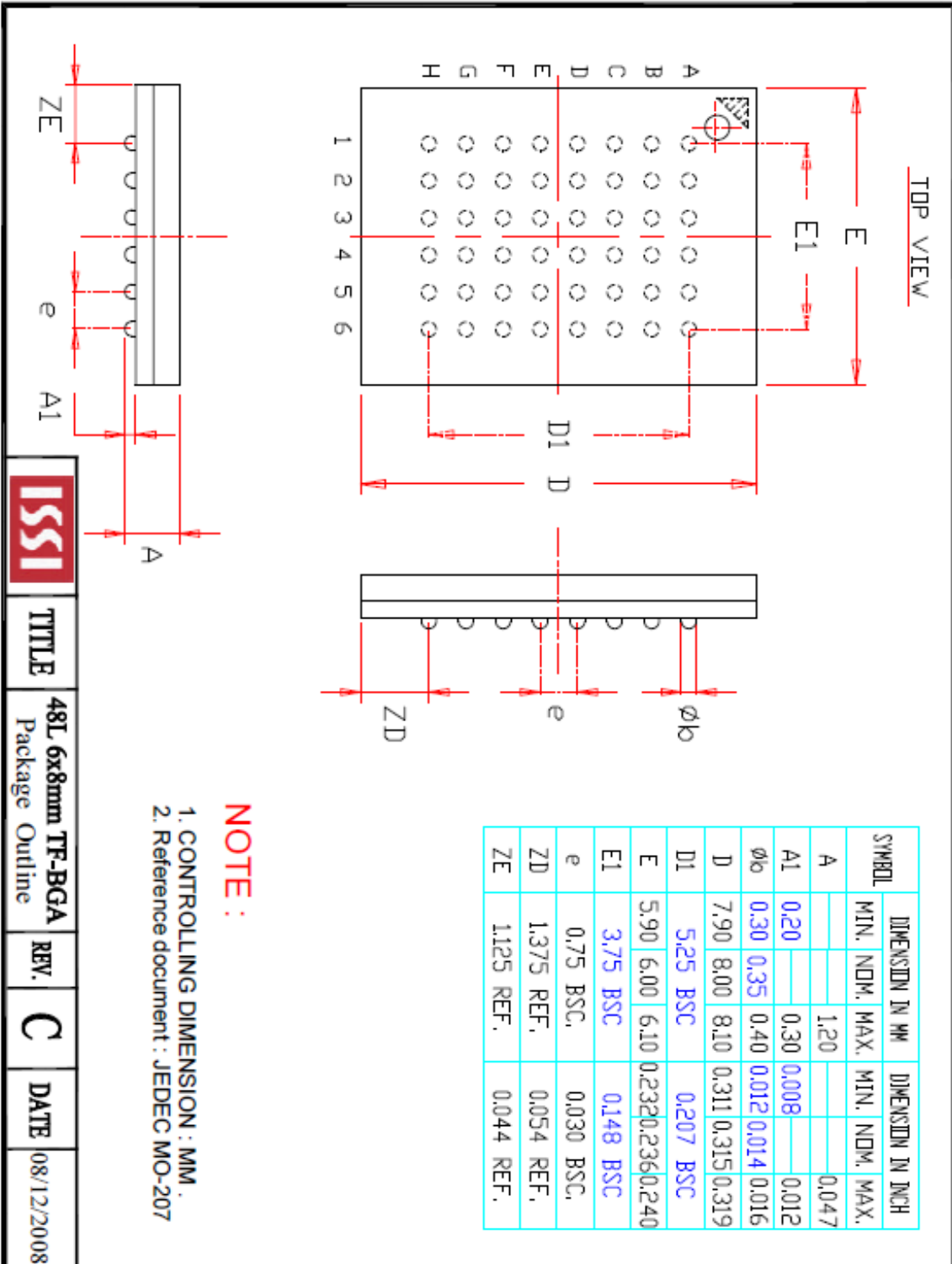
44L 400mil TSOP-2
Package Outline

REV.

F

DATE

06/04/2008



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