HV9911

Switch-Mode LED Driver IC with High Current Accuracy

Features

- Switch-mode Controller for Single-switch Drivers:
  - Buck
  - Boost
  - Buck-boost
  - SEPIC
- Works with High-side Current Sensing
- Closed-loop Control of Output Current
- High Pulse-Width Modulation (PWM) Dimming Ratio
- Internal 250V Linear Regulator (can be extended using external Zener Diodes)
- Internal 2% Voltage Reference (0°C < T_A < 85°C)
- Constant Frequency or Constant Off-time Operation
- Programmable Slope Compensation
- Logic Input for Enable and PWM Dimming
- +0.2A/-0.4A Gate Driver
- Output Short-circuit Protection
- Output Overvoltage Protection
- Synchronization Capability
- Programmable Metal-Oxide Semiconductor Field-Effect Transistor (MOSFET) Current Limit

Applications

- RGB Backlight Applications
- Battery-powered LED Lamps
- Other DC/DC LED Drivers

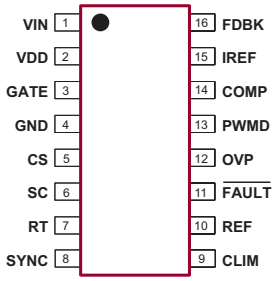
General Description

The HV9911 is an LED driver IC designed to control single-switch PWM converters (buck, boost, buck-boost and SEPIC) in a Constant Frequency or Constant Off-time mode. The controller uses a peak current control scheme with programmable slope compensation and includes an internal transconductance amplifier to control the output current in closed loop, enabling high output current accuracy. In the Constant Frequency mode, multiple HV9911s can be synchronized with each other or with an external clock using the sync pin. Programmable MOSFET current limit enables current limiting during Input Undervoltage and Output Overload conditions. The IC also includes a 0.2A source and 0.4A sink gate driver for high-power applications. An internal 9V–250V linear regulator powers the IC, eliminating the need for a separate power supply. The HV9911 provides a TTL-compatible PWM dimming input that can accept an external control signal with a duty ratio of 0%–100% and a frequency of up to a few kilohertz. The IC also provides a $\overline{\text{FAULT}}$ output which, can be used to disconnect the LEDs in case of a Fault condition, using an external disconnect FET.

The HV9911-based LED driver is ideal for RGB backlight applications with DC inputs. HV9911-based LED lamp drivers can achieve efficiency in excess of 90% for buck and boost applications.

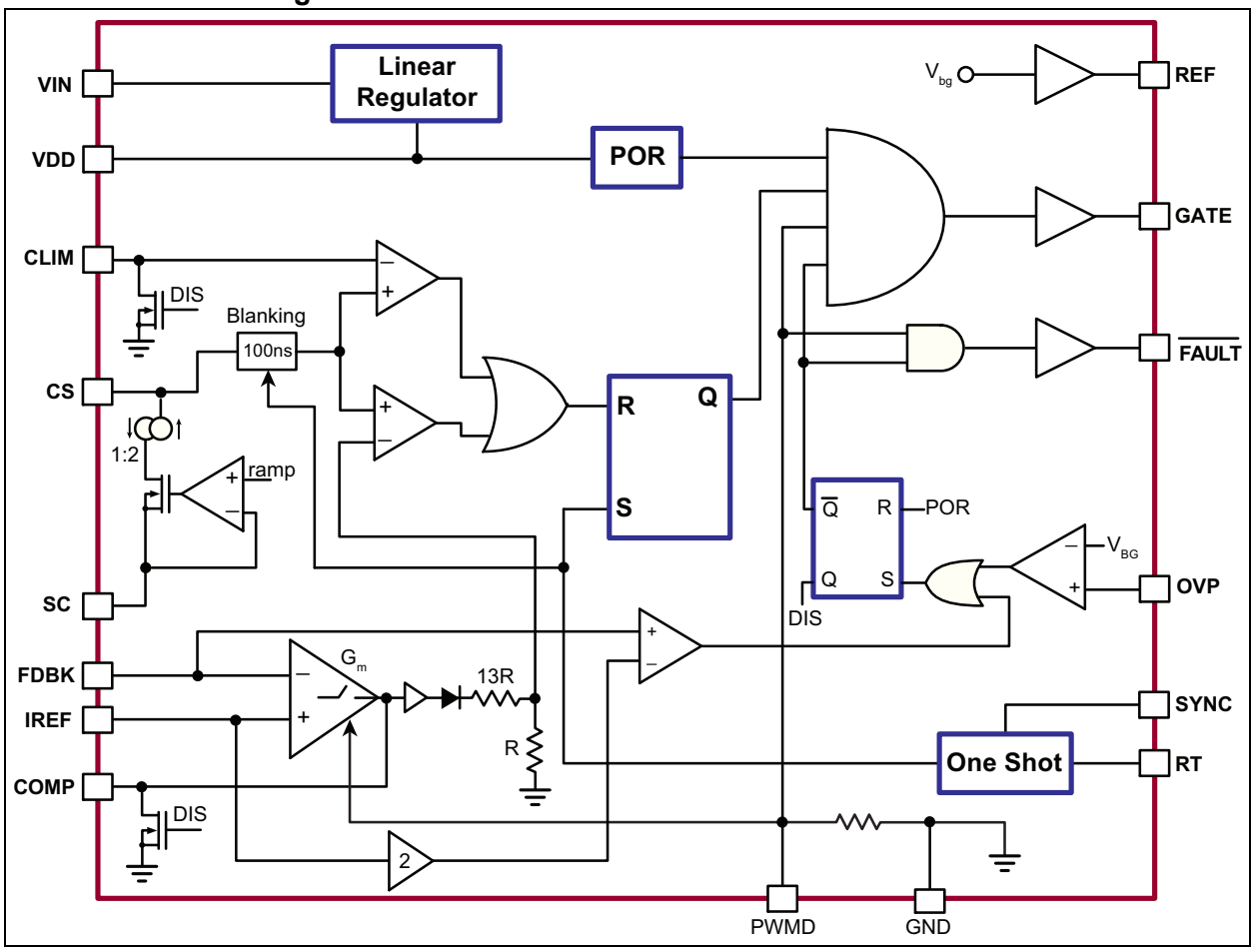
Package Type

16-lead SOIC
(Top view)

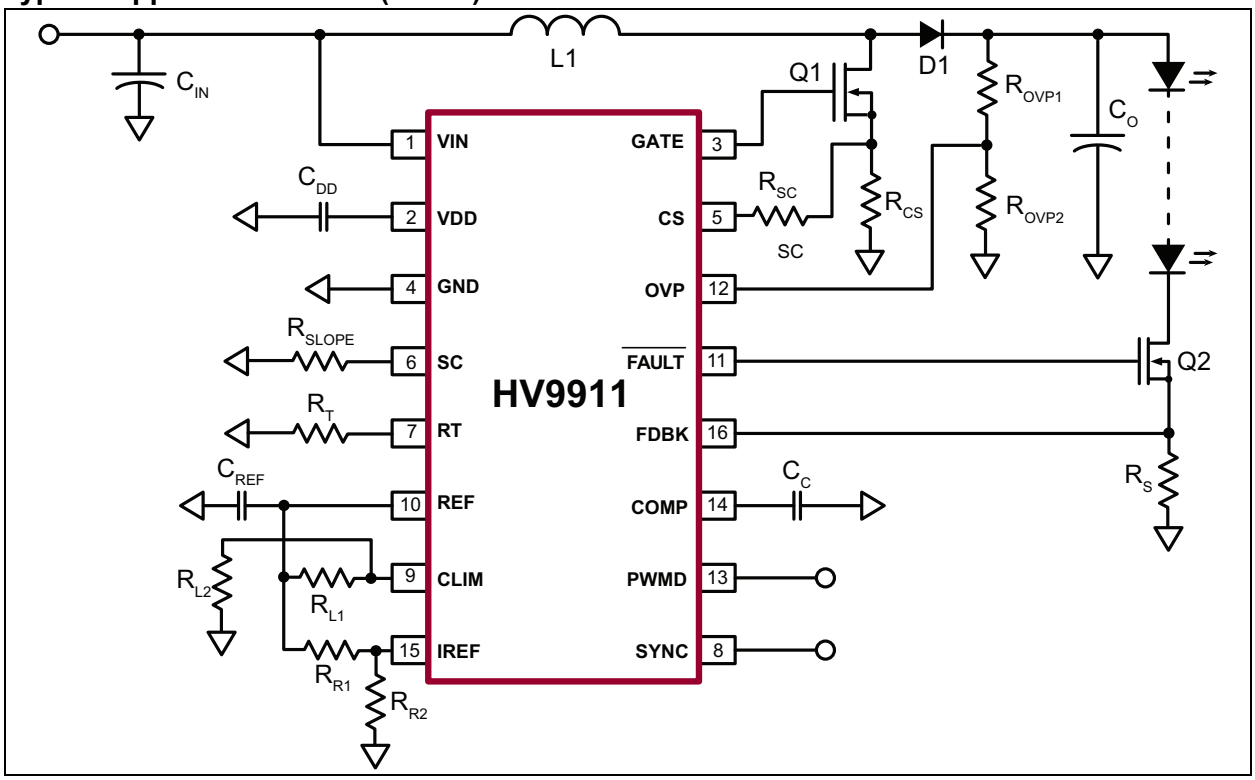


See Table 2-1 for pin information.

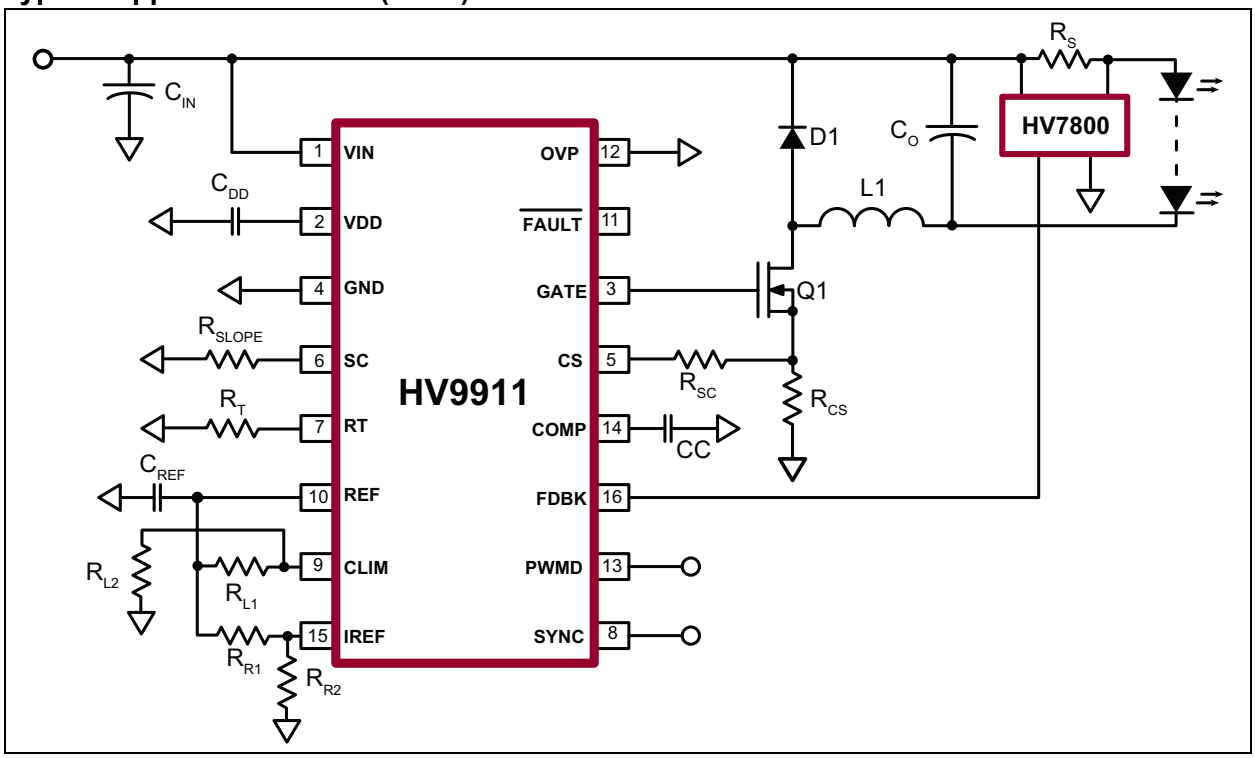
Functional Block Diagram



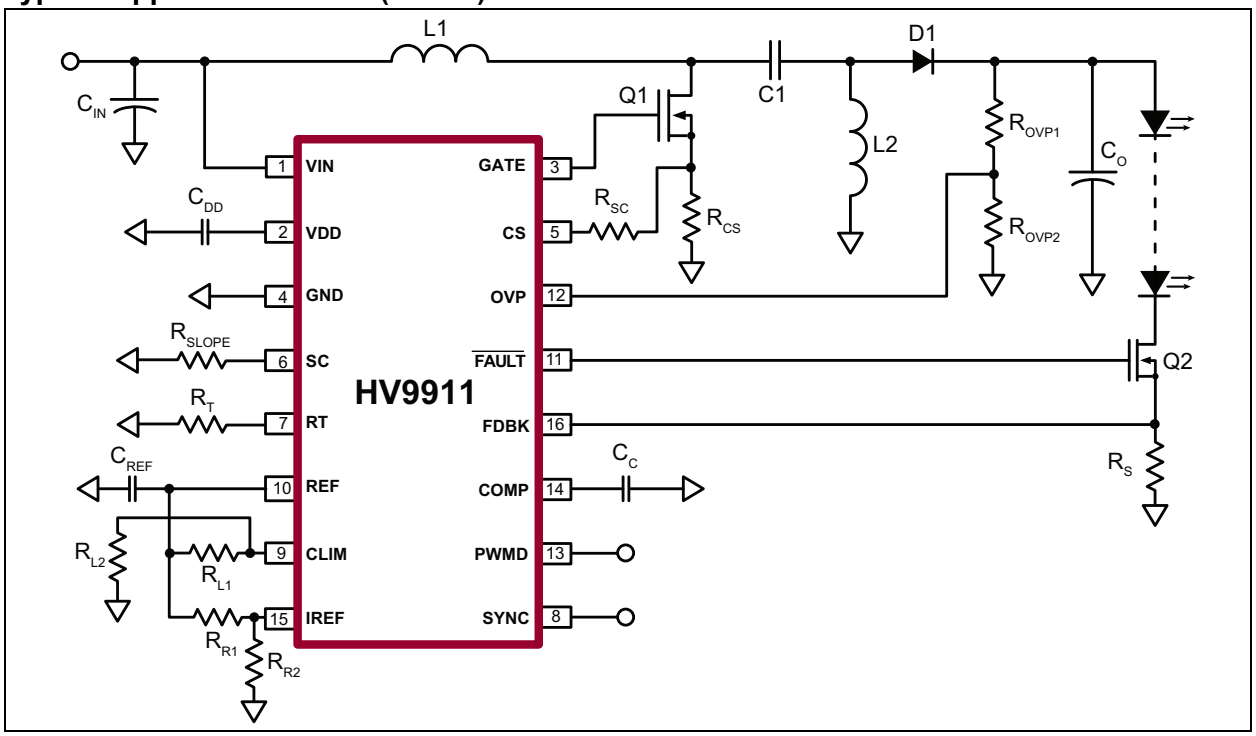
Typical Application Circuit (Boost)



Typical Application Circuit (Buck)



Typical Application Circuit (SEPIC)



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

V_{IN} to GND ..... –0.5 to +250V
V_{DD} to GND ..... –0.3V to +13.5V
CS to GND ..... –0.3V to (V_{DD}+0.3V)
PWMD to GND ..... –0.3V to (V_{DD}+0.3V)
Gate to GND ..... –0.3V to (V_{DD}+0.3V)
All Other Pins to GND ..... –0.3V to (V_{DD}+0.3V)
Continuous Power Dissipation (T_A= +25°C; Derate 10 mW/°C above +25°C) ..... 1000 mW
Operating Ambient Temperature, T_A ..... –40°C to +85°C
Maximum Junction Temperature, $T_{J(MAX)}$ ..... +125°C
Storage Temperature, T_S ..... –65°C to +150°C

† Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

Electrical Specifications: T_A = 25°C and V_{IN} = 24V unless otherwise specified.

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
INPUT						
Input DC Supply Voltage Range	V_{INDC}	**Note 2**	—	250	V	DC input voltage (**Note 1**)
Shutdown Mode Supply Current	I_{INSD}	—	1	1.5	mA	PWMD connected to GND, V_{IN} = 24V (**Note 1**)
INTERNAL REGULATOR						
Internally Regulated Voltage	V_{DD}	7.25	7.75	8.25	V	V_{IN} = 9V–250V, $I_{DD(EXT)}$ = 0, PWMD connected to GND (**Note 1**)
V_{DD} Undervoltage Lockout Threshold	UVLO	6.65	6.9	7.2	V	V_{DD} Rising
V_{DD} Undervoltage Lockout Hysteresis	ΔUVLO	—	500	—	mV	
Steady State External Voltage that can be applied at the V_{DD} Pin	$V_{DD(EXT)}$	—	—	12	V	**Note 3**
REFERENCE						
REF Pin Voltage	V_{REF}	1.225	1.25	1.275	V	REF bypassed with a 0.1 µF capacitor to GND, I_{REF} = 0, V_{DD} = 7.75V, PWMD = GND (**Note 1**)
Line Regulation of Reference Voltage	$V_{REFLINE}$	0	—	20	mV	REF bypassed with a 0.1 µF capacitor to GND, I_{REF} = 0, V_{DD} = 7.25V–12V, PWMD = GND

Note 1: Denotes specifications which apply over the full operating ambient temperature range of –40°C < T_A < +85°C

2: See **Section 3.3 "Minimum Input Voltage at VIN Pin"** for minimum input voltage.

3: Parameters might not be within specifications if the external V_{DD} voltage is greater than $V_{DD(EXT)}$ or if V_{DD} is less than 7.25V.

4: For design guidance only

ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Specifications: T_A = 25°C and V_{IN} = 24V unless otherwise specified.

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
Load Regulation of Reference Voltage	$V_{REFLOAD}$	0	—	10	mV	REF bypassed with a 0.1 µF capacitor to GND, I_{REF} = 0µ–500µ, PWMD = GND
PMW DIMMING						
PWMD Input Low Voltage	$V_{PWMD(LO)}$	—	—	0.8	V	V_{DD} = 7.25V–12V (**Note 1**)
PWMD Input High Voltage	$V_{PWMD(HI)}$	2	—	—	V	V_{DD} = 7.25V–12V (**Note 1**)
PWMD Pull-down Resistance	R_{PWMD}	50	100	150	kΩ	V_{PWMD} = 5V
GATE						
Gate Short-circuit Current	I_{SOURCE}	0.2	—	—	A	V_{GATE} = 0V, V_{DD} = 7.75V
Gate Sinking Current	I_{SINK}	0.4	—	—	A	V_{GATE} = 7.75V, V_{DD} = 7.75V
Gate Output Rise Time	T_{RISE}	—	50	85	ns	C_{GATE} = 1 nF, V_{DD} = 7.75V
Gate Output Fall Time	T_{FALL}	—	25	45	ns	C_{GATE} = 1 nF, V_{DD} = 7.75V
OVERVOLTAGE PROTECTION						
IC Shutdown Voltage	V_{OVP}	1.215	1.25	1.285	V	V_{DD} = 7.25V–12V, OVP rising (**Note 1**)
CURRENT SENSE						
Leading Edge Blanking	T_{BLANK}	100	—	375	ns	
Delay to Output of COMP Comparator	T_{DELAY1}	—	—	180	ns	COMP = V_{DD}, C_{LIM} = REF, V_{CS} = 0 mV to 600 mV (step up)
Delay to Output of C_{LIMIT} Comparator	T_{DELAY2}	—	—	180	ns	COMP = V_{DD}, C_{LIM} = 300 mV, V_{CS} = 0 mV to 400 mV (step up)
Comparator Offset Voltage	V_{OFFSET}	–10	—	10	mV	
INTERNAL TRANSCONDUCTANCE OPAMP						
Gain Bandwidth Product	GB	—	1	—	MHz	75 pF capacitance at COMP pin (**Note 4**)
Open-loop DC Gain	A_V	66	—	—	dB	Output open
Input Common Mode Range	V_{CM}	–0.3	—	3	V	**Note 4**
Output Voltage Range	V_O	0.7	—	6.75	—	V_{DD} = 7.75V (**Note 4**)
Transconductance	g_m	340	435	530	µA/V	
Input Offset Voltage	V_{OFFSET}	–2	—	4	mV	
Input Bias Current	I_{BIAS}	—	0.5	1	nA	**Note 4**
OSCILLATOR						
Oscillator Frequency	f_{OSC1}	88	100	112	kHz	R_T = 909 kΩ (**Note 1**)
	f_{OSC2}	308	350	392	kHz	R_T = 261 kΩ (**Note 1**)
Maximum Duty Cycle	D_{MAX}	—	90	—	%	
Sync Output Current	$I_{OUTSYNC}$	—	10	20	µA	
Sync Input Current	I_{INSYNC}	0	—	200	µA	V_{SYNC} < 0.1V

Note 1: Denotes specifications which apply over the full operating ambient temperature range of –40°C < T_A < +85°C

2: See **Section 3.3 "Minimum Input Voltage at VIN Pin"** for minimum input voltage.

3: Parameters might not be within specifications if the external V_{DD} voltage is greater than $V_{DD(EXT)}$ or if V_{DD} is less than 7.25V.

4: For design guidance only

ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Specifications: T_A = 25°C and V_{IN} = 24V unless otherwise specified.						
Parameter	**Sym.**	**Min.**	**Typ.**	**Max.**	**Unit**	**Conditions**
OUTPUT SHORT CIRCUIT						
Propagation Time for Short-circuit Detection	T_{OFF}	—	—	250	ns	I_{REF} = 200 mV, FDBK = 450 mV, $\overline{FAULT}$ goes from high to low
Fault Output Rise Time	$T_{RISE, FAULT}$	—	—	300	ns	1 nF capacitor at $\overline{FAULT}$ pin
Fault Output Fall Time	$T_{FALL, FAULT}$	—	—	200	ns	1 nF capacitor at $\overline{FAULT}$ pin
Amplifier Gain at I_{REF} Pin	G_{FAULT}	1.8	2	2.2	—	I_{REF} = 200 mV
SLOPE COMPENSATION						
Current sourced out of SC Pin	I_{SLOPE}	0	—	100	µA	
Internal Current Mirror Ratio	G_{SLOPE}	1.8	2	2.2	—	I_{SLOPE} = 50 µA, RC_{SENSE}= 1 kΩ

Note 1: Denotes specifications which apply over the full operating ambient temperature range of –40°C < T_A < +85°C

2: See **Section 3.3 "Minimum Input Voltage at VIN Pin"** for minimum input voltage.

3: Parameters might not be within specifications if the external V_{DD} voltage is greater than $V_{DD(EXT)}$ or if V_{DD} is less than 7.25V.

4: For design guidance only

TEMPERATURE SPECIFICATIONS

Temperature Characteristics: Unless otherwise noted, for all specifications T_A =T_J = +25°C.						
Parameter	**Sym.**	**Min.**	**Typ.**	**Max.**	**Unit**	**Conditions**
TEMPERATURE RANGE						
Operating Ambient Temperature	T_A	–40	—	+85	°C	
Maximum Junction Temperature	$T_{J(MAX)}$	—	—	+125	°C	
Storage Temperature	Ts	–65	—	+150	°C	
PACKAGE THERMAL RESISTANCE						
16-lead SOIC	θ_{JA}	—	83	—	°C/W	

2.0 PIN DESCRIPTION

Table 2-1 shows the description of pins in HV9911.
Refer to **Package Type** for the location of pins.

TABLE 2-1: PIN DESCRIPTION TABLE

Pin Number	Pin Name	Description
1	VIN	This pin is the input of a 250V high-voltage regulator.
2	VDD	This is a power supply pin for all internal circuits. It must be bypassed with a low ESR capacitor to GND (at least 0.1 uF).
3	Gate	This pin is the output gate driver for an external N-channel power MOSFET.
4	GND	This is the ground return for all circuits. This pin must be connected to the return path from the input.
5	CS	This pin is used to sense the drain current of the external power FET. It includes a built-in 100 ns (minimum) blanking time.
6	SC	This is slope compensation for current sense. A resistor between SC and GND will program the slope compensation. In case of constant Off-time mode of operation, slope compensation is unnecessary and the pin can be left open.
7	RT	This pin sets the frequency or the off-time of the power circuit. A resistor between RT and GND will program the circuit in Constant Frequency mode. A resistor between RT and gate will program the circuit in a constant Off-time mode.
8	Sync	This I/O pin may be connected to the sync pin of other HV9911 circuits and will cause the oscillators to lock to the highest frequency oscillator.
9	CLIM	This pin provides a programmable input current limit for the converter. The current limit can be set by using a resistor divider from the REF pin.
10	REF	This pin provides 2% accurate reference voltage. It must be bypassed with at least a 10 nF–0.22 µF capacitor to GND.
11	$\overline{\text{FAULT}}$	This pin is pulled to ground when there is an Output Short-circuit condition or Output Overvoltage condition. This pin can be used to drive an external MOSFET in the case of boost converters to disconnect the load from the source.
12	OVP	This pin provides the overvoltage protection for the converter. When the voltage at this pin exceeds 1.25V, the gate output of the HV9911 is turned off and $\overline{\text{FAULT}}$ goes low. The IC will turn on when the power is recycled.
13	PWMD	When this pin is pulled to GND (or left open), switching of the HV9911 is disabled. When an external TTL high level is applied to it, switching will resume.
14	COMP	Stable closed-loop control can be accomplished by connecting a compensation network between COMP and GND.
15	IREF	The voltage at this pin sets the output current level. The current reference can be set using a resistor divider from the REF pin.
16	FDBK	This pin provides output current feedback to the HV9911 by using a current sense resistor.

3.0 DETAILED DESCRIPTION

3.1 Power Topology

The built-in linear regulator of the HV9911 can operate up to 250V at the V_{IN} pin. The linear regulator provides an internally regulated voltage of 7.75V (typical) at V_{DD} if the input voltage is within 9V to 250V. This voltage is used to power the IC and also provide the power to external circuits connected at the V_{DD} and V_{REF} pins. This linear regulator can be turned off by overdriving the V_{DD} pin using an external bootstrap circuit at voltages higher than 8.25V (up to 12V).

In practice, the input voltage range of the IC is limited by the current drawn by the IC. Thus, it becomes important to determine the current drawn by the IC to find out the maximum and minimum operating voltages at the V_{IN} pin. The main component of the current drawn by the IC is the current drawn by the switching FET driver at the gate pin. To estimate this current, we need to know a few parameters of the FET being used in the design and the switching frequency.

The typical waveform of the current being sourced out of gate is illustrated in Figure 3-1. Figure 3-2 shows the equivalent circuit of the gate driver and the external FET. The values of V_{DD} and R_{GATE} for the HV9911 are 7.75V and 40Ω, respectively.

Note: The equations given below are approximations and are to be used for estimation purposes only. The actual values will likely differ from the computed values.

Consider the case when the external FET is FDS3692 and the switching frequency is f_S = 200 kHz with an LED string voltage V_O = 80V. With the FET's specifications, the following parameters can be determined:

$$C_{ISS} = 746pF$$
$$C_{GD} = C_{RSS} = 27pF$$
$$C_{GS} = C_{ISS} - C_{GD} = 719pF$$
$$V_{TH} = 3V$$

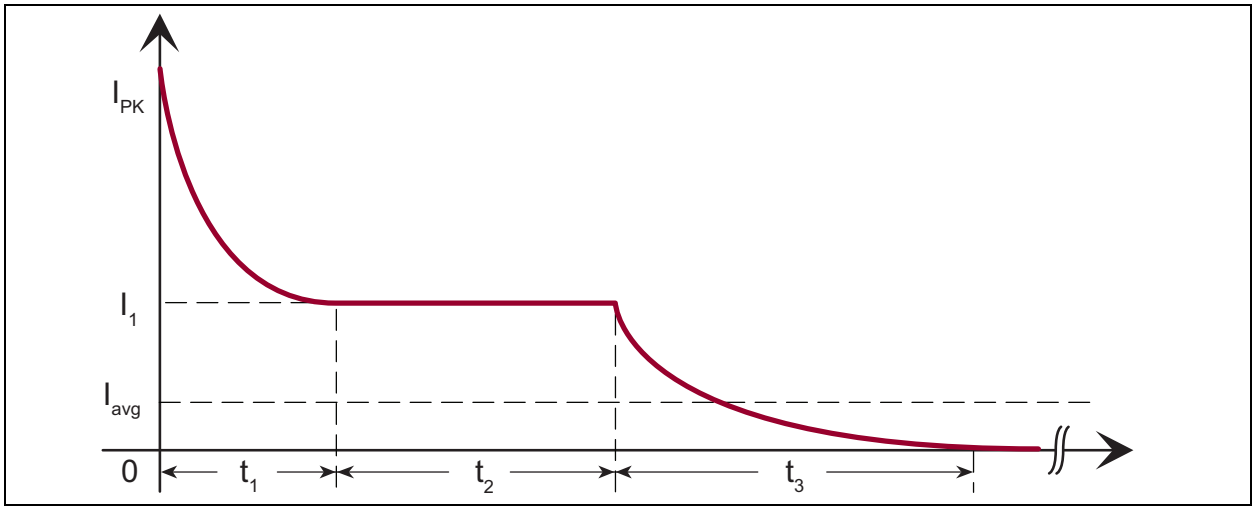


FIGURE 3-1: *Current Sourced Out of Gate at FET Turn-on Driver.*

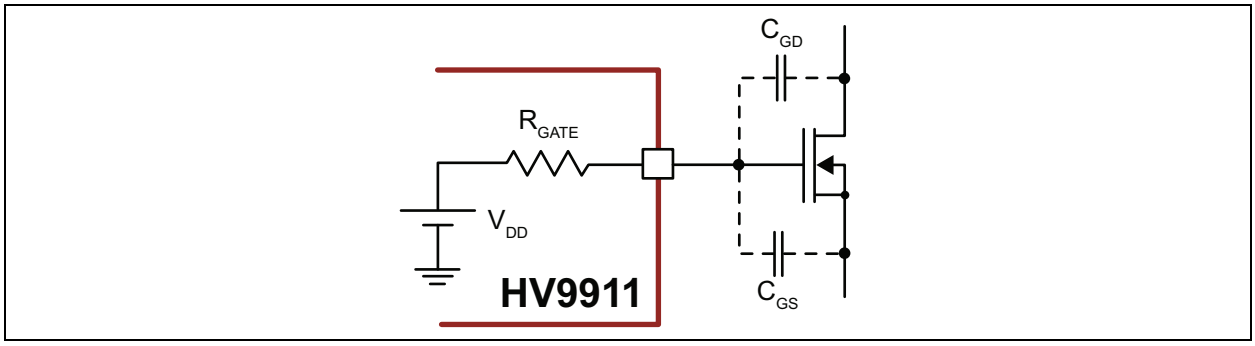


FIGURE 3-2: *Equivalent Circuit of the Gate Driver.*

When the external FET is being turned on, current is being sourced out of the gate, and that current is being drawn from the input. Thus, the average current drawn from V_{DD} (and from V_{IN}) needs to be computed. Without going into the details of the FET operation, the various values in the graph in Figure 3-1 can be computed as specified in Table 3-1.

TABLE 3-1:

Parameter	Formula	Value (for a given example)
I_{PK}	V_{DD}/R_{GATE}	193.75 mA
I_1	$(V_{DD} - V_{TH})/R_{GATE}$	118.75 mA
t_1	$-R_{GATE}$ x C_{ISS} x ln (I_1/I_{PK})	14.61 ns
t_2	$[(V_O - V_{TH})$ x $C_{GD}]/I_1$ (**1**)	17.5 ns
	$[(V_{IN} - V_{TH})$ x $_{GD}]/I_1$ (**2**)	
t_3	2.3 x R_{GATE} x C_{GS}	66 ns
I_{avg}	$[I_1$ x $(t_1 + t_2)$ + 0.5 x $(I_{PK} - I_1)$ x t_1 + 0.5 x I_1 x $t_3]$ x f_S	1.66 mA

Note 1: For a boost converter

2: For a buck converter

The total current being drawn from the linear regulator for a typical HV9911 circuit can be computed as shown in Table 3-2.

TABLE 3-2:

Current	Formula	Typical Value (**2**)
Quiescent Current	1000 µA	1000 µA
Current sourced out of REF pin	$(V_{REF}/R_{L1} + R_{L2}) + (V_{REF}/R_{R1} + R_{R2})$	100 µA
Current sourced out of RT pin	$6V/R_T$	13.25 µA
Current sourced out of SC pin (**1**)	$(1/2)$ x $(2.5V/R_{SLOPE})$	30.8 µA
Current sourced out of CS pin (**1**)	$2.5V/R_{SLOPE}$	61.6 µA
Current drawn by FET Gate Driver	I_{AVG}	1660 µA
Total Current drawn from the Linear Regulator		**2.865 mA**

Note 1: For a Discontinuous mode converter, the currents sourced out of the SC and CS pins will be zero.

2: The values provided are based on the Continuous Conduction mode boost design in the Microchip application note, "*AN-H55 Boost Converter LED Drivers Using the HV9911.*"

3.2 Maximum Input Voltage at V_{IN} Pin Computed using the Power Dissipation Limit

When the regulator is drawing about 2.8 mA, the maximum input voltage that the HV9911 can withstand without damage will depend on the ambient temperature. If we consider an ambient temperature of 40°C, the power dissipation in the package cannot exceed the P_{MAX} in Equation 3-1:

EQUATION 3-1:

$$\begin{aligned} P_{MAX} &= 1000mW - 10mW \times (40°C - 25°C) \\ &= 850mW \end{aligned}$$

The above equation is based on package power dissipation limits as indicated in the **Absolute Maximum Ratings †** of this data sheet.

To dissipate a maximum power of 850 mW in the package, the maximum input voltage cannot exceed the value in Equation 3-2:

EQUATION 3-2:

$$\begin{aligned} V_{INMAX} &= P_{MAX}/I_{TOTAL} \\ &= 296V \end{aligned}$$

Since the maximum voltage is far greater than the actual input voltage of 24V, power dissipation will not be a problem for this design.

For this design, at 24V input, the increase in the junction temperature of the IC (over ambient) is determined as show in Equation 3-3:

EQUATION 3-3:

$$\begin{aligned} \Delta\theta &= V_{IN} \times I_{TOTAL} \times \theta_{ja} \\ &= 5.64°C \end{aligned}$$

Where:

θ_{ja} is the junction to ambient thermal impedance of HV9911's 16-lead SOIC package.

3.3 Minimum Input Voltage at V_{IN} Pin

The minimum input voltage at which the converter will start and stop depends on the minimum voltage drop required for the linear regulator. The internal linear regulator will control the voltage at the V_{DD} pin when V_{IN} is between 9V and 250V. However, when V_{IN} is less than 9V, the converter will still function as long as V_{DD} is greater than the undervoltage lockout. Thus, the converter might be able to start at input voltages lower than 9V. The start/stop voltages at the V_{IN} pin can be determined using the minimum voltage drop across the linear regulator as a function of the current drawn. This data is shown in Figure 3-3 for different junction temperatures.

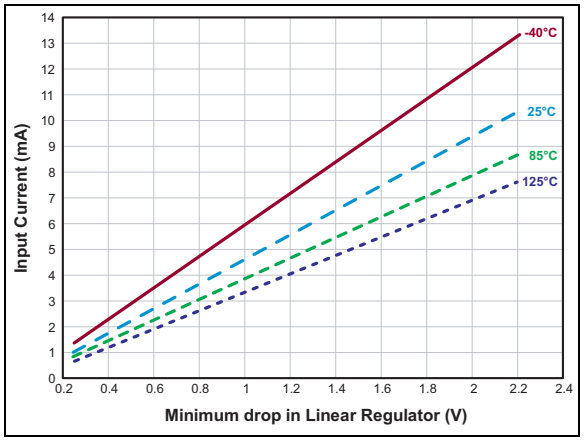


FIGURE 3-3: *Graph of the Input Current vs. Minimum Voltage Drop Across Linear Regulator for Different Junction Temperatures.*

Assume a maximum junction temperature of 85°C (this gives a reasonable temperature rise of 45°C at an ambient temperature of 40°C). At 2.86 mA input current, the minimum voltage drop from Figure 3-3 can be approximately estimated to be V_{DROP} = 0.75V. However, before the IC starts switching, the current drawn will be the total current minus the gate drive current. In this case, that current is I_{Q_TOTAL} = 1.2 mA. At this current level, the voltage drop is approximately V_{DROP1} = 0.4V. Thus, the start/stop V_{IN} voltages can be computed as demonstrated in Equation 3-4 and Equation 3-5 below.

EQUATION 3-4:

$$\begin{aligned} V_{IN(START)} &= UVLO_{MAX} + V_{DROP1} \\ &= 7.2V + 0.4V \\ &= 7.60V \end{aligned}$$

EQUATION 3-5:

$$\begin{aligned} V_{IN(STOP)} &= UVLO_{MAX} - 0.5V + V_{DROP} \\ &= 7.2V - 0.5V + 0.75V \\ &= 7.45V \end{aligned}$$

Note: In some cases, if the gate drive draws too much current, $V_{IN(START)}$ might be less than $V_{IN(STOP)}$. In such cases, the control IC will oscillate between on and off if the input voltage is between the start and stop voltages. In these circumstances, it is recommended that the input voltage be kept higher than $V_{IN(STOP)}$.

3.4 Reference

The HV9911 includes a 2% accurate 1.25V reference, which can be used as the reference for the output current as well as to set the switch current limit. This reference is also used internally to set the overvoltage protection threshold. The reference is buffered so that it can deliver a maximum of 500 µA external current to drive the external circuitry. The reference should be bypassed with at least a 10 nF low ESR capacitor.

Note: To avoid abnormal startup conditions, the bypass capacitor at the REF pin should not exceed 0.22 µF.

3.5 Oscillator

The oscillator can be set in two ways. Connecting the oscillator resistor between the R_T and gate pins will program the off-time. Connecting the resistor between R_T and GND will program the time period.

In both cases, resistor R_T sets the current, which charges an internal oscillator capacitor. The capacitor voltage ramps up linearly and when the voltage increases beyond the internal set voltage, a comparator triggers the set input of the internal SR flip-flop. This starts the next switching cycle. The time period of the oscillator can be computed as shown in Equation 3-6.

EQUATION 3-6:

$$T_S \approx R_T \times 11pF$$

3.6 Slope Compensation

For converters operating in the Constant Frequency mode, slope compensation becomes necessary to ensure stability of the Peak Current mode controller, if the operating duty cycle is greater than 50%. Choosing a slope compensation which is one half of the down slope of the inductor current ensures that the converter will be stable for all duty cycles.

Slope compensation can be programmed by two resistors R_{SLOPE} and R_{SC}. Assuming a down slope of DS (A/µs) for the inductor current, the slope compensation resistors can be computed as illustrated in Equation 3-7.

EQUATION 3-7:

$$R_{SLOPE} = (10 \times R_{SC})/(DS \times 10^6 \times T_S \times R_{CS})$$

A typical value for R_{SC} is 499Ω.

Note: The maximum current that can be sourced out of the SC pin is 100 µA. This limits the minimum value of the R_{SLOPE} resistor to 25 kΩ. If the equation for slope compensation produces a value of R_{SLOPE} less than this value, then R_{SC} would have to be increased accordingly. It is recommended that R_{SLOPE} be chosen within the range of 25 kΩ–50 kΩ.

3.7 Current Sense

The current sense input of the HV9911 includes a built-in 100 ns (minimum) blanking time to prevent spurious turn off due to the initial current spike when the FET turns on.

The HV9911 includes two high-speed comparators—one is used during normal operation and the other is used to limit the maximum input current during Input Undervoltage or Overload conditions.

The IC includes an internal resistor divider network, which steps down the voltage at the COMP pin by a factor of 15. This stepped-down voltage is given to one of the comparators as the current reference. The reference to the other comparator, which acts to limit the maximum inductor current, is given externally.

It is recommended that the sense resistor R_{CS} be chosen so as to provide about 250 mV current sense signal.

3.8 Current Limit

Current limit has to be set by a resistor divider from the 1.25V reference available on the IC. Assuming a maximum operating inductor current I_{pk} (including the ripple current), the voltage at the CLIM pin can be set as shown in Equation 3-8.

EQUATION 3-8:

$$V_{CLIM} \geq 1.2 \times I_{PK} \times R_{CS} + (5 \times R_{SC}/R_{SLOPE}) \times 0.9$$

Note that this equation assumes a current limit at 120% of the maximum input current. Also, if V_{CLIM} is greater than 450 mV, the saturation of the internal opamp will determine the limit on the input current rather than the CLIM pin. In such a case, the sense resistor R_{CS} should be reduced until V_{CLIM} reduces below 450 mV.

It is recommended that no capacitor be connected between CLIM and GND.

3.9 Fault Protection

The HV9911 has a built-in output overvoltage protection and output short-circuit protection. Both protection features are latched, which means that the power to the IC must be recycled to reset the IC. The IC also includes a $\overline{\text{FAULT}}$ pin which goes low during any Fault condition. At startup, a monoshot circuit (triggered by the POR circuit) resets an internal flip-flop which causes $\overline{\text{FAULT}}$ to go high and remains high during normal operation. This also allows the gate drive to function normally. This pin can be used to drive an external disconnect switch (Q2 in the **Typical Application Circuit (Boost)**) which will disconnect the load during a Fault condition. This disconnect switch is very important in a boost converter, as turning off the switching FET (Q1) during an Output Short-circuit condition will not remove the fault (Q1 is not in the path of the fault current). The disconnect switch will help to disconnect the shorted load from the input.

3.10 Overvoltage Protection

Overvoltage protection is achieved by connecting the output voltage to the OVP pin through a resistive divider. The voltage at the OVP pin is constantly compared to the internal 1.25V. When the voltage at this pin exceeds 1.25V, the IC is turned off and $\overline{\text{FAULT}}$ goes low.

3.11 Output Short-circuit Protection

The output short circuit condition is indicated by $\overline{\text{FAULT}}$. As mentioned earlier, at startup, a monoshot circuit (triggered by the POR circuit) resets an internal flip-flop, which causes $\overline{\text{FAULT}}$ to go high and remains high during normal operation. This also makes the gate drive function normally.

The steady state current is reflected in the reference voltage connected to the transconductance amplifier. The instantaneous output current is sensed from the FDBK terminal of the amplifier. The short circuit threshold current is internally set to 200% of the steady-state current.

During Short-circuit condition, when the current exceeds the internally set threshold, the SR flip-flop is set and $\overline{\text{FAULT}}$ goes low. At the same time, the gate driver of the power FET is inhibited, providing a latching protection. The system can be reset by cycling the input voltage to the IC.

Note: The short circuit FET should be connected before the current sense resistor as reversing R_S and Q_2 will affect the accuracy of the output current (due to the additional voltage drop across Q_2 which will be sensed).

3.12 Synchronization

The sync pin is an input/output (I/O) port to a fault tolerant peer-to-peer and/or master clock synchronization circuit. For synchronization, the sync pins of multiple HV9911-based converters can be connected together and may also be connected to the open drain output of a master clock. When connected in this manner, the oscillators will lock to the device with the highest operating frequency. When synchronizing multiple ICs, it is recommended that the same timing resistor corresponding to the switching frequency be used in all the HV9911 circuits.

Due to the length of the connecting lines for the sync pins, a resistor between sync and GND may be required to damp any ringing due to parasitic capacitances on rare occasions. It is recommended that the resistor chosen be greater than 300 kΩ.

When synchronized in this manner, a permanent High or Low condition on the sync pin will result in a loss of synchronization, but the HV9911-based converters will continue to operate at their individually set operating frequencies. Since loss of synchronization will not result in a total system failure, the sync pin is considered fault tolerant.

Note:	The HV9911 is designed to sync up to four ICs at a time without the use of an external buffer. To sync more than four ICs, it is recommended that a buffered external clock be used.

3.13 Internal 1 MHz Transconductance Amplifier

The HV9911 includes a built-in 1 MHz transconductance amplifier with tri-state output, which can be used to close the feedback loop. The output current sense signal is connected to the FDBK pin and the current reference is connected to the I_{REF} pin.

The output of the opamp is controlled by the signal applied to the PWMD pin. When PWMD is high, the output of the opamp is connected to the COMP pin. When PWMD is low, the output is left open. This enables the integrating capacitor to hold the charge when the PWMD signal has turned off the gate drive. When the IC is enabled, the voltage on the integrating capacitor will force the converter into Steady state almost instantaneously.

The output of the opamp is buffered and connected to the current sense comparator using a 15:1 divider. The buffer helps prevent the integrator capacitor from discharging during the PWM Dimming state.

3.14 Linear Dimming

Linear dimming can be achieved by varying the voltage at the I_{REF} pin, as the output current is proportional to the voltage at the I_{REF} pin. This can be done either by using a potentiometer from the I_{REF} pin or applying an external voltage source to the I_{REF} pin.

Note:	Due to the offset voltage of the transconductance opamp, pulling the I_{REF} pin very close to GND will cause the internal short circuit comparator to trigger and shut down the IC. This limits the linear dimming range of the IC. However, a 1:10 linear dimming range can be easily obtained. It is recommended that the PWMD pin be used to get zero output current rather than pull the I_{REF} pin to GND.

3.15 PWM Dimming

PWM dimming can be achieved by driving the PWMD pin with a TTL-compatible source. The PWM signal is connected internally to three different nodes—the transconductance amplifier, the $\overline{\text{FAULT}}$ output and the gate output.

When the PWMD signal is high, the gate and $\overline{\text{FAULT}}$ pins are enabled, and the transconductance opamp's output is connected to the external compensation network. Thus, the internal amplifier controls the output current. When the PWMD signal goes low, the output of the transconductance amplifier is disconnected from the compensation network. Therefore the integrating capacitor maintains the voltage across it. The gate is disabled, so the converter stops switching and the $\overline{\text{FAULT}}$ pin goes low, turning off the disconnect switch.

The output capacitor of the converter determines the converter's PWM dimming response because the capacitor has to get charged and discharged whenever the PWMD signal goes high or low. In the case of a buck converter, since the inductor current is continuous, a very small capacitor is used across the LEDs. This minimizes the effect of the capacitor on the PWM dimming response of the converter. However, in the case of a boost converter, the output current is discontinuous, and a very large output capacitor is required to reduce the ripple in the LED current. Thus, this capacitor will have a significant impact on the PWM dimming response. By turning off the disconnect switch when PWMD goes low, the output capacitor is prevented from being discharged. This dramatically improves the boost converter's PWM dimming response.

Note: Disconnecting the capacitor might cause a sudden spike in the capacitor voltage as the energy in the inductor is dumped into the capacitor. This might trigger the OVP comparator if the OVP point is set too close to the maximum operating voltage. Thus, either the capacitor has to be sized slightly larger or the OVP set point has to be increased.

Note: Pulling the PWMD pin 0.3V below the GND may cause latch-up conditions on the HV911 IC. This abnormal condition can happen if there is a long cable between the PWM signal and the PWMD pin of the IC. It is recommended that a 1 kΩ resistor be connected between the PWMD pin and the PWM signal input to the HV9911. This resistor, when placed close to the IC, will damp out any ringing that might cause the voltage at the PWMD pin to go below GND.

3.16 Avoiding False Shutdowns of the HV9911

The HV9911 has two fault modes which trigger a latched Protection mode—an Overcurrent (or Short-circuit) Protection and an Overvoltage Protection.

To prevent false triggering due to the tripping of the overvoltage comparator resulting from noise in the GND traces on the PCB, it is recommended that a 1 nF–10 nF capacitor be connected between the OVP pin and GND. Although this capacitor slightly slows down the response of the Overvoltage Protection circuitry, it does not affect the overall performance of the converter as the large output capacitance in the boost design will limit the rate of output voltage increase.

In some cases, the Overcurrent Protection may be triggered during PWM dimming, when the $\overline{\text{FAULT}}$ goes high and the disconnect switch is turned on. This triggering of the Overcurrent Protection is related to the parasitic capacitance of the LED string (shown as a lumped capacitance C_{LED} in Figure 3-4).

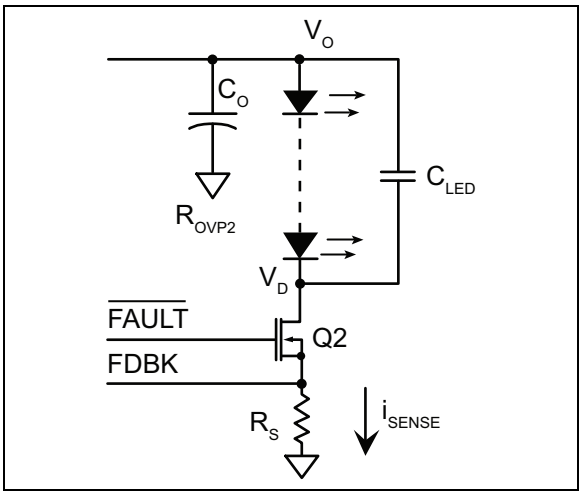


FIGURE 3-4: *Output of the Boost Converter Showing LED Parsed Capacitance.*

During normal PWM dimming operation, the HV9911 maintains the voltage across the output capacitor (C_O) by turning off the disconnect switch and preserving the charge in the output capacitance when the PWM dimming signal is low. At the same time, the voltage at the drain of the disconnect FET is some non-zero value V_D. When the PWM dimming signal goes high, FET Q_2 is turned on. This causes the voltage at the drain of the FET (V_D) to instantly become zero. Assuming a constant output voltage V_O, i_{sense} can be computed as shown in Equation 3-9.

EQUATION 3-9:

$$\begin{aligned} i_{SENSE} &= C_{LED} \times d \times (V_O - V_D)/dt \\ &= -C_{LED} \times dV_D/dt \end{aligned}$$

In this case, the rate of fall of the disconnect FET's drain voltage is a large value (since the FET turns on very quickly) and this causes a spike of current through the sense resistor, which could trigger the overcurrent protection (depending on the parasitic capacitance of the LED string).

To prevent this condition, a simple RC low-pass filter network can be added as shown in Figure 3-5. Typical values are R_F = 1 kΩ and C_F = 470 pF. This filter will block the FDBK pin from seeing the turn-on spike and normalize the PWM dimming operation of the HV9911 boost converter. This will have a minimal effect on the stability of the loop but will increase the response time to an output short. If the increase in the response time is large, it might damage the output current sense resistor due to exceeding its peak-current rating.

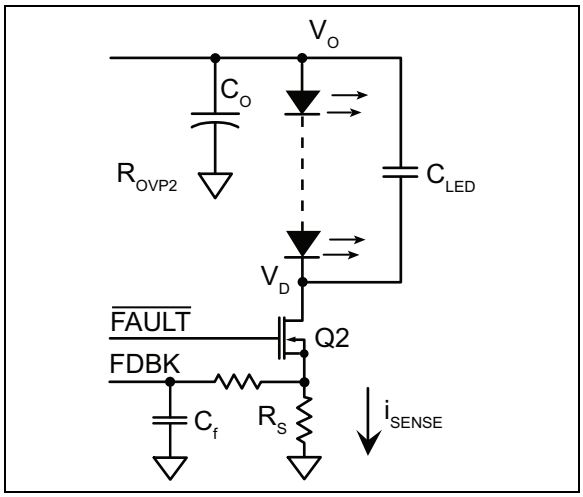


FIGURE 3-5: *Adding a Low-pass Filter to Prevent Pulse Triggering.*

The increase in the short-circuit response time can be computed using the various component values of the boost converter. Consider a boost converter with a nominal output current I_O = 350 mA, an output sense resistor R_S = 1.24Ω, LED string voltage V_O = 100V and an output capacitor C_O = 2 mF. The disconnect FET is a TN2510N8 which has a saturation current I_{SAT} = 3A (at V_{GS} = 6V). See *"TN2510N8 N-Channel Enhancement-Mode Vertical DMOS FET."* The increase in the short-circuit response time due to the RC filter can then be computed as shown in Equation 3-10:

EQUATION 3-10:

$$\Delta t \approx R_F \times C_F \times \left| In\left(1 - \frac{I_O}{I_{SAT} - I_O}\right)\right|$$
$$= 1k\Omega \times 470pF \times \left| In\left(1 - \frac{0.35A}{3A - 0.35A}\right)\right|$$
$$\approx 66ns$$

This increase is found to be negligible (note that the equation is valid for ΔT << R_S x C_O). In this case, R_S x C_O = 2.48 µs, and the condition holds.

3.17 Sizing the Output Sense Resistor

To avoid exceeding the peak current rating of the output sense resistor during Short-circuit conditions, the power rating of the resistor has to be chosen properly.

In this case, the maximum power dissipated in the sense resistor can be determined as demonstrated in Equation 3-11.

EQUATION 3-11:

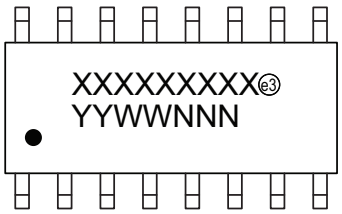
$$P_{SC} = I_{SAT}^2 \times R_S$$
$$= 11W$$

For a 1.24Ω 1/4W resistor, the maximum power it can dissipate for a single 1 ms pulse of current is 11W. Since the total short-circuit time is about 350 ns, including the 300 ns time for turn-off, the resistor should be able to handle the current.

4.0 PACKAGING INFORMATION

4.1 Package Marking Information

16-lead SOIC



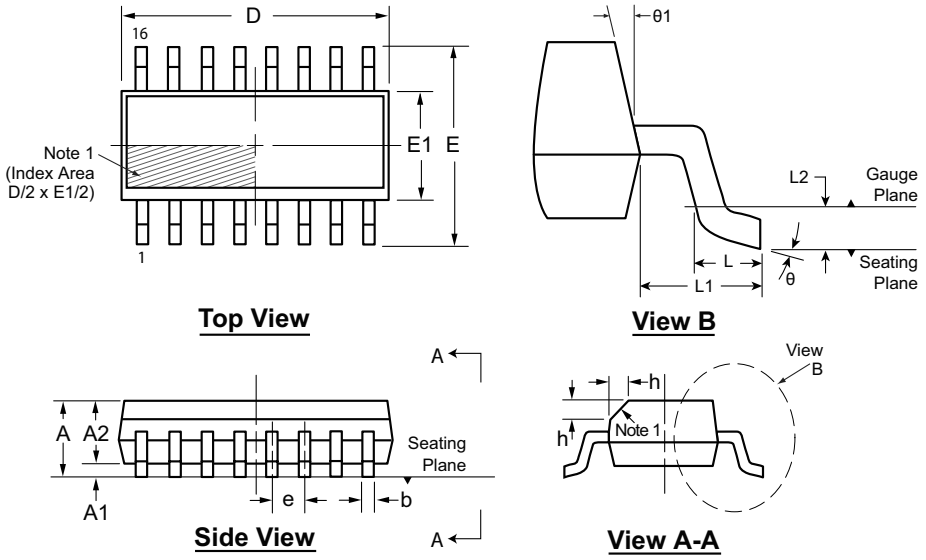
Example

Legend:	XX...X	Product Code or Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for product code or customer-specific information. Package may or not include the corporate logo.

16-Lead SOIC (Narrow Body) Package Outline (NG)

9.90x3.90mm body, 1.75mm height (max), 1.27mm pitch



Note: For the most current package drawings, see the Microchip Packaging Specification at www.microchip.com/packaging.

Note:

1. *This chamfer feature is optional. If it is not present, then a Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.*

Symbol		A	A1	A2	b	D	E	E1	e	h	L	L1	L2	θ	θ1
Dimension (mm)	MIN	1.35*	0.10	1.25	0.31	9.80*	5.80*	3.80*	1.27 BSC	0.25	0.40	1.04 REF	0.25 BSC	0°	5°
	NOM	-	-	-	-	9.90	6.00	3.90		-	-			-	-
	MAX	1.75	0.25	1.65*	0.51	10.00*	6.20*	4.00*		0.50	1.27			8°	15°

JEDEC Registration MS-012, Variation AC, Issue E, Sept. 2005.
** This dimension is not specified in the JEDEC drawing.*
Drawings are not to scale.

NOTES:

APPENDIX A: REVISION HISTORY

Revision A (February 2017)

- Converted Supertex Doc# DSFP-HV9911 to Microchip DS20005580A
- Changed the packing quantity of the NG M901 media type from 1000/Reel to 2600/Reel
- Changed the packaging quantity of the NG M934 media type from 2500/Reel to 2600/Reel
- Made minor text changes throughout the document

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

PART NO.	XX	-	X	-	X
Device	Package Options		Environmental		Media Type

Device:	HV9911	=	Switch-mode LED Driver IC with High Current Accuracy
Package:	NG	=	16-lead SOIC
Environmental:	G	=	Lead (Pb)-free/RoHS-compliant Package
Media Types:	(blank)	=	45/Tube for an NG Package
	M901	=	2600/Reel for an NG package
	M934	=	2600/Reel for an NG package

Note: For Media Types M901 and M934, the base quantity for tape and reel was standardized to 2600/reel. Both options will result in the delivery of the same number of parts/reel.

Examples:

a) HV9911NG-G: Switch-mode LED Driver IC with High Current Accuracy, 16-lead SOIC Package, 45/Tube

b) HV9911NG-G-M901: Switch-mode LED Driver IC with High Current Accuracy, 16-lead SOIC, 2600/Reel

c) HV9911NG-G-M934: Switch-mode LED Driver IC with High Current Accuracy, 16-lead SOIC, 2600/Reel

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