

# 74AHC1G02-Q100; 74AHCT1G02-Q100

## 2-input NOR gate

Rev. 1 — 6 November 2013

Product data sheet

## 1. General description

74AHC1G02-Q100 and 74AHCT1G02-Q100 are high-speed Si-gate CMOS devices. They provide a 2-input NOR function.

The AHC device has CMOS input switching levels and supply voltage range 2 V to 5.5 V.

The AHCT device has TTL input switching levels and supply voltage range 4.5 V to 5.5 V.

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 1) and is suitable for use in automotive applications.

## 2. Features and benefits

- Automotive product qualification in accordance with AEC-Q100 (Grade 1)
  - ◆ Specified from  $-40\text{ }^{\circ}\text{C}$  to  $+85\text{ }^{\circ}\text{C}$  and from  $-40\text{ }^{\circ}\text{C}$  to  $+125\text{ }^{\circ}\text{C}$
- Symmetrical output impedance
- High noise immunity
- Low power dissipation
- Balanced propagation delays
- SOT353-1 and SOT753 package options
- ESD protection:
  - ◆ MIL-STD-883, method 3015 exceeds 2000 V
  - ◆ HBM JESD22-A114F exceeds 2000 V
  - ◆ MM JESD22-A115-A exceeds 200 V (C = 200 pf, R = 0  $\Omega$ )

## 3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74AHC1G02GW-Q100 74AHCT1G02GW-Q100	$-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$	TSSOP5	plastic thin shrink small outline package; 5 leads; body width 1.25 mm	SOT353-1
74AHC1G02GV-Q100 74AHCT1G02GV-Q100	$-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$	SC-74A	plastic surface-mounted package; 5 leads	SOT753

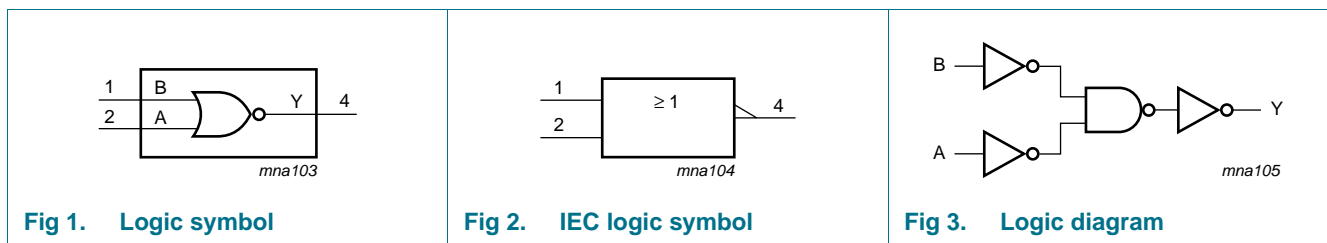
## 4. Marking

Table 2. Marking codes

Type number	Marking <sup>[1]</sup>
74AHC1G02GW-Q100	AB
74AHC1G02GV-Q100	A02
74AHCT1G02GW-Q100	CB
74AHCT1G02GV-Q100	C02

[1] The pin 1 indicator is located on the lower left corner of the device, below the marking code.

## 5. Functional diagram



## 6. Pinning information

### 6.1 Pinning



### 6.2 Pin description

Table 3. Pin description

Symbol	Pin	Description
B	1	data input B
A	2	data input A
GND	3	ground (0 V)
Y	4	data output Y
V <sub>CC</sub>	5	supply voltage

## 7. Functional description

**Table 4. Function table**

*H = HIGH voltage level; L = LOW voltage level*

Inputs		Output
A	B	Y
L	L	H
L	H	L
H	L	L
H	H	L

## 8. Limiting values

**Table 5. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134).*

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	supply voltage		-0.5	+7.0	V
$V_I$	input voltage		-0.5	+7.0	V
$I_{IK}$	input clamping current	$V_I < -0.5$ V	-20	-	mA
$I_{OK}$	output clamping current	$V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V	[1] -	±20	mA
$I_O$	output current	$-0.5$ V < $V_O$ < $V_{CC} + 0.5$ V	-	±25	mA
$I_{CC}$	supply current		-	75	mA
$I_{GND}$	ground current		-75	-	mA
$T_{stg}$	storage temperature		-65	+150	°C
$P_{tot}$	total power dissipation	$T_{amb} = -40$ °C to +125 °C	[2] -	250	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For both TSSOP5 and SC-74A packages: above 87.5 °C the value of  $P_{tot}$  derates linearly with 4.0 mW/K.

## 9. Recommended operating conditions

**Table 6. Recommended operating conditions**

*Voltages are referenced to GND (ground = 0 V).*

Symbol	Parameter	Conditions	74AHC1G02-Q100			74AHCT1G02-Q100			Unit
			Min	Typ	Max	Min	Typ	Max	
$V_{CC}$	supply voltage		2.0	5.0	5.5	4.5	5.0	5.5	V
$V_I$	input voltage		0	-	5.5	0	-	5.5	V
$V_O$	output voltage		0	-	$V_{CC}$	0	-	$V_{CC}$	V
$T_{amb}$	ambient temperature		-40	+25	+125	-40	+25	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 3.3$ V ± 0.3 V	-	-	100	-	-	-	ns/V
		$V_{CC} = 5.0$ V ± 0.5 V	-	-	20	-	-	20	ns/V

## 10. Static characteristics

**Table 7. Static characteristics**

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
<b>74AHC1G02-Q100</b>										
V <sub>IH</sub>	HIGH-level input voltage	V <sub>CC</sub> = 2.0 V	1.5	-	-	1.5	-	1.5	-	V
		V <sub>CC</sub> = 3.0 V	2.1	-	-	2.1	-	2.1	-	V
		V <sub>CC</sub> = 5.5 V	3.85	-	-	3.85	-	3.85	-	V
V <sub>IL</sub>	LOW-level input voltage	V <sub>CC</sub> = 2.0 V	-	-	0.5	-	0.5	-	0.5	V
		V <sub>CC</sub> = 3.0 V	-	-	0.9	-	0.9	-	0.9	V
		V <sub>CC</sub> = 5.5 V	-	-	1.65	-	1.65	-	1.65	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>								
		I <sub>O</sub> = -50 μA; V <sub>CC</sub> = 2.0 V	1.9	2.0	-	1.9	-	1.9	-	V
		I <sub>O</sub> = -50 μA; V <sub>CC</sub> = 3.0 V	2.9	3.0	-	2.9	-	2.9	-	V
		I <sub>O</sub> = -50 μA; V <sub>CC</sub> = 4.5 V	4.4	4.5	-	4.4	-	4.4	-	V
		I <sub>O</sub> = -4.0 mA; V <sub>CC</sub> = 3.0 V	2.58	-	-	2.48	-	2.40	-	V
		I <sub>O</sub> = -8.0 mA; V <sub>CC</sub> = 4.5 V	3.94	-	-	3.8	-	3.70	-	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>								
		I <sub>O</sub> = 50 μA; V <sub>CC</sub> = 2.0 V	-	0	0.1	-	0.1	-	0.1	V
		I <sub>O</sub> = 50 μA; V <sub>CC</sub> = 3.0 V	-	0	0.1	-	0.1	-	0.1	V
		I <sub>O</sub> = 50 μA; V <sub>CC</sub> = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I <sub>O</sub> = 4.0 mA; V <sub>CC</sub> = 3.0 V	-	-	0.36	-	0.44	-	0.55	V
		I <sub>O</sub> = 8.0 mA; V <sub>CC</sub> = 4.5 V	-	-	0.36	-	0.44	-	0.55	V
I <sub>I</sub>	input leakage current	V <sub>I</sub> = 5.5 V or GND; V <sub>CC</sub> = 0 V to 5.5 V	-	-	0.1	-	1.0	-	2.0	μA
I <sub>CC</sub>	supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0 A; V <sub>CC</sub> = 5.5 V	-	-	1.0	-	10	-	40	μA
C <sub>I</sub>	input capacitance		-	1.5	10	-	10	-	10	pF
<b>74AHCT1G02-Q100</b>										
V <sub>IH</sub>	HIGH-level input voltage	V <sub>CC</sub> = 4.5 V to 5.5 V	2.0	-	-	2.0	-	2.0	-	V
V <sub>IL</sub>	LOW-level input voltage	V <sub>CC</sub> = 4.5 V to 5.5 V	-	-	0.8	-	0.8	-	0.8	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>CC</sub> = 4.5 V								
		I <sub>O</sub> = -50 μA	4.4	4.5	-	4.4	-	4.4	-	V
		I <sub>O</sub> = -8.0 mA	3.94	-	-	3.8	-	3.70	-	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>CC</sub> = 4.5 V								
		I <sub>O</sub> = 50 μA	-	0	0.1	-	0.1	-	0.1	V
		I <sub>O</sub> = 8.0 mA	-	-	0.36	-	0.44	-	0.55	V
I <sub>I</sub>	input leakage current	V <sub>I</sub> = 5.5 V or GND; V <sub>CC</sub> = 0 V to 5.5 V	-	-	0.1	-	1.0	-	2.0	μA

**Table 7. Static characteristics ...continued**  
 Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
$I_{CC}$	supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 5.5$ V	-	-	1.0	-	10	-	40	$\mu$ A
$\Delta I_{CC}$	additional supply current	per input pin; $V_I = 3.4$ V; other inputs at $V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 5.5$ V	-	-	1.35	-	1.5	-	1.5	mA
$C_I$	input capacitance		-	1.5	10	-	10	-	10	pF

## 11. Dynamic characteristics

**Table 8. Dynamic characteristics**  
 $GND = 0$  V;  $t_r = t_f = \leq 3.0$  ns. For test circuit, see [Figure 6](#).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
<b>74AHC1G02-Q100</b>										
$t_{pd}$	propagation delay	A and B to Y; see <a href="#">Figure 5</a>	<a href="#">[1]</a>							
		$V_{CC} = 3.0$ V to 3.6 V	<a href="#">[2]</a>							
		$C_L = 15$ pF	-	4.4	7.9	1.0	9.5	1.0	10.5	ns
		$C_L = 50$ pF	-	6.3	11.4	1.0	13	1.0	14.5	ns
		$V_{CC} = 4.5$ V to 5.5 V	<a href="#">[3]</a>							
		$C_L = 15$ pF	-	3.2	5.5	1.0	6.5	1.0	7.0	ns
$C_{PD}$	power dissipation capacitance	per buffer; $C_L = 50$ pF; $f = 1$ MHz; $V_I = GND$ to $V_{CC}$	<a href="#">[4]</a>							
			-	18	-	-	-	-	-	pF
<b>74AHCT1G02-Q100</b>										
$t_{pd}$	propagation delay	A and B to Y; see <a href="#">Figure 5</a>	<a href="#">[1]</a>							
		$V_{CC} = 4.5$ V to 5.5 V	<a href="#">[3]</a>							
		$C_L = 15$ pF	-	3.5	5.5	1.0	6.5	1.0	7.0	ns
$C_{PD}$	power dissipation capacitance	per buffer; $C_L = 50$ pF; $f = 1$ MHz; $V_I = GND$ to $V_{CC}$	<a href="#">[4]</a>							
			-	19	-	-	-	-	-	pF

[1]  $t_{pd}$  is the same as  $t_{PLH}$  and  $t_{PHL}$ .

[2] Typical values are measured at  $V_{CC} = 3.3$  V.

[3] Typical values are measured at  $V_{CC} = 5.0$  V.

[4]  $C_{PD}$  is used to determine the dynamic power dissipation  $P_D$  ( $\mu$ W).

$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$  where:

$f_i$  = input frequency in MHz;  $f_o$  = output frequency in MHz;

$C_L$  = output load capacitance in pF;

$V_{CC}$  = supply voltage in Volts.

## 12. Waveforms

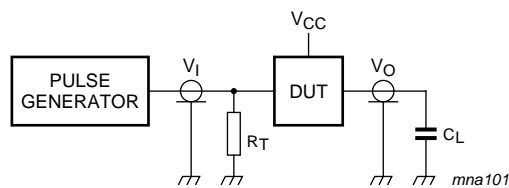


Measurement points are given in [Table 9](#).

**Fig 5. The inputs (A and B) to output (Y) propagation delays**

**Table 9. Measurement point**

Type	Input		Output
	$V_I$	$V_M$	$V_M$
74AHC1G02-Q100	GND to $V_{CC}$	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$
74AHCT1G02-Q100	GND to 3.0 V	1.5 V	$0.5 \times V_{CC}$



Test data is given in [Table 8](#). Definitions for test circuit:

$C_L$  = Load capacitance including jig and probe capacitance.

$R_T$  = Termination resistance should be equal to output impedance  $Z_o$  of the pulse generator.

**Fig 6. Test circuit for measuring switching times**

13. Package outline

TSSOP5: plastic thin shrink small outline package; 5 leads; body width 1.25 mm

SOT353-1



Fig 7. Package outline SOT353-1 (TSSOP5)

Plastic surface-mounted package; 5 leads

SOT753



Fig 8. Package outline SOT753 (SC-74A)



## 14. Abbreviations

Table 10. Abbreviations

Acronym	Description
CDM	Charged Device Model
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

## 15. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74AHC_AHCT1G02_Q100 v.1	20131106	Product data sheet	-	-

## 16. Legal information

### 16.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
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