FAIRCHILD SEMICONDUCTOR®

January 2008

74AC245, 74ACT245 Octal Bidirectional Transceiver with 3-STATE Inputs/Outputs

Features

- I_{CC} and I_{OZ} reduced by 50%
- Non-inverting buffers
- Bidirectional data path
- A and B outputs source/sink 24mA
- ACT245 has TTL-compatible inputs

General Description

The AC/ACT245 contains eight non-inverting bidirectional buffers with 3-STATE outputs and is intended for bus-oriented applications. Current sinking capability is 24mA at both the A and B ports. The Transmit/Receive ($T/\overline{R}$) input determines the direction of data flow through the bidirectional transceiver. Transmit (active-HIGH) enables data from A ports to B ports; Receive (active-LOW) enables data from B ports to A ports. The Output Enable input, when HIGH, disables both A and B ports by placing them in a HIGH Z condition.

Ordering Information

Order Number	Package Number	Package Description
74AC245SC	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
74AC245SJ	M20D	20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74AC245MTC	MTC20	20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74AC245PC	N20A	20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
74ACT245SC	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
74ACT245SJ	M20D	20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74ACT245MSA	MSA20	20-Lead Shrink Small Outline Package (SSOP), JEDEC MO-150, 5.3mm Wide
74ACT245MTC	MTC20	20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74ACT245PC	N20A	20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Device also available in Tape and Reel. Specify by appending suffix letter “X” to the ordering number.

All packages are lead free per JEDEC: J-STD-020B standard.

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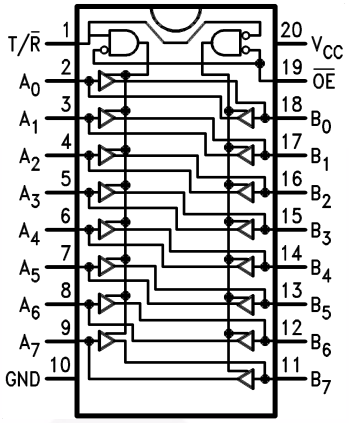
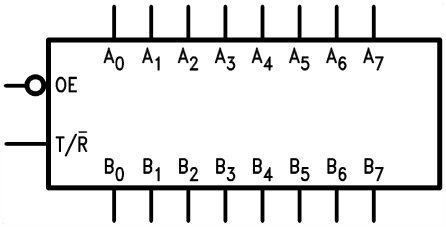
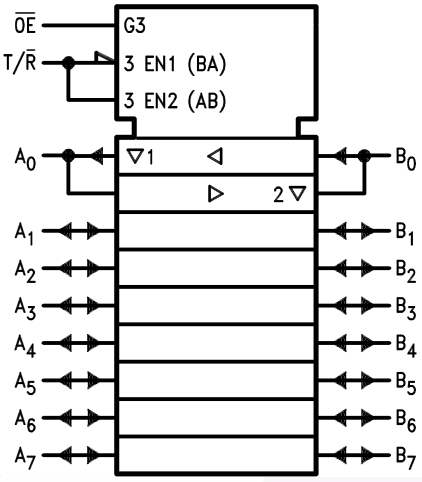
Connection Diagram



Logic Symbol



IEEE/IEC



Pin Description

Pin Names	Description
$\overline{OE}$	Output Enable Input
T/$\overline{R}$	Transmit/Receive Input
A_0–A_7	Side A 3-STATE Inputs or 3-STATE Outputs
B_0–B_7	Side B 3-STATE Inputs or 3-STATE Outputs

Truth Table

Inputs		Outputs
$\overline{OE}$	T/$\overline{R}$	
L	L	Bus B Data to Bus A
L	H	Bus A Data to Bus B
H	X	HIGH-Z State

H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Rating
V_{CC}	Supply Voltage	–0.5V to +7.0V
I_{IK}	DC Input Diode Current $V_I = -0.5V$	–20mA
	$V_I = V_{CC} + 0.5$	+20mA
V_I	DC Input Voltage	–0.5V to V_{CC} + 0.5V
I_{OK}	DC Output Diode Current $V_O = -0.5V$	–20mA
	$V_O = V_{CC} + 0.5V$	+20mA
V_O	DC Output Voltage	–0.5V to V_{CC} + 0.5V
I_O	DC Output Source or Sink Current	±50mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current per Output Pin	±50mA
T_{STG}	Storage Temperature	–65°C to +150°C
T_J	Junction Temperature	140°C

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Rating
V_{CC}	Supply Voltage AC	2.0V to 6.0V
	ACT	4.5V to 5.5V
V_I	Input Voltage	0V to V_{CC}
V_O	Output Voltage	0V to V_{CC}
T_A	Operating Temperature	–40°C to +85°C
$\Delta V / \Delta t$	Minimum Input Edge Rate, AC Devices: V_{IN} from 30% to 70% of V_{CC}, V_{CC} @ 3.3V, 4.5V, 5.5V	125mV/ns
$\Delta V / \Delta t$	Minimum Input Edge Rate, ACT Devices: V_{IN} from 0.8V to 2.0V, V_{CC} @ 4.5V, 5.5V	125mV/ns

DC Electrical Characteristics for AC

Symbol	Parameter	V_{CC} (V)	Conditions	$T_A = +25°C$ Typ.	$T_A = -40°C$ to $+85°C$ Guaranteed Limits		Units
V_{IH}	Minimum HIGH Level Input Voltage	3.0	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$	1.5	2.1	2.1	V
		4.5		2.25	3.15	3.15	
		5.5		2.75	3.85	3.85	
V_{IL}	Maximum LOW Level Input Voltage	3.0	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$	1.5	0.9	0.9	V
		4.5		2.25	1.35	1.35	
		5.5		2.75	1.65	1.65	
V_{OH}	Minimum HIGH Level Output Voltage	3.0	$I_{OUT} = -50\mu A$	2.99	2.9	2.9	V
		4.5		4.49	4.4	4.4	
		5.5		5.49	5.4	5.4	
		3.0	$V_{IN} = V_{IL}$ or V_{IH}, $I_{OH} = -12mA$		2.56	2.46	
		4.5	$V_{IN} = V_{IL}$ or V_{IH}, $I_{OH} = -24mA$		3.86	3.76	
		5.5	$V_{IN} = V_{IL}$ or V_{IH}, $I_{OH} = -24mA$(1)		4.86	4.76	
V_{OL}	Maximum LOW Level Output Voltage	3.0	$I_{OUT} = 50\mu A$	0.002	0.1	0.1	V
		4.5		0.001	0.1	0.1	
		5.5		0.001	0.1	0.1	
		3.0	$V_{IN} = V_{IL}$ or V_{IH}, $I_{OL} = 12mA$		0.36	0.44	
		4.5	$V_{IN} = V_{IL}$ or V_{IH}, $I_{OL} = 24mA$		0.36	0.44	
		5.5	$V_{IN} = V_{IL}$ or V_{IH}, $I_{OL} = 24mA$(1)		0.36	0.44	
I_{IN}(2)	Maximum Input Leakage Current	5.5	$V_I = V_{CC}$, GND		±0.1	±1.0	μA
I_{OLD}	Minimum Dynamic Output Current(3)	5.5	$V_{OLD} = 1.65V$ Max.			75	mA
I_{OHD}		5.5	$V_{OHD} = 3.85V$ Min.			–75	mA
I_{CC}(2)	Maximum Quiescent Supply Current	5.5	$V_{IN} = V_{CC}$ or GND		4.0	40.0	μA
I_{OZT}	Maximum I/O Leakage Current	5.5	V_I (OE) = V_{IL}, V_{IH}; $V_I = V_{CC}$, GND; $V_O = V_{CC}$, GND		±0.3	±3.0	μA

Notes:

1. All outputs loaded; thresholds on input associated with output under test.
2. I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}.
3. Maximum test duration 2.0ms, one output loaded at a time.

DC Electrical Characteristics for ACT

Symbol	Parameter	V_{CC} (V)	Conditions	$T_A = +25°C$ Typ.	$T_A = -40°C$ to $+85°C$ Guaranteed Limits		Units
V_{IH}	Minimum HIGH Level Input Voltage	4.5	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$	1.5	2.0	2.0	V
		5.5		1.5	2.0	2.0	
V_{IL}	Maximum LOW Level Input Voltage	4.5	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$	1.5	0.8	0.8	V
		5.5		1.5	0.8	0.8	
V_{OH}	Minimum HIGH Level Output Voltage	4.5	$I_{OUT} = -50\mu A$	4.49	4.4	4.4	V
		5.5		5.49	5.4	5.4	
		4.5	$V_{IN} = V_{IL}$ or V_{IH}, $I_{OH} = -24mA$		3.86	3.76	
		5.5	$V_{IN} = V_{IL}$ or V_{IH}, $I_{OH} = -24mA$(4)		4.86	4.76	
V_{OL}	Maximum LOW Level Output Voltage	4.5	$I_{OUT} = 50\mu A$	0.001	0.1	0.1	V
		5.5		0.001	0.1	0.1	
		4.5	$V_{IN} = V_{IL}$ or V_{IH}, $I_{OL} = 24mA$		0.36	0.44	
		5.5	$V_{IN} = V_{IL}$ or V_{IH}, $I_{OL} = 24mA$(4)		0.36	0.44	
I_{IN}	Maximum Input Leakage Current	5.5	$V_I = V_{CC}$, GND		±0.1	±1.0	μA
I_{CCT}	Maximum I_{CC}/Input	5.5	$V_I = V_{CC} - 2.1V$	0.6		1.5	mA
I_{OLD}	Minimum Dynamic Output Current(5)	5.5	$V_{OLD} = 1.65V$ Max.			75	mA
I_{OHD}		5.5	$V_{OHD} = 3.85V$ Min.			–75	mA
I_{CC}	Maximum Quiescent Supply Current	5.5	$V_{IN} = V_{CC}$ or GND		4.0	40.0	μA
I_{OZT}	Maximum I/O Leakage Current	5.5	V_I (OE) = V_{IL}, V_{IH}; $V_I = V_{CC}$, GND; $V_O = V_{CC}$, GND		±0.3	±3.0	μA

Notes:

4. All outputs loaded; thresholds on input associated with output under test.
5. Maximum test duration 2.0ms, one output loaded at a time.

AC Electrical Characteristics for AC

Symbol	Parameter	V_{CC} (V)[6]	$T_A = +25°C$, $C_L = 50pF$			$T_A = -40°C$ to $+85°C$, $C_L = 50pF$		Units
			Min.	Typ.	Max.	Min.	Max.	
t_{PLH}	Propagation Delay, A_n to B_n or B_n to A_n	3.3	1.5	5.0	8.5	1.0	9.0	ns
		5.0	1.5	3.5	6.5	1.0	7.0	
t_{PHL}	Propagation Delay, A_n to B_n or B_n to A_n	3.3	1.5	5.0	8.5	1.0	9.0	ns
		5.0	1.5	3.5	6.0	1.0	7.0	
t_{PZH}	Output Enable Time	3.3	2.5	7.0	11.5	2.0	12.5	ns
		5.0	1.5	5.0	8.5	1.0	9.0	
t_{PZL}	Output Enable Time	3.3	2.5	7.5	12.0	2.0	13.5	ns
		5.0	1.5	5.5	9.0	1.0	9.5	
t_{PHZ}	Output Disable Time	3.3	2.0	6.5	12.0	1.0	12.5	ns
		5.0	1.5	5.5	9.0	1.0	10.0	
t_{PLZ}	Output Disable Time	3.3	2.0	7.0	11.5	1.5	13.0	ns
		5.0	1.5	5.5	9.0	1.0	10.0	

Note:

6. Voltage range 3.3 is 3.3V ± 0.3V. Voltage range 5.0 is 5.0V ± 0.5V.

AC Electrical Characteristics for ACT

Symbol	Parameter	V_{CC} (V)[7]	$T_A = +25°C$, $C_L = 50pF$			$T_A = -40°C$ to $+85°C$, $C_L = 50pF$		Units
			Min.	Typ.	Max.	Min.	Max.	
t_{PLH}	Propagation Delay, A_n to B_n or B_n to A_n	5.0	1.5	4.0	7.5	1.5	8.0	ns
t_{PHL}	Propagation Delay, A_n to B_n or B_n to A_n	5.0	1.5	4.0	8.0	1.0	9.0	ns
t_{PZH}	Output Enable Time	5.0	1.5	5.0	10.0	1.5	11.0	ns
t_{PZL}	Output Enable Time	5.0	1.5	5.5	10.0	1.5	12.0	ns
t_{PHZ}	Output Disable Time	5.0	1.5	5.5	10.0	1.0	11.0	ns
t_{PLZ}	Output Disable Time	5.0	2.0	5.0	10.0	1.5	11.0	ns

Note:

7. Voltage range 5.0 is 5.0V ± 0.5V.

Capacitance

Symbol	Parameter	Conditions	Typ.	Units
C_{IN}	Input Capacitance	V_{CC} = OPEN	4.5	pF
$C_{I/O}$	Input/Output Capacitance	V_{CC} = 5.0V	15.0	pF
C_{PD}	Power Dissipation Capacitance	V_{CC} = 5.0V	45.0	pF

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Physical Dimensions

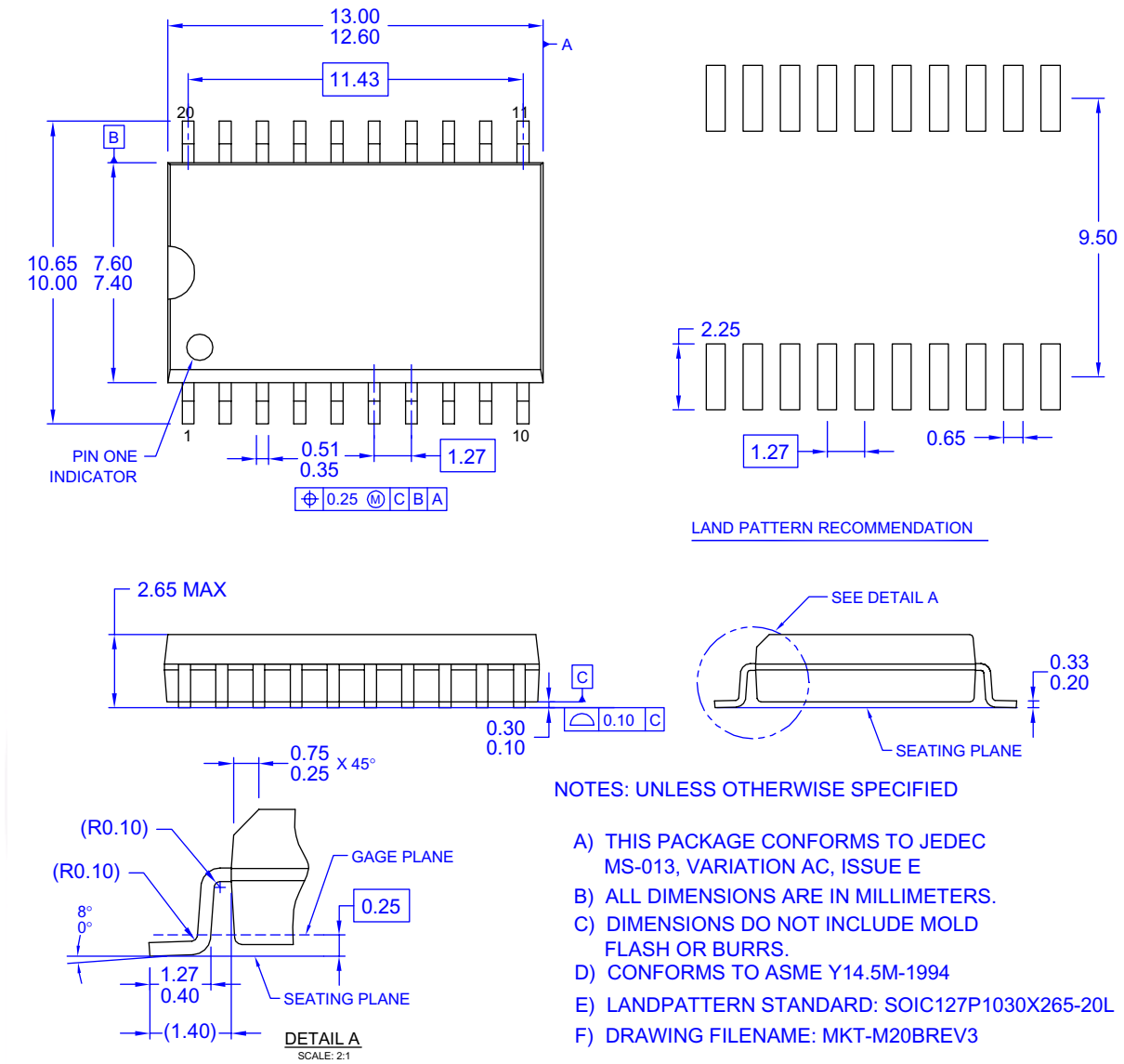

Figure 1. 20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide

Package drawings are provided as a service to customers considering Fairchild components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a Fairchild Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of Fairchild's worldwide terms and conditions, specifically the warranty therein, which covers Fairchild products.

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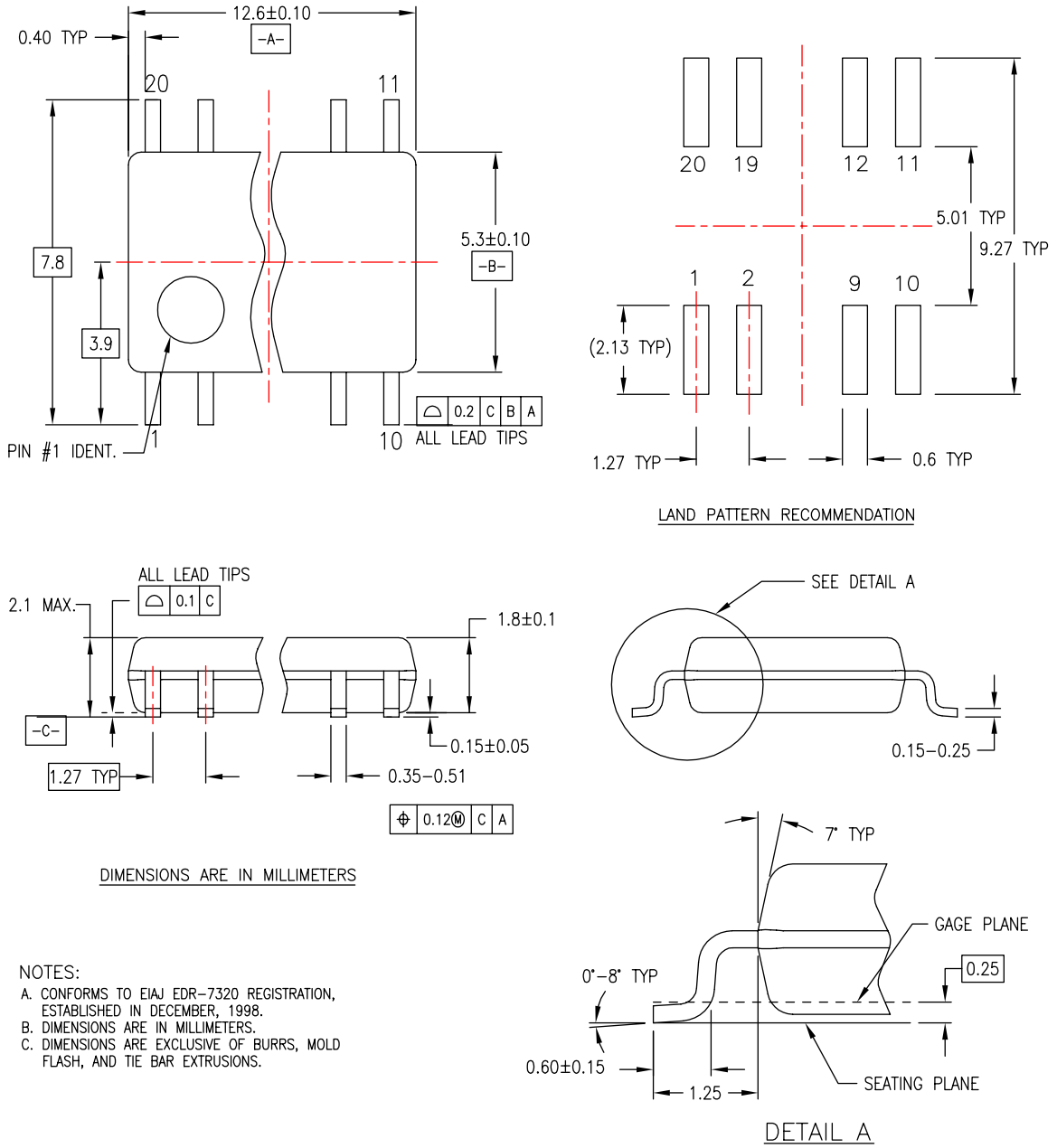
Physical Dimensions (Continued)



NOTES:
A. CONFORMS TO EIAJ EDR–7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.
B. DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

Figure 2. 20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide

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Physical Dimensions (Continued)

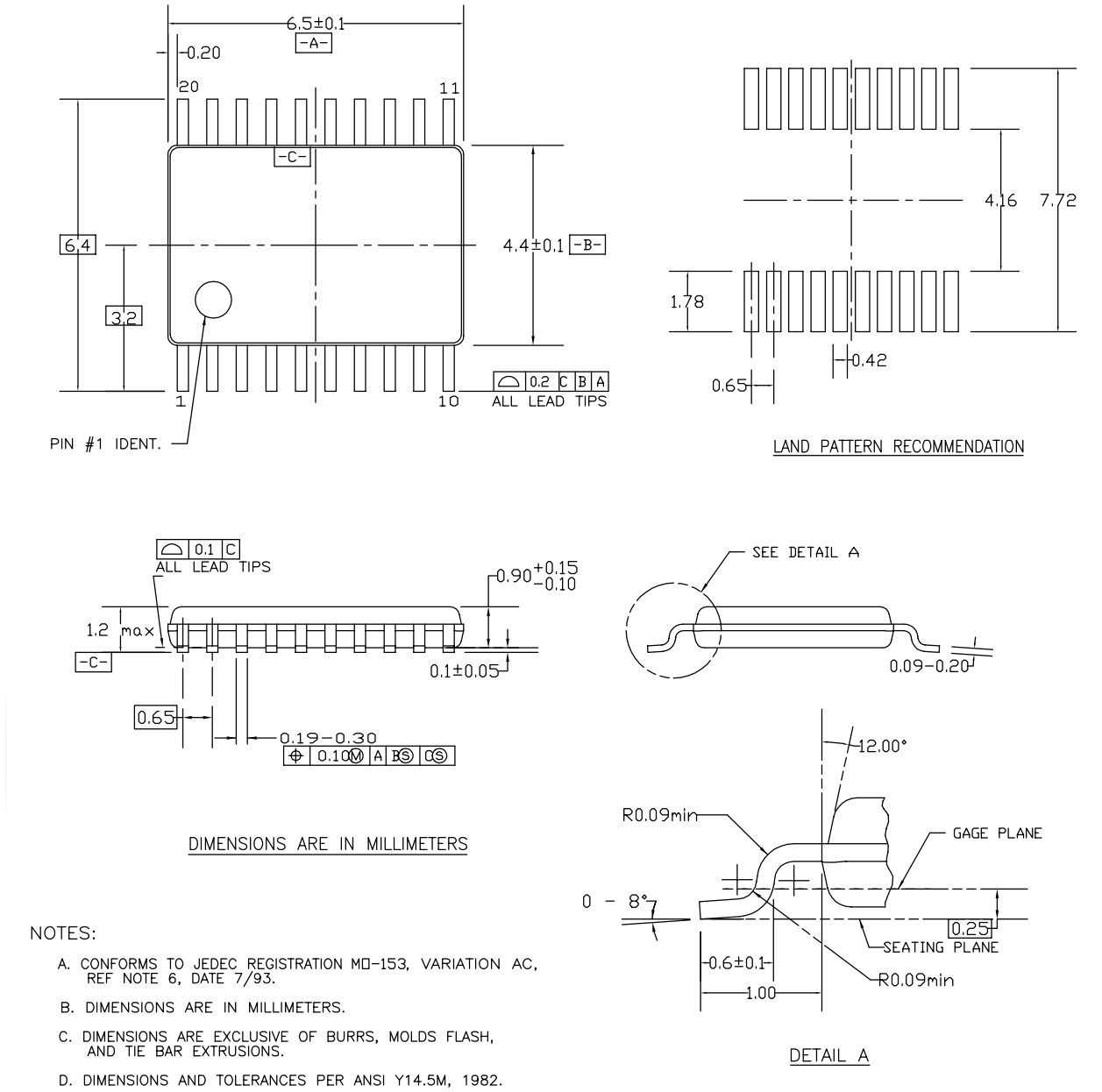

Figure 3. 20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

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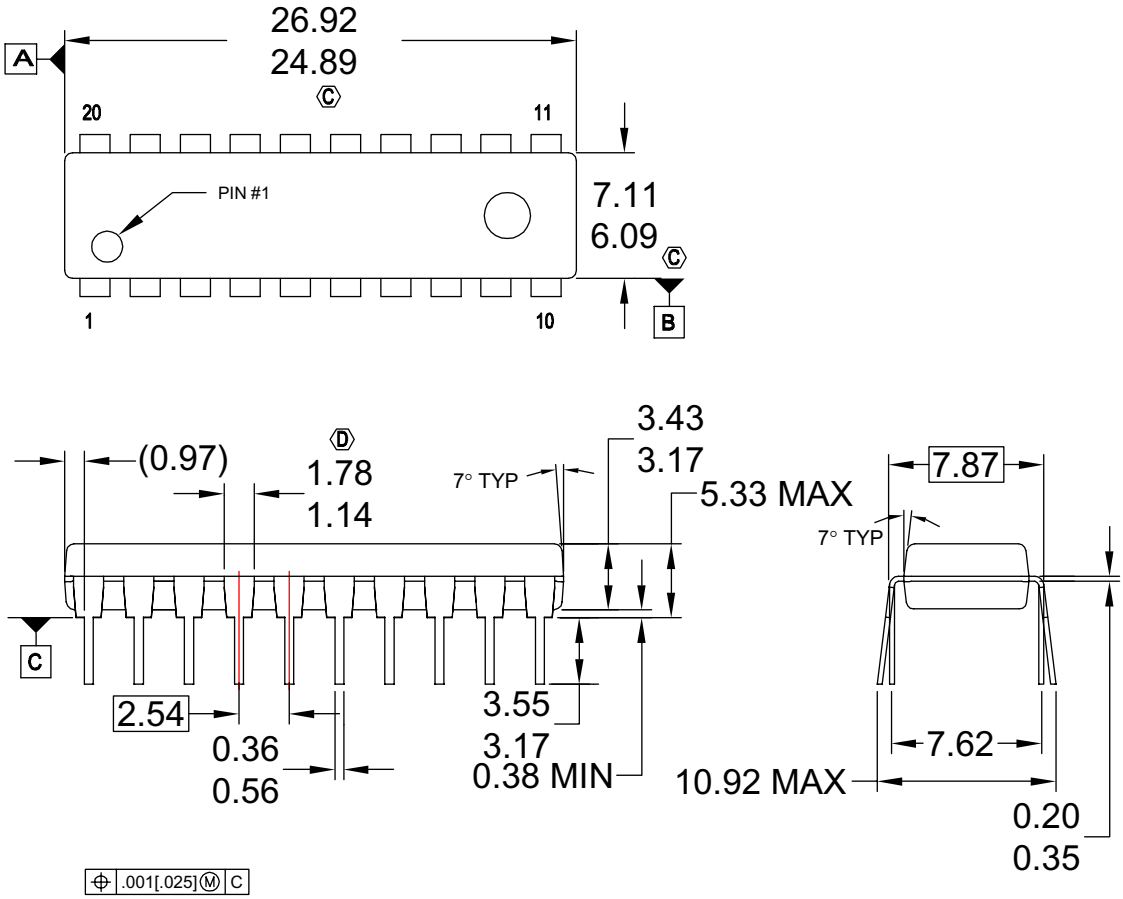
Physical Dimensions (Continued)



NOTES:

A. CONFORMS TO JEDEC REGISTRATION MS-001, VARIATIONS AD.

B. ALL DIMENSIONS ARE IN MILLIMETERS

C. DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.25MM.

D. DOES NOT INCLUDE DAMBAR PROTRUSIONS. DAMBAR PROTRUSIONS SHALL NOT EXCEED 0.25MM.

E. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.

F. DRAWING FILE NAME: N20AREV8

Figure 4. 20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

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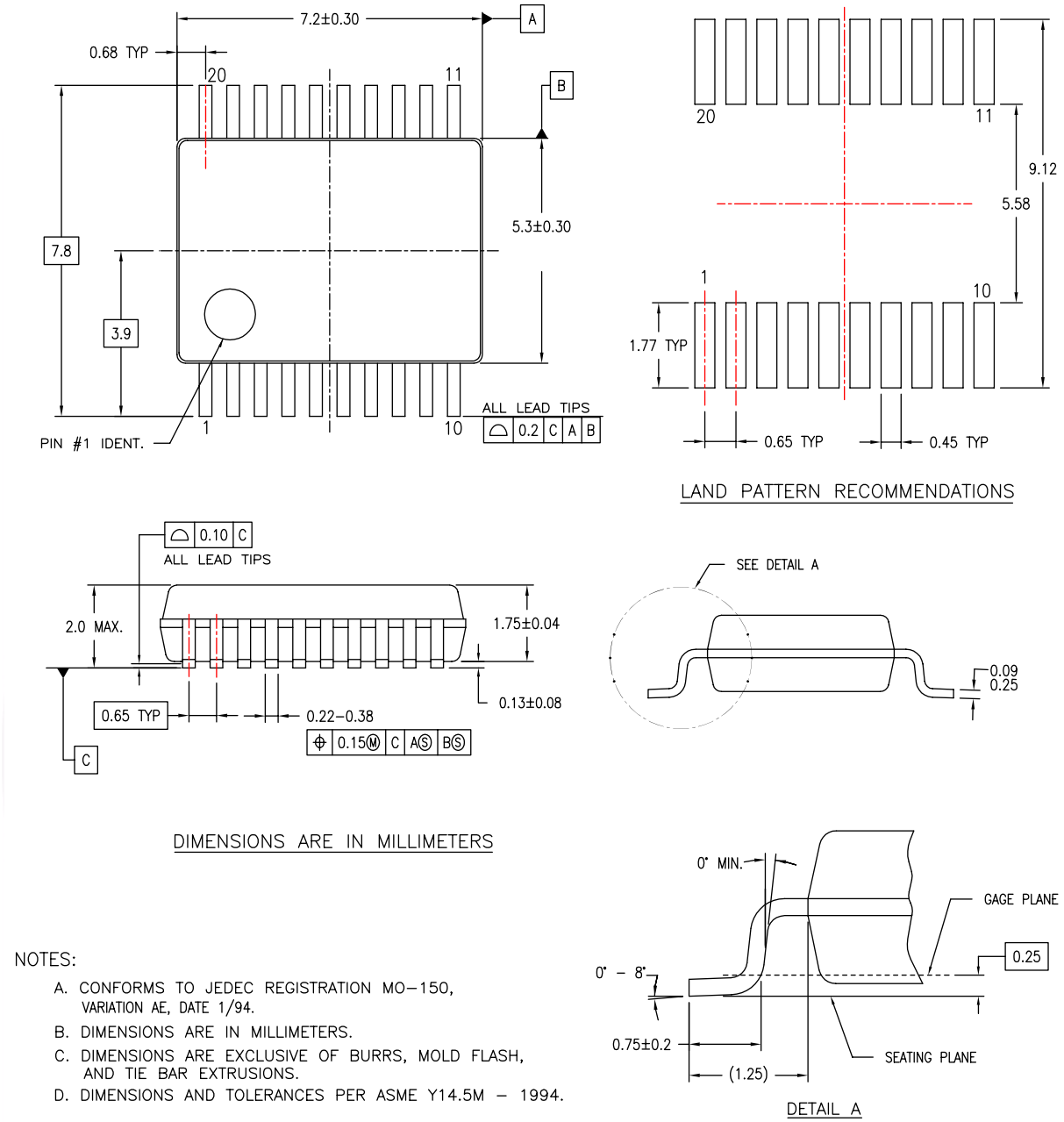
Physical Dimensions (Continued)



NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO–150, VARIATION AE, DATE 1/94.

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

D. DIMENSIONS AND TOLERANCES PER ASME Y14.5M – 1994.

MSA20REVB

Figure 5. 20-Lead Shrink Small Outline Package (SSOP), JEDEC MO-150, 5.3mm Wide

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Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild Semiconductor. The datasheet is printed for reference information only.

Rev. I32

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Адрес: 105318, г.Москва, ул.Щербаковская д.3, офис 1107

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Нашей специализацией является поставка электронной компонентной базы двойного назначения, продукции таких производителей как XILINX, Intel (ex.ALTERA), Vicor, Microchip, Texas Instruments, Analog Devices, Mini-Circuits, Amphenol, Glenair.

Сотрудничество с глобальными дистрибьюторами электронных компонентов, предоставляет возможность заказывать и получать с международных складов практически любой перечень компонентов в оптимальные для Вас сроки.

На всех этапах разработки и производства наши партнеры могут получить квалифицированную поддержку опытных инженеров.

Система менеджмента качества компании отвечает требованиям в соответствии с ГОСТ Р ИСО 9001, ГОСТ РВ 0015-002 и ЭС РД 009

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