

# MAX5800/MAX5801/MAX5802

## Ultra-Small, Dual-Channel, 8-/10-/12-Bit Buffered Output DACs with Internal Reference and I<sup>2</sup>C Interface

### General Description

The MAX5800/MAX5801/MAX5802 2-channel, low-power, 8-/10-/12-bit, voltage-output digital-to-analog converters (DACs) include output buffers and an internal reference that is selectable to be 2.048V, 2.500V, or 4.096V. The MAX5800/MAX5801/MAX5802 accept a wide supply voltage range of 2.7V to 5.5V with extremely low power (1.5mW) consumption to accommodate most low-voltage applications. A precision external reference input allows rail-to-rail operation and presents a 100k $\Omega$  (typ) load to an external reference.

The MAX5800/MAX5801/MAX5802 have an I<sup>2</sup>C-compatible, 2-wire interface that operates at clock rates up to 400kHz. The DAC output is buffered and has a low supply current of less than 250 $\mu$ A per channel and a low offset error of  $\pm 0.5$ mV (typ). On power-up, the MAX5800/MAX5801/MAX5802 reset the DAC outputs to zero, providing additional safety for applications that drive valves or other transducers which need to be off on power-up. The internal reference is initially powered down to allow use of an external reference. The MAX5800/MAX5801/MAX5802 allow simultaneous output updates using software LOAD commands.

A clear logic input ( $\overline{\text{CLR}}$ ) allows the contents of the CODE and the DAC registers to be cleared asynchronously and sets the DAC outputs to zero. The MAX5800/MAX5801/MAX5802 are available in a small 10-pin  $\mu$ MAX<sup>®</sup> and an ultra-small, 10-pin TDFN package and are specified over the -40°C to +125°C temperature range.

### Applications

- Programmable Voltage and Current Sources
- Gain and Offset Adjustment
- Automatic Tuning and Optical Control
- Power Amplifier Control and Biasing
- Process Control and Servo Loops
- Portable Instrumentation
- Data Acquisition

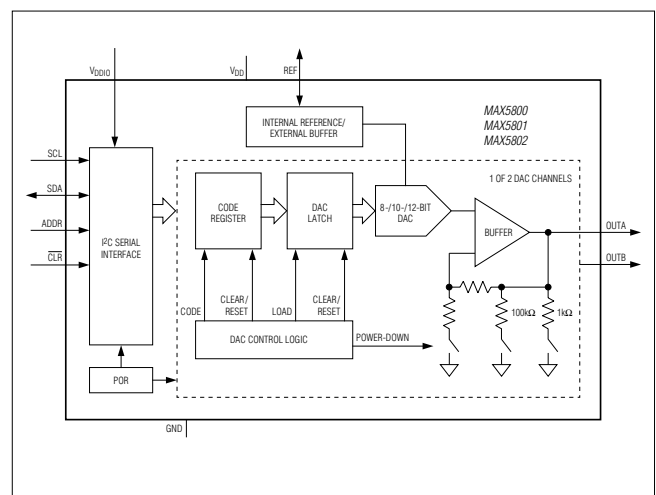
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**Ordering Information** appears at end of data sheet.

### Benefits and Features

- ◆ **Two High-Accuracy DAC Channels**
  - ◇ 12-Bit Accuracy Without Adjustment
  - ◇  $\pm 1$  LSB INL Buffered Voltage Output
  - ◇ Monotonic Over All Operating Conditions
  - ◇ Independent Mode Settings for Each DAC
- ◆ **Three Precision Selectable Internal References**
  - ◇ 2.048V, 2.500V, or 4.096V
- ◆ **Internal Output Buffer**
  - ◇ Rail-to-Rail Operation with External Reference
  - ◇ 4.5 $\mu$ s Settling Time
  - ◇ Outputs Directly Drive 2k $\Omega$  Loads
- ◆ **Small 5mm x 3mm 10-Pin  $\mu$ MAX or Ultra-Small 3mm x 3mm 10-Pin TDFN Package**
- ◆ **Wide 2.7V to 5.5V Supply Range**
- ◆ **Separate 1.8V to 5.5V V<sub>DDIO</sub> Power-Supply Input**
- ◆ **Fast 400kHz I<sup>2</sup>C-Compatible, 2-Wire Serial Interface**
- ◆ **Power-On-Reset to Zero-Scale DAC Output**
- ◆  **$\overline{\text{CLR}}$  For Asynchronous Control**
- ◆ **Three Software-Selectable Power-Down Output Impedances**
  - ◇ 1k $\Omega$ , 100k $\Omega$ , or High Impedance
- ◆ **Low 350 $\mu$ A Supply Current at 3V V<sub>DD</sub>**

### Functional Diagram



For related parts and recommended products to use with this part, refer to: [www.maximintegrated.com/MAX5800.related](http://www.maximintegrated.com/MAX5800.related)

**For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at [www.maximintegrated.com](http://www.maximintegrated.com).**

# MAX5800/MAX5801/MAX5802

## Ultra-Small, Dual-Channel, 8-/10-/12-Bit Buffered Output DACs with Internal Reference and I<sup>2</sup>C Interface

### ABSOLUTE MAXIMUM RATINGS

|   |   |   |                 |
|---|---|---|-----------------|
| V <sub>DD</sub> , V <sub>DDIO</sub> to GND .....      | -0.3V to +6V  | TDFN (derate at 24.4mW/°C above 70°C).....    | 1951mW          |
| OUT <sub>-</sub> , REF to GND .....                   | -0.3V to the lower of<br>(V <sub>DD</sub> + 0.3V) and +6V   | Maximum Continuous Current into Any Pin ..... | ±50mA           |
| SCL, SDA, $\overline{\text{CLR}}$ to GND .....        | -0.3V to +6V  | Operating Temperature Range .....             | -40°C to +125°C |
| ADDR to GND .....                                     | -0.3V to the lower of<br>(V <sub>DDIO</sub> + 0.3V) and +6V | Storage Temperature Range.....                | -65°C to +150°C |
| Continuous Power Dissipation (T <sub>A</sub> = +70°C) |   | Lead Temperature (soldering, 10s) .....       | +300°C          |
| μMAX (derate at 8.8mW/°C above 70°C).....             | 707mW   | Soldering Temperature (reflow) .....          | +260°C          |

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### PACKAGE THERMAL CHARACTERISTICS (Note 1)

|   |         |   |        |
|---|---------|---|--------|
| μMAX  |         | TDFN  |        |
| Junction-to-Ambient Thermal Resistance (θ <sub>JA</sub> ) ..... | 113°C/W | Junction-to-Ambient Thermal Resistance (θ <sub>JA</sub> ) ..... | 41°C/W |
| Junction-to-Case Thermal Resistance (θ <sub>JC</sub> ) .....    | 42°C/W  | Junction-to-Case Thermal Resistance (θ <sub>JC</sub> ) .....    | 9°C/W  |

**Note 1:** Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to [www.maximintegrated.com/thermal-tutorial](http://www.maximintegrated.com/thermal-tutorial).

### ELECTRICAL CHARACTERISTICS

(V<sub>DD</sub> = 2.7V to 5.5V, V<sub>DDIO</sub> = 1.8V to 5.5V, V<sub>GND</sub> = 0V, C<sub>L</sub> = 200pF, R<sub>L</sub> = 2kΩ, T<sub>A</sub> = -40°C to +125°C, unless otherwise noted. Typical values are at T<sub>A</sub> = +25°C.) (Note 2)

| PARAMETER                          | SYMBOL | CONDITIONS                       | MIN   | TYP   | MAX   | UNITS        |
|------------------------------------|--------|----------------------------------|-------|-------|-------|--------------|
| <b>DC PERFORMANCE (Note 3)</b>     |        |                                  |       |       |       |              |
| Resolution and Monotonicity        | N      | MAX5800                          | 8     |       |       | Bits         |
|                                    |        | MAX5801                          | 10    |       |       |              |
|                                    |        | MAX5802                          | 12    |       |       |              |
| Integral Nonlinearity (Note 4)     | INL    | MAX5800                          | -0.25 | ±0.05 | +0.25 | LSB          |
|                                    |        | MAX5801                          | -0.5  | ±0.25 | +0.5  |              |
|                                    |        | MAX5802                          | -1    | ±0.5  | +1    |              |
| Differential Nonlinearity (Note 4) | DNL    | MAX5800                          | -0.25 | ±0.05 | +0.25 | LSB          |
|                                    |        | MAX5801                          | -0.5  | ±0.1  | +0.5  |              |
|                                    |        | MAX5802                          | -1    | ±0.2  | +1    |              |
| Offset Error (Note 5)              | OE     |                                  | -5    | ±0.5  | +5    | mV           |
| Offset Error Drift                 |        |                                  |       | ±10   |       | μV/°C        |
| Gain Error (Note 5)                | GE     |                                  | -1.0  | ±0.1  | +1.0  | %FS          |
| Gain Temperature Coefficient       |        | With respect to V <sub>REF</sub> |       | ±3.0  |       | ppm of FS/°C |
| Zero-Scale Error                   |        |                                  | 0     |       | 10    | mV           |
| Full-Scale Error                   |        | With respect to V <sub>REF</sub> | -0.5  |       | +0.5  | %FS          |

# MAX5800/MAX5801/MAX5802

## Ultra-Small, Dual-Channel, 8-/10-/12-Bit Buffered Output DACs with Internal Reference and I<sup>2</sup>C Interface

### ELECTRICAL CHARACTERISTICS (continued)

(V<sub>DD</sub> = 2.7V to 5.5V, V<sub>DDIO</sub> = 1.8V to 5.5V, V<sub>GND</sub> = 0V, C<sub>L</sub> = 200pF, R<sub>L</sub> = 2kΩ, T<sub>A</sub> = -40°C to +125°C, unless otherwise noted. Typical values are at T<sub>A</sub> = +25°C.) (Note 2)

| PARAMETER                               | SYMBOL         | CONDITIONS  | MIN  | TYP | MAX                   | UNITS |
|---|----------------|---|--|-----|-----------------------|-------|
| <b>DAC OUTPUT CHARACTERISTICS</b>       |                |   |  |     |                       |       |
| Output Voltage Range (Note 6)           |                | No load   | 0  |     | V <sub>DD</sub>       | V     |
|   |                | 2kΩ load to GND   | 0  |     | V <sub>DD</sub> - 0.2 |       |
|   |                | 2kΩ load to V <sub>DD</sub>                               | 0.2  |     | V <sub>DD</sub>       |       |
| Load Regulation                         |                | V <sub>OUT</sub> = V <sub>FS</sub> /2                     | V <sub>DD</sub> = 3V ±10%,<br> I <sub>OUT</sub>   ≤ 5mA  | 300 |                       | μV/mA |
|   |                |   | V <sub>DD</sub> = 5V ±10%,<br> I <sub>OUT</sub>   ≤ 10mA | 300 |                       |       |
| DC Output Impedance                     |                | V <sub>OUT</sub> = V <sub>FS</sub> /2                     | V <sub>DD</sub> = 3V ±10%,<br> I <sub>OUT</sub>   ≤ 5mA  | 0.3 |                       | Ω     |
|   |                |   | V <sub>DD</sub> = 5V ±10%,<br> I <sub>OUT</sub>   ≤ 10mA | 0.3 |                       |       |
| Maximum Capacitive Load Handling        | C <sub>L</sub> |   |  | 500 |                       | pF    |
| Resistive Load Handling                 | R <sub>L</sub> |   | 2  |     |                       | kΩ    |
| Short-Circuit Output Current            |                | V <sub>DD</sub> = 5.5V                                    | Sourcing (output shorted to GND)                         | 30  |                       | mA    |
|   |                |   | Sinking (output shorted to V <sub>DD</sub> )             | 50  |                       |       |
| DC Power-Supply Rejection               |                | V <sub>DD</sub> = 3V ±10% or 5V ±10%                      |  | 100 |                       | μV/V  |
| <b>DYNAMIC PERFORMANCE</b>              |                |   |  |     |                       |       |
| Voltage-Output Slew Rate                | SR             | Positive and negative                                     |  | 1.0 |                       | V/μs  |
| Voltage-Output Settling Time            |                | ¼ scale to ¾ scale, to ≤ 1 LSB, MAX5800                   |  | 2.2 |                       | μs    |
|   |                | ¼ scale to ¾ scale, to ≤ 1 LSB, MAX5801                   |  | 2.6 |                       |       |
|   |                | ¼ scale to ¾ scale, to ≤ 1 LSB, MAX5802                   |  | 4.5 |                       |       |
| DAC Glitch Impulse                      |                | Major code transition                                     |  | 7   |                       | nV*s  |
| Channel-to-Channel Feedthrough (Note 7) |                | External reference  |  | 3.5 |                       | nV*s  |
|   |                | Internal reference  |  | 3.3 |                       |       |
| Digital Feedthrough                     |                | Code = 0, all digital inputs from 0V to V <sub>DDIO</sub> |  | 0.2 |                       | nV*s  |
| Power-Up Time                           |                | Startup calibration time (Note 8)                         |  | 200 |                       | μs    |
|   |                | From power-down   |  | 50  |                       | μs    |

# MAX5800/MAX5801/MAX5802

## Ultra-Small, Dual-Channel, 8-/10-/12-Bit Buffered Output DACs with Internal Reference and I<sup>2</sup>C Interface

### ELECTRICAL CHARACTERISTICS (continued)

(V<sub>DD</sub> = 2.7V to 5.5V, V<sub>DDIO</sub> = 1.8V to 5.5V, V<sub>GND</sub> = 0V, C<sub>L</sub> = 200pF, R<sub>L</sub> = 2kΩ, T<sub>A</sub> = -40°C to +125°C, unless otherwise noted. Typical values are at T<sub>A</sub> = +25°C.) (Note 2)

| PARAMETER  | SYMBOL | CONDITIONS                |                     | MIN | TYP | MAX | UNITS             |
|--|--------|---------------------------|---------------------|-----|-----|-----|-------------------|
| Output Voltage-Noise Density<br>(DAC Output at Midscale)   |        | External reference        | f = 1kHz            |     | 90  |     | nV/√Hz            |
|  |        |                           | f = 10kHz           |     | 82  |     |                   |
|  |        | 2.048V internal reference | f = 1kHz            |     | 112 |     |                   |
|  |        |                           | f = 10kHz           |     | 102 |     |                   |
|  |        | 2.5V internal reference   | f = 1kHz            |     | 125 |     |                   |
|  |        |                           | f = 10kHz           |     | 110 |     |                   |
|  |        | 4.096V internal reference | f = 1kHz            |     | 160 |     |                   |
|  |        |                           | f = 10kHz           |     | 145 |     |                   |
| Integrated Output Noise<br>(DAC Output at Midscale)        |        | External reference        | f = 0.1Hz to 10Hz   |     | 12  |     | μV <sub>P-P</sub> |
|  |        |                           | f = 0.1Hz to 10kHz  |     | 76  |     |                   |
|  |        |                           | f = 0.1Hz to 300kHz |     | 385 |     |                   |
|  |        | 2.048V internal reference | f = 0.1Hz to 10Hz   |     | 14  |     |                   |
|  |        |                           | f = 0.1Hz to 10kHz  |     | 91  |     |                   |
|  |        |                           | f = 0.1Hz to 300kHz |     | 450 |     |                   |
|  |        | 2.5V internal reference   | f = 0.1Hz to 10Hz   |     | 15  |     |                   |
|  |        |                           | f = 0.1Hz to 10kHz  |     | 99  |     |                   |
|  |        |                           | f = 0.1Hz to 300kHz |     | 470 |     |                   |
|  |        | 4.096V internal reference | f = 0.1Hz to 10Hz   |     | 16  |     |                   |
|  |        |                           | f = 0.1Hz to 10kHz  |     | 124 |     |                   |
|  |        |                           | f = 0.1Hz to 300kHz |     | 490 |     |                   |
| Output Voltage-Noise Density<br>(DAC Output at Full Scale) |        | External reference        | f = 1kHz            |     | 114 |     | nV/√Hz            |
|  |        |                           | f = 10kHz           |     | 99  |     |                   |
|  |        | 2.048V internal reference | f = 1kHz            |     | 175 |     |                   |
|  |        |                           | f = 10kHz           |     | 153 |     |                   |
|  |        | 2.5V internal reference   | f = 1kHz            |     | 200 |     |                   |
|  |        |                           | f = 10kHz           |     | 174 |     |                   |
|  |        | 4.096V internal reference | f = 1kHz            |     | 295 |     |                   |
|  |        |                           | f = 10kHz           |     | 255 |     |                   |
| Integrated Output Noise<br>(DAC Output at Full Scale)      |        | External reference        | f = 0.1Hz to 10Hz   |     | 13  |     | μV <sub>P-P</sub> |
|  |        |                           | f = 0.1Hz to 10kHz  |     | 94  |     |                   |
|  |        |                           | f = 0.1Hz to 300kHz |     | 540 |     |                   |
|  |        | 2.048V internal reference | f = 0.1Hz to 10Hz   |     | 19  |     |                   |
|  |        |                           | f = 0.1Hz to 10kHz  |     | 143 |     |                   |
|  |        |                           | f = 0.1Hz to 300kHz |     | 685 |     |                   |
|  |        | 2.5V internal reference   | f = 0.1Hz to 10Hz   |     | 21  |     |                   |
|  |        |                           | f = 0.1Hz to 10kHz  |     | 159 |     |                   |
|  |        |                           | f = 0.1Hz to 300kHz |     | 705 |     |                   |
|  |        | 4.096V internal reference | f = 0.1Hz to 10Hz   |     | 26  |     |                   |
|  |        |                           | f = 0.1Hz to 10kHz  |     | 213 |     |                   |
|  |        |                           | f = 0.1Hz to 300kHz |     | 750 |     |                   |

# MAX5800/MAX5801/MAX5802

## Ultra-Small, Dual-Channel, 8-/10-/12-Bit Buffered Output DACs with Internal Reference and I<sup>2</sup>C Interface

### ELECTRICAL CHARACTERISTICS (continued)

(V<sub>DD</sub> = 2.7V to 5.5V, V<sub>DDIO</sub> = 1.8V to 5.5V, V<sub>GND</sub> = 0V, C<sub>L</sub> = 200pF, R<sub>L</sub> = 2kΩ, T<sub>A</sub> = -40°C to +125°C, unless otherwise noted. Typical values are at T<sub>A</sub> = +25°C.) (Note 2)

| PARAMETER                                  | SYMBOL            | CONDITIONS  | MIN                 | TYP   | MAX             | UNITS             |
|--|-------------------|---|---------------------|-------|-----------------|-------------------|
| <b>REFERENCE INPUT</b>                     |                   |   |                     |       |                 |                   |
| Reference Input Range                      | V <sub>REF</sub>  |   | 1.24                |       | V <sub>DD</sub> | V                 |
| Reference Input Current                    | I <sub>REF</sub>  | V <sub>REF</sub> = V <sub>DD</sub> = 5.5V         |                     | 55    | 74              | μA                |
| Reference Input Impedance                  | R <sub>REF</sub>  |   | 75                  | 100   |                 | kΩ                |
| <b>REFERENCE OUTPUT</b>                    |                   |   |                     |       |                 |                   |
| Reference Output Voltage                   | V <sub>REF</sub>  | V <sub>REF</sub> = 2.048V, T <sub>A</sub> = +25°C | 2.043               | 2.048 | 2.053           | V                 |
|  |                   | V <sub>REF</sub> = 2.5V, T <sub>A</sub> = +25°C   | 2.494               | 2.5   | 2.506           |                   |
|  |                   | V <sub>REF</sub> = 4.096V, T <sub>A</sub> = +25°C | 4.086               | 4.096 | 4.106           |                   |
| Reference Output Noise Density             | V <sub>REF</sub>  | V <sub>REF</sub> = 2.048V                         | f = 1kHz            | 129   |                 | nV/√Hz            |
|  |                   |   | f = 10kHz           | 122   |                 |                   |
|  |                   | V <sub>REF</sub> = 2.500V                         | f = 1kHz            | 158   |                 |                   |
|  |                   |   | f = 10kHz           | 151   |                 |                   |
|  |                   | V <sub>REF</sub> = 4.096V                         | f = 1kHz            | 254   |                 |                   |
|  |                   |   | f = 10kHz           | 237   |                 |                   |
| Integrated Reference Output Noise          | V <sub>REF</sub>  | V <sub>REF</sub> = 2.048V                         | f = 0.1Hz to 10Hz   | 12    |                 | μV <sub>P-P</sub> |
|  |                   |   | f = 0.1Hz to 10kHz  | 110   |                 |                   |
|  |                   |   | f = 0.1Hz to 300kHz | 390   |                 |                   |
|  |                   | V <sub>REF</sub> = 2.500V                         | f = 0.1Hz to 10Hz   | 15    |                 |                   |
|  |                   |   | f = 0.1Hz to 10kHz  | 129   |                 |                   |
|  |                   |   | f = 0.1Hz to 300kHz | 430   |                 |                   |
|  |                   | V <sub>REF</sub> = 4.096V                         | f = 0.1Hz to 10Hz   | 20    |                 |                   |
|  |                   |   | f = 0.1Hz to 10kHz  | 205   |                 |                   |
|  |                   |   | f = 0.1Hz to 300kHz | 525   |                 |                   |
| Reference Temperature Coefficient (Note 9) |                   | MAX5802A  |                     | ±3.7  | ±10             | ppm/°C            |
|  |                   | MAX5800/MAX5801/MAX5802B                          |                     | ±10   | ±25             |                   |
| Reference Drive Capacity                   |                   | External load                                     |                     | 25    |                 | kΩ                |
| Reference Capacitive Load                  |                   |   |                     | 200   |                 | pF                |
| Reference Load Regulation                  |                   | I <sub>SOURCE</sub> = 0 to 500μA                  |                     | 2     |                 | mV/mA             |
| Reference Line Regulation                  |                   |   |                     | 0.05  |                 | mV/V              |
| <b>POWER REQUIREMENTS</b>                  |                   |   |                     |       |                 |                   |
| Supply Voltage                             | V <sub>DD</sub>   | V <sub>REF</sub> = 4.096V                         | 4.5                 |       | 5.5             | V                 |
|  |                   | All other options                                 | 2.7                 |       | 5.5             |                   |
| I/O Supply Voltage                         | V <sub>DDIO</sub> |   | 1.8                 |       | 5.5             | V                 |
| Interface Supply Current (Note 10)         | I <sub>DDIO</sub> |   |                     |       | 1               | μA                |

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## Ultra-Small, Dual-Channel, 8-/10-/12-Bit Buffered Output DACs with Internal Reference and I<sup>2</sup>C Interface

### ELECTRICAL CHARACTERISTICS (continued)

(V<sub>DD</sub> = 2.7V to 5.5V, V<sub>DDIO</sub> = 1.8V to 5.5V, V<sub>GND</sub> = 0V, C<sub>L</sub> = 200pF, R<sub>L</sub> = 2kΩ, T<sub>A</sub> = -40°C to +125°C, unless otherwise noted. Typical values are at T<sub>A</sub> = +25°C.) (Note 2)

| PARAMETER  | SYMBOL                            | CONDITIONS   | MIN                       | TYP  | MAX   | UNITS |
|--|-----------------------------------|--|---------------------------|------|-------|-------|
| Supply Current (Note 10)                                     | I <sub>DD</sub>                   | Internal reference   | V <sub>REF</sub> = 2.048V | 0.55 | 0.75  | mA    |
|  |                                   |  | V <sub>REF</sub> = 2.5V   | 0.60 | 0.80  |       |
|  |                                   |  | V <sub>REF</sub> = 4.096V | 0.65 | 0.90  |       |
|  |                                   | External reference   | V <sub>REF</sub> = 3V     | 0.40 | 0.60  |       |
|  |                                   |  | V <sub>REF</sub> = 5V     | 0.55 | 0.75  |       |
| Power-Down Mode Supply Current                               | I <sub>PD</sub>                   | Both DACs off, internal reference ON                                   | 140                       |      |       | μA    |
|  |                                   | Both DACs off, internal reference OFF, T <sub>A</sub> = -40°C to +85°C | 0.5                       | 1    |       |       |
|  |                                   | Both DACs off, internal reference OFF, T <sub>A</sub> = +125°C         | 1.2                       | 2.5  |       |       |
| <b>DIGITAL INPUT CHARACTERISTICS (SCL, SDA, ADDR, CLR)</b>   |                                   |  |                           |      |       |       |
| Input High Voltage   | V <sub>IH</sub>                   | 2.2V < V <sub>DDIO</sub> < 5.5V  | 0.7 x                     |      |       | V     |
|  |                                   | 1.8V < V <sub>DDIO</sub> < 2.2V  | 0.8 x                     |      |       | V     |
| Input Low Voltage  | V <sub>IL</sub>                   | 2.2V < V <sub>DDIO</sub> < 5.5V  |                           |      | 0.3 x | V     |
|  |                                   | 1.8V < V <sub>DDIO</sub> < 2.2V  |                           |      | 0.2 x |       |
| Hysteresis Voltage   | V <sub>H</sub>                    |  | 0.15                      |      |       | V     |
| Input Leakage Current  | I <sub>IN</sub>                   | V <sub>IN</sub> = 0V or V <sub>DDIO</sub> (Note 10)                    |                           | ±0.1 | ±1    | μA    |
| Input Capacitance (Note 10)                                  | C <sub>IN</sub>                   |  |                           |      | 10    | pF    |
| ADDR Pullup/Pulldown Strength                                | R <sub>PU</sub> , R <sub>PD</sub> | (Note 11)  | 30                        | 50   | 90    | kΩ    |
| <b>DIGITAL OUTPUT (SDA)</b>                                  |                                   |  |                           |      |       |       |
| Output Low Voltage   | V <sub>OL</sub>                   | I <sub>SINK</sub> = 3mA  |                           |      | 0.2   | V     |
| <b>I<sup>2</sup>C TIMING CHARACTERISTICS (SCL, SDA, CLR)</b> |                                   |  |                           |      |       |       |
| SCL Clock Frequency  | f <sub>SCL</sub>                  |  |                           |      | 400   | kHz   |
| Bus Free Time Between a STOP and a START Condition           | t <sub>BUF</sub>                  |  | 1.3                       |      |       | μs    |
| Hold Time Repeated for a START Condition                     | t <sub>HD;STA</sub>               |  | 0.6                       |      |       | μs    |
| SCL Pulse Width Low  | t <sub>LOW</sub>                  |  | 1.3                       |      |       | μs    |
| SCL Pulse Width High   | t <sub>HIGH</sub>                 |  | 0.6                       |      |       | μs    |
| Setup Time for Repeated START Condition                      | t <sub>SU;STA</sub>               |  | 0.6                       |      |       | μs    |
| Data Hold Time   | t <sub>HD;DAT</sub>               |  | 0                         |      | 900   | ns    |
| Data Setup Time  | t <sub>SU;DAT</sub>               |  | 100                       |      |       | ns    |

# MAX5800/MAX5801/MAX5802

## Ultra-Small, Dual-Channel, 8-/10-/12-Bit Buffered Output DACs with Internal Reference and I<sup>2</sup>C Interface

### ELECTRICAL CHARACTERISTICS (continued)

( $V_{DD} = 2.7V$  to  $5.5V$ ,  $V_{DDIO} = 1.8V$  to  $5.5V$ ,  $V_{GND} = 0V$ ,  $C_L = 200pF$ ,  $R_L = 2k\Omega$ ,  $T_A = -40^\circ C$  to  $+125^\circ C$ , unless otherwise noted. Typical values are at  $T_A = +25^\circ C$ .) (Note 2)

| PARAMETER   | SYMBOL       | CONDITIONS                | MIN           | TYP | MAX | UNITS   |
|---|--------------|---------------------------|---------------|-----|-----|---------|
| SDA and SCL Receiving Rise Time                           | $t_r$        |                           | $20 + C_B/10$ |     | 300 | ns      |
| SDA and SCL Receiving Fall Time                           | $t_f$        |                           | $20 + C_B/10$ |     | 300 | ns      |
| SDA Transmitting Fall Time                                | $t_f$        |                           | $20 + C_B/10$ |     | 250 | ns      |
| Setup Time for STOP Condition                             | $t_{SU;STO}$ |                           | 0.6           |     |     | $\mu s$ |
| Bus Capacitance Allowed                                   | $C_B$        | $V_{DD} = 2.7V$ to $5.5V$ | 10            |     | 400 | $\mu F$ |
| Pulse Width of Suppressed Spike                           | $t_{sp}$     |                           |               | 50  |     | ns      |
| $\overline{CLR}$ Removal Time Prior to a Recognized START | $t_{CLRSTA}$ |                           | 100           |     |     | ns      |
| $\overline{CLR}$ Pulse Width Low                          | $t_{CLPW}$   |                           | 20            |     |     | ns      |

**Note 2:** Electrical specifications are production tested at  $T_A = +25^\circ C$ . Specifications over the entire operating temperature range are guaranteed by design and characterization. Typical specifications are at  $T_A = +25^\circ C$  and are not guaranteed.

**Note 3:** DC Performance is tested without load.

**Note 4:** Linearity is tested with unloaded outputs to within 20mV of GND and  $V_{DD}$ .

**Note 5:** Gain and offset calculated from measurements made with  $V_{REF} = V_{DD}$  at codes 30 and 4065 for MAX5802, codes 8 and 1016 for MAX5801, and codes 2 and 254 for MAX5800.

**Note 6:** Subject to zero and full-scale error limits and  $V_{REF}$  settings.

**Note 7:** Measured with the DAC outputs at midscale with one channel transitioning 0 to full scale.

**Note 8:** On power-up, the device initiates an internal 200 $\mu s$  (typ) calibration sequence. All commands issued during this time will be ignored.

**Note 9:** Guaranteed by design.

**Note 10:** Both channels active at  $V_{FS}$ , unloaded. Static logic inputs with  $V_{IL} = V_{GND}$  and  $V_{IH} = V_{DDIO}$ .

**Note 11:** An unconnected condition on the ADDR pin is sensed via a resistive pullup and pulldown operation; for proper operation, the ADDR pin should be tied to  $V_{DDIO}$ , GND, or left unconnected with minimal capacitance.

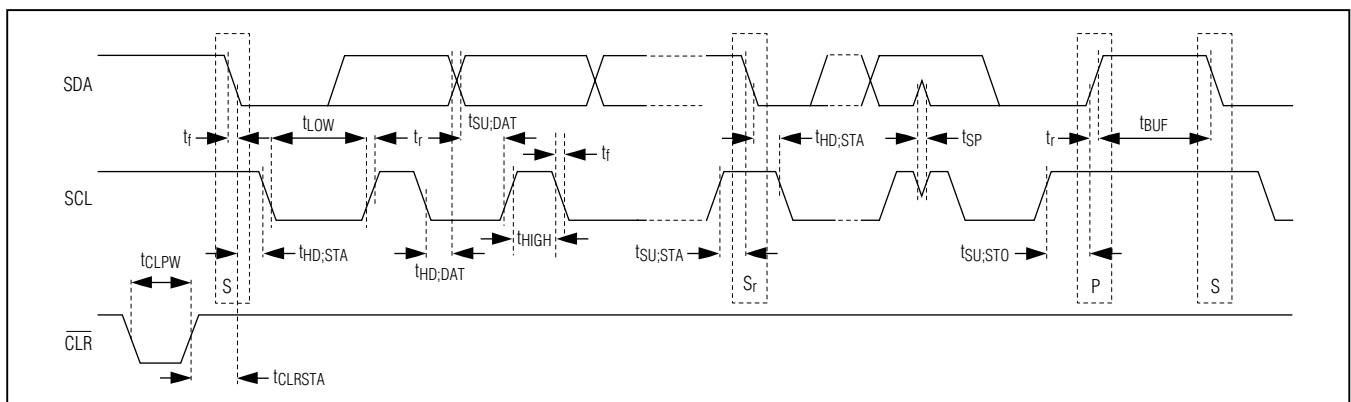


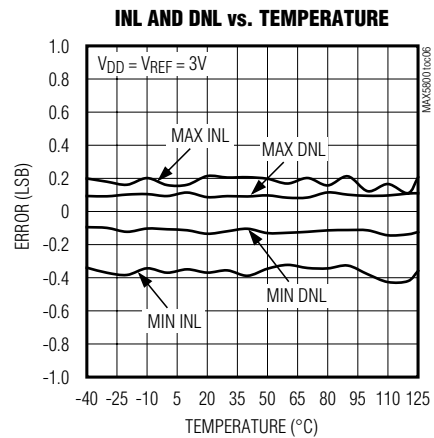
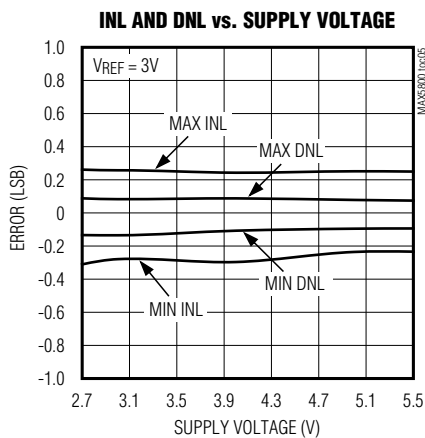
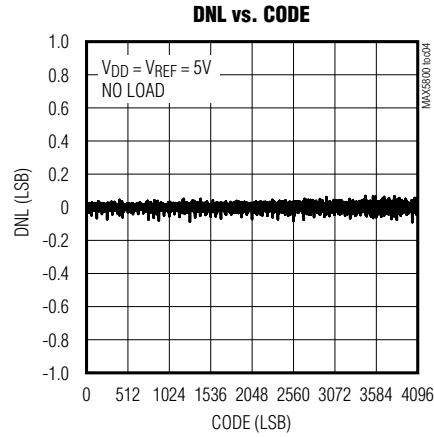
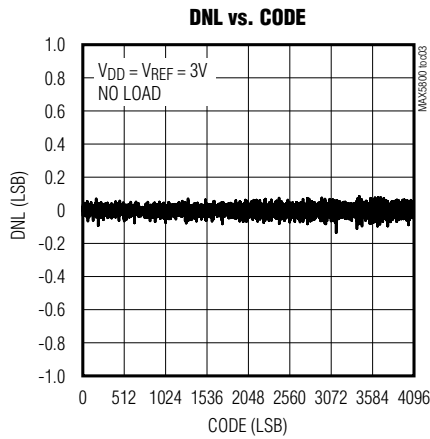
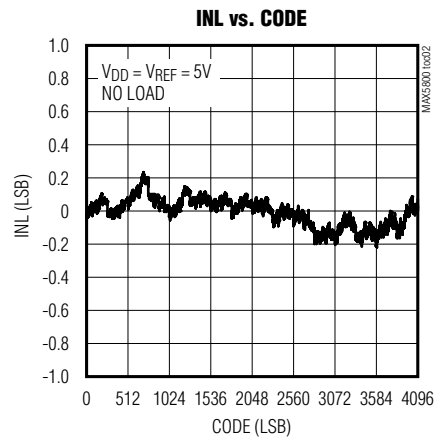
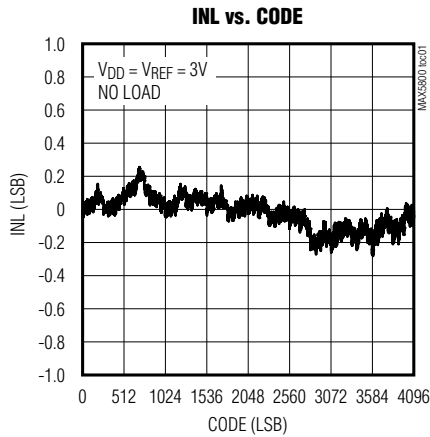
Figure 1. I<sup>2</sup>C Serial Interface Timing Diagram

# MAX5800/MAX5801/MAX5802

## Ultra-Small, Dual-Channel, 8-/10-/12-Bit Buffered Output DACs with Internal Reference and I<sup>2</sup>C Interface

### Typical Operating Characteristics

(MAX5802, 12-bit performance,  $T_A = +25^\circ\text{C}$ , unless otherwise noted.)



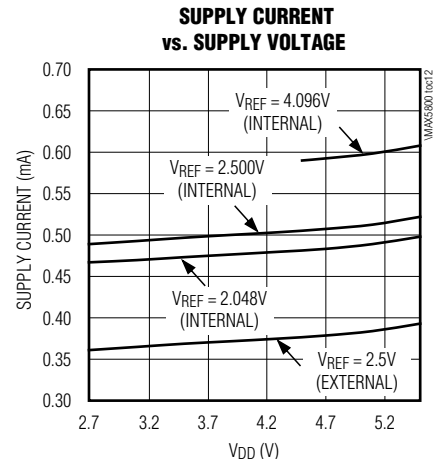
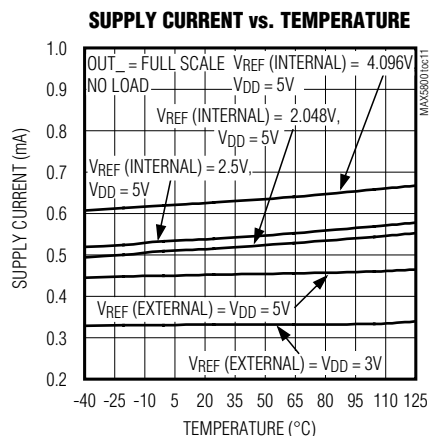
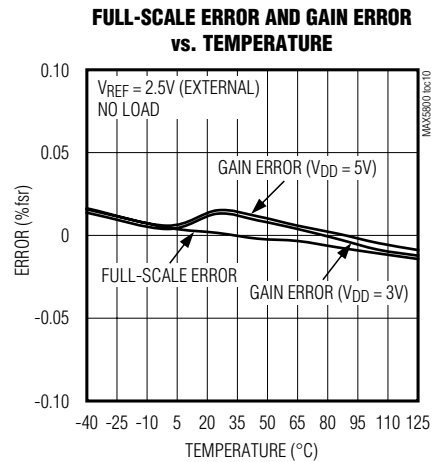
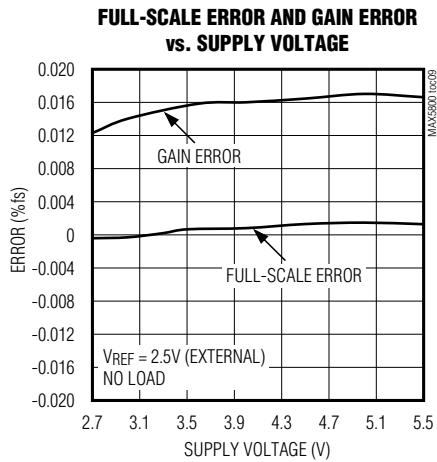
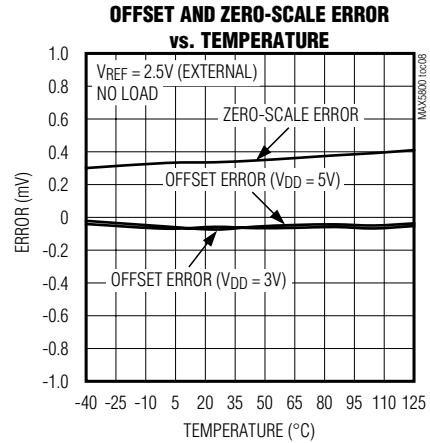
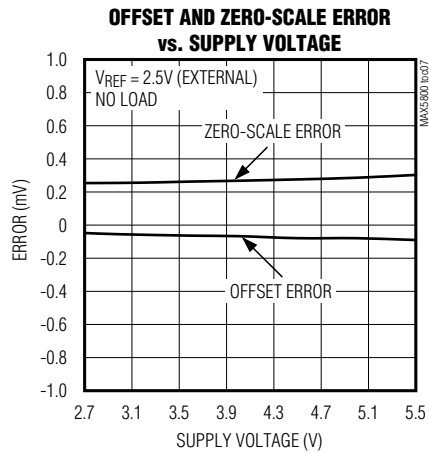


# MAX5800/MAX5801/MAX5802

## Ultra-Small, Dual-Channel, 8-/10-/12-Bit Buffered Output DACs with Internal Reference and I<sup>2</sup>C Interface

### Typical Operating Characteristics (continued)

(MAX5802, 12-bit performance,  $T_A = +25^\circ\text{C}$ , unless otherwise noted.)



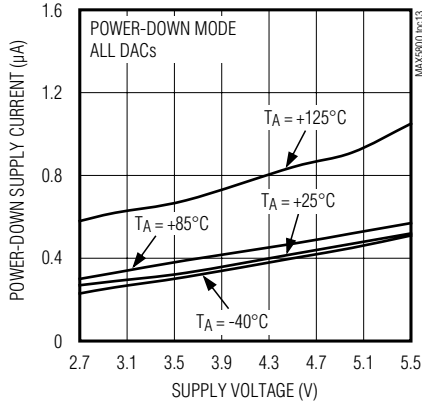
# MAX5800/MAX5801/MAX5802

## Ultra-Small, Dual-Channel, 8-/10-/12-Bit Buffered Output DACs with Internal Reference and I<sup>2</sup>C Interface

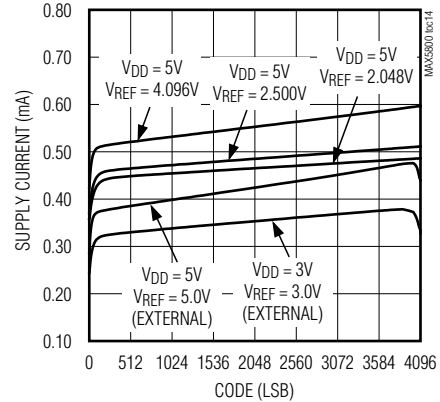
### Typical Operating Characteristics (continued)

(MAX5802, 12-bit performance, T<sub>A</sub> = +25°C, unless otherwise noted.)

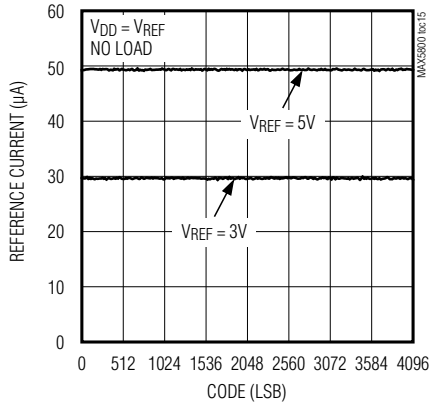
**POWER-DOWN MODE SUPPLY CURRENT vs. TEMPERATURE**



**SUPPLY CURRENT vs. CODE**

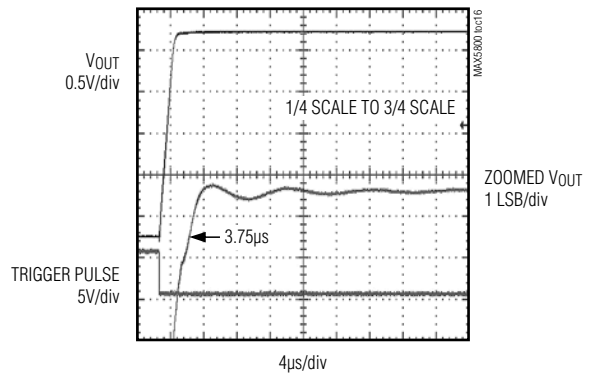


**I<sub>REF</sub> (EXTERNAL) vs. CODE**



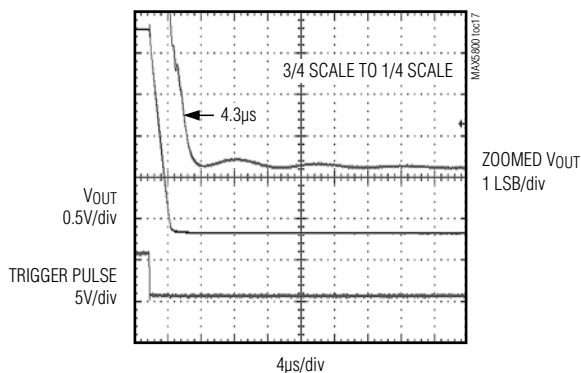
**SETTLING TO ±1 LSB**

(V<sub>DD</sub> = V<sub>REF</sub> = 5V, R<sub>L</sub> = 2kΩ, C<sub>L</sub> = 200pF)



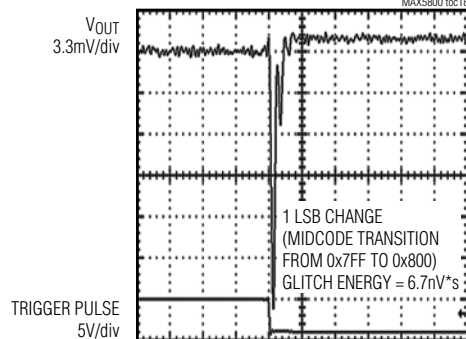
**SETTLING TO ±1 LSB**

(V<sub>DD</sub> = V<sub>REF</sub> = 5V, R<sub>L</sub> = 2kΩ, C<sub>L</sub> = 200pF)



**MAJOR CODE TRANSITION GLITCH ENERGY**

(V<sub>DD</sub> = V<sub>REF</sub> = 5V, R<sub>L</sub> = 2kΩ, C<sub>L</sub> = 200pF)



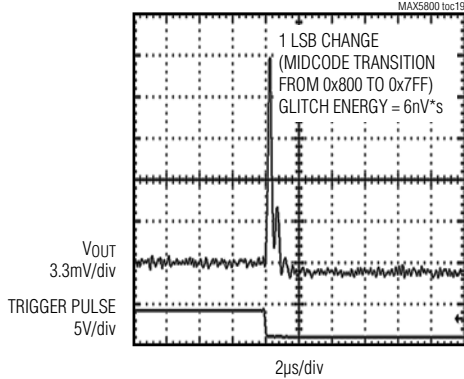
# MAX5800/MAX5801/MAX5802

## Ultra-Small, Dual-Channel, 8-/10-/12-Bit Buffered Output DACs with Internal Reference and I<sup>2</sup>C Interface

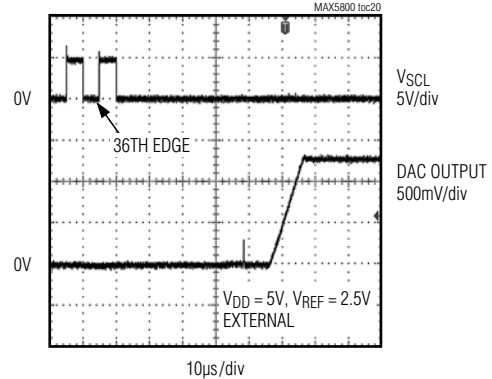
### Typical Operating Characteristics (continued)

(MAX5802, 12-bit performance,  $T_A = +25^\circ\text{C}$ , unless otherwise noted.)

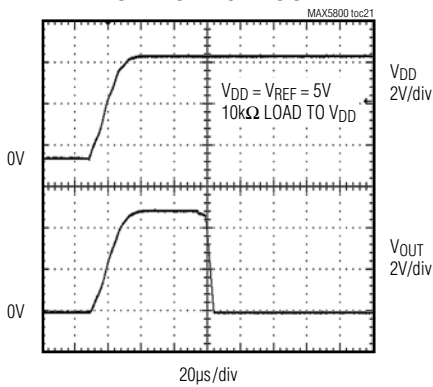
**MAJOR CODE TRANSITION GLITCH ENERGY**  
( $V_{DD} = V_{REF} = 5\text{V}$ ,  $R_L = 2\text{k}\Omega$ ,  $C_L = 200\text{pF}$ )



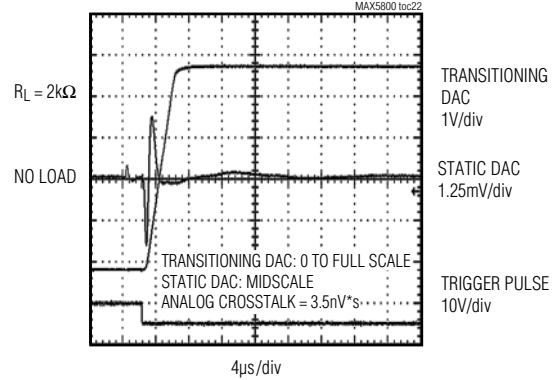
**V<sub>OUT</sub> vs. TIME TRANSIENT EXITING POWER-DOWN**



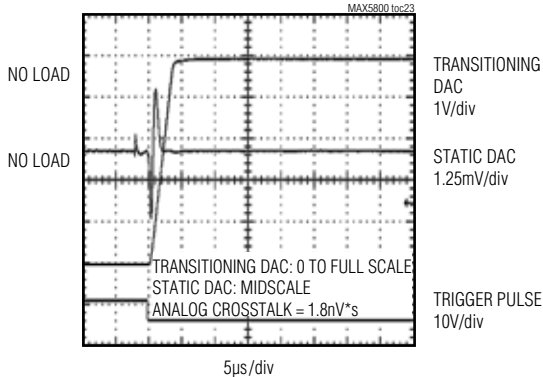
**POWER-ON RESET TO 0V**



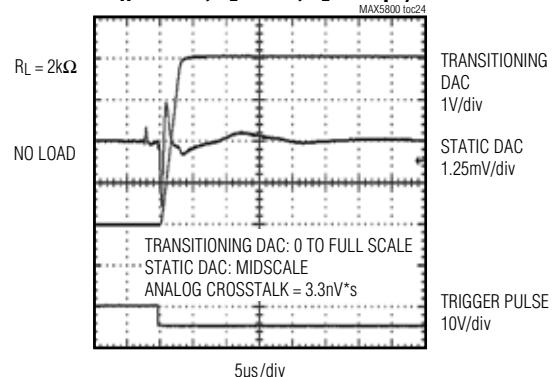
**CHANNEL-TO-CHANNEL FEEDTHROUGH**  
( $V_{DD} = V_{REF} = 5\text{V}$ ,  $T_A = +25^\circ\text{C}$ ,  $R_L = 2\text{k}\Omega$ ,  $C_L = 200\text{pF}$ )



**CHANNEL-TO-CHANNEL FEEDTHROUGH**  
( $V_{DD} = V_{REF} = 5\text{V}$ ,  $T_A = +25^\circ\text{C}$ , NO LOAD)



**CHANNEL-TO-CHANNEL FEEDTHROUGH**  
( $V_{DD} = 5\text{V}$ ,  $V_{REF} = 4.096\text{V}$  (INTERNAL),  $T_A = +25^\circ\text{C}$ ,  $R_L = 2\text{k}\Omega$ ,  $C_L = 200\text{pF}$ )



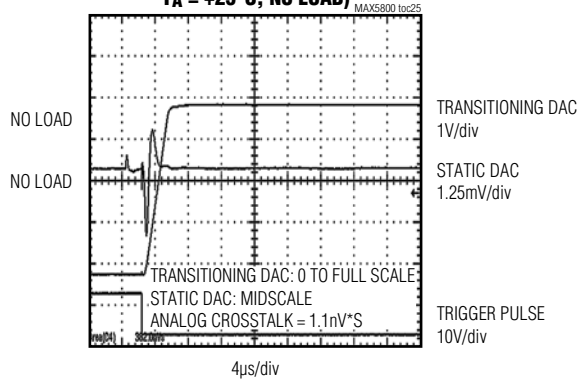
# MAX5800/MAX5801/MAX5802

## Ultra-Small, Dual-Channel, 8-/10-/12-Bit Buffered Output DACs with Internal Reference and I<sup>2</sup>C Interface

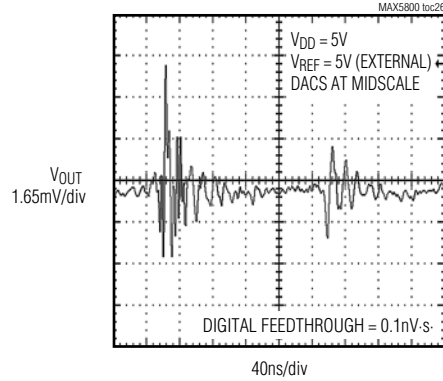
### Typical Operating Characteristics (continued)

(MAX5802, 12-bit performance,  $T_A = +25^\circ\text{C}$ , unless otherwise noted.)

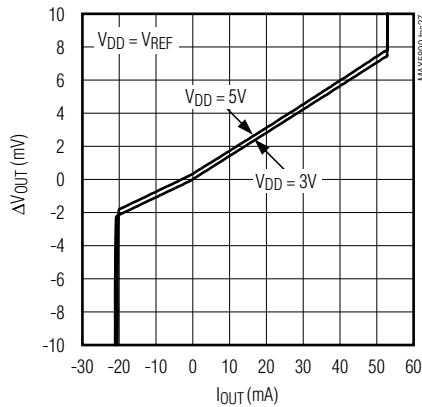
**CHANNEL-TO-CHANNEL FEEDTHROUGH**  
( $V_{DD} = 5\text{V}$ ,  $V_{REF} = 4.096\text{V}$  (INTERNAL),  
 $T_A = +25^\circ\text{C}$ , NO LOAD)



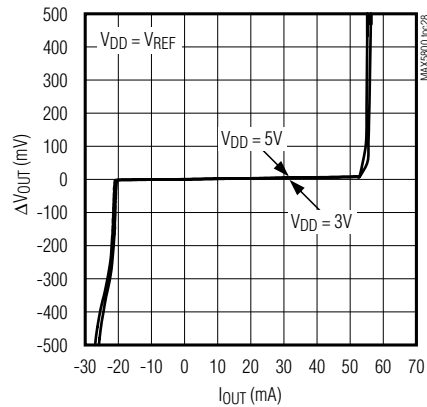
**DIGITAL FEEDTHROUGH**  
( $V_{DD} = V_{REF} = 5\text{V}$ ,  $R_L = 2\text{k}\Omega$ ,  $C_L = 200\text{pF}$ )



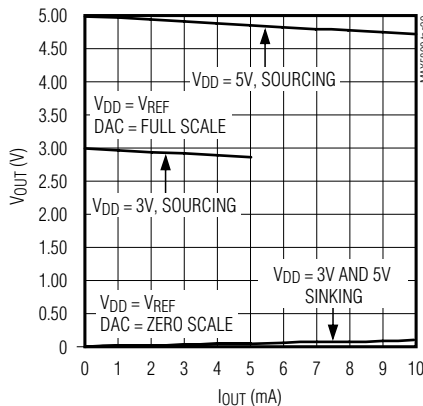
**OUTPUT LOAD REGULATION**



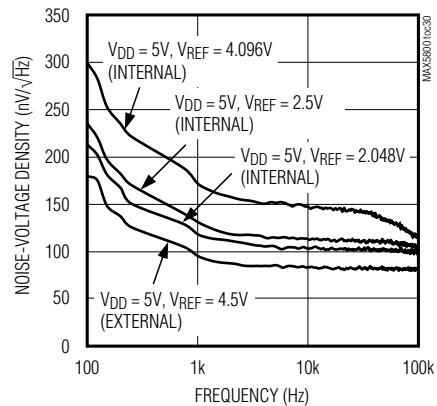
**OUTPUT CURRENT LIMITING**



**HEADROOM AT RAILS vs. OUTPUT CURRENT**



**NOISE-VOLTAGE DENSITY vs. FREQUENCY (DAC AT MIDSACLE)**



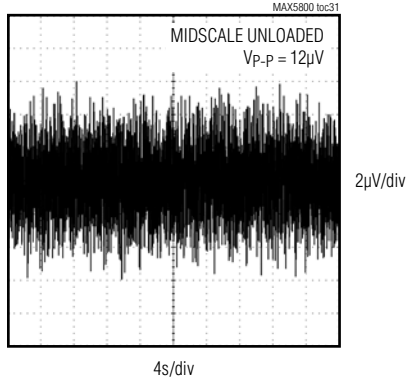
# MAX5800/MAX5801/MAX5802

## Ultra-Small, Dual-Channel, 8-/10-/12-Bit Buffered Output DACs with Internal Reference and I<sup>2</sup>C Interface

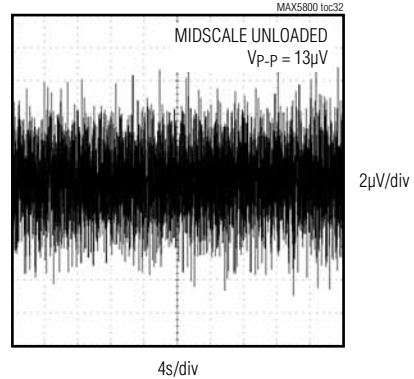
### Typical Operating Characteristics (continued)

(MAX5802, 12-bit performance,  $T_A = +25^\circ\text{C}$ , unless otherwise noted.)

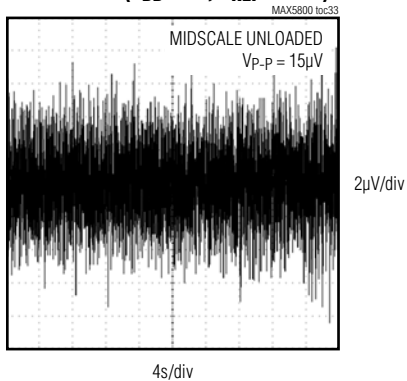
**0.1Hz TO 10Hz OUTPUT NOISE, EXTERNAL REFERENCE ( $V_{DD} = 5\text{V}$ ,  $V_{REF} = 4.5\text{V}$ )**



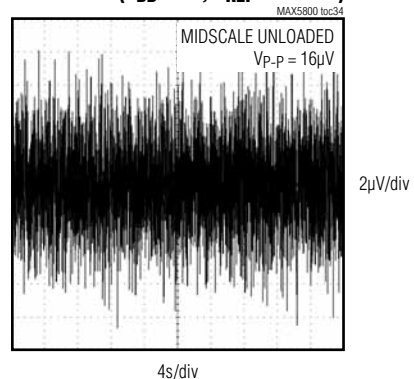
**0.1Hz TO 10Hz OUTPUT NOISE, INTERNAL REFERENCE ( $V_{DD} = 5\text{V}$ ,  $V_{REF} = 2.048\text{V}$ )**



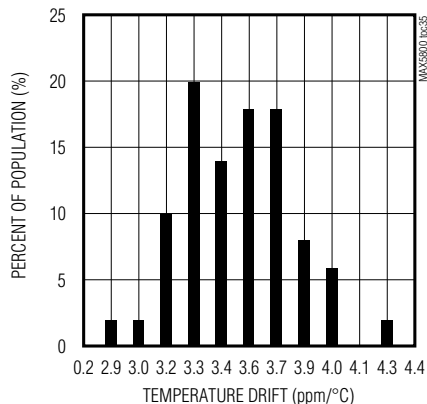
**0.1Hz TO 10Hz OUTPUT NOISE, INTERNAL REFERENCE ( $V_{DD} = 5\text{V}$ ,  $V_{REF} = 2.5\text{V}$ )**



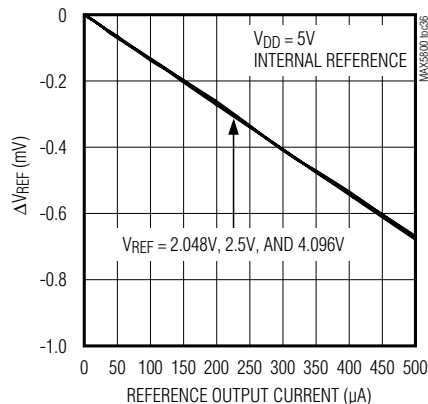
**0.1Hz TO 10Hz OUTPUT NOISE, INTERNAL REFERENCE ( $V_{DD} = 5\text{V}$ ,  $V_{REF} = 4.096\text{V}$ )**



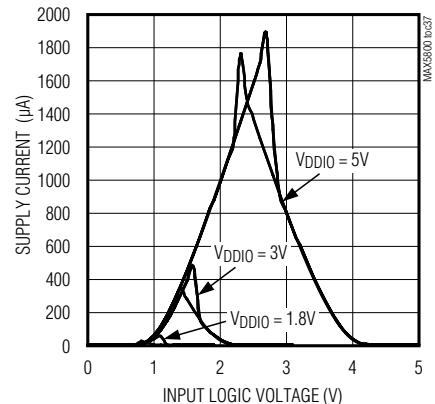
**V<sub>REF</sub> DRIFT vs. TEMPERATURE**



**REFERENCE LOAD REGULATION**



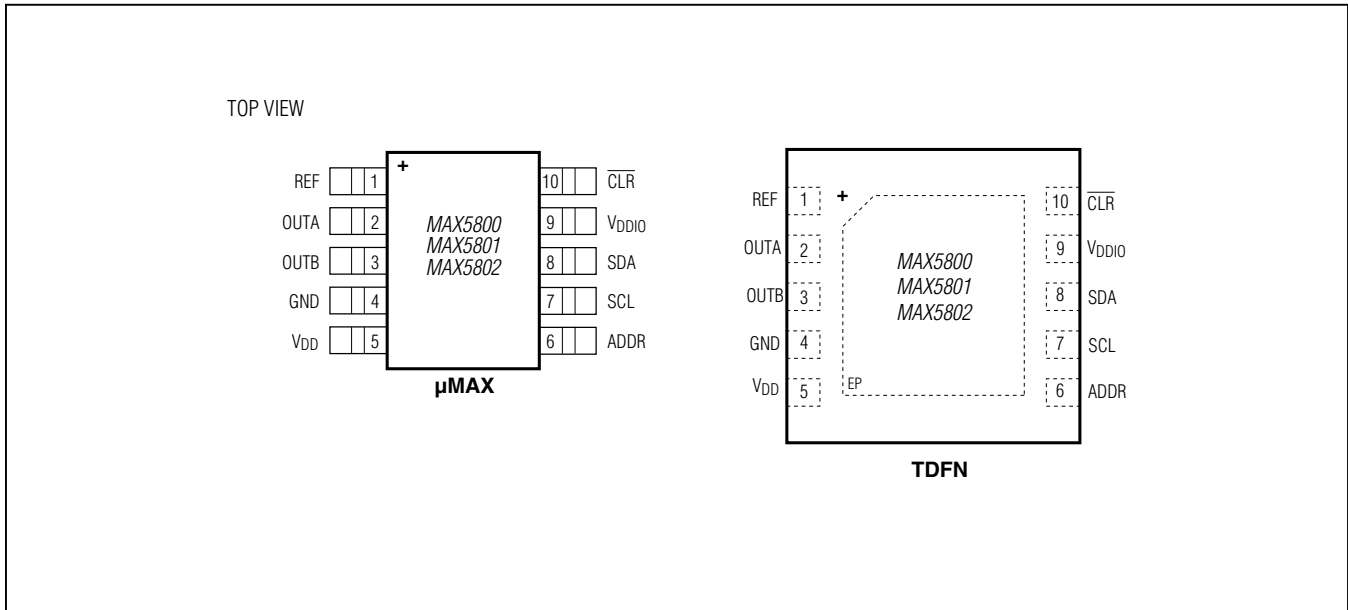
**SUPPLY CURRENT vs. INPUT LOGIC VOLTAGE**



# MAX5800/MAX5801/MAX5802

## Ultra-Small, Dual-Channel, 8-/10-/12-Bit Buffered Output DACs with Internal Reference and I<sup>2</sup>C Interface

### Pin Configurations



### Pin Description

| PIN | NAME              | FUNCTION   |
|-----|-------------------|--|
| 1   | REF               | Reference Voltage Input/Output   |
| 2   | OUTA              | Buffered Channel A DAC Output  |
| 3   | OUTB              | Buffered Channel B DAC Output  |
| 4   | GND               | Ground   |
| 5   | V <sub>DD</sub>   | Supply Voltage Input. Bypass V <sub>DD</sub> with at least a 0.1μF capacitor to GND. |
| 6   | ADDR              | I <sup>2</sup> C Interface Address Selection Bit                                     |
| 7   | SCL               | I <sup>2</sup> C Interface Clock Input   |
| 8   | SDA               | I <sup>2</sup> C Bidirectional Serial Data   |
| 9   | V <sub>DDIO</sub> | Digital Interface Power-Supply Input   |
| 10  | CLR               | Active-Low Clear Input   |
| —   | EP                | Exposed Pad (TDFN Only). Connect to ground.  |

# MAX5800/MAX5801/MAX5802

## Ultra-Small, Dual-Channel, 8-/10-/12-Bit Buffered Output DACs with Internal Reference and I<sup>2</sup>C Interface

### **Detailed Description**

The MAX5800/MAX5801/MAX5802 are 2-channel, low-power, 8-/10-/12-bit buffered voltage-output DACs. The 2.7V to 5.5V wide supply voltage range and low-power consumption accommodates most low-power and low-voltage applications. The devices present a 100kΩ load to the external reference. The internal output buffers allow rail-to-rail operation. An internal voltage reference is available with software selectable options of 2.048V, 2.5V, or 4.096V. The devices feature a fast 400kHz I<sup>2</sup>C-compatible interface. The MAX5800/MAX5801/MAX5802 include a serial-in/parallel-out shift register, internal CODE and DAC registers, a power-on-reset (POR) circuit to initialize the DAC outputs to code zero, and control logic.  $\overline{\text{CLR}}$  is available to asynchronously clear the device independent of the serial interface.

### **DAC Outputs (OUT<sub>-</sub>)**

The MAX5800/MAX5801/MAX5802 include internal buffers on both DAC outputs. The internal output buffers provide improved load regulation for the DAC outputs. The output buffers slew at 1V/μs (typ) and drive up to 2kΩ in parallel with 500pF. The analog supply voltage (V<sub>DD</sub>) determines the maximum output voltage range of the devices as V<sub>DD</sub> powers the output buffer. Under no-load conditions, the output buffers drive from GND to V<sub>DD</sub>, subject to offset and gain errors. With a 2kΩ load to GND, the output buffers drive from GND to within 200mV of V<sub>DD</sub>. With a 2kΩ load to V<sub>DD</sub>, the output buffers drive from V<sub>DD</sub> to within 200mV of GND.

The DAC ideal output voltage is defined by:

$$V_{\text{OUT}} = V_{\text{REF}} \times \frac{D}{2^N}$$

where D = code loaded into the DAC register, V<sub>REF</sub> = reference voltage, N = resolution.

### **Internal Register Structure**

The user interface is separated from the DAC logic to minimize digital feedthrough. Within the serial interface is an input shift register, the contents of which can be routed to control registers, individual, or multiple DACs as determined by the user command.

Within each DAC channel there is a CODE register followed by a DAC latch register (see the *Detailed Functional Diagram*). The contents of the CODE register

hold pending DAC output settings which can later be loaded into the DAC registers. The CODE register can be updated using both CODE and CODE\_LOAD user commands. The contents of the DAC register hold the current DAC output settings. The DAC register can be updated directly from the serial interface using the CODE\_LOAD commands or can upload the current contents of the CODE register using LOAD commands.

The contents of both CODE and DAC registers are maintained during power-down states, so that when the DACs are powered on, they return to their previously stored output settings. Any CODE or LOAD commands issued during power-down states continue to update the register contents. SW\_CLEAR and SW\_RESET commands reset the contents of all CODE and DAC registers to their zero-scale defaults.

### **Internal Reference**

The MAX5800/MAX5801/MAX5802 include an internal precision voltage reference that is software selectable to be 2.048V, 2.500V, or 4.096V. When an internal reference is selected, that voltage is available on the REF pin for other external circuitry (see the [Typical Operating Circuits](#)) and can drive a 25kΩ load.

### **External Reference**

The external reference input has a typical input impedance of 100kΩ and accepts an input voltage from +1.24V to V<sub>DD</sub>. Connect an external voltage supply between REF and GND to apply an external reference. The MAX5800/MAX5801/MAX5802 power up and reset to external reference mode. Visit [www.maximintegrated.com/products/references](http://www.maximintegrated.com/products/references) for a list of available external voltage-reference devices.

### **Clear Input ( $\overline{\text{CLR}}$ )**

The MAX5800/MAX5801/MAX5802 feature an asynchronous active-low  $\overline{\text{CLR}}$  logic input that simultaneously sets both DAC outputs to zero. Driving  $\overline{\text{CLR}}$  low clears the contents of both the CODE and DAC registers and also aborts the on-going I<sup>2</sup>C command. To allow a new I<sup>2</sup>C command, drive  $\overline{\text{CLR}}$  high, satisfying the t<sub>CLRSTA</sub> timing requirement.

### **Interface Power Supply (V<sub>DDIO</sub>)**

The MAX5800/MAX5801/MAX5802 feature a separate supply pin (V<sub>DDIO</sub>) for the digital interface (1.8V to 5.5V). Connect V<sub>DDIO</sub> to the I/O supply of the host processor.

# MAX5800/MAX5801/MAX5802

## Ultra-Small, Dual-Channel, 8-/10-/12-Bit Buffered Output DACs with Internal Reference and I<sup>2</sup>C Interface

### I<sup>2</sup>C Serial Interface

The MAX5800/MAX5801/MAX5802 feature an I<sup>2</sup>C-/SMBus™-compatible, 2-wire serial interface consisting of a serial data line (SDA) and a serial clock line (SCL). SDA and SCL enable communication between the MAX5800/MAX5801/MAX5802 and the master at clock rates up to 400kHz. [Figure 1](#) shows the 2-wire interface timing diagram. The master generates SCL and initiates data transfer on the bus. The master device writes data to the MAX5800/MAX5801/MAX5802 by transmitting the proper slave address followed by the command byte and then the data word. Each transmit sequence is framed by a START (S) or Repeated START (Sr) condition and a STOP (P) condition. Each word transmitted to the MAX5800/MAX5801/MAX5802 is 8 bits long and is followed by an acknowledge clock pulse. A master reading data from the MAX5800/MAX5801/MAX5802 must transmit the proper slave address followed by a series of nine SCL pulses for each byte of data requested. The MAX5800/MAX5801/MAX5802 transmit data on SDA in sync with the master-generated SCL pulses. The master acknowledges receipt of each byte of data. Each read sequence is framed by a START or Repeated START condition, a not acknowledge, and a STOP condition. SDA operates as both an input and an open-drain output. A pullup resistor, typically 4.7kΩ is required on SDA. SCL operates only as an input. A pullup resistor, typically 4.7kΩ, is required on SCL if there are multiple masters on the bus, or if the single master has an open-drain SCL output.

Series resistors in line with SDA and SCL are optional. Series resistors protect the digital inputs of the MAX5800/MAX5801/MAX5802 from high voltage spikes on the bus lines and minimize crosstalk and undershoot of the bus signals. The MAX5800/MAX5801/MAX5802 can accommodate bus voltages higher than V<sub>DDIO</sub> up to a limit of 5.5V; bus voltages lower than V<sub>DDIO</sub> are not recommended and may result in significantly increased interface currents. The MAX5800/MAX5801/MAX5802 digital inputs are double buffered. Depending on the command issued through the serial interface, the CODE register(s) can be loaded without affecting the DAC register(s) using the write command. To update the DAC registers, use the software LOAD command.

### I<sup>2</sup>C START and STOP Conditions

SDA and SCL idle high when the bus is not in use. A master initiates communication by issuing a START condition. A START condition is a high-to-low transition on SDA with

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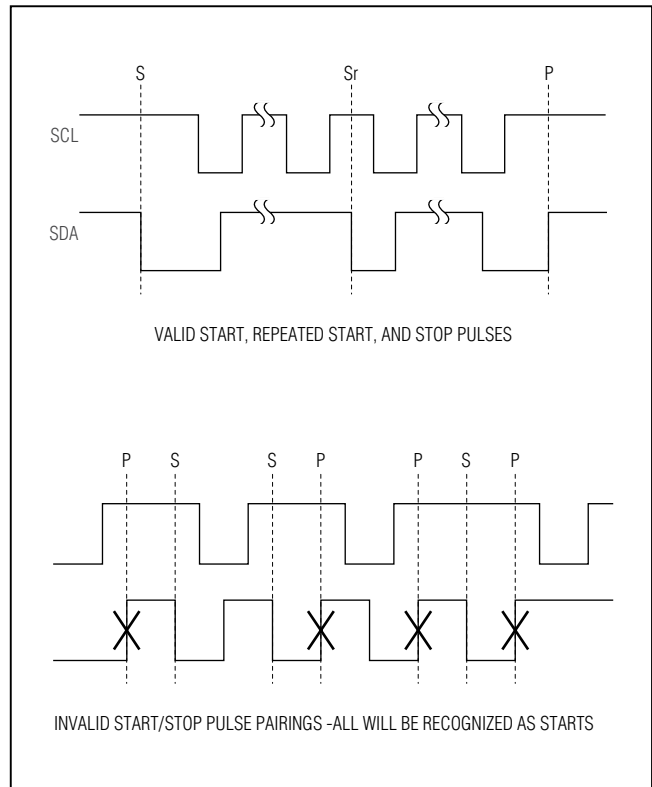


Figure 2. I<sup>2</sup>C START, Repeated START, and STOP Conditions

SCL high. A STOP condition is a low-to-high transition on SDA while SCL is high ([Figure 2](#)). A START condition from the master signals the beginning of a transmission to the MAX5800/MAX5801/MAX5802. The master terminates transmission and frees the bus, by issuing a STOP condition. The bus remains active if a Repeated START condition is generated instead of a STOP condition.

### I<sup>2</sup>C Early STOP and Repeated START Conditions

The MAX5800/MAX5801/MAX5802 recognize a STOP condition at any point during data transmission except if the STOP condition occurs in the same high pulse as a START condition. Transmissions ending in an early STOP condition will not impact the internal device settings. If the STOP occurs during a readback byte, the transmission is terminated and a later read mode request will begin transfer of the requested register data from the beginning (this applies to combined format I<sup>2</sup>C read mode transfers only, interface verification mode transfers will be corrupted). See [Figure 2](#).



# MAX5800/MAX5801/MAX5802

## Ultra-Small, Dual-Channel, 8-/10-/12-Bit Buffered Output DACs with Internal Reference and I<sup>2</sup>C Interface

### I<sup>2</sup>C Slave Address

The slave address is defined as the seven most significant bits (MSBs) followed by the R/W bit. See Figure 4. The five most significant bits are 00011 with the 2 LSBs determined by ADDR as shown in Table 1. Setting the R/W bit to 1 configures the MAX5800/MAX5801/MAX5802 for read mode. Setting the R/W bit to 0 configures the MAX5800/MAX5801/MAX5802 for write mode. The slave address is the first byte of information sent to the MAX5800/MAX5801/MAX5802 after the START condition.

The MAX5800/MAX5801/MAX5802 have the ability to detect an unconnected state on the ADDR input for additional address flexibility; if leaving the ADDR input unconnected, be certain to minimize all loading on the pin (i.e. provide a landing for the pin, but do not allow any board traces).

### I<sup>2</sup>C Broadcast Address

A broadcast address is provided for the purpose of updating or configuring all MAX5800/MAX5801/MAX5802 devices on a given I<sup>2</sup>C bus. All MAX5800/MAX5801/MAX5802 devices acknowledge and respond to the broadcast device address 00010000. The devices will respond to the broadcast address, regardless of the state of the address pins. The broadcast mode is intended for use in write mode only (as indicated by R/W = 0 in the address given).

### I<sup>2</sup>C Acknowledge

In write mode, the acknowledge bit (ACK) is a clocked 9th bit that the MAX5800/MAX5801/MAX5802 use to hand-

shake receipt of each byte of data as shown in Figure 3. The MAX5800/MAX5801/MAX5802 pull down SDA during the entire master-generated 9th clock pulse if the previous byte is successfully received. Monitoring ACK allows for detection of unsuccessful data transfers. An unsuccessful data transfer occurs if a receiving device is busy or if a system fault has occurred. In the event of an unsuccessful data transfer, the bus master will retry communication.

Table 1. I<sup>2</sup>C Slave Address LSBs

| A[6:2] = 00011    |    |    |
|-------------------|----|----|
| ADDR              | A1 | A0 |
| V <sub>DDIO</sub> | 0  | 0  |
| N.C.              | 1  | 0  |
| GND               | 1  | 1  |

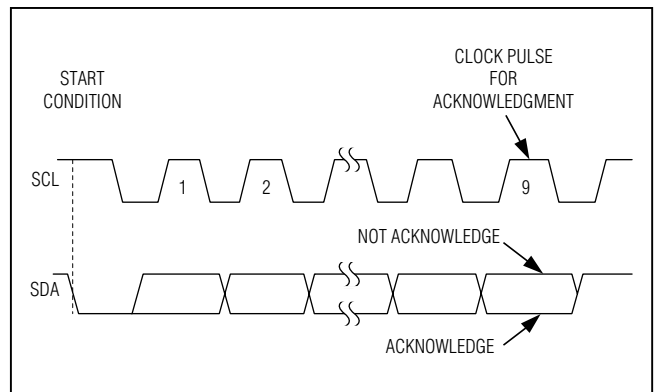


Figure 3. I<sup>2</sup>C Acknowledge

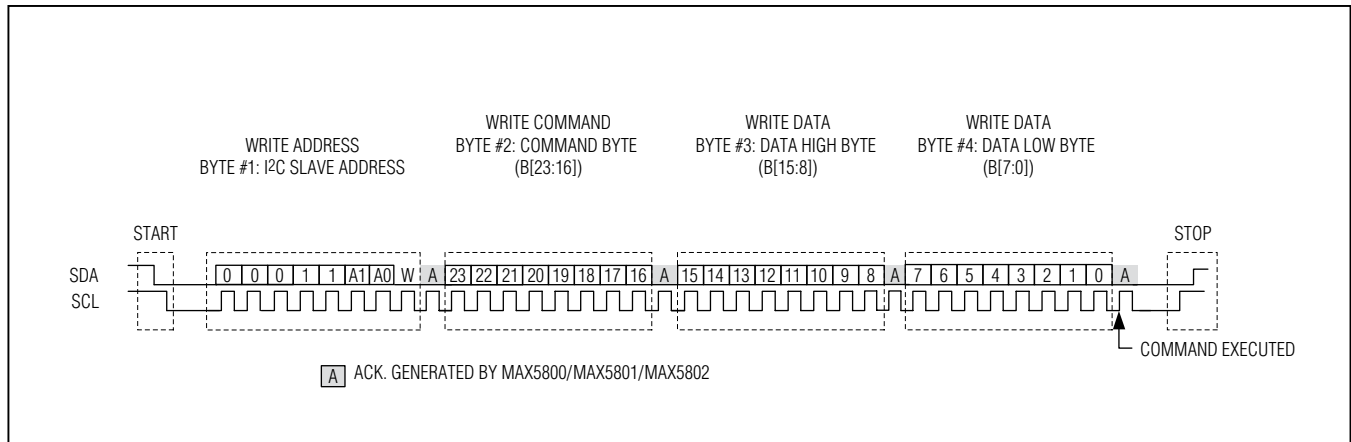


Figure 4. I<sup>2</sup>C Single Register Write Sequence

# MAX5800/MAX5801/MAX5802

## Ultra-Small, Dual-Channel, 8-/10-/12-Bit Buffered Output DACs with Internal Reference and I<sup>2</sup>C Interface

In read mode, the master pulls down SDA during the 9th clock cycle to acknowledge receipt of data from the MAX5800/MAX5801/MAX5802. An acknowledge is sent by the master after each read byte to allow data transfer to continue. A not-acknowledge is sent when the master reads the final byte of data from the MAX5800/MAX5801/MAX5802, followed by a STOP condition.

### I<sup>2</sup>C Command Byte and Data Bytes

A command byte follows the slave address. A command byte is typically followed by two data bytes unless it is the last byte in the transmission. If data bytes follow the command byte, the command byte indicates the address of the register that is to receive the following two data bytes. The data bytes are stored in a temporary register and then transferred to the appropriate register during the ACK periods between bytes. This avoids any glitching or digital feedthrough to the DACs while the interface is active.

### I<sup>2</sup>C Write Operations

A master device communicates with the MAX5800/MAX5801/MAX5802 by transmitting the proper slave address followed by command and data words. Each transmit sequence is framed by a START or Repeated START condition and a STOP condition as described above. Each word is 8 bits long and is always followed by an acknowledge clock (ACK) pulse as shown in the Figure 4 and Figure 5. The first byte contains the address of the MAX5800/MAX5801/MAX5802 with  $R/\bar{W} = 0$  to indicate a write. The second byte contains the register (or com-

mand) to be written and the third and fourth bytes contain the data to be written. By repeating the register address plus data pairs (Byte #2 through Byte #4 in Figure 4 and Figure 5), the user can perform multiple register writes using a single I<sup>2</sup>C command sequence. There is no limit as to how many registers the user can write with a single command. The MAX5800/MAX5801/MAX5802 support this capability for all user-accessible write mode commands.

### Combined Format I<sup>2</sup>C Readback Operations

Each readback sequence is framed by a START or Repeated START condition and a STOP condition. Each word is 8 bits long and is followed by an acknowledge clock pulse as shown in Figure 6. The first byte contains the address of the MAX5800/MAX5801/MAX5802 with  $R/\bar{W} = 0$  to indicate a write. The second byte contains the register that is to be read back. There is a Repeated START condition, followed by the device address with  $R/\bar{W} = 1$  to indicate a read and an acknowledge clock. The master has control of the SCL line but the MAX5800/MAX5801/MAX5802 take over the SDA line. The final two bytes in the frame contain the register data readback followed by a STOP condition. If additional bytes beyond those required to readback the requested data are provided, the MAX5800/MAX5801/MAX5802 will continue to readback ones.

Readback of individual CODE registers is supported for the CODE command ( $B[23:20] = 0000$ ). For this command, which supports a DAC address, the requested

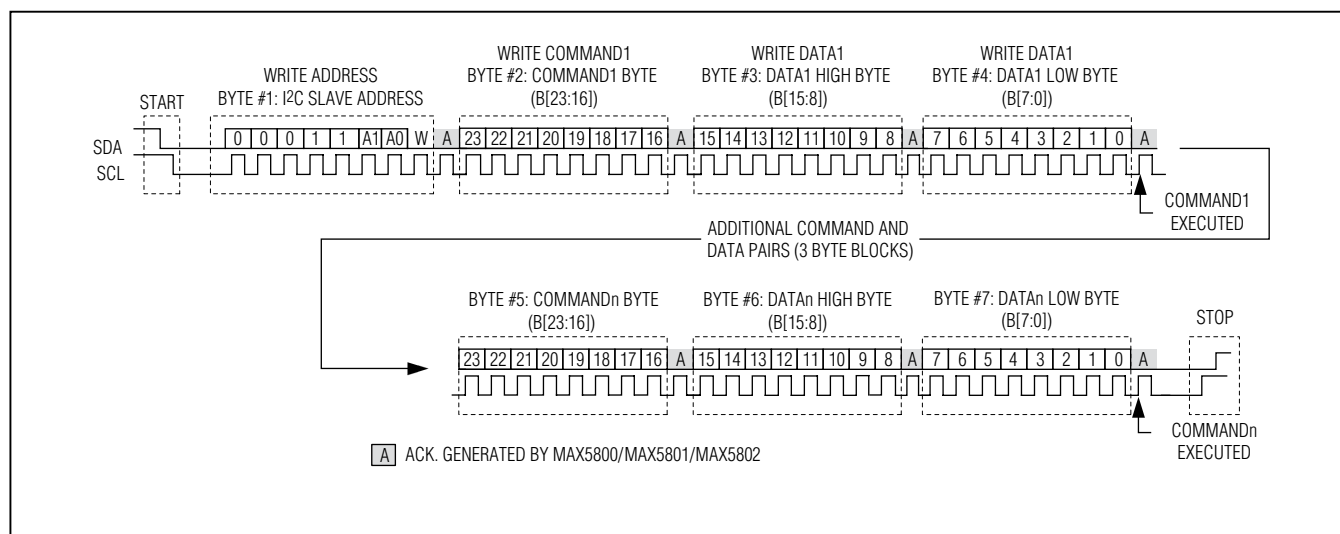


Figure 5. Multiple Register Write Sequence (Standard I<sup>2</sup>C Protocol)

# MAX5800/MAX5801/MAX5802

## Ultra-Small, Dual-Channel, 8-/10-/12-Bit Buffered Output DACs with Internal Reference and I<sup>2</sup>C Interface

channel CODE register content will be returned; if both DACs are selected, CODEA content will be returned.

Readback of individual DAC registers is supported for all LOAD commands (B[23:20] = 0001, 0010, or 0011). For these commands, which support a DAC address, the requested DAC register content will be returned. If both DACs are selected, DACA content will be returned.

Modified readback of the POWER register is supported for the POWER command (B[23:20] = 0100). The power status of each DAC is reported in locations B[1:0], with a 1 indicating the DAC is powered down and a 0 indicating the DAC is operational (see Table 2).

Readback of all other registers is not directly supported. All requests to read unsupported registers reads back the device's reference status and the device ID and revision information in the format as shown in Table 2.

### Interface Verification I<sup>2</sup>C Readback Operations

While the MAX5800/MAX5801/MAX5802 support standard I<sup>2</sup>C readback of selected registers, it is also capable of functioning in an interface verification mode. This mode is accessed any time a readback operation follows an executed write mode command. In this mode, the last executed three-byte command is read back in its entirety. This behavior allows verification of the interface.

Sample command sequences are shown in Figure 7. The first command transfer is given in write mode with R/W = 0 and must be run to completion to qualify for interface verification readback. There is now a STOP/START pair or Repeated START condition required, followed by the readback transfer with R/W = 1 to indicate a read and an acknowledge clock from the MAX5800/MAX5801/MAX5802. The master still has control of the

**Table 2. Standard I<sup>2</sup>C User Readback Data**

| COMMAND BYTE (REQUEST) |     |     |     |               |     |     |     | READBACK DATA HIGH BYTE |     |     |     |     |     |    |    | READBACK DATA LOW BYTE |    |    |                      |    |                     |     |     |
|------------------------|-----|-----|-----|---------------|-----|-----|-----|-------------------------|-----|-----|-----|-----|-----|----|----|------------------------|----|----|----------------------|----|---------------------|-----|-----|
| B23                    | B22 | B21 | B20 | B19           | B18 | B17 | B16 | B15                     | B14 | B13 | B12 | B11 | B10 | B9 | B8 | B7                     | B6 | B5 | B4                   | B3 | B2                  | B1  | B0  |
| 0                      | 0   | 0   | 0   | DAC selection |     |     |     | CODEn[11:4]             |     |     |     |     |     |    |    | CODEn[3:0]             |    |    | 0                    | 0  | 0                   | 0   |     |
| 0                      | 0   | 0   | 1   | DAC selection |     |     |     | DACn[11:4]              |     |     |     |     |     |    |    | DACn[3:0]              |    |    | 0                    | 0  | 0                   | 0   |     |
| 0                      | 0   | 1   | 0   | DAC selection |     |     |     | DACn[11:4]              |     |     |     |     |     |    |    | DACn[3:0]              |    |    | 0                    | 0  | 0                   | 0   |     |
| 0                      | 0   | 1   | 1   | DAC selection |     |     |     | DACn[11:4]              |     |     |     |     |     |    |    | DACn[3:0]              |    |    | 0                    | 0  | 0                   | 0   |     |
| 0                      | 1   | 0   | 0   | 0             | 0   | X   | X   | 0                       | 0   | 0   | 0   | 0   | 0   | 0  | 0  | 0                      | 0  | 0  | 0                    | 0  | 0                   | PWB | PWA |
| 1                      | 0   | 0   | 0   | 0             | 0   | 0   | 0   | CODEA[11:4]             |     |     |     |     |     |    |    | CODEA[3:0]             |    |    | 0                    | 0  | 0                   | 0   |     |
| 1                      | 0   | 0   | 0   | 0             | 0   | 0   | 1   | DACA[11:4]              |     |     |     |     |     |    |    | DACA[3:0]              |    |    | 0                    | 0  | 0                   | 0   |     |
| 1                      | 0   | 1   | 0   | 0             | 0   | 1   | 0   | DACA[11:4]              |     |     |     |     |     |    |    | DACA[3:0]              |    |    | 0                    | 0  | 0                   | 0   |     |
| 1                      | 0   | 1   | 1   | 0             | 0   | 1   | 1   | DACA[11:4]              |     |     |     |     |     |    |    | DACA[3:0]              |    |    | 0                    | 0  | 0                   | 0   |     |
| Any other command      |     |     |     |               |     |     |     | 1001 1000               |     |     |     |     |     |    |    | 000                    |    |    | REV_ID[2:0]<br>(011) |    | REF MODE<br>RF[1:0] |     |     |

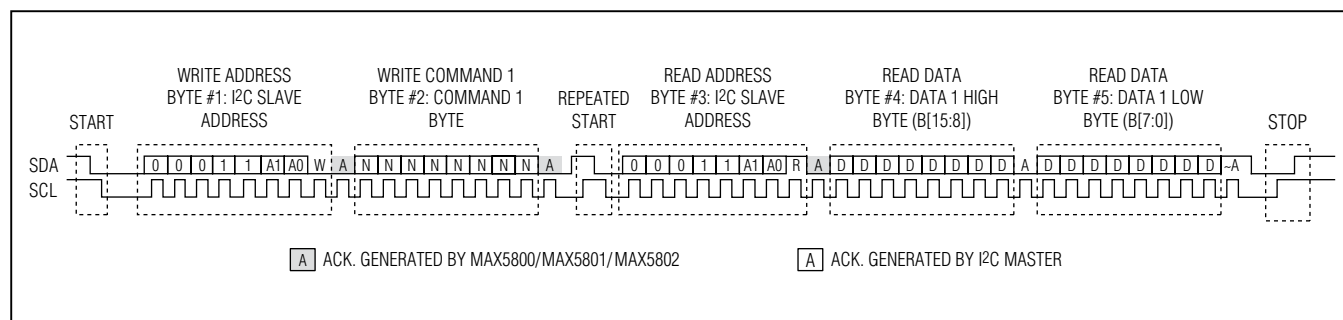


Figure 6. Standard I<sup>2</sup>C Register Read Sequence

# MAX5800/MAX5801/MAX5802

## Ultra-Small, Dual-Channel, 8-/10-/12-Bit Buffered Output DACs with Internal Reference and I<sup>2</sup>C Interface

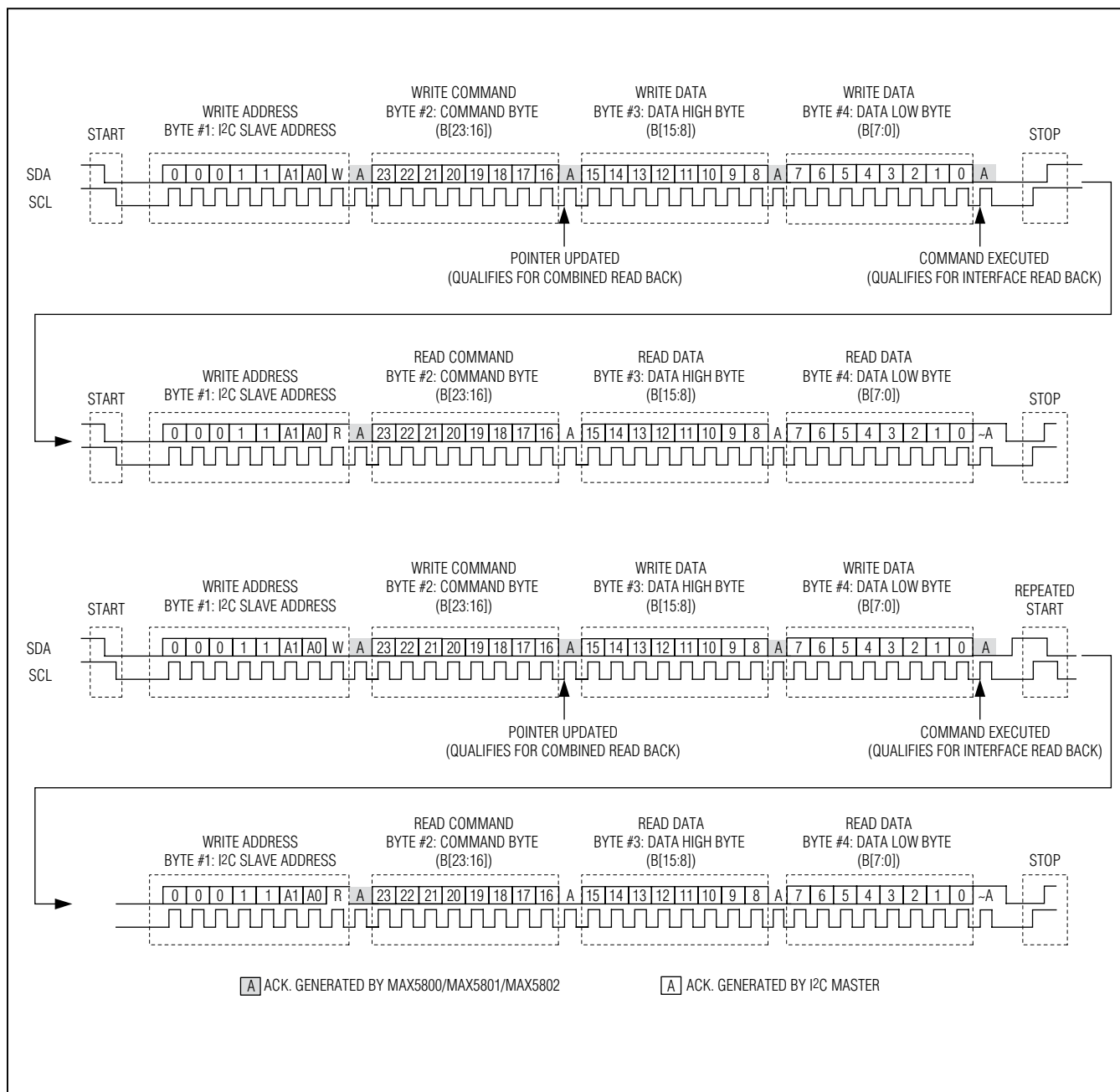


Figure 7. Interface Verification I<sup>2</sup>C Register Read Sequences

# MAX5800/MAX5801/MAX5802

## Ultra-Small, Dual-Channel, 8-/10-/12-Bit Buffered Output DACs with Internal Reference and I<sup>2</sup>C Interface

SCL line but the MAX5800/MAX5801/MAX5802 take over the SDA line. The final three bytes in the frame contain the command and register data written in the first transfer presented for readback, followed by a STOP condition. If additional bytes beyond those required to read back the requested data are provided, the MAX5800/MAX5801/MAX5802 will continue to read back ones.

It is not necessary for the write and read mode transfers to occur immediately in sequence. I<sup>2</sup>C transfers involving other devices do not impact the MAX5800/MAX5801/MAX5802 readback mode. Toggling between readback modes is based on the length of the preceding write mode transfer. Combined format I<sup>2</sup>C readback operation is resumed if a write command greater than two bytes but less than four bytes is supplied. For commands written using multiple register write sequences, only the last command executed is read back. For each command written, the readback sequence can only be completed one time; partial and/or multiple attempts to readback executed in succession will not yield usable data.

### I<sup>2</sup>C Compatibility

The MAX5800/MAX5801/MAX5802 are fully compatible with existing I<sup>2</sup>C systems. SCL and SDA are high-impedance inputs; SDA has an open drain which pulls the data line low to transmit data or ACK pulses. [Figure 8](#) shows a typical I<sup>2</sup>C application.

### I<sup>2</sup>C User-Command Register Map

This section lists the user accessible commands and registers for the MAX5800/MAX5801/MAX5802. Each serial operation word is 24-bits long. The DAC data is left justified as shown in Table 3.

[Table 4](#) provides detailed information about the Command Registers.

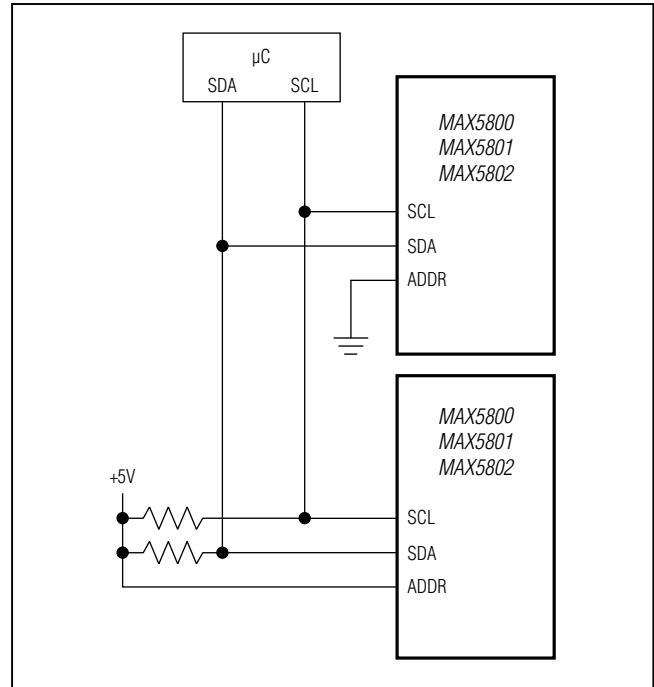


Figure 8. Typical I<sup>2</sup>C Application Circuit

Table 3. Format DAC Data Bit Positions

| PART    | B15 | B14 | B13 | B12 | B11 | B10 | B9 | B8 | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|---------|-----|-----|-----|-----|-----|-----|----|----|----|----|----|----|----|----|----|----|
| MAX5800 | D7  | D6  | D5  | D4  | D3  | D2  | D1 | D0 | X  | X  | X  | X  | X  | X  | X  | X  |
| MAX5801 | D9  | D8  | D7  | D6  | D5  | D4  | D3 | D2 | D1 | D0 | X  | X  | X  | X  | X  | X  |
| MAX5802 | D11 | D10 | D9  | D8  | D7  | D6  | D5 | D4 | D3 | D2 | D1 | D0 | X  | X  | X  | X  |

# MAX5800/MAX5801/MAX5802

## Ultra-Small, Dual-Channel, 8-/10-/12-Bit Buffered Output DACs with Internal Reference and I<sup>2</sup>C Interface

**Table 4. I<sup>2</sup>C Commands Summary**

| COMMAND                       | B23 | B22 | B21 | B20 | B19 | B18           | B17 | B16 | B15 | B14 | B13 | B12 | B11 | B10 | B9 | B8    | B7 | B6 | B5                      | B4 | B3 | B2 | B1 | B0 | DESCRIPTION   |   |
|-------------------------------|-----|-----|-----|-----|-----|---------------|-----|-----|-----|-----|-----|-----|-----|-----|----|-------|----|----|-------------------------|----|----|----|----|----|---|---|
| <b>DAC COMMANDS</b>           |     |     |     |     |     |               |     |     |     |     |     |     |     |     |    |       |    |    |                         |    |    |    |    |    |   |   |
| CODEn                         | 0   | 0   | 0   | 0   |     |               |     |     |     |     |     |     |     |     |    |       |    |    | CODE REGISTER DATA[3:0] |    |    |    |    | X  | Writes data to the selected CODE register(s)  |   |
| LOADn                         | 0   | 0   | 0   | 1   |     | DAC SELECTION |     |     | X   | X   | X   | X   | X   | X   | X  | X     | X  | X  | X                       |    |    |    |    | X  | Transfers data from the selected CODE register(s) to the selected DAC register(s)                   |   |
| CODEn_LOAD_ALL                | 0   | 0   | 1   | 0   |     | DAC SELECTION |     |     |     |     |     |     |     |     |    |       |    |    | CODE REGISTER DATA[3:0] |    |    |    |    | X  | Simultaneously writes data to the selected CODE register(s) while updating all DAC registers        |   |
| CODEn_LOADn                   | 0   | 0   | 1   | 1   |     | DAC SELECTION |     |     | X   | X   | X   | X   | X   | X   | X  | X     | X  | X  | CODE REGISTER DATA[3:0] |    |    |    |    | X  | Simultaneously writes data to the selected CODE register(s) while updating selected DAC register(s) |   |
| <b>CONFIGURATION COMMANDS</b> |     |     |     |     |     |               |     |     |     |     |     |     |     |     |    |       |    |    |                         |    |    |    |    |    |   |   |
| POWER                         | 0   | 1   | 0   | 0   | 0   |               |     |     | X   | X   | X   | X   | X   | X   | X  | DAC A | X  | X  | X                       | X  | X  | X  | X  | X  | X   | Sets the power mode of the selected DACs (DACs selected with a 1 in the corresponding DACn bit are updated, DACs with a 0 in the corresponding DACn bit are not impacted) |
| SW_CLEAR                      | 0   | 1   | 0   | 1   | 0   | 0             | 0   | 0   | X   | X   | X   | X   | X   | X   | X  | DAC B | X  | X  | X                       | X  | X  | X  | X  | X  | X   | Executes a software clear (all CODE and DAC registers cleared to their default values)  |
| SW_RESET                      | 0   | 1   | 0   | 1   | 0   | 0             | 1   | 0   | X   | X   | X   | X   | X   | X   | X  |       | X  | X  | X                       | X  | X  | X  | X  | X  | Executes a software reset (all CODE, DAC, and control registers returned to their default values)   |   |

# MAX5800/MAX5801/MAX5802

## Ultra-Small, Dual-Channel, 8-/10-/12-Bit Buffered Output DACs with Internal Reference and I<sup>2</sup>C Interface

Table 4. I<sup>2</sup>C Commands Summary (continued)

| COMMAND   | B23 | B22 | B21 | B20 | B19 | B18 | B17 | B16   | B15 | B14                      | B13 | B12 | B11 | B10 | B9                      | B8    | B7 | B6  | B5 | B4 | B3 | B2 | B1 | B0 | DESCRIPTION   |
|---|-----|-----|-----|-----|-----|-----|-----|---|-----|--------------------------|-----|-----|-----|-----|-------------------------|-------|----|---|----|----|----|----|----|----|---|
| CONFIG  | 0   | 1   | 1   | 0   | 0   | 0   | 0   | LD_EN   | X   | X                        | X   | X   | X   | X   | DAC B                   | DAC A | X  | X   | X  | X  | X  | X  | X  | X  | Sets the DAC Latch Mode of the selected DACs. Only DACs with a 1 in the selection bit are updated by the command.<br>LD_EN = 0: DAC latch is operational (LOAD controlled)<br>LD_EN = 1: DAC latch is transparent |
| REF   | 0   | 1   | 1   | 1   | 0   | 0   | 0   | REF Mode<br>0= EXT<br>01 = 2.5V<br>10 = 2.0V<br>11 = 4.1V | X   | X                        | X   | X   | X   | X   | X                       | X     | X  | X   | X  | X  | X  | X  | X  | X  | Sets the reference operating mode.<br>REF Power (B18):<br>0 = Internal reference is only powered if at least one DAC is powered<br>1 = Internal reference is always powered                                       |
| <b>ALL DAC COMMANDS</b>   |     |     |     |     |     |     |     |   |     |                          |     |     |     |     |                         |       |    |   |    |    |    |    |    |    |   |
| CODE_ALL  | 1   | 0   | 0   | 0   | 0   | 0   | 0   | 0   |     | CODE REGISTER DATA[11:4] |     |     |     |     | CODE REGISTER DATA[3:0] |       |    | Writes data to all CODE registers   |    |    |    |    |    |    |   |
| LOAD_ALL  | 1   | 0   | 0   | 0   | 0   | 0   | 1   | 0   | X   | X                        | X   | X   | X   | X   | X                       | X     | X  | X   | X  | X  | X  | X  | X  | X  | Updates all DAC latches with current CODE register data   |
| CODE_ALL_LOAD_ALL   | 1   | 0   | 0   | 0   | 0   | 0   | 1   | X   |     | CODE REGISTER DATA[11:4] |     |     |     |     | CODE REGISTER DATA[3:0] |       |    | Simultaneously writes data to all CODE registers while updating all DAC registers |    |    |    |    |    |    |   |
| <b>NO OPERATION COMMANDS</b>  |     |     |     |     |     |     |     |   |     |                          |     |     |     |     |                         |       |    |   |    |    |    |    |    |    |   |
| No Operation  | 1   | 0   | 0   | 1   | X   | X   | X   | X   | X   | X                        | X   | X   | X   | X   | X                       | X     | X  | X   | X  | X  | X  | X  | X  | X  | These commands will have no effect on the device  |
| Reserved Commands: Any commands not specifically listed above are reserved for Maxim internal use only. |     |     |     |     |     |     |     |   |     |                          |     |     |     |     |                         |       |    |   |    |    |    |    |    |    |   |

# MAX5800/MAX5801/MAX5802

## Ultra-Small, Dual-Channel, 8-/10-/12-Bit Buffered Output DACs with Internal Reference and I<sup>2</sup>C Interface

### **CODEn Command**

The CODEn command (B[23:20] = 0000) updates the CODE register contents for the selected DAC(s). Changes to the CODE register content based on this command will not affect DAC outputs directly unless the DAC latch has been configured to be transparent. Issuing the CODEn command with DAC SELECTION = ALL DACs is equivalent to CODE\_ALL (B[23:16] = 10000000). See [Table 4](#) and [Table 5](#).

### **LOADn Command**

The LOADn command (B[23:20] = 0001) updates the DAC register content for the selected DAC(s) by uploading the current contents of the CODE register. The LOADn command can be used with DAC SELECTION = ALL DACs to issue a software load for both DACs, which is equivalent to the LOAD\_ALL (B[23:16] = 10000001) command. See [Table 4](#) and [Table 5](#).

### **CODEn\_LOAD\_ALL Command**

The CODEn\_LOAD\_ALL command (B[23:20] = 0010) updates the CODE register contents for the selected DAC(s) as well as the DAC register content of both DACs. Channels for which the CODE register content has not been modified since the last load to DAC register operation will not be updated to reduce digital crosstalk. Issuing this command with DAC\_ADDRESS = ALL is equivalent to the CODE\_ALL\_LOAD\_ALL command. The CODEn\_LOAD\_ALL command by definition will modify at least one CODE register. To avoid this, use the LOADn command with DAC SELECTION = ALL DACs or use the LOAD\_ALL command. See [Table 4](#) and [Table 5](#).

### **CODEn\_LOADn Command**

The CODEn\_LOADn command (B[23:20] = 0011) updates the CODE register contents for the selected DAC(s) as well as the DAC register content of the selected DAC(s). Channels for which the CODE register content has not been modified since the last load to DAC register operation will not be updated to reduce digital crosstalk. Issuing this command with DAC SELECTION = ALL DACs is equivalent to the CODE\_ALL\_LOAD\_ALL command. See [Table 4](#) and [Table 5](#).

### **CODE\_ALL Command**

The CODE\_ALL command (B[23:16] = 10000000) updates the CODE register contents for both DACs. See [Table 4](#).

### **LOAD\_ALL Command**

The LOAD\_ALL command (B[23:16] = 10000001) updates the DAC register content for both DACs by uploading the current contents of the CODE registers. See [Table 4](#).

### **CODE\_ALL\_LOAD\_ALL Command**

The CODE\_ALL\_LOAD\_ALL command (B[23:16] = 1000001x) updates the CODE register contents for both DACs as well as the DAC register content of both DACs. See [Table 4](#).

**Table 5. DAC Selection**

| B19 | B18 | B17 | B16 | DAC SELECTED |
|-----|-----|-----|-----|--------------|
| 0   | 0   | 0   | 0   | DAC A        |
| 0   | 0   | 0   | 1   | DAC B        |
| 0   | 0   | 1   | X   | No effect    |
| X   | 1   | X   | X   | ALL DACs     |
| 1   | X   | X   | X   | ALL DACs     |



# MAX5800/MAX5801/MAX5802

## Ultra-Small, Dual-Channel, 8-/10-/12-Bit Buffered Output DACs with Internal Reference and I<sup>2</sup>C Interface

### POWER Command

The MAX5800/MAX5801/MAX5802 feature a software-controlled power-mode (POWER) command (B[23:18] = 010000). The POWER command updates the power-mode settings of the selected DACs while the power settings of the rest of the DACs remain unchanged. The new power setting is determined by bits B[17:16] while the affected DAC(s) are selected by bits B[9:8]. If all DACs are powered down, the device enters a STANDBY mode.

In power-down, the DAC output is disconnected from the buffer and is grounded with either one of the two selectable internal resistors or set to high impedance. See [Table 7](#) for the selectable internal resistor values in power-down mode. In power-down mode, the DAC register retains its value so

that the output is restored when the device powers up. The serial interface remains active in power-down mode.

In STANDBY mode, the internal reference can be powered down or it can be set to remain powered-on for external use. Also, in STANDBY mode, devices using the external reference do not load the REF pin. See [Table 6](#).

### SW\_RESET and SW\_CLEAR Command

The SW\_RESET (B[23:16] = 01010001) and SW\_CLEAR (B[23:16] = 01010000) commands provide a means of issuing a software reset or software clear operation. Use SW\_CLEAR to issue a software clear operation to return all CODE and DAC registers to the zero-scale value. Use SW\_RESET to reset all CODE, DAC, and configuration registers to their default values.

**Table 6. POWER Command Format**

| B23                       | B22 | B21 | B20 | B19 | B18 | B17   | B16 | B15        | B14 | B13 | B12 | B11 | B10 | B9  | B8 | B7         | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|---------------------------|-----|-----|-----|-----|-----|---|-----|------------|-----|-----|-----|-----|-----|---|----|------------|----|----|----|----|----|----|----|
| 0                         | 1   | 0   | 0   | 0   | 0   | PD1   | PD0 | X          | X   | X   | X   | X   | X   | B   | A  | X          | X  | X  | X  | X  | X  | X  | X  |
| POWER Command             |     |     |     |     |     | Power Mode:<br>00 = Normal<br>01 = 1kΩ<br>10 = 100kΩ<br>11 = Hi-Z |     | Don't Care |     |     |     |     |     | DAC Select:<br>1 = DAC Selected<br>0 = DAC Not Selected |    | Don't Care |    |    |    |    |    |    |    |
| Default Values (all DACs) |     |     |     |     |     | 0   | 0   | X          | X   | X   | X   | X   | X   | 1   | 1  | X          | X  | X  | X  | X  | X  | X  | X  |

**Table 7. Selectable DAC Output Impedance in Power-Down Mode**

| PD1 (B17) | PD0 (B16) | OPERATING MODE   |
|-----------|-----------|--|
| 0         | 0         | Normal operation   |
| 0         | 1         | Power-down with internal 1kΩ pulldown resistor to GND.   |
| 1         | 0         | Power-down with internal 100kΩ pulldown resistor to GND. |
| 1         | 1         | Power-down with high-impedance output.                   |

# MAX5800/MAX5801/MAX5802

## Ultra-Small, Dual-Channel, 8-/10-/12-Bit Buffered Output DACs with Internal Reference and I<sup>2</sup>C Interface

### CONFIG Command

The CONFIG command (B[23:17] = 0110000) updates the LOAD functions of selected DACs. Issue the command with B16 = 0 to allow the DAC latches to operate normally or with B16 = 1 to disable the DAC latches, making them perpetually transparent. Mode settings of the selected DACs are updated while the mode settings of the rest of the DACs remain unchanged; DAC(s) are selected by bits B[9:8]. See [Table 8](#).

### REF Command

The REF command (B[23:19] = 01110) updates the global reference setting used for both DAC channels. Set B[17:16] = 00 to use an external reference for the DACs

or set B[17:16] to 01, 10, or 11 to select either the 2.5V, 2.048V, or 4.096V internal reference, respectively.

If RF2 (B18) is set to zero (default) in the REF command, the reference will be powered down any time both DAC channels are powered down (in STANDBY mode). If RF2 (B18 = 1) is set to one, the reference will remain powered even if both DAC channels are powered down, allowing continued operation of external circuitry. In this mode, the 1µA shutdown state is not available. See [Table 9](#).

**Table 8. CONFIG Command Format**

| B23                       | B22 | B21 | B20 | B19 | B18 | B17 | B16                           | B15        | B14 | B13 | B12 | B11 | B10 | B9  | B8         | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |   |   |
|---------------------------|-----|-----|-----|-----|-----|-----|-------------------------------|------------|-----|-----|-----|-----|-----|---|------------|----|----|----|----|----|----|----|----|---|---|
| 0                         | 1   | 1   | 0   | 0   | 0   | 0   | LDB                           | X          | X   | X   | X   | X   | X   | B   | A          | X  | X  | X  | X  | X  | X  | X  | X  |   |   |
| CONFIG Command            |     |     |     |     |     |     | 0 = Normal<br>1 = Transparent | Don't Care |     |     |     |     |     | DAC Select:<br>1 = DAC Selected<br>0 = DAC Not Selected | Don't Care |    |    |    |    |    |    |    |    |   |   |
| Default Values (all DACs) |     |     |     |     |     |     | 0                             | X          | X   | X   | X   | X   | X   | 1   | 1          | X  | X  | X  | X  | X  | X  | X  | X  | X | X |

**Table 9. REF Command Format**

| B23            | B22 | B21 | B20 | B19 | B18                                     | B17  | B16 | B15        | B14 | B13 | B12 | B11 | B10 | B9         | B8 | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|----------------|-----|-----|-----|-----|---|--|-----|------------|-----|-----|-----|-----|-----|------------|----|----|----|----|----|----|----|----|----|
| 0              | 1   | 1   | 1   | 0   | RF2                                     | RF1  | RF0 | X          | X   | X   | X   | X   | X   | X          | X  | X  | X  | X  | X  | X  | X  | X  | X  |
| REF Command    |     |     |     |     | 0 = Off in Standby<br>1 = On in Standby | REF Mode:<br>00 = EXT<br>01 = 2.5V<br>10 = 2.0V<br>11 = 4.0V |     | Don't Care |     |     |     |     |     | Don't Care |    |    |    |    |    |    |    |    |    |
| Default Values |     |     |     |     | 0                                       | 0  | 0   | X          | X   | X   | X   | X   | X   | X          | X  | X  | X  | X  | X  | X  | X  | X  | X  |

# MAX5800/MAX5801/MAX5802

## Ultra-Small, Dual-Channel, 8-/10-/12-Bit Buffered Output DACs with Internal Reference and I<sup>2</sup>C Interface

### Applications Information

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#### **Power-On Reset (POR)**

When power is applied to V<sub>DD</sub> and V<sub>DDIO</sub>, the DAC output is set to zero scale. To optimize DAC linearity, wait until the supplies have settled and the internal setup and calibration sequence completes (200µs, typ).

#### **Power Supplies and Bypassing Considerations**

Bypass V<sub>DD</sub> and V<sub>DDIO</sub> with high-quality ceramic capacitors to a low-impedance ground as close as possible to the device. Minimize lead lengths to reduce lead inductance. Connect the GND to the analog ground plane.

#### **Layout Considerations**

Digital and AC transient signals on GND can create noise at the output. Connect GND to form the star ground for the DAC system. Refer remote DAC loads to this system ground for the best possible performance. Use proper grounding techniques, such as a multilayer board with a low-inductance ground plane, or star connect all ground return paths back to the MAX5800/MAX5801/MAX5802 GND. Carefully layout the traces between channels to reduce AC cross-coupling. Do not use wire-wrapped boards and sockets. Use shielding to minimize noise immunity. Do not run analog and digital signals parallel to one another, especially clock signals. Avoid routing digital lines underneath the MAX5800/MAX5801/MAX5802 package.

### Definitions

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#### **Integral Nonlinearity (INL)**

INL is the deviation of the measured transfer function from a straight line drawn between two codes once offset and gain errors have been nullified.

#### **Differential Nonlinearity (DNL)**

DNL is the difference between an actual step height and the ideal value of 1 LSB. If the magnitude of the DNL  $\leq$  1 LSB, the DAC guarantees no missing codes and is monotonic. If the magnitude of the DNL  $\geq$  1 LSB, the DAC output may still be monotonic.

#### **Offset Error**

Offset error indicates how well the actual transfer function matches the ideal transfer function. The offset error is calculated from two measurements near zero code and near maximum code.

#### **Gain Error**

Gain error is the difference between the ideal and the actual full-scale output voltage on the transfer curve, after nullifying the offset error. This error alters the slope of the transfer function and corresponds to the same percentage error in each step.

#### **Zero-Scale Error**

Zero-scale error is the difference between the DAC output voltage when set to code zero and ground. This includes offset and other die level nonidealities.

#### **Full-Scale Error**

Full-scale error is the difference between the DAC output voltage when set to full scale and the reference voltage. This includes offset, gain error, and other die level nonidealities.

#### **Settling Time**

The settling time is the amount of time required from the start of a transition, until the DAC output settles to the new output value within the converter's specified accuracy.

#### **Digital Feedthrough**

Digital feedthrough is the amount of noise that appears on the DAC output when the DAC digital control lines are toggled.

#### **Digital-to-Analog Glitch Impulse**

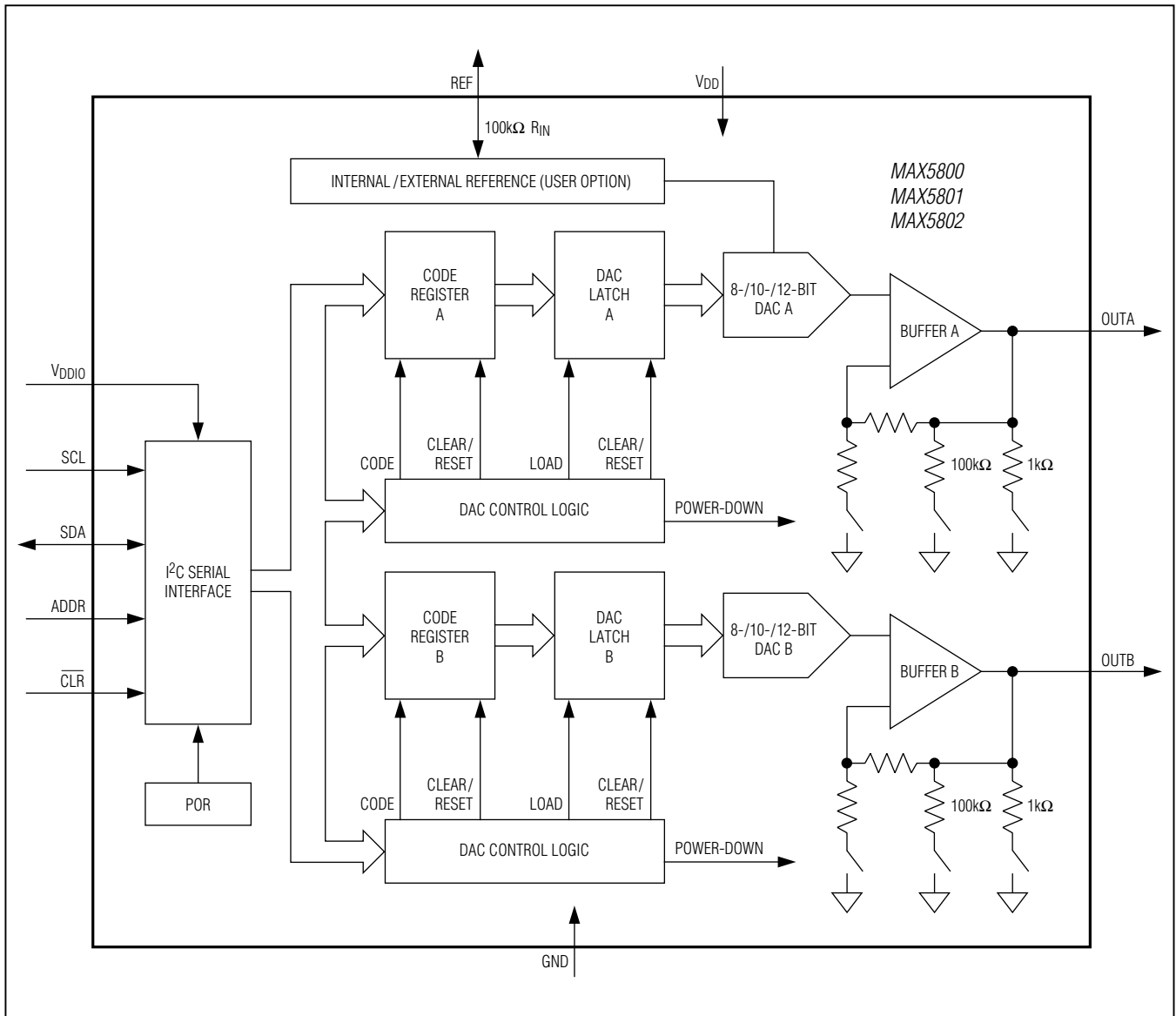
A major carry transition occurs at the midscale point where the MSB changes from low to high and all other bits change from high to low, or where the MSB changes from high to low and all other bits change from low to high. The duration of the magnitude of the switching glitch during a major carry transition is referred to as the digital-to-analog glitch impulse.

The digital-to-analog power-up glitch is the duration of the magnitude of the switching glitch that occurs as the device exits power-down mode.

# MAX5800/MAX5801/MAX5802

## Ultra-Small, Dual-Channel, 8-/10-/12-Bit Buffered Output DACs with Internal Reference and I<sup>2</sup>C Interface

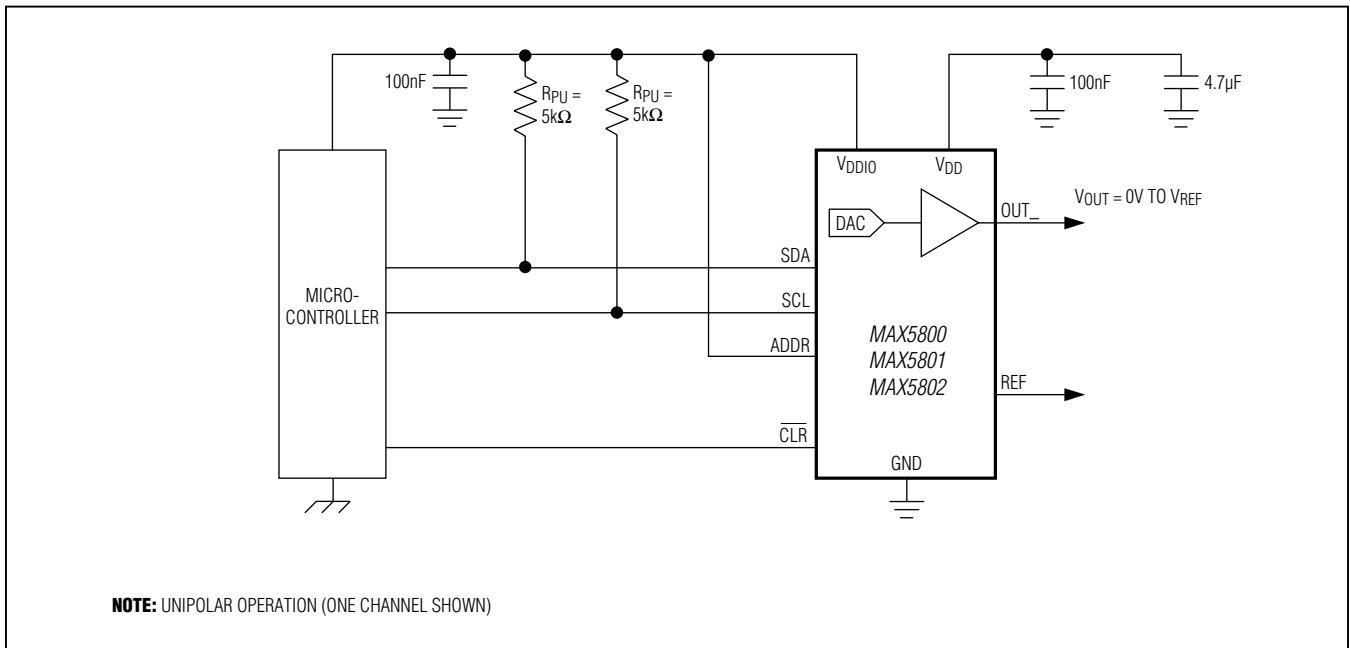
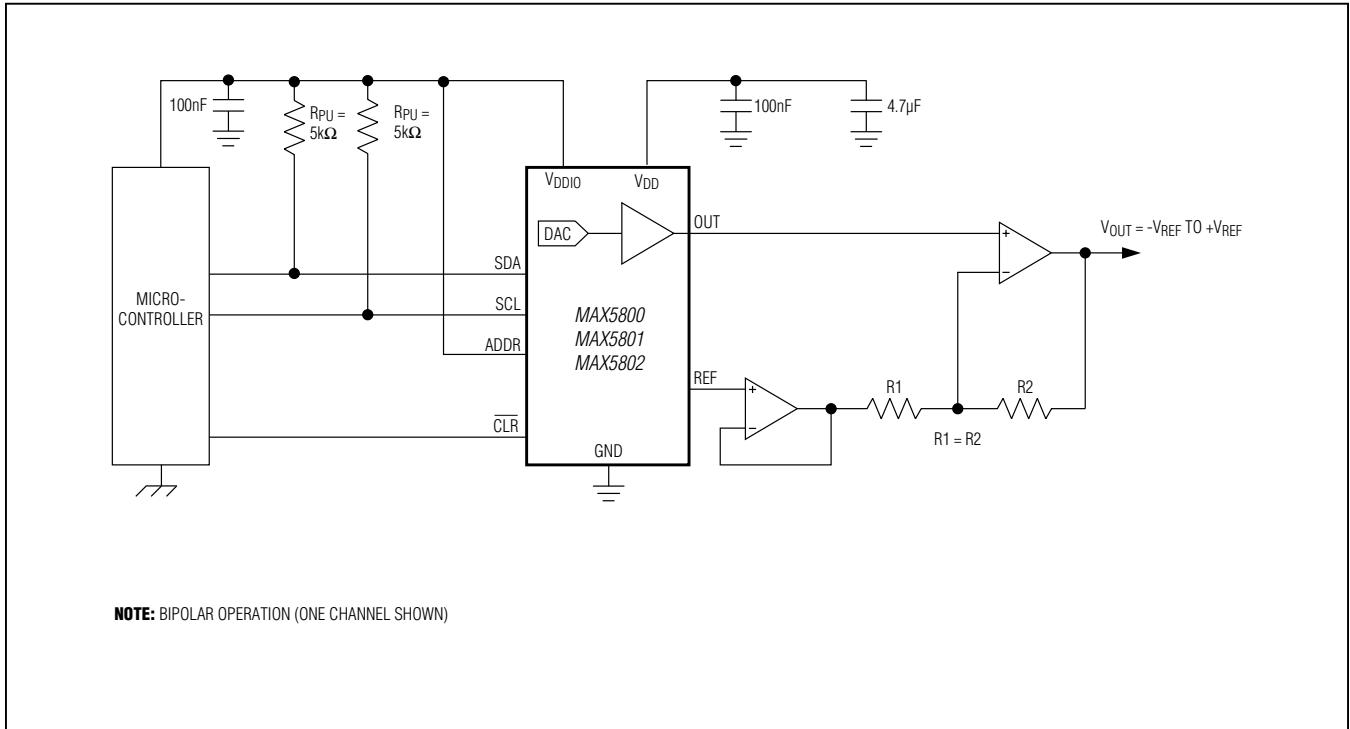
### Detailed Functional Diagram



# MAX5800/MAX5801/MAX5802

## Ultra-Small, Dual-Channel, 8-/10-/12-Bit Buffered Output DACs with Internal Reference and I<sup>2</sup>C Interface

### Typical Operating Circuits



# MAX5800/MAX5801/MAX5802

## Ultra-Small, Dual-Channel, 8-/10-/12-Bit Buffered Output DACs with Internal Reference and I<sup>2</sup>C Interface

### Ordering Information

| PART           | PIN-PACKAGE  | RESOLUTION (BIT) | INTERNAL REFERENCE TEMPCO (ppm/°C) |
|----------------|--------------|------------------|------------------------------------|
| MAX5800ATB+T*  | 10 TDFN-EP** | 8                | 10 (typ), 25 (max)                 |
| MAX5800AUB+T*  | 10 μMAX      | 8                | 10 (typ), 25 (max)                 |
| MAX5801ATB+T*  | 10 TDFN-EP** | 10               | 10 (typ), 25 (max)                 |
| MAX5801AUB+T*  | 10 μMAX      | 10               | 10 (typ), 25 (max)                 |
| MAX5802AAUB+T  | 10 μMAX      | 12               | 3 (typ), 10 (max)                  |
| MAX5802BATB+T* | 10 TDFN-EP** | 12               | 10 (typ), 25 (max)                 |
| MAX5802BAUB+T* | 10 μMAX      | 12               | 10 (typ), 25 (max)                 |

**Note:** All devices are specified over the -40°C to +125°C temperature range.

+Denotes a lead(Pb)-free/RoHS-compliant package.

T = Tape and reel.

\*Future product—Contact factory for availability.

\*\*EP = Exposed pad.

### Chip Information

PROCESS: BiCMOS

### Package Information

For the latest package outline information and land patterns (footprints), go to [www.maximintegrated.com/packages](http://www.maximintegrated.com/packages). Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

| PACKAGE TYPE | PACKAGE CODE | OUTLINE NO.             | LAND PATTERN NO.        |
|--------------|--------------|-------------------------|-------------------------|
| 10 μMAX      | U10+2        | <a href="#">21-0061</a> | <a href="#">90-0330</a> |
| 10 TDFN-EP   | T1033+1      | <a href="#">21-0137</a> | <a href="#">90-0003</a> |

# MAX5800/MAX5801/MAX5802

## Ultra-Small, Dual-Channel, 8-/10-/12-Bit Buffered Output DACs with Internal Reference and I<sup>2</sup>C Interface

### Revision History

| REVISION NUMBER | REVISION DATE | DESCRIPTION   | PAGES CHANGED |
|-----------------|---------------|---|---------------|
| 0               | 9/12          | Initial release   | —             |
| 1               | 12/12         | Updated <i>Electrical Characteristics</i> and <i>Ordering Information</i> | 2, 30         |



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