HF900

900V Offline Switching Regulator

The Future of Analog IC Technology

DESCRIPTION

The HF900 is a flyback regulator with an integrated 900V MOSFET. Requiring a minimum number of external components, the HF900 provides excellent power regulation in AC/DC applications that require high reliability. These applications include smart meters, large appliances, industrial controls, and products powered by unstable AC grids.

The regulator uses peak-current-mode control to provide excellent transient response and easy loop compensation. When the output power falls below a given level, the regulator enters burst mode to lower the standby power consumption.

The MPS proprietary 900V monolithic process enables over-temperature protection (OTP) on the same silicon of the 900V power FET, offering precise thermal protection. Also, it offers a full suite of protection features such as V_{CC} under-voltage lockout, over-load protection, over-voltage protection, and short-circuit protection.

The HF900 is designed to minimize electromagnetic interference for wireless communication in home and building automation applications. The operating frequency is programmed externally with a single resistor, so the power supply's radiated energy can be designed to avoid the interference with wireless communication.

In addition to the programmable frequency, the HF900 employs a frequency jittering function that not only greatly reduces the noise level but also reduces the cost of the EMI filter.

The HF900 is available in SOIC14-11 and PDIP8-7EP packages.

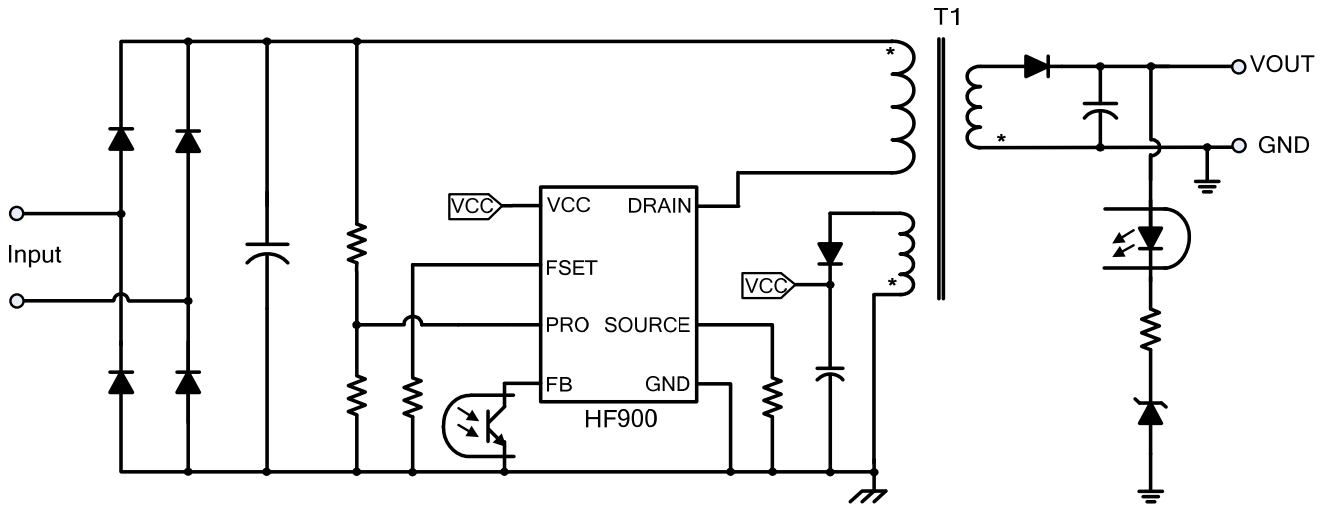
FEATURES

- Internal Integrated 900V MOSFET
- Programmable Fixed Switching Frequency up to 300kHz
- Frequency Jittering
- Current-Mode Operation
- Internal High-Voltage Current Source
- Low Standby Power Consumption via Active Burst Mode
- Internal Leading Edge Blanking
- Built-In Soft-Start Function
- Internal Slope Compensation
- Built-In Input Over-Voltage Protection
- Over-Temperature Protection (OTP)
- V_{CC} Under-Voltage Lockout with Hysteresis
- Over-Voltage Protection on V_{CC}
- Time-Based Overload Protection
- Short-Circuit Protection (SCP)

APPLICATIONS

- Smart Power Meters
- Large Appliances
- Industrial Controls
- All AC/DC Supplies Sold Where Power Grid may be Unstable

TYPICAL APPLICATION



ORDERING INFORMATION

Part Number*	Package	Top Marking
HF900GPR	PDIP8-7EP	*See Below*
HF900GS	SOIC14-11	*See Below*

* For Tape & Reel, add suffix –Z (e.g. HF900GPR–Z);

TOP MARKING (PDIP8-7EP)

HF900
MPSYYWW
LLLLLLLL

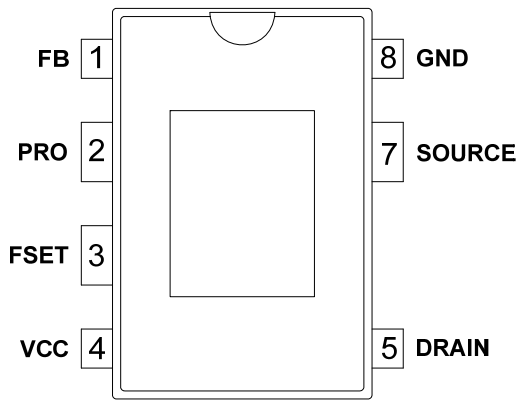
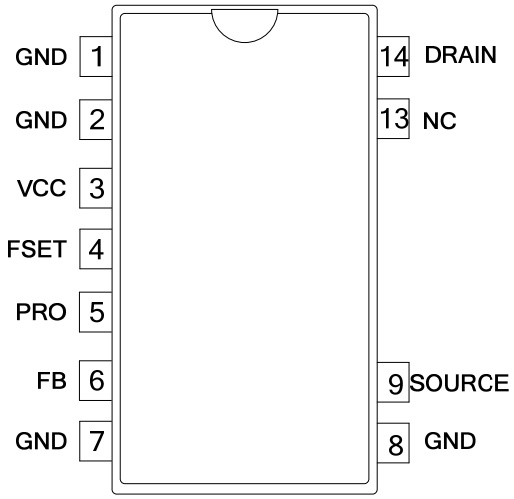
HF900: part number;
MPS: MPS prefix:
YY: year code;
WW: week code:
LLLLLLLL: lot number;

TOP MARKING (SOIC14-11)

MPSYYWW
HF900
LLLLLLLLL

MPS: MPS prefix:
YY: year code;
WW: week code:
HF900: part number;
LLLLLLLLL: lot number;

PACKAGE REFERENCE

TOP VIEW	TOP VIEW
	
PDIP8-7EP	SOIC14-11

ABSOLUTE MAXIMUM RATINGS (1)

DRAIN.....–0.3V to 900V
VCC .....–0.3V to 30V
All other pins .....–0.3V to 6.5V
Continuous power dissipation (T_A = +25°C) (2)
PDIP8-7EP 1.47W
SOIC14-11 ..... 1.45W
Junction temperature .....150°C
Lead temperature .....260°C
Storage temperature..... -60°C to +150°C
ESD capability human body model 2.0kV
ESD capability charged device model 2.0kV

Recommended Operation Conditions (3)

VCC to GND .....10.1 V to 24.5 V
Operating junction temp (T_J).. -40 °C to +125 °C

Thermal Resistance (4) θ_{JA} θ_{JC}

	θ_{JA}	θ_{JC}	
PDIP8-7EP	68	7	°C/W
SOIC14-11	70	35	°C/W

NOTES:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

V_{CC} =12V, T_J=-40°C~125°C, Min & Max are guaranteed by characterization, typical is tested under 25°C, unless otherwise noted.

Parameter	Symbol	Conditions		Min	Typ	Max	Unit
Start-Up Current Source (DRAIN)							
Supply current from DRAIN	I_{Charge}	VCC = 6V; V_{Drain} = 400V		1.35	2	3.1	mA
Leakage current from DRAIN	I_{Leak}	VCC = 13V; V_{Drain} = 400V			15	30	μA
Breakdown voltage	$V_{(BR)DSS}$	$I_{leakage}$ = 100μA		900			V
On-state resistance	$R_{DS(ON)}$	VCC = 10.1V; I_{Drain} = 100mA	T_J = 25°C		13	17	Ω
			T_J = 125°C		22	26	Ω
Supply Voltage Management (VCC)							
VCC upper level where the IC switches on	V_{CCH}			11.5	13.0	14.5	V
VCC lower level where the IC switches off	V_{CCL}			8.9	9.4	10.1	V
VCC hysteresis	V_{CC_HYS}			2.7	3.6	4.6	V
VCC OVP level	V_{OVP}			24.5	26.0	27.3	V
VCC re-charge level where the protection occurs	V_{CCR}			4.5	5.3	6	V
Quiescent current at protection phase	I_{Pro}	VCC = 6V				700	μA
Quiescent current	I_Q	VCC = 13V			780	980	μA
Operation current	I_{CC}	VCC = 13V; f_S = 100kHz			1.7	2	mA
Feedback Management (FB)							
Internal pull-up resistor	R_{FB}				10		kΩ
Internal pull-up voltage	V_{UP}			3.8	4.1	4.4	V
FB to current-set-point division ratio	I_{div}				3.3	3.6	
Internal soft-start time	T_{SS}				3		ms
FB decreasing level where the regulator enters burst mode	V_{BURL}			0.4	0.5	0.6	V
FB increasing level where the regulator leaves burst mode	V_{BURH}			0.58	0.70	0.86	V
Overload set point	V_{OLP}			3.5	3.8	4.1	V
Overload delay time	T_{Delay}	f_S = 100kHz			82		ms
Timing Resistor (FSET)							
FSET reference voltage	V_{FSET}			1.15	1.23	1.3	V
Frequency spectrum jittering range in percentage of Fs	$R_{Jittering}$	Example: f_S = 100kHz, then jittering is ±4kHz			±4		%
Typical operating frequency	f_S	T_J = 25°C; R_{FSET} = 100kΩ		90	104	118	kHz

ELECTRICAL CHARACTERISTICS

V_{CC} =12V, T_J=-40°C~125°C, Min & Max are guaranteed by characterization, typical is tested under 25°C, unless otherwise noted.

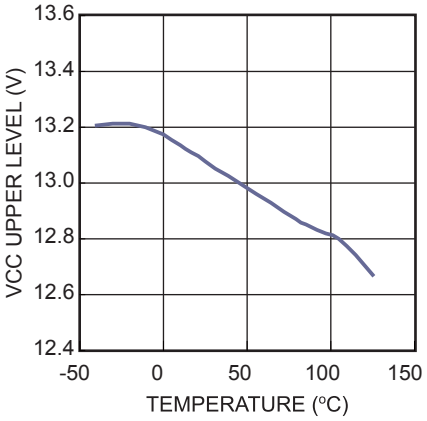
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Current Sampling Management (SOURCE)						
Leading edge blanking for current sensor	T_{LEB1}			350		ns
Leading edge blanking for SCP	T_{LEB2}			300		ns
Maximum current set point	V_{CS}		0.90	0.97	1.04	V
Short-circuit protection set point	V_{SC}		1.32	1.42	1.62	V
Slope compensation ramp	S_{Ramp}	f_S = 100kHz		40		mV/μs
Protection Management (PRO)						
Protection voltage	V_{PRO}		2.92	3.1	3.32	V
Protection hysteresis	V_{HY}			0.2		V
Thermal Shutdown						
Thermal shutdown threshold(5)				150		°C
Thermal shutdown recovery hysteresis(5)				30		°C

Notes:

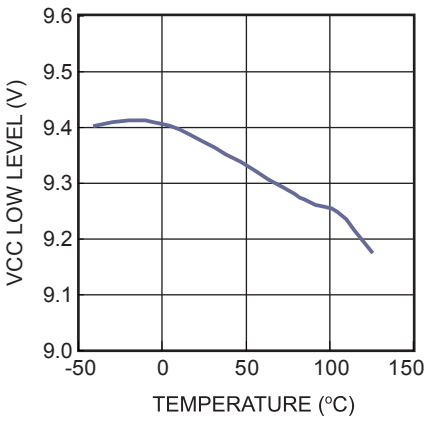
5) Guaranteed by Design & Characterization.

TYPICAL CHARACTERISTICS

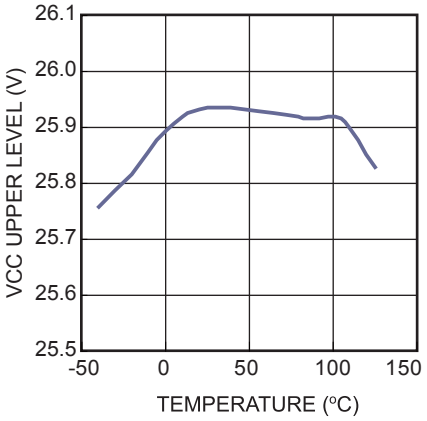
VCC Upper Level vs. Temperature



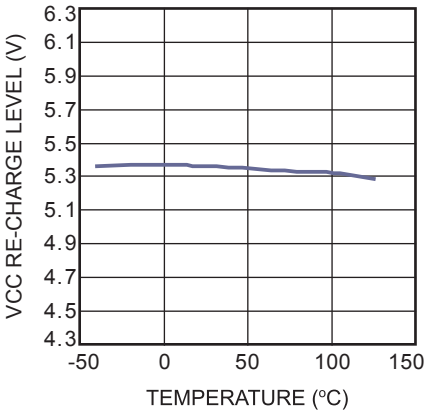
VCC Low Level vs. Temperature



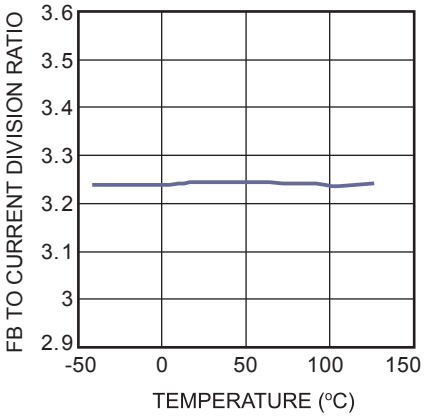
VCC OVP Threshold Voltage vs. Temperature



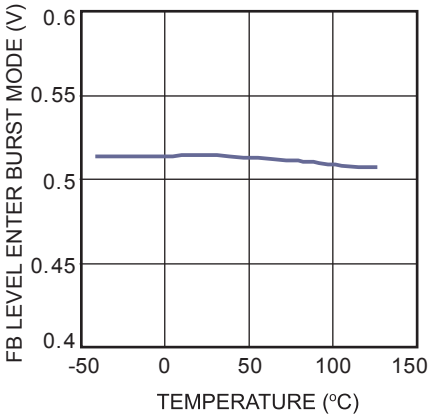
VCC Re-Charge Level vs. Temperature



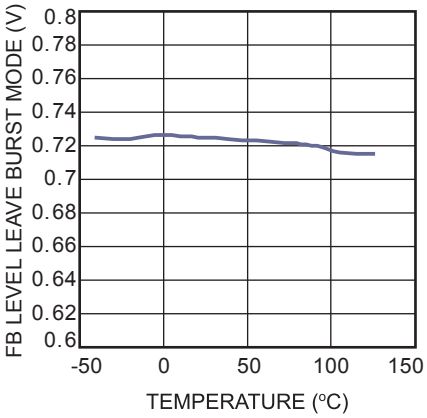
FB to Current Division Ratio vs. Temperature



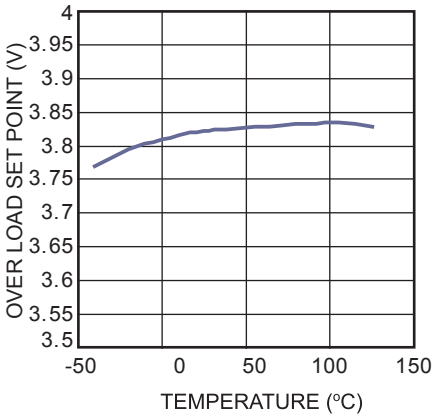
FB Level Enter Burst Mode vs. Temperature



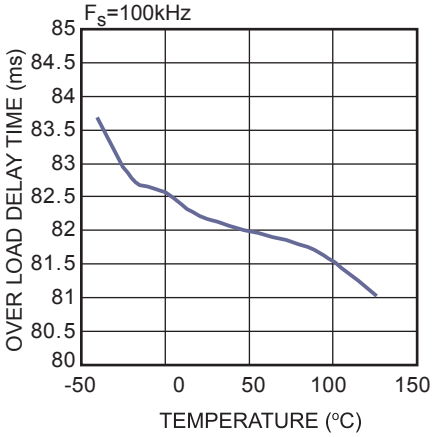
FB Level Leave Burst Mode vs. Temperature



Over Load Set Point vs. Temperature

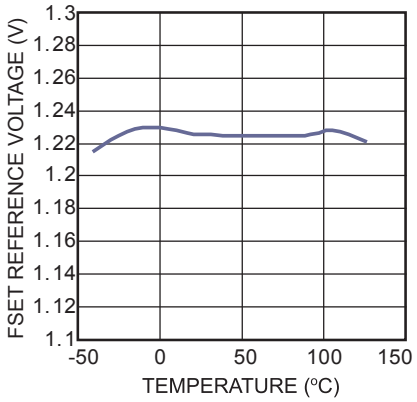


Over Load Delay Time vs. Temperature

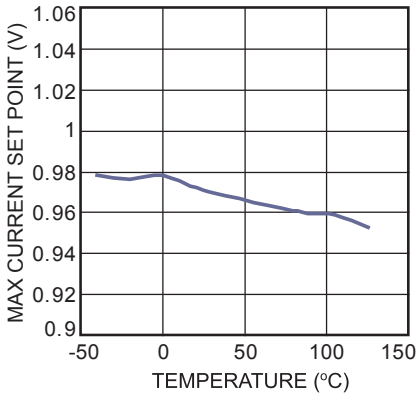


TYPICAL CHARACTERISTICS *(continued)*

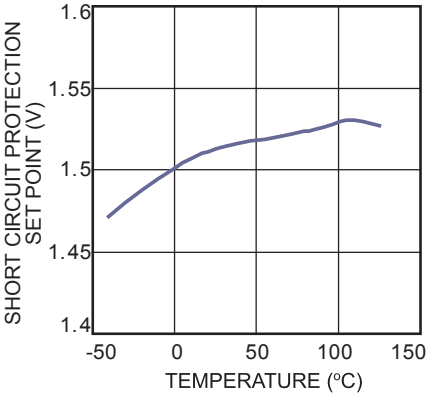
Fset Reference Voltage vs. Temperature



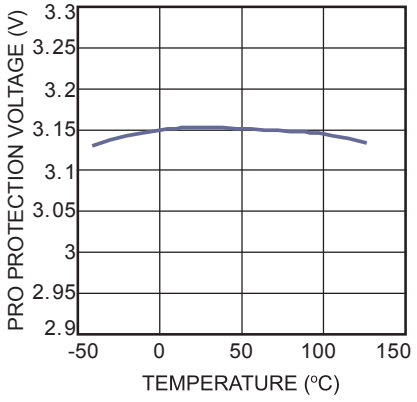
Max Current Set Point vs. Temperature



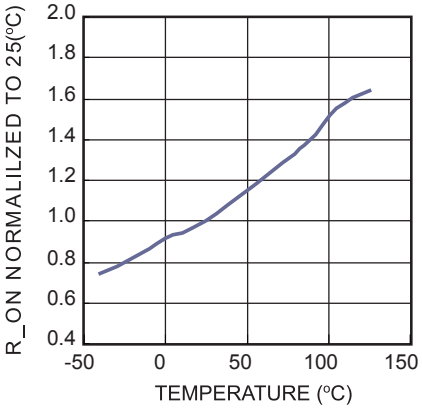
Short Circuit Protection Set Point vs. Temperature



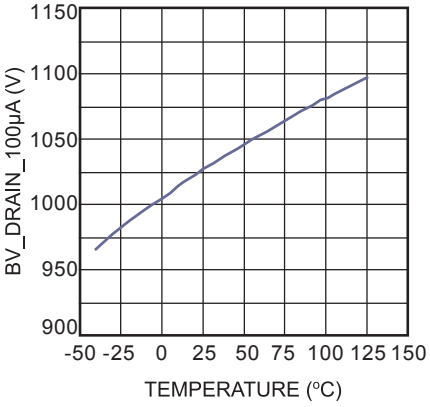
Pro Protection Voltage vs. Temperature



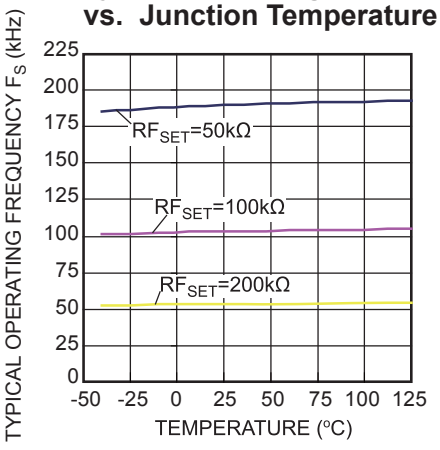
R_ON@V_{CC}=10.1V vs. Temperature



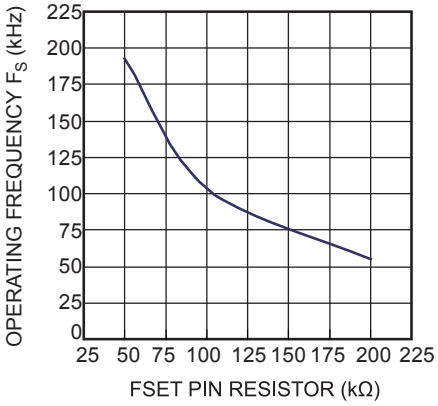
BV_Drain_100µA vs. Temperature



Typical Operating Frequency vs. Junction Temperature



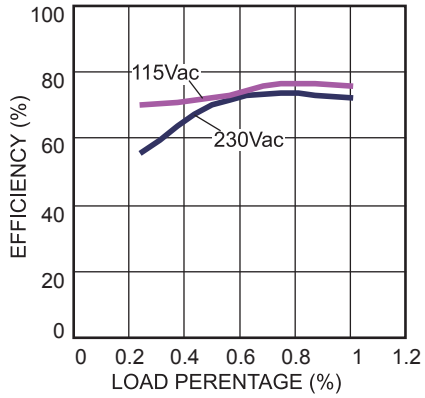
Typical Operating Frequency when T_J=25°C



TYPICAL PERFORMANCE CHARACTERISTICS

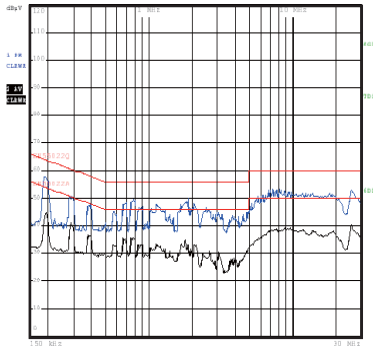
Performance waveforms are tested on the evaluation board of the Design Example section. V_{IN} = 230V, V_{OUT1} = 12.5V, V_{OUT2} = 5V, Primary Inductance=2.5mH, N_P:N_{AUX}:N_{S1}:N_{S2} = 125:14:14:9, T_A = 25°C, unless otherwise noted.

Efficiency



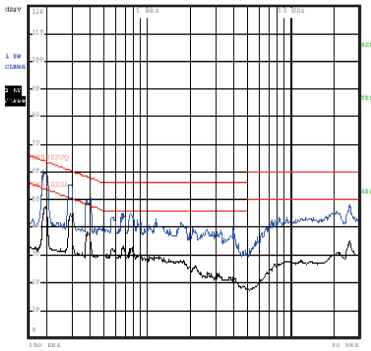
EMI

230Vac, Full Load, L Line



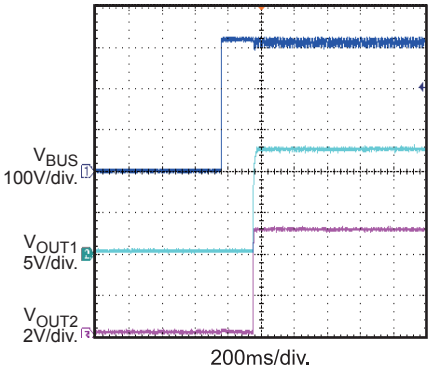
EMI

230Vac, Full Load, N Line



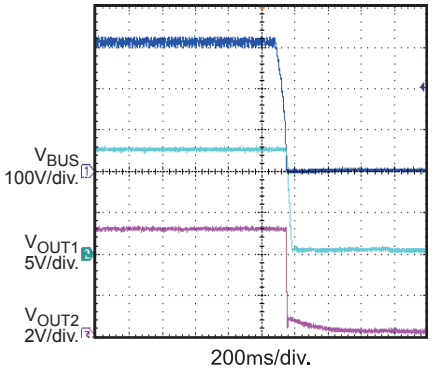
Startup

230Vac, Full Load



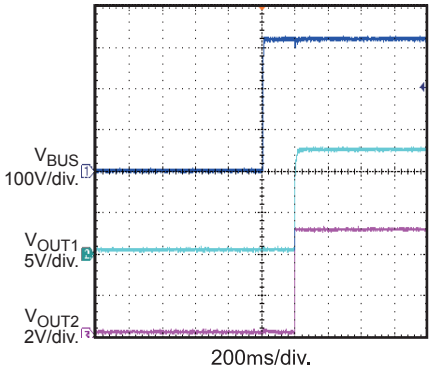
Shutdown

230Vac, Full Load



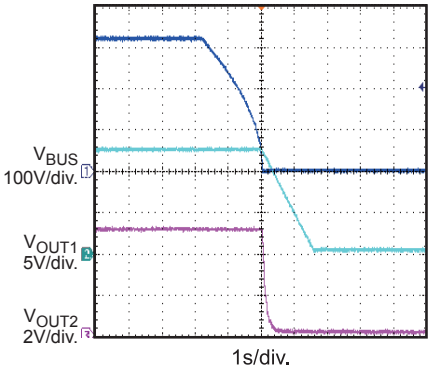
Startup

230Vac, No Load



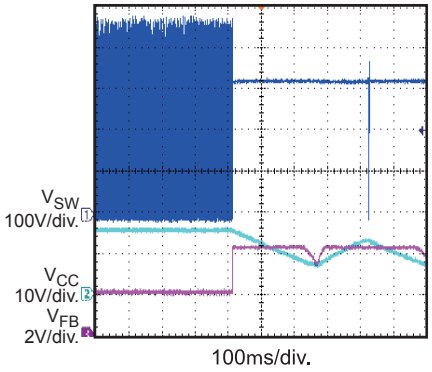
Shutdown

230Vac, No Load



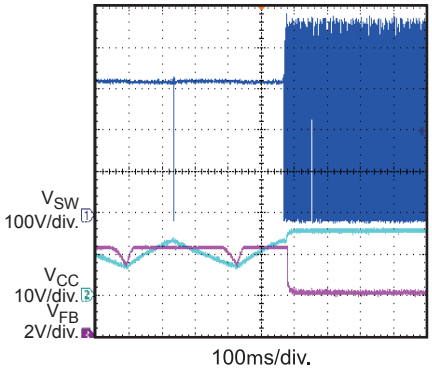
SCP Entry

230Vac, Full Load



SCP Recovery

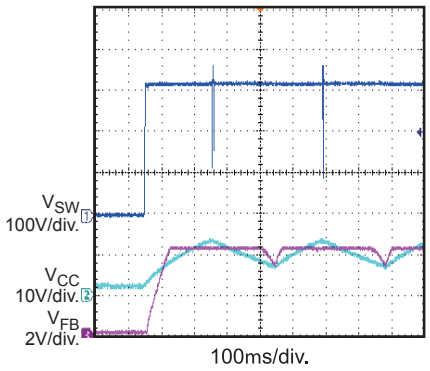
230Vac, Full Load



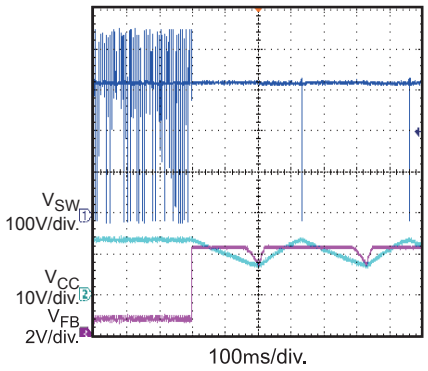
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board of the Design Example section. V_{IN} = 230V, V_{OUT1} = 12.5V, V_{OUT2} = 5V, Primary Inductance=2.5mH, N_P:N_{AUX}:N_{S1}:N_{S2} = 125:14:14:9, T_A = 25°C, unless otherwise noted.

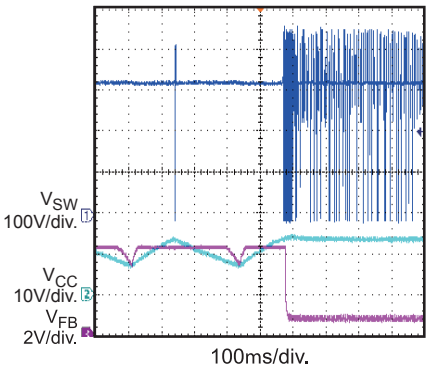
SCP Startup
230Vac, Full Load



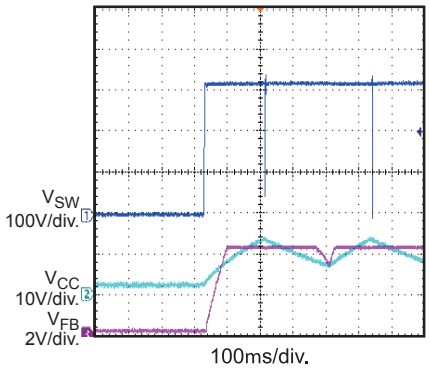
SCP Entry
230Vac, No Load



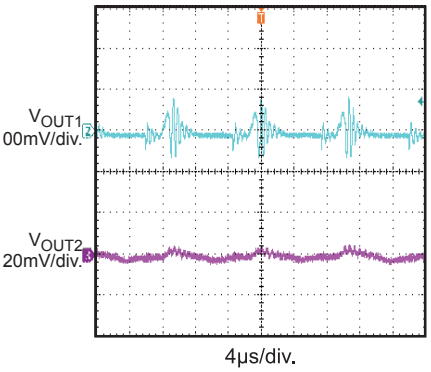
SCP Recovery
230Vac, No Load



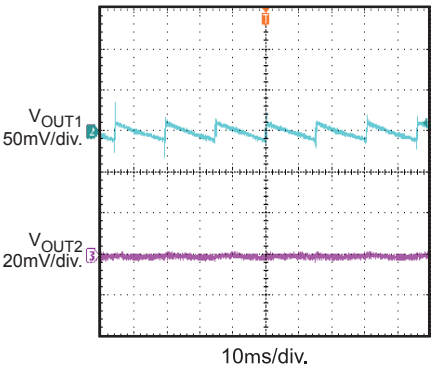
SCP Startup
230Vac, No Load



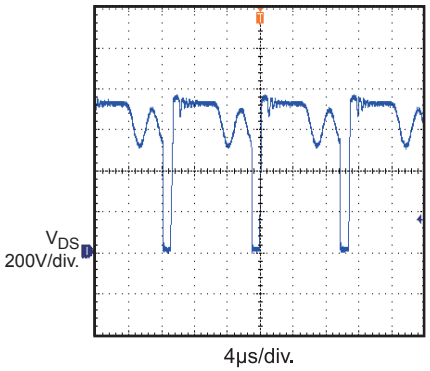
Output Ripple
230Vac, Full Load



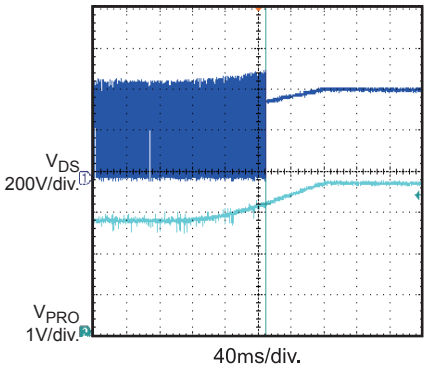
Output Ripple
230Vac, No Load



Stress
420Vac, Full Load



Pro Protection
230Vac, 300Vac Protection, Full Load



PIN FUNCTIONS

Pin # PDIP8-7EP	Pin # SOIC14-11	Name	Description
1	6	FB	**Feedback.** The output voltage from the external compensation circuit is fed into this pin. FB and the current sense signal from SOURCE determines the PWM duty cycle. A feedback voltage of V_{OLP} triggers overload protection while V_{BURL} triggers burst-mode operation. The regulator exits burst-mode operation and enters normal operation when the FB voltage reaches V_{BURH}.
2	5	PRO	**Input over-voltage protection.** When voltage on PRO rises to V_{PRO}, the IC is shut down with hysteresis.
3	4	FSET	**Switching converter frequency set.** Connect a resistor to GND to set the switching frequency up to 300kHz.
4	3	VCC	**Supply voltage**. Connect a 22μF bulk capacitor and a 0.1μF ceramic capacitor for most applications. When V_{CC} rises to V_{CCH}, the IC starts switching; when it falls below V_{CCL}, the IC stops switching.
5	14	DRAIN	**Drain of the internal MOSFET**. Input for the start-up high-voltage current source.
7	9	SOURCE	**Source of the internal MOSFET.** Input of the primary current sense signal.
8	1,2,7,8	GND	**IC ground.**
	13	NC	**Not connected.**

FUNCTIONAL BLOCK DIAGRAM

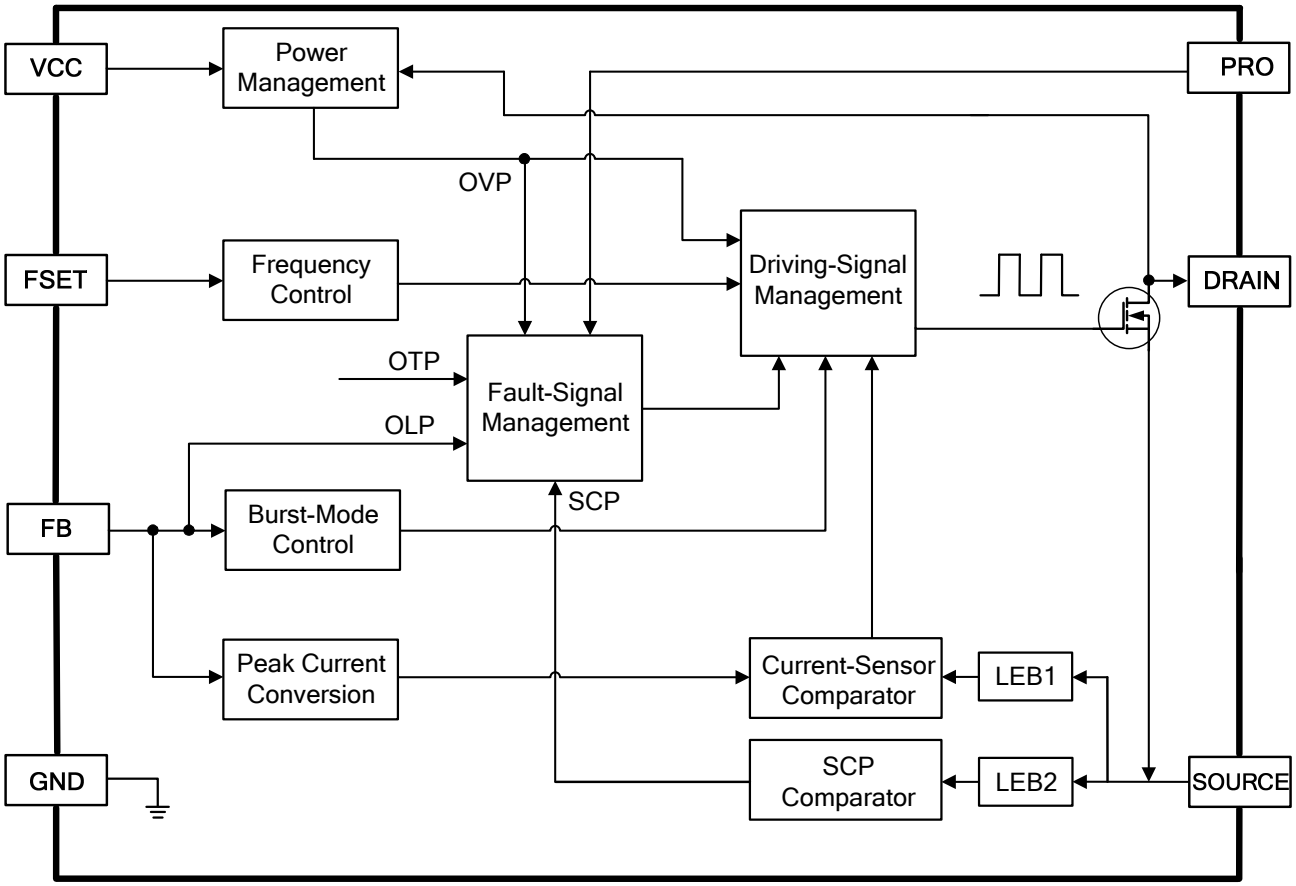


Figure 1: Internal Function Block Diagram

OPERATION

The HF900 integrates a 900V MOSFET for a reliable switch-mode power supply solution. It has burst-mode operation to minimize the standby power consumption at light load. Protection features such as auto-recovery for overload protection (OLP), short-circuit protection (SCP), over-voltage protection (OVP), and thermal shutdown for over-temperature protection (OTP) contribute to a safer converter design with minimal external components.

PWM Operation

The HF900 employs peak-current-mode control. On the secondary side, the output voltage is divided by a voltage divider network. This voltage is fed back to the primary side as voltage on the FB using an optocoupler and a shunt regulator. The voltage at FB is compared to the V_{Sense} voltage, which measures the MOSFET switching current. The integrated MOSFET turns on at the beginning of each clock cycle. The current in the transformer magnetizing inductance increases until it reaches the value set by the FB voltage, and then the integrated MOSFET turns off.

Start-Up and VCC UVLO

Initially, the IC is driven by the internal current source, which is drawn from the high-voltage DRAIN. The IC starts switching, and the internal high-voltage current source turns off as soon as the voltage on VCC reaches V_{CCH}. At this point, the supply of the IC is taken over by the auxiliary winding of the transformer. When VCC falls below V_{CCL}, the regulator stops switching, and the internal high-voltage current source turns on again (see Figure 2).

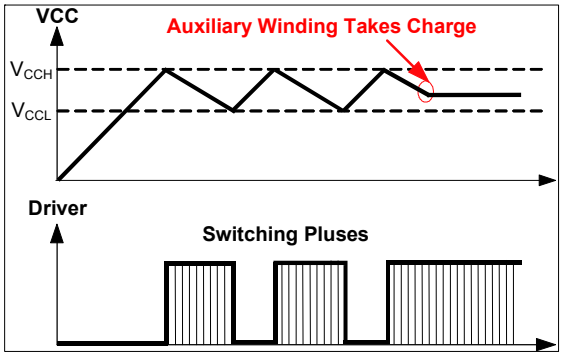


Figure 2: VCC Start-Up

The lower threshold of VCC UVLO decreases from V_{CCL} to V_{CCR} when fault conditions such as SCP, OLP, OVP, and OTP occur.

Soft Start

The HF900 implements an internal soft-start circuit to reduce stress on the primary-side MOSFET and the secondary diode and smoothly establish the output voltage during start-up. The internal soft-start circuit increases the primary current sense threshold gradually, which determines the MOSFET peak current during start-up. The pulse width of the power switching device is increased progressively to establish correct operating conditions until the feedback control loop takes charge (see Figure 3).

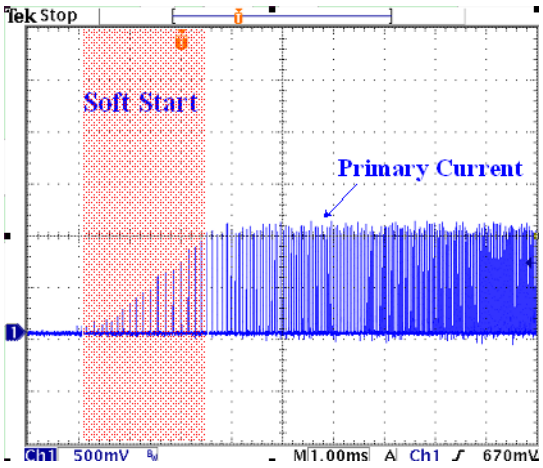


Figure 3: Soft Start

Switching Frequency

The switching frequency of the HF900 can be set by FSET. The frequency can be set by a resistor between FSET and GND. The oscillator frequency can be attained using Equation (1):

$$f_S = \frac{1}{200\times10^{-9} + 112.5\times10^{-12}\times\frac{R_{FSET}}{V_{FST}}}\ Hz \quad (1)$$

V_{FST} (1.23V) is the FSET pin reference voltage.

Over-Voltage Protection (OVP)

Monitoring the VCC voltage via a 20μs time constant filter allows the HF900 to enter OVP during an over-voltage condition, typically when V_{CC} goes above V_{OVP}. The regulator will resume operation once the fault disappears.

Overload Protection (OLP)

The HF900 shuts down when the power supply experiences an overload. OLP is achieved by monitoring the FB voltage continuously. A fault signal is triggered when FB pulls up to 3.8V (V_{OLP}, typical value) and after an 82ms delay (8192 switching cycle, f_S = 100kHz). If the fault signal is still present, the HF900 shuts down. When the fault disappears, the power supply resumes operation. The OLP delay time can be attained using Equation (2):

$$T_{Delay} = \frac{82ms \times 100kHz}{f_S} \quad (2)$$

Short-Circuit Protection (SCP)

The HF900 shuts down when voltage on CS is higher than V_{SC}, which indicates a short circuit. The HF900 enters a safe low-power mode that prevents any thermal or stress damage. As soon as the fault disappears, the power supply resumes operation.

Thermal Shutdown (OTP)

When the junction temperature of the IC exceeds 150℃, the over-temperature protection is activated and stops output driver switching to prevent the HF900 from any thermal damage. As soon as the junction temperature drops below 120℃, the regulator resumes operation. During the protection period, the regulator enters auto-recovery mode. The VCC voltage is discharged to V_{CCR} and is re-charged to V_{CCH} by the internal high-voltage current source.

Burst Operation

To minimize standby power consumption, the HF900 implements burst mode at no load and light load. As the load decreases, the FB voltage decreases. The IC stops switching when the FB voltage drops below 0.5V (V_{BRUL}, typical value). As the load power increases, the output voltage drops at a rate dependent on the load. This causes the FB voltage to rise again due to the negative feedback control loop. Once the FB voltage exceeds 0.7V (V_{BRUH}, typical value), the switching pulse resumes. The FB voltage then decreases, and the whole process repeats. Burst-mode operation alternately enables and disables the switching pulse of the MOSFET. Hence switching loss at no load and light load conditions is reduced greatly.

Figure 4 shows the burst-mode operation of the HF900.

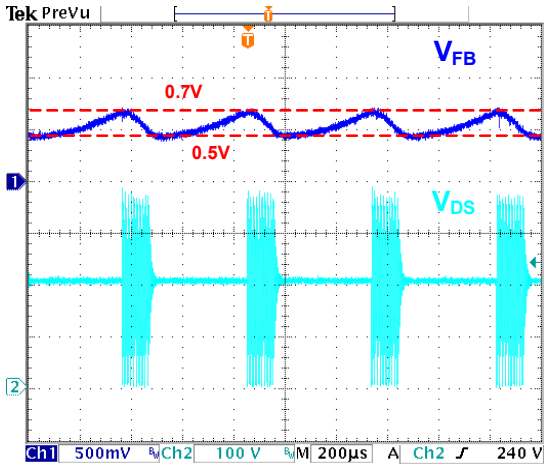


Figure 4: Burst-Mode Operation

PRO

PRO provides extra protection against abnormal conditions. Use PRO for input OVP or other protections (input UVP, over-temperature protection for key components, etc.). If the PRO voltage exceeds 3.1V (V_{PRO}, typical value), the IC shuts down to enter auto-recovery mode. Once the fault disappears, the power supply resumes operation.

Peak Current Limit

In normal operation, the primary peak current is sensed by a sensing resistor between SOURCE and GND. The turn-off threshold of the MOSFET is set by the FB voltage ($V_{Sense} = V_{FB}/I_{div}$). When the sensing resistor voltage reaches V_{Sense}, the MOSFET turns off. The I_{div} is the FB to the current-set-point division ratio.

During an overload condition, the primary peak current threshold is limited internally to the maximum value of 0.97V (V_{CS}, typical value), even if the V_{FB} voltage exceeds 3.2V, to avoid excessive output power and lower the switch voltage rating.

During the start-up period, the primary peak current threshold increases internally to the maximum current set point (V_{CS}) gradually.

Leading Edge Blanking (LEB)

In order to avoid turning off the MOSFET by mis-trigger spikes shortly after the switch turns

on, the IC implements leading edge blanking. During the blanking time, any trigger signal on SOURCE is blocked. An internal leading edge blanking (LEB) unit containing two LEB times is employed between SOURCE and the current comparator input to avoid premature switching pulse termination due to the parasitic capacitances. During the blanking time, the current comparator is disabled and cannot turn off the MOSFET.

Current sensor leading edge blanking inhibits the current limitation comparator for 350ns (T_{LEB1}, typical value), and the SCP leading edge blanking inhibits the SCP current comparator for 300ns (T_{LEB2}, typical value). Figure 5 shows the primary current sense waveform and the leading edge blanking.

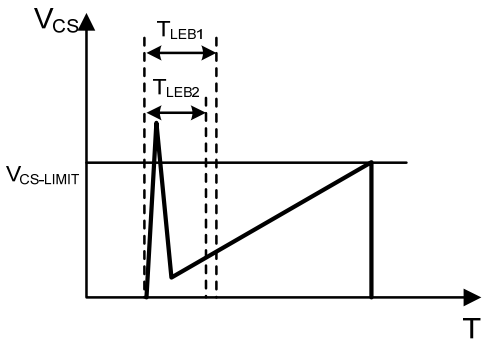


Figure 5: Leading Edge Blanking

APPLICATION INFORMATION

Selecting the Input Capacitor

The bulk capacitors of the rectifier bridge filter the rectified AC input, which supplies the DC input voltage for the converter. Figure 6 shows the typical DC bus voltage waveform of a full-bridge rectifier.

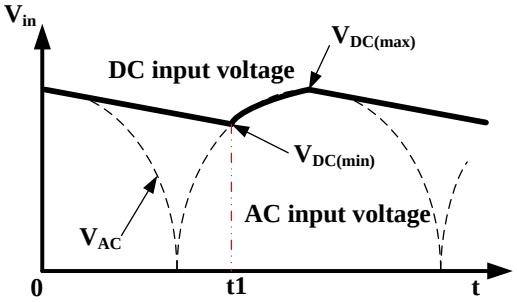


Figure 6: Input Voltage Waveform

When the full-bridge rectifier is used, usually the input capacitor is set at 2μF/W for the universal input condition (85~265V_{AC}). For high-voltage input (>185VAC) application, cut the capacitor values in half. The input power (P_{in}) is estimated with Equation (3):

$$P_{in} = \frac{V_O \times I_O}{\eta} \quad (3)$$

Where V_O is the output voltage, I_O is the rated output current, and η is the estimated efficiency. Generally, η is between 0.75 and 0.85 depending on the input range and output application.

From the waveform in Figure 6, the AC input voltage (V_{AC}) and the DC input voltage (V_{DC}) are calculated using Equation (4):

$$V_{DC}(V_{AC}, t) = \sqrt{2 \times V_{AC}^2 - \frac{2 \times P_{in}}{C_{in}} \times t} \quad (4)$$

V_{AC} starts to charge the input capacitor when the DC bus voltage reaches the minimum value (V_{DC} = $V_{AC,}$ approximately). t1 can be calculated using Equation (5):

$$V_{DC(min)} = V_{DC}(V_{AC(min)}, t1) \quad (5)$$

Very low DC input voltage can cause a thermal problem in a full load. It is recommended that the minimum DC voltage is higher than 70V. Otherwise the input capacitor value should be increased.

As a 900V offline regulator, the HF900 suits very high-voltage input applications. General input capacitors with 400V voltage ratings cannot satisfy the safety requirement. Thus, stack capacitors can be used in very high input voltage applications such as a 420VAC input (see Figure 7).

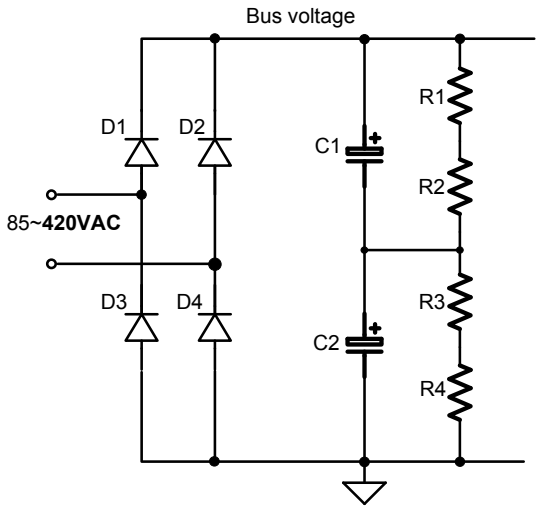


Figure 7: Input Stack Capacitor Circuit

C1 and C2 endure half of the input DC voltage rating, respectively. R1 to R4 should use the same value resistor to equalize the C1 and C2 voltage stress. It is recommended to use a 1206 package for R1 to R4 to satisfy the safety requirement. Also, the R1 to R4 values should be large enough for energy saving. For example, the total value of R1 to R4 is 20MΩ, which consumes about 18mW in 600VDC bus voltage.

Primary-Side Inductor Design (L_m)

Normally, the converter is designed to operate in CCM with low input voltage. CCM is needed to satisfy the output energy requirement for the universal input condition. With a built-in slope compensation function, the HF900 supports CCM when the duty cycle exceeds 50%. Set the ratio (K_P) of the primary inductor ripple current amplitude vs. the peak current value to $0 < K_P \leq 1$, where K_P = 1 for DCM. Figure 8 shows the relevant waveforms. A larger inductor leads to a smaller K_P, which reduces RMS current but increases the transformer size. For 5W application, an optimal K_P value is between 0.8

and 1 for the universal input range and 1 for a 230VAC input range.

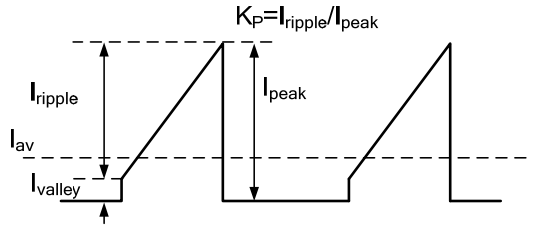


Figure 8: Typical Primary Current Waveform

For CCM at a minimum input, the converter duty cycle is determined using Equation (6):

$$D = \frac{(V_O + V_F) \times N}{(V_O + V_F) \times N + V_{DC(min)}} \quad (6)$$

Where:

V_F is the secondary diode's forward voltage, and

N is the transformer turns ratio.

The MOSFET turn-on time is calculated with Equation (7):

$$T_{ON} = \frac{D}{f_S} \quad (7)$$

Where, f_S is the operating frequency.

The input average current, ripple current, peak current, and valley current of the primary side are calculated using Equation (8), Equation (9), Equation (10) and Equation (11):

$$I_{AV} = \frac{P_{in}}{V_{DC(min)}} \quad (8)$$

$$I_{ripple} = K_P \times I_{peak} \quad (9)$$

$$I_{peak} = \frac{I_{AV}}{(1 - \frac{K_P}{2}) \times D} \quad (10)$$

$$I_{valley} = (1 - K_P) \times I_{peak} \quad (11)$$

Estimate L_m using Equation (12):

$$L_m = \frac{V_{DC(min)} \times T_{ON}}{I_{ripple}} \quad (12)$$

Current-Sense Resistor

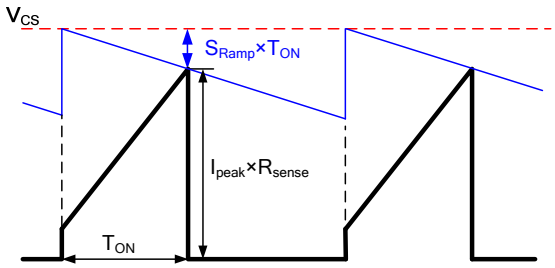


Figure 9: Slope Compensation Waveform

Figure 9 shows the slope compensation waveform. When the sum of the sense resistor voltage and the slope compensation voltage reaches the peak current limit (V_{CS}), the HF900 turns off the internal MOSFET. The maximum peak current limit is 0.97V (V_{CS}, typical value), and the slope compensation slew rate is 40mV/μs. Considering the margin, use $0.95 \times V_{CS}$ as the peak current limit at full load. The voltage on the sense resistor is given using Equation (13):

$$V_{sense} = 0.95 \times V_{CS} - S_{Ramp} \times T_{ON} \quad (13)$$

The value of the sense resistor is calculated using Equation (14):

$$R_{sense} = \frac{V_{sense}}{I_{peak}} \quad (14)$$

Use Equation (15) to select the current sense resistor with an appropriate power rating based on the power loss:

$$P_{sense} = \left[\left(\frac{I_{peak} + I_{valley}}{2} \right)^2 + \frac{1}{12} \times \left(I_{peak} - I_{valley} \right)^2 \right] \times D \times R_{sense} \quad (15)$$

PRO

Extra protection can be enabled using the HF900 PRO. A typical input over-voltage protection circuitry is shown in Figure 10.

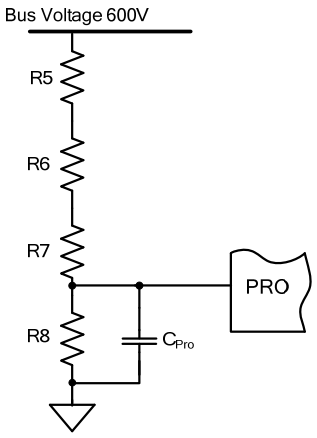


Figure 10: Input Over-Voltage Protection Setup

The input over-voltage protection point can be calculated using Equation (16):

$$V_{INOVP} = V_{PRO} \times \frac{R5 + R6 + R7 + R8}{R8} \quad (16)$$

For resistors R5 to R7, 1206 packages should be used for safety considerations. The total value should be larger than 10MΩ for energy saving purposes.

Switching voltage noise can occur if R% to R* have large values, which disturbs the PRO protection action. One ceramic capacitor (around 1nF) should be paralleled with PRO and GND. It should be located near the IC to decouple the switching voltage noise.

Frequency Jittering

The HF900 provides a frequency jittering function, which simplifies the input EMI filter design and decreases the system cost. The HF900 has optimized frequency jittering with a ±4% frequency deviation range and a $256T_S$ carrier cycle that effectively improves EMI by spreading the energy dissipation over the frequency range.

Thermal Performance Optimization

The HF900 is dedicated to high input voltage application. However, the high input voltage can cause greater switching loss on the MOSFET, especially under a high frequency, which may lead to poor thermal performance. Tests show that turn-on loss is dominant under a high input, so thermal performance optimization should focus mainly on reducing turn-on loss.

As we know that turn-on loss is caused by a turn-on current spike and V_{DS}, measures should be taken to reduce either the V_{DS} or the turn-on spike to get better thermal performance.

In order to reduce V_{DS}, use a small turns ratio-N to minimize the reflected output voltage on the primary MOSFET.

To suppress a turn-on spike of the MOSFET, CCM operation should be avoided, especially under a high input. The transformer structure should be designed to achieve minimum parasitic capacitance of each winding and between the primary and secondary windings.

For the HF900 PDIP8-7EP package, a heat sink can be used to further improve thermal performance in very critical applications.

In addition, choose an appropriate operating frequency for better thermal performance and EMI.

Table 1 shows the maximum output power test results of the HF900 (both packages were tested without a heat sink).

Table 1: Maximum Output Power

Package	f_s (kHz)	P_{MAX} (W)
PDIP8-7EP	50	7
	100	3
SOIC14-11	50	8
	100	4

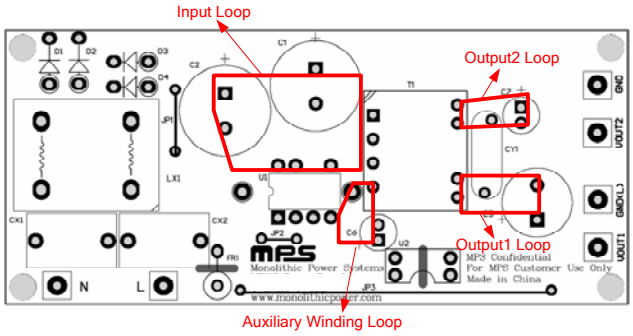
NOTES:
1. The maximum output power is tested under T_A = 50°C.
2. In order to reduce V_{DS}, the turns ratio is set to 5.
3. V_{IN} = 85~420VAC, single output, V_{OUT} = 12.5V.
4. PDIP8-7EP package is tested without a heat sink, and GND is connected to 2cm^2 copper areas. GND of the SOIC14-11 package is connected to 2.5cm^2 copper areas.
5. Working condition under V_{IN} = 85VAC is set to BCM.

PCB Layout Guidelines

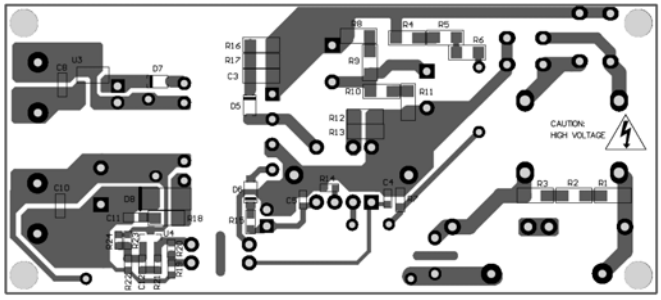
Efficient PCB layout is critical to achieve reliable operation, good EMI performance, and good thermal performance. For best results, refer to Figure 11 and follow the guidelines below:

1) Minimize the power stage switching stage loop area. This includes the input loop (C2–C1-T1–U1–R12/R13–C2), the auxiliary winding loop (T1–D6–C6–T1), the output loop (T1–D8–C9–T1 and T1–D7–C7–T1), and the RCD loop (T1–D5–R16/R17/C3–T1).
2) Keep the input loop, GND, and control circuit separate and only connect them at C2.

3) Connect the heat sink to the primary GND plane to improve EMI and thermal dissipation.
4) Place the control circuit capacitors (for FB, PRO, and VCC) close to the IC to decouple the switching voltage noise.
5) Enlarge the GND pad near the IC for good thermal dissipation.
6) Keep the EMI filter far away from the switching point.
7) Ensure the two outputs clearance distance satisfy the insulation requirement.



a) Top



b) Bottom

Figure 11: Recommended PCB Layout

Design Example

Table 2 is a design example using the application guidelines for the given specifications:

Table 2: Design Example

V_{IN}	85 to 420VAC
V_{OUT1}	12.5V
I_{OUT1}	0.4A
V_{OUT2}	5V
I_{OUT2}	0.05A
f_S	100kHz

The detailed application schematic is shown in Figure 12. The typical performance and circuit waveforms have been shown in the typical performance characteristics section. For more device applications, please refer to the related evaluation board datasheets.

TYPICAL APPLICATION CIRCUITS

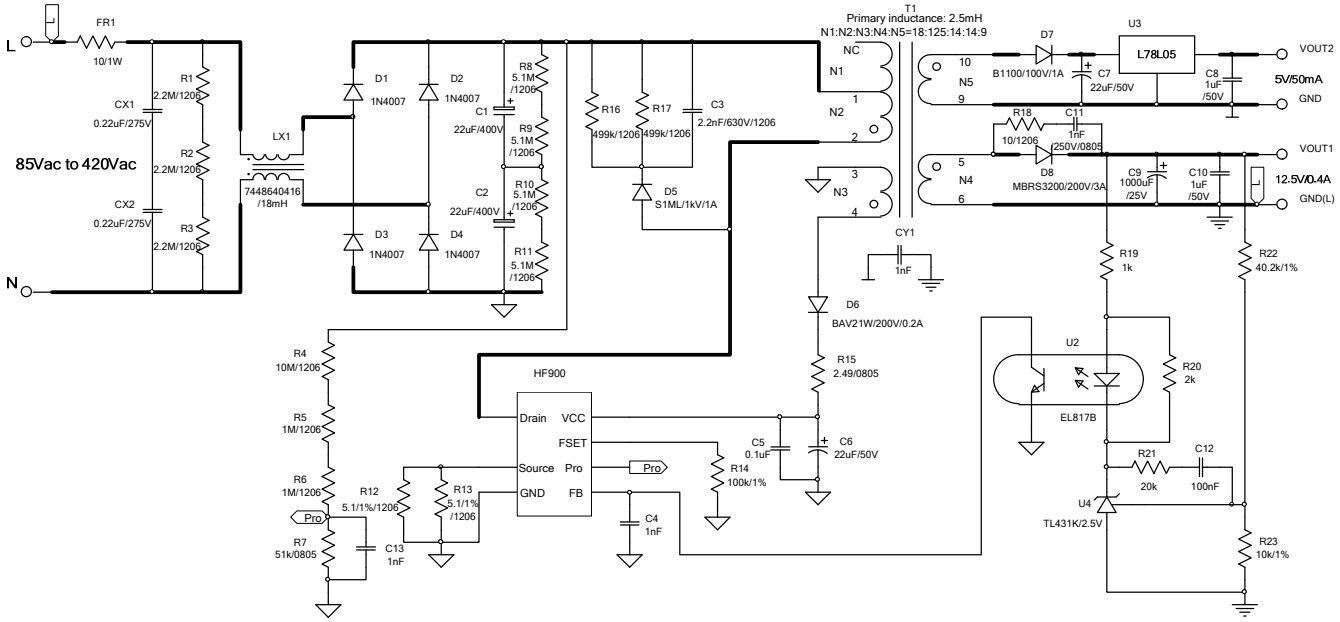
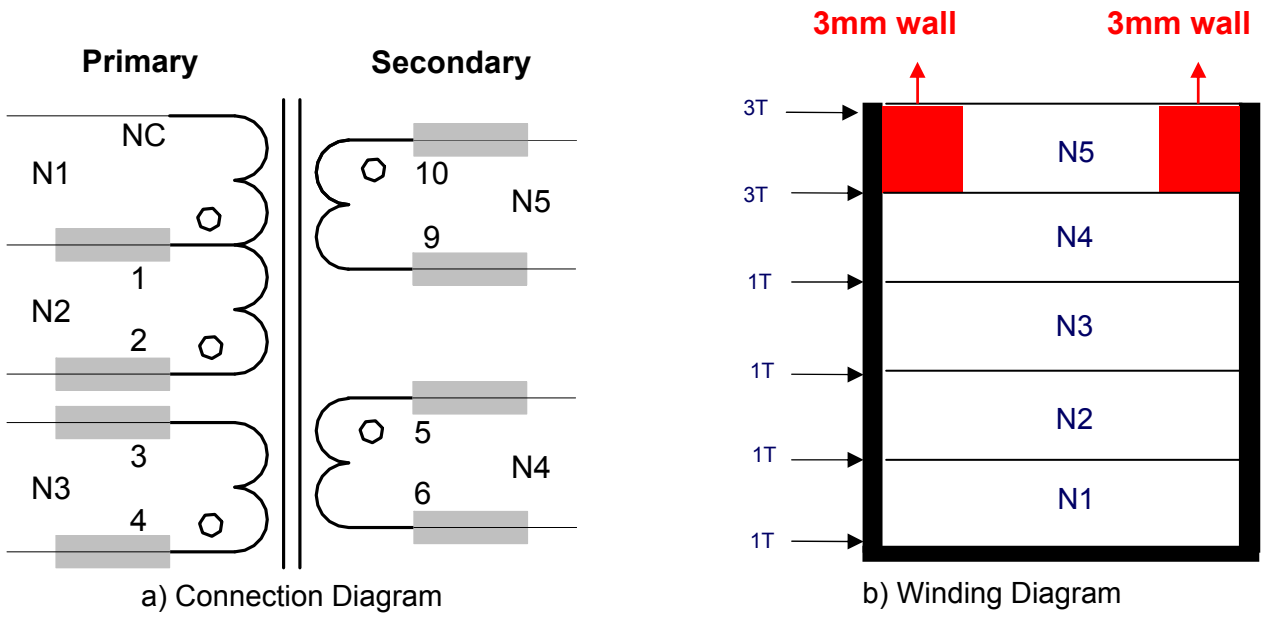


Figure 12: Typical Application Schematic



a) Connection Diagram

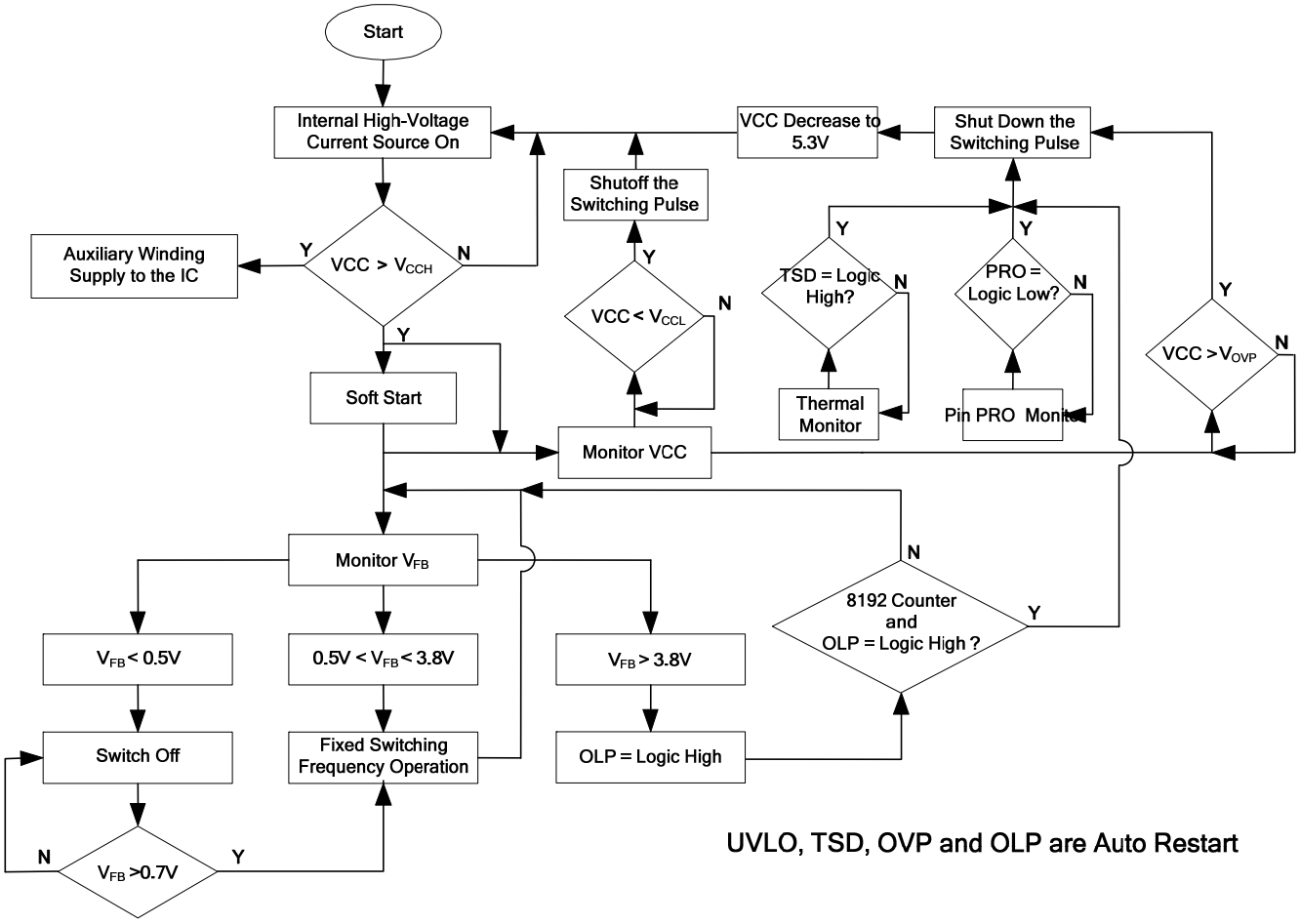
b) Winding Diagram

Figure 13: Transformer Structure

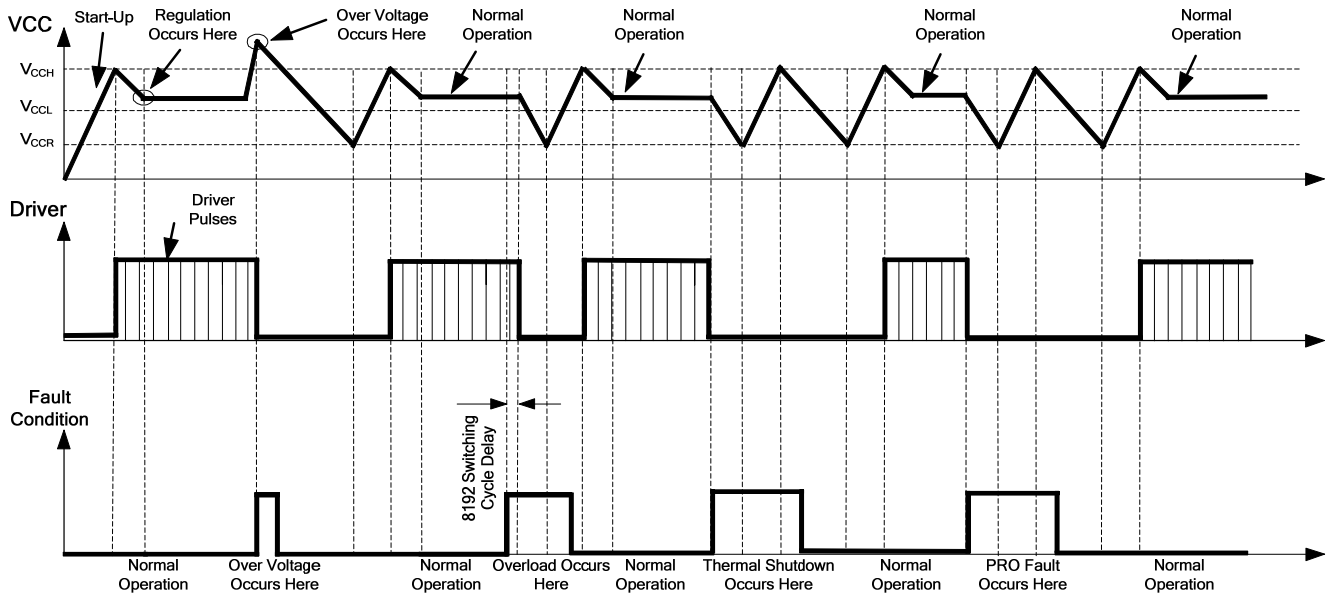
Table 3: Winding Order

Tape (T)	Winding	Margin Wall PRI side	Terminal Start—>End	Margin Wall SEC side	Wire Size (φ)	Turns (T)
1	N1	0mm	1→NC	0mm	0.18mm*2	18
1	N2	0mm	2→1	0mm	0.18mm*1	125
1	N3	0mm	4→3	0mm	0.15mm*1	14
1	N4	0mm	5→6	0mm	0.4mm*1	14
3	N5	3mm	10→9	3mm	0.2mm*1	9
3						

FLOW CHART

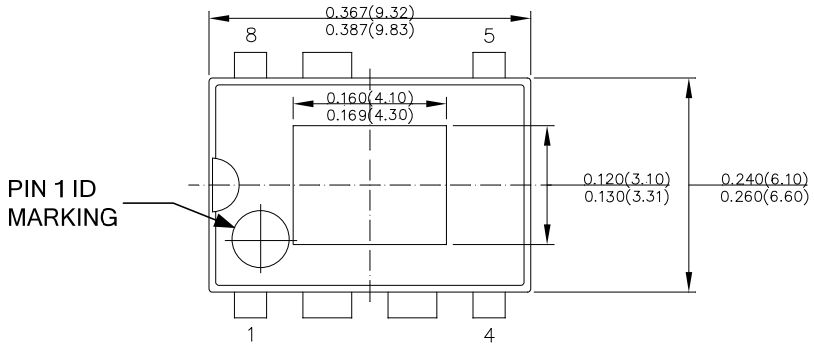


EVOLUTION OF THE SIGNALS IN PRESENCE OF FAULTS

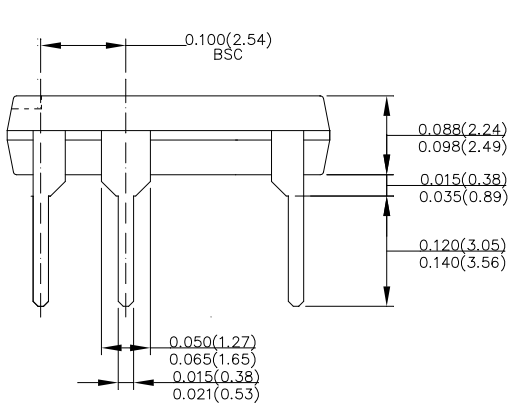


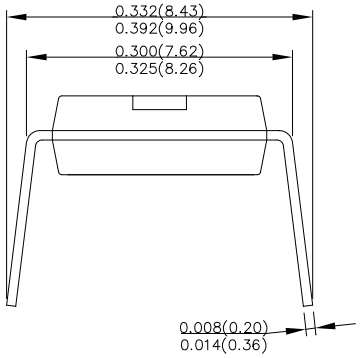
PACKAGE INFORMATION

PDIP8-7EP



TOP VIEW



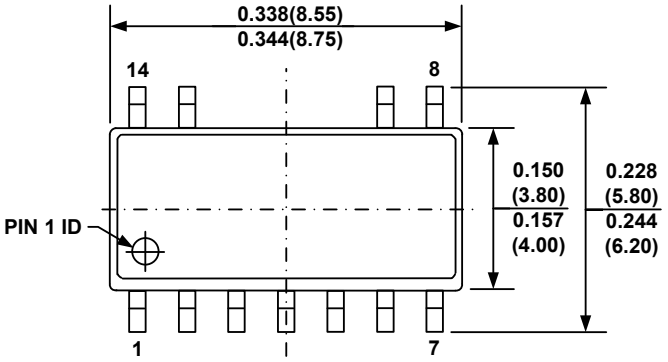


SIDE VIEW

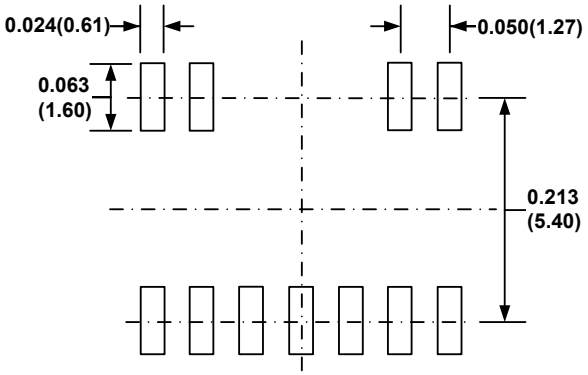
NOTE :

1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS .
2) PACKAGE LENGTH AND WIDTH DO NOT INCLUDE MOLD FLASH ,OR PROTRUSIONS.
3) JEDEC REFERENCE IS MS-001, VARIATION BA .
4) DRAWING IS NOT TO SCALE .

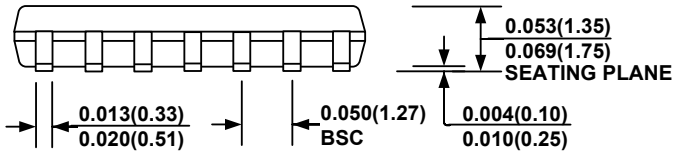
SOIC14-11



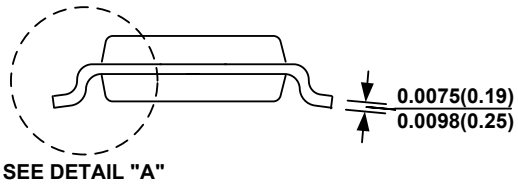
TOP VIEW



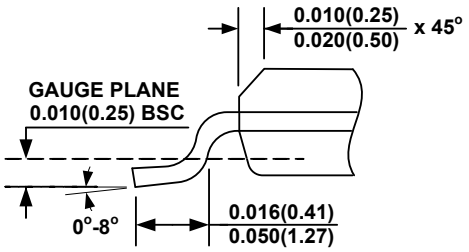
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW



DETAIL "A"

NOTE:

1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
5) DRAWING CONFORMS TO JEDEC MS-012, VARIATION AB.
6) DRAWING IS NOT TO SCALE.

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Для оперативного оформления запроса Вам необходимо перейти по данной ссылке:

http://moschip.ru/get-element

Вы можете разместить у нас заказ для любого Вашего проекта, будь то серийное производство или разработка единичного прибора.

В нашем ассортименте представлены ведущие мировые производители активных и пассивных электронных компонентов.

Нашей специализацией является поставка электронной компонентной базы двойного назначения, продукции таких производителей как XILINX, Intel (ex.ALTERA), Vicor, Microchip, Texas Instruments, Analog Devices, Mini-Circuits, Amphenol, Glenair.

Сотрудничество с глобальными дистрибьюторами электронных компонентов, предоставляет возможность заказывать и получать с международных складов практически любой перечень компонентов в оптимальные для Вас сроки.

На всех этапах разработки и производства наши партнеры могут получить квалифицированную поддержку опытных инженеров.

Система менеджмента качества компании отвечает требованиям в соответствии с ГОСТ Р ИСО 9001, ГОСТ РВ 0015-002 и ЭС РД 009

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