



CYPRESS

PRELIMINARY

W48S87-04

## Spread Spectrum 3 DIMM Desktop Clock

### Features

- **Outputs**
  - 4 CPU Clock (2.5V or 3.3V, 50 to 83.3 MHz)
  - 7 PCI (3.3V)
  - 1 48-MHz for USB (3.3V)
  - 1 24-MHz for Super I/O (3.3V)
  - 2 REF (3.3V)
  - 1 IOAPIC (2.5V or 3.3V)
  - 12 SDRAM
- Serial data interface provides additional frequency selection, individual clock output disable, and other functions
- Smooth transition supports dynamic frequency assignment
- Frequency selection not affected during power down/up cycle
- Supports a variety of power-saving options
- 3.3V operation
- Available in 48-pin SSOP (300 mils)

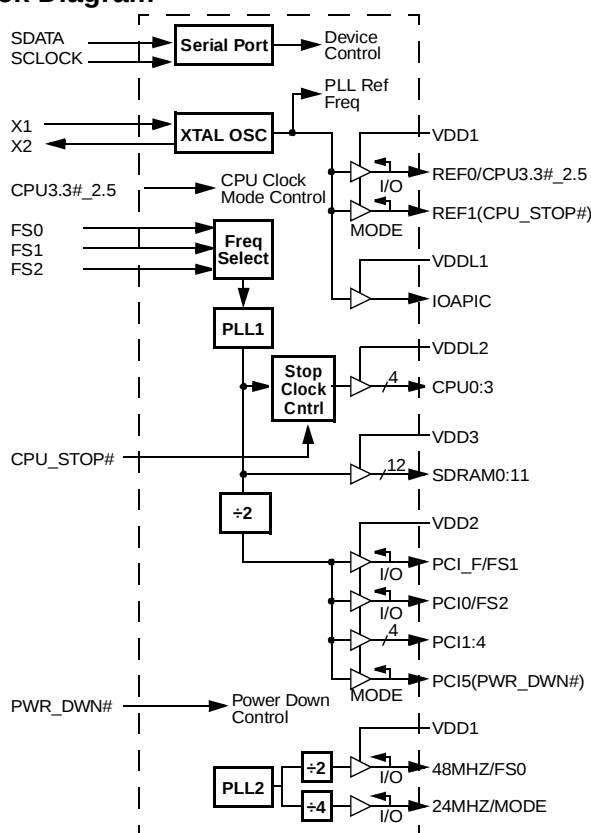
### Key Specifications

±0.5% Spread Spectrum Modulation: ..... ±0.5%  
Jitter (Cycle-to-Cycle): ..... 250 ps  
Duty Cycle: ..... 45-55%  
CPU-PCI Skew: ..... 1 to 4 ns  
PCI-PCI or CPU-CPU Skew: ..... 250 ps

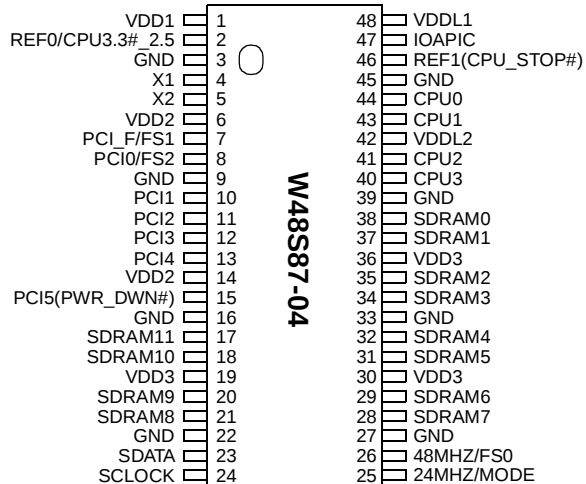
Table 1. Pin Selectable Frequency<sup>[1]</sup>

| Input Address |     |     | CPU, SDRAM<br>Clocks (MHz) | PCI Clocks<br>(MHz) |
|---------------|-----|-----|----------------------------|---------------------|
| FS2           | FS1 | FS0 |                            |                     |
| 0             | 0   | 0   | 50.0                       | 25.0                |
| 0             | 0   | 1   | 75.0                       | 32.0                |
| 0             | 1   | 0   | 83.3                       | 41.65               |
| 0             | 1   | 1   | 68.5                       | 34.25               |
| 1             | 0   | 0   | 55.0                       | 27.5                |
| 1             | 0   | 1   | 75.0                       | 37.5                |
| 1             | 1   | 0   | 60.0                       | 30.0                |
| 1             | 1   | 1   | 66.8                       | 33.4                |

### Block Diagram



### Pin Configuration<sup>[2]</sup>



#### Notes:

1. Additional frequency selections provided by serial data interface; refer to Table 5 on page 10.
2. Signal names in parenthesis denotes function is selectable through mode pin register strapping.

**Pin Definitions**

| Pin Name       | Pin No.                                        | Pin Type          | Pin Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |             |               |               |   |                  |                   |   |               |               |
|----------------|------------------------------------------------|-------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------|---------------|---------------|---|------------------|-------------------|---|---------------|---------------|
| CPU0:3         | 44, 43, 41, 40                                 | O                 | <b>CPU Clock Outputs 0 through 3:</b> These four CPU clock outputs are controlled by the CPU_STOP# control pin. Output voltage swing is controlled by voltage applied to VDDL2 and output characteristics are adjusted by input CPU3.3#_2.5.                                                                                                                                                                                                                                                                                                                                                                                                                                 |             |               |               |   |                  |                   |   |               |               |
| PCI_F/FS1      | 7                                              | I/O               | <b>Fixed PCI Clock Output and Frequency Selection Bit 1:</b> As an output, this pin works in conjunction with PCI0:5. Output voltage swing is controlled by voltage applied to VDD2.<br><br>When an input, this pin functions as part of the frequency selection address. The value of FS0:2 determines the power-up default frequency of device output clocks as per the <i>Table 1</i> , “Pin Selectable Frequency” on page 1.                                                                                                                                                                                                                                             |             |               |               |   |                  |                   |   |               |               |
| PCI0/FS2       | 8                                              | I/O               | <b>PCI Bus Clock Output 0 and Frequency Selection Bit 2:</b> As an output, this pin works in conjunction with PCI1:5 and PCI_F. Output voltage swing is controlled by voltage applied to VDD2.<br><br>When an input, this pin functions as part of the frequency selection address. The value of FS0:2 determines the power-up default frequency of device output clocks as per the <i>Table 1</i> , “Pin Selectable Frequency” on page 1.                                                                                                                                                                                                                                   |             |               |               |   |                  |                   |   |               |               |
| PCI1:4         | 10, 11, 12, 13                                 | O                 | <b>PCI Bus Clock Outputs 1 through 4:</b> Output voltage swing is controlled by voltage applied to VDD2.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |             |               |               |   |                  |                   |   |               |               |
| PCI5(PWR_DWN#) | 15                                             | I/O               | <b>PCI Bus Clock Output 5 or Power-Down Control:</b> As an output, this pin works in conjunction with PCI0:4 and PCI_F. Output voltage swing is controlled by voltage applied to VDD2.<br><br>If programmed as an input (refer to MODE pin description), this pin is used for power-down control. When LOW, the device goes into a low-power standby condition. All outputs are actively held LOW while in power-down. CPU, SDRAM, and PCI clock outputs are stopped LOW after completing a full clock cycle (2–4 CPU clock cycle latency). When brought HIGH, CPU, SDRAM, and PCI outputs start with a full clock cycle at full operating frequency (3 ms maximum latency). |             |               |               |   |                  |                   |   |               |               |
| SDRAM0:11      | 38, 37, 35, 34, 32, 31, 29, 28, 21, 20, 18, 17 | O                 | <b>SDRAM Clock Outputs 0 through 11:</b> These twelve SDRAM clock outputs run synchronous to the CPU clock outputs. Output voltage swing is controlled by voltage applied to VDD3.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |             |               |               |   |                  |                   |   |               |               |
| IOAPIC         | 47                                             | O                 | <b>I/O APIC Clock Output:</b> Provides 14.318-MHz fixed frequency. The output voltage swing is controlled by VDDL1.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |             |               |               |   |                  |                   |   |               |               |
| 48MHZ/FS0      | 26                                             | I/O               | <b>48-MHz Output and Frequency Selection Bit 0:</b> Fixed clock output that defaults to 48 MHz following device power-up. Output voltage swing is controlled by voltage applied to VDD1.<br><br>When an input, this pin functions as part of the frequency selection address. The value of FS0:2 determines the power-up default frequency of device output clocks as per the <i>Table 1</i> , “Pin Selectable Frequency” on page 1.                                                                                                                                                                                                                                         |             |               |               |   |                  |                   |   |               |               |
| 24MHZ/MODE     | 25                                             | I/O               | <b>24-MHz Output and Mode Control Input:</b> Fixed clock output that defaults to 24 MHz following device power-up. Output voltage swing is controlled by voltage applied to VDD1.<br><br>When an input, this pin is used for pin programming selection. It determines the functions for pins 15 and 46:<br><table><tr><td><b>MODE</b></td><td><b>Pin 15</b></td><td><b>Pin 46</b></td></tr><tr><td>0</td><td>PWR_DWN# (input)</td><td>CPU_STOP# (input)</td></tr><tr><td>1</td><td>PCI5 (output)</td><td>REF1 (output)</td></tr></table>                                                                                                                                     | <b>MODE</b> | <b>Pin 15</b> | <b>Pin 46</b> | 0 | PWR_DWN# (input) | CPU_STOP# (input) | 1 | PCI5 (output) | REF1 (output) |
| <b>MODE</b>    | <b>Pin 15</b>                                  | <b>Pin 46</b>     |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |             |               |               |   |                  |                   |   |               |               |
| 0              | PWR_DWN# (input)                               | CPU_STOP# (input) |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |             |               |               |   |                  |                   |   |               |               |
| 1              | PCI5 (output)                                  | REF1 (output)     |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |             |               |               |   |                  |                   |   |               |               |

**Pin Definitions** (continued)

| Pin Name           | Pin No.                             | Pin Type | Pin Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |                    |                                     |   |      |   |      |
|--------------------|-------------------------------------|----------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------|-------------------------------------|---|------|---|------|
| REF0/CPU3.3#_2.5   | 2                                   | I/O      | <p><b>Fixed 14.318-MHz Output 0 and CPU Output Voltage Swing Selection Input:</b> As an output, this pin is used for various system applications. Output voltage swing is controlled by voltage applied to VDD1. REF0 is stronger than REF1 and should be used for driving ISA slots.</p> <p>When an input, this pin selects the CPU clock output buffer characteristics that are optimized for either 3.3V or 2.5V operation.</p> <table><tr><td><b>CPU3.3#_2.5</b></td><td><b>VDDQ2 Voltage (CPU0:3 Swing)</b></td></tr><tr><td>0</td><td>3.3V</td></tr><tr><td>1</td><td>2.5V</td></tr></table> <p>This input adjusts CPU clock output impedance so that a nominal 20Ω output impedance is maintained. This eliminates or reduces the need to adjust external clock tuning components when changing VDDL2 voltage. CPU clock phase is also adjusted so that both CPU and SDRAM and CPU-to-PCI clock skew is maintained over the two VDDL2 voltage options. This input does not adjust IOAPIC clock output characteristics.</p> | <b>CPU3.3#_2.5</b> | <b>VDDQ2 Voltage (CPU0:3 Swing)</b> | 0 | 3.3V | 1 | 2.5V |
| <b>CPU3.3#_2.5</b> | <b>VDDQ2 Voltage (CPU0:3 Swing)</b> |          |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |                    |                                     |   |      |   |      |
| 0                  | 3.3V                                |          |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |                    |                                     |   |      |   |      |
| 1                  | 2.5V                                |          |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |                    |                                     |   |      |   |      |
| REF1(CPU_Stop#)    | 46                                  | I/O      | <p><b>Fixed 14.318-MHz Output 0 or CPU Clock Output Stop Control:</b> Used for various system applications. Output voltage swing is controlled by voltage applied to VDD1. REF0 is stronger than REF1 and should be used for driving ISA slots.</p> <p>If programmed as an input (refer to MODE pin description), this pin is used for stopping the CPU clock outputs. When brought LOW, clock outputs CPU0:3 are stopped LOW after completing a full clock cycle (2–3 CPU clock latency). When brought HIGH, clock outputs CPU0:3 are starting beginning with a full clock cycle (2–3 CPU clock latency).</p>                                                                                                                                                                                                                                                                                                                                                                                                                    |                    |                                     |   |      |   |      |
| X1                 | 4                                   | I        | <p><b>Crystal Connection or External Reference Frequency Input:</b> This pin has dual functions. It can be used as an external 14.318-MHz crystal connection or as an external reference frequency input.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |                    |                                     |   |      |   |      |
| X2                 | 5                                   | I        | <p><b>Crystal Connection:</b> An input connection for an external 14.318-MHz crystal. If using an external reference, this pin must be left unconnected.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |                    |                                     |   |      |   |      |
| SDATA              | 23                                  | I        | <p><b>Serial Data Input:</b> Data input for Serial Data Interface. Refer to Serial Data Interface section that follows.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |                    |                                     |   |      |   |      |
| SCLOCK             | 24                                  | I        | <p><b>Serial Clock Input:</b> Clock input for Serial Data Interface. Refer to Serial Data Interface section that follows.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |                    |                                     |   |      |   |      |
| VDD1               | 1                                   | P        | <p><b>Power Connection:</b> Power supply for crystal oscillator and REF0:1 output buffers. Connected to 3.3V supply.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |                    |                                     |   |      |   |      |
| VDD2               | 6,14                                | P        | <p><b>Power Connection:</b> Power supply for PCI clock output buffers. Connected to 3.3V supply.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |                    |                                     |   |      |   |      |
| VDDL1              | 48                                  | P        | <p><b>Power Connection:</b> Power supply for IOAPIC output buffer. Connected to 2.5V or 3.3V supply.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |                    |                                     |   |      |   |      |
| VDDL2              | 42                                  | P        | <p><b>Power Connection:</b> Power supply for CPU clock output buffers. Connected to 2.5V or 3.3V supply.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |                    |                                     |   |      |   |      |
| VDD3               | 19, 30, 36                          | P        | <p><b>Power Connection:</b> Power supply for SDRAM clock output buffers. Connected to 3.3V supply.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |                    |                                     |   |      |   |      |
| GND                | 3, 9, 16, 22, 27, 33, 39, 45        | G        | <p><b>Ground Connection:</b> Connect all ground pins to the common system ground plane.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |                    |                                     |   |      |   |      |

## Overview

The W48S87-04, a motherboard clock synthesizer, can provide either a 2.5V or 3.3V CPU clock swing, making it suitable for a variety of CPU options. Twelve SDRAM clocks are provided in phase with the CPU clock outputs. This provides clock support for up to three SDRAM DIMMs. Fixed output frequency clocks are provided for other system functions.

## Functional Description

### I/O Pin Operation

Pins 2, 7, 8, 25, and 26 are dual-purpose I/O pins. Upon power-up these pins act as logic inputs, allowing the determination of assigned device functions. A short time after power-up, the logic state of these pins is latched and the pins then become clock outputs. This feature reduces device pin count by combining clock outputs with input select pins.

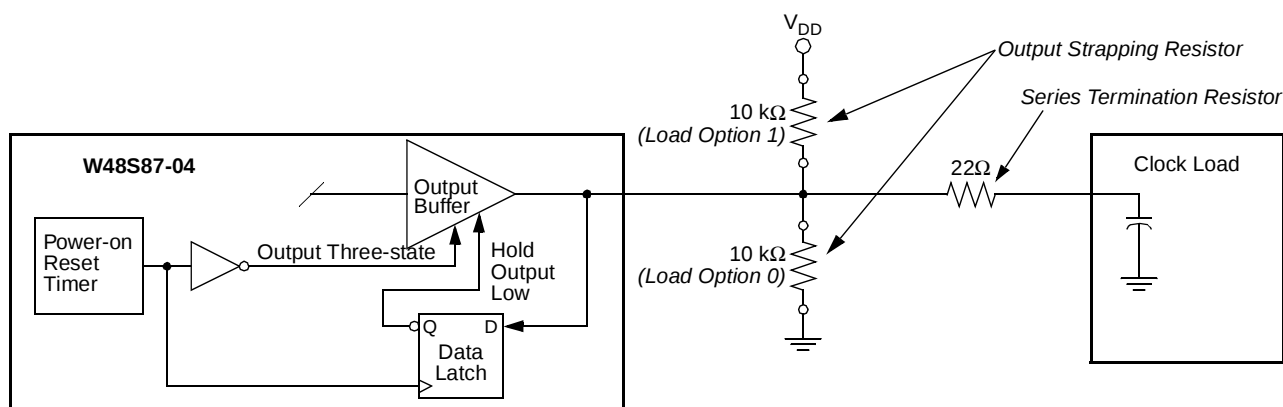
An external 10-k $\Omega$  "strapping" resistor is connected between each I/O pin and ground or  $V_{DD3}$ . Connection to ground sets a latch to "0", connection to  $V_{DD3}$  sets a latch to "1". *Figure 1* and *Figure 2* show two suggested methods for strapping resistor connection.

Upon W48S87-04 power-up, the first 2 ms of operation is used for input logic selection. During this period, these dual-purpose

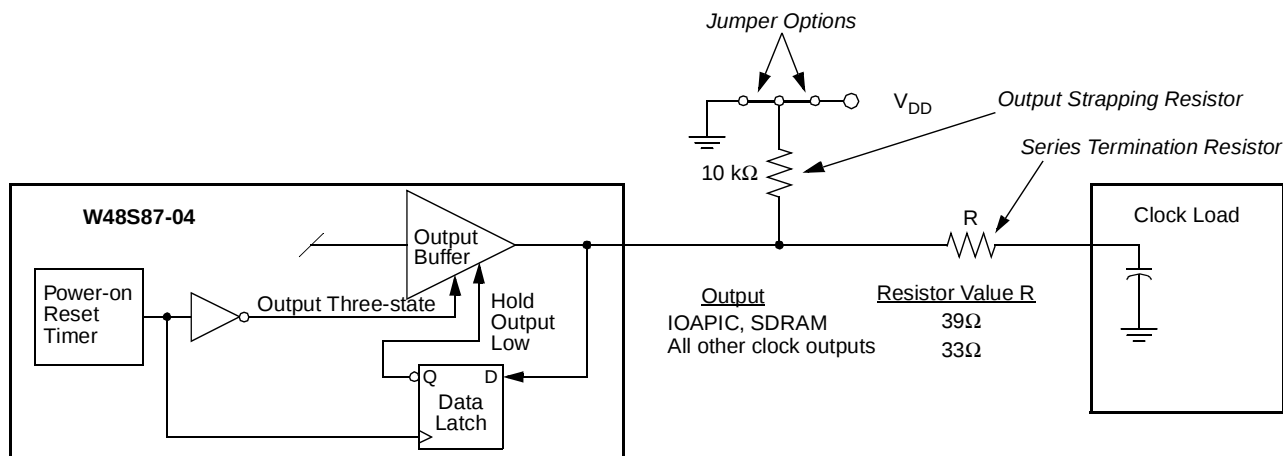
I/O pins are three-stated, allowing the output strapping resistor on each I/O pin to pull the pin and its associated capacitive clock load to either a logic HIGH or LOW state. At the end of the 2-ms period, the established logic 0 or 1 condition of each I/O is pin is then latched. Next the output buffers are enabled, which converts the I/O pins into operating clock outputs. The 2-ms timer is started when  $V_{DD}$  reaches 2.0V. The input bits can only be reset by turning  $V_{DD}$  off and then back on again.

It should be noted that the strapping resistors have no significant effect on clock output signal integrity. The drive impedance of both clock outputs is  $<40\Omega$  (nominal) which is minimally affected by the 10-k $\Omega$  strap to ground or  $V_{DD}$ . As with the series termination resistor, the output strapping resistor should be placed as close to the I/O pin as possible in order to keep the interconnecting trace short. The trace from the resistor to ground or  $V_{DD}$  should be kept less than two inches in length to prevent system noise coupling during input logic sampling.

When the clock outputs are enabled following the 2-ms input period, target (normal) output frequency is delivered assuming that  $V_{DD}$  has stabilized. If  $V_{DD}$  has not yet reached full value, output frequency initially may be below target but will increase to target once  $V_{DD}$  voltage has stabilized. In either case, a short output clock cycle may be produced from the CPU clock outputs when the outputs are enabled.



**Figure 1. Input Logic Selection Through Resistor Load Option**



**Figure 2. Input Logic Selection Through Jumper Option**

#### CPU/PCI Frequency Selection

CPU frequency is selected with I/O pins 26, 7, and 8 (48MHz/FS0, PCI\_F/FS1, and PCI0/FS2, respectively). Refer to *Table 1* for CPU/PCI frequency programming information. Additional frequency selections are available through the serial data interface. Refer to *Table 5* on page 10.

#### Output Buffer Configuration

##### Clock Outputs

All clock outputs are designed to drive serial terminated clock lines. The W48S87-04 outputs are CMOS-type, which provide rail-to-rail output swing. To accommodate the limited voltage swing required by some processors, the output buffers of CPU0:3 use a special VDDL2 power supply pin that can be tied to 2.5V nominal.

##### Crystal Oscillator

The W48S87-04 requires one input reference clock to synthesize all output frequencies. The reference clock can be either an externally generated clock signal or the clock generated by

the internal crystal oscillator. When using an external clock signal, pin X1 is used as the clock input and pin X2 is left open. The input threshold voltage of pin X1 is  $V_{DD}/2$ .

The internal crystal oscillator is used in conjunction with a quartz crystal connected to device pins X1 and X2. This forms a parallel resonant crystal oscillator circuit. The W48S87-04 incorporates the necessary feedback resistor and crystal load capacitors. Including typical stray circuit capacitance, the total load presented to the crystal is approximately 20 pF. For optimum frequency accuracy without the addition of external capacitors, a parallel-resonant mode crystal specifying a load of 20 pF should be used. This will typically yield reference frequency accuracies within  $\pm 100$  ppm.

##### Dual Supply Voltage Operation

The W48S87-04 is designed for dual power supply operation. Supply pins VDD1, VDD2, and VDD3 are connected to a 3.3V supply and supply power to the internal core circuit and to the clock output buffers, except for outputs CPU0:3 and IOAPIC. Supply pins VDDL1 and VDDL2 may be connected to either a 2.5V or 3.3V supply.

## Spread Spectrum Generator

The device generates a clock that is frequency modulated in order to increase the bandwidth that it occupies. By increasing the bandwidth of the fundamental and its harmonics, the amplitudes of the radiated electromagnetic emissions are reduced. This effect is depicted in *Figure 3*.

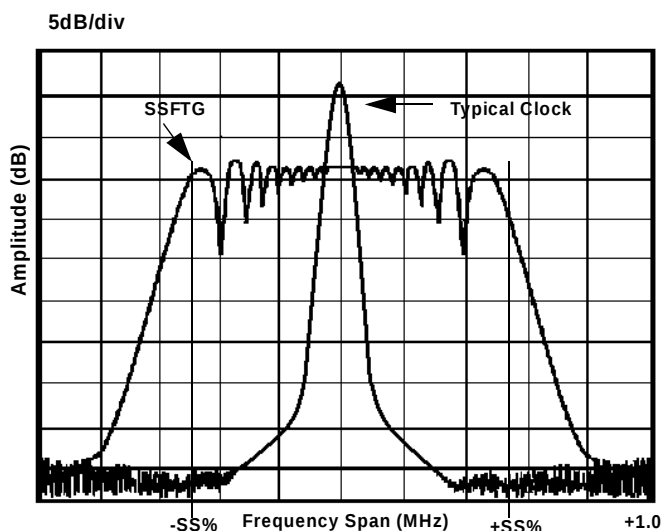
As depicted in *Figure 3*, a harmonic of a modulated clock has a much lower amplitude than that of an unmodulated signal. The reduction in amplitude is dependent on the harmonic number and the frequency deviation or spread. The equation for the reduction is

$$dB = 6.5 + 9 \cdot \log_{10}(P) + 9 \cdot \log_{10}(F)$$

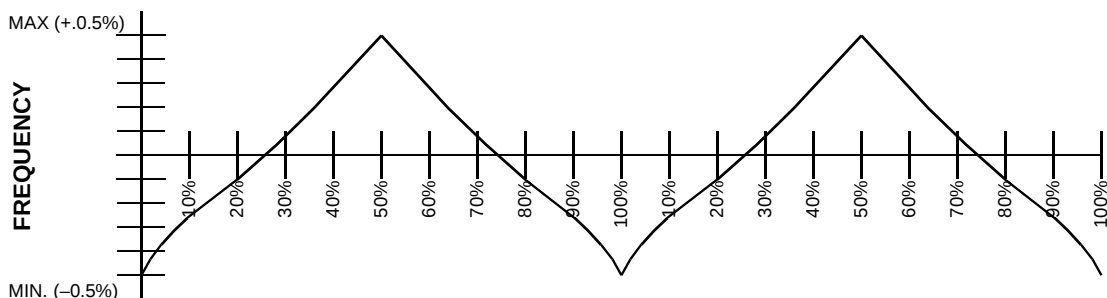
Where  $P$  is the percentage of deviation and  $F$  is the frequency in MHz where the reduction is measured.

The output clock is modulated with a waveform depicted in *Figure 4*. This waveform, as discussed in "Spread Spectrum Clock Generation for the Reduction of Radiated Emissions" by Bush, Fessler, and Hardin produces the maximum reduction in the amplitude of radiated electromagnetic emissions. The deviation selected for this chip is  $\pm 0.5\%$  of the center frequency. *Figure 4* details the Cypress spreading pattern. Cypress does offer options with more spread and greater EMI reduction. Contact your local Sales representative for details on these devices.

Spread Spectrum clocking is activated or deactivated by selecting the appropriate values for bits 1–0 in data byte 0 of the I<sup>2</sup>C data stream. Refer to *Table 4* for more details.



**Figure 3. Clock Harmonic with and without SSCG Modulation Frequency Domain Representation**



**Figure 4. Typical Modulation Profile**

## Serial Data Interface

The W48S87-04 features a two-pin, serial data interface that can be used to configure internal register settings that control particular device functions. Upon power-up, the W48S87-04 initializes with default register settings, therefore the use of this serial data interface is optional. The serial interface is write-only (to the clock chip) and is the dedicated function of device pins SDATA and SCLOCK. In motherboard applications, SDATA and SCLOCK are typically driven by two logic outputs

of the chipset. Clock device register changes are normally made upon system initialization, if any are required. The interface can also be used during system operation for power management functions. *Table 2* summarizes the control functions of the serial data interface.

### Operation

Data is written to the W48S87-04 in ten bytes of eight bits each. Bytes are written in the order shown in *Table 3*.

**Table 2. Serial Data Interface Control Functions Summary**

| Control Function              | Description                                                                                                                                                                                      | Common Application                                                                                                                              |
|-------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------|
| Clock Output Disable          | Any individual clock output(s) can be disabled. Disabled outputs are actively held LOW.                                                                                                          | Unused outputs are disabled to reduce EMI and system power. Examples are clock outputs to unused SDRAM DIMM socket or PCI slot.                 |
| CPU Clock Frequency Selection | Provides CPU/PCI frequency selections beyond the 50- and 66.8-MHz selections that are provided by the FS0:2 power-on default selection. Frequency is changed in a smooth and controlled fashion. | For alternate CPU devices, and power management options. Smooth frequency transition allows CPU frequency change under normal system operation. |
| Output Three-state            | Puts all clock outputs into a high-impedance state.                                                                                                                                              | Production PCB testing.                                                                                                                         |
| Test Mode                     | All clock outputs toggle in relation with X1 input, internal PLL is bypassed. Refer to <i>Table 4</i> .                                                                                          | Production PCB testing.                                                                                                                         |
| (Reserved)                    | Reserved function for future device revision or production device testing.                                                                                                                       | No user application. Register bit must be written as 0.                                                                                         |

**Table 3. Byte Writing Sequence**

| Byte Sequence | Byte Name     | Bit Sequence            | Byte Description                                                                                                                                                                                                                                                                                                                                                                                                          |
|---------------|---------------|-------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1             | Slave Address | 11010010                | Commands the W48S87-04 to accept the bits in Data Bytes 0–6 for internal register configuration. Since other devices may exist on the same common serial data bus, it is necessary to have a specific slave address for each potential receiver. The slave receiver address for the W48S87-04 is 11010010. Register setting will not be made if the Slave Address is not correct (or is for an alternate slave receiver). |
| 2             | Command Code  | Don't Care              | Unused by the W48S87-04, therefore bit values are ignored ("don't care"). This byte must be included in the data write sequence to maintain proper byte allocation. The Command Code Byte is part of the standard serial communication protocol and may be used when writing to another addressed slave receiver on the serial data bus.                                                                                  |
| 3             | Byte Count    | Don't Care              | Unused by the W48S87-04, therefore bit values are ignored ("don't care"). This byte must be included in the data write sequence to maintain proper byte allocation. The Byte Count Byte is part of the standard serial communication protocol and may be used when writing to another addressed slave receiver on the serial data bus.                                                                                    |
| 4             | Data Byte 0   | Refer to <i>Table 4</i> | The data bits in these bytes set internal W48S87-04 registers that control device operation. The data bits are only accepted when the Address Byte bit sequence is 11010010, as noted above. For description of bit control functions, refer to <i>Table 4</i> , Data Byte Serial Configuration Map.                                                                                                                      |
| 5             | Data Byte 1   |                         |                                                                                                                                                                                                                                                                                                                                                                                                                           |
| 6             | Data Byte 2   |                         |                                                                                                                                                                                                                                                                                                                                                                                                                           |
| 7             | Data Byte 3   |                         |                                                                                                                                                                                                                                                                                                                                                                                                                           |
| 8             | Data Byte 4   |                         |                                                                                                                                                                                                                                                                                                                                                                                                                           |
| 9             | Data Byte 5   |                         |                                                                                                                                                                                                                                                                                                                                                                                                                           |
| 10            | Data Byte 6   |                         |                                                                                                                                                                                                                                                                                                                                                                                                                           |

### Writing Data Bytes

Each bit in the data bytes control a particular device function except for the “reserved” bits which must be written as a logic 0. Bits are written MSB (most significant bit) first, which is bit

7. *Table 4* gives the bit formats for registers located in Data Bytes 0–6. *Table 5* details additional frequency selections that are available through the serial data interface. *Table 6* details the select functions for Byte 0, bits 1 and 0.

**Table 4. Data Bytes 0–6 Serial Configuration Map**

| Bit(s)      | Affected Pin |          | Control Function                                                                                                                 | Bit Control                                        |                                        | Default |
|-------------|--------------|----------|----------------------------------------------------------------------------------------------------------------------------------|----------------------------------------------------|----------------------------------------|---------|
|             | Pin No.      | Pin Name |                                                                                                                                  | 0                                                  | 1                                      |         |
| Data Byte 0 |              |          |                                                                                                                                  |                                                    |                                        |         |
| 7           | --           | --       | (Reserved)                                                                                                                       | --                                                 | --                                     | 0       |
| 6           | --           | --       | BYT0_SEL2                                                                                                                        | Refer to <i>Table 5</i>                            |                                        | 0       |
| 5           | --           | --       | BYT0_SEL1                                                                                                                        | Refer to <i>Table 5</i>                            |                                        | 0       |
| 4           | --           | --       | BYT0_SEL0                                                                                                                        | Refer to <i>Table 5</i>                            |                                        | 0       |
| 3           |              |          | BYT0_FS#                                                                                                                         | Frequency Controlled by FS (2:0)                   | Frequency Controlled by BYT0_SEL (2:0) | 0       |
| 2           | 22           |          | (Reserved)                                                                                                                       |                                                    |                                        | 0       |
| 1–0         | --           | --       | Bit 1   Bit 0<br>0   0   Normal Operation<br>0   1   Test Mode<br>1   0   Spread Spectrum On<br>1   1   All Outputs Three-stated | Function (See <i>Table 6</i> for function details) |                                        | 00      |
| Data Byte 1 |              |          |                                                                                                                                  |                                                    |                                        |         |
| 7           | 26           | 48MHZ    | Clock Output Disable                                                                                                             | Low                                                | Active                                 | 1       |
| 6           | 25           | 24MHZ    | Clock Output Disable                                                                                                             | Low                                                | Active                                 | 1       |
| 5           | --           | --       | (Reserved)                                                                                                                       | --                                                 | --                                     | 0       |
| 4           | --           | --       | (Reserved)                                                                                                                       | --                                                 | --                                     | 0       |
| 3           | 40           | CPU3     | Clock Output Disable                                                                                                             | Low                                                | Active                                 | 1       |
| 2           | 41           | CPU2     | Clock Output Disable                                                                                                             | Low                                                | Active                                 | 1       |
| 1           | 43           | CPU1     | Clock Output Disable                                                                                                             | Low                                                | Active                                 | 1       |
| 0           | 44           | CPU0     | Clock Output Disable                                                                                                             | Low                                                | Active                                 | 1       |
| Data Byte 2 |              |          |                                                                                                                                  |                                                    |                                        |         |
| 7           | --           | --       | (Reserved)                                                                                                                       | --                                                 | --                                     | 0       |
| 6           | 7            | PCI_F    | Clock Output Disable                                                                                                             | Low                                                | Active                                 | 1       |
| 5           | 15           | PCI5     | Clock Output Disable                                                                                                             | Low                                                | Active                                 | 1       |
| 4           | 13           | PCI4     | Clock Output Disable                                                                                                             | Low                                                | Active                                 | 1       |
| 3           | 12           | PCI3     | Clock Output Disable                                                                                                             | Low                                                | Active                                 | 1       |
| 2           | 11           | PCI2     | Clock Output Disable                                                                                                             | Low                                                | Active                                 | 1       |
| 1           | 10           | PCI1     | Clock Output Disable                                                                                                             | Low                                                | Active                                 | 1       |
| 0           | 8            | PCI0     | Clock Output Disable                                                                                                             | Low                                                | Active                                 | 1       |

**Table 4. Data Bytes 0–6 Serial Configuration Map (continued)**

| Bit(s)      | Affected Pin |          | Control Function     | Bit Control |        | Default |
|-------------|--------------|----------|----------------------|-------------|--------|---------|
|             | Pin No.      | Pin Name |                      | 0           | 1      |         |
| Data Byte 3 |              |          |                      |             |        |         |
| 7           | 28           | SDRAM7   | Clock Output Disable | Low         | Active | 1       |
| 6           | 29           | SDRAM6   | Clock Output Disable | Low         | Active | 1       |
| 5           | 31           | SDRAM5   | Clock Output Disable | Low         | Active | 1       |
| 4           | 32           | SDRAM4   | Clock Output Disable | Low         | Active | 1       |
| 3           | 34           | SDRAM3   | Clock Output Disable | Low         | Active | 1       |
| 2           | 35           | SDRAM2   | Clock Output Disable | Low         | Active | 1       |
| 1           | 37           | SDRAM1   | Clock Output Disable | Low         | Active | 1       |
| 0           | 38           | SDRAM0   | Clock Output Disable | Low         | Active | 1       |
| Data Byte 4 |              |          |                      |             |        |         |
| 7           | --           | --       | (Reserved)           | --          | --     | 0       |
| 6           | --           | --       | (Reserved)           | --          | --     | 0       |
| 5           | --           | --       | (Reserved)           | --          | --     | 0       |
| 4           | --           | --       | (Reserved)           | --          | --     | 0       |
| 3           | 17           | SDRAM11  | Clock Output Disable | Low         | Active | 1       |
| 2           | 18           | SDRAM10  | Clock Output Disable | Low         | Active | 1       |
| 1           | 20           | SDRAM9   | Clock Output Disable | Low         | Active | 1       |
| 0           | 21           | SDRAM8   | Clock Output Disable | Low         | Active | 1       |
| Data Byte 5 |              |          |                      |             |        |         |
| 7           | --           | --       | (Reserved)           | --          | --     | 0       |
| 5           | --           | --       | (Reserved)           | --          | --     | 0       |
| 5           | --           | --       | (Reserved)           | --          | --     | 0       |
| 4           | 47           | IOAPIC   | Clock Output Disable | Low         | Active | 1       |
| 3           | --           | --       | (Reserved)           | --          | --     | 0       |
| 2           | --           | --       | (Reserved)           | --          | --     | 0       |
| 1           | 46           | REF1     | Clock Output Disable | Low         | Active | 1       |
| 0           | 2            | REF0     | Clock Output Disable | Low         | Active | 1       |
| Data Byte 6 |              |          |                      |             |        |         |
| 7           | --           | --       | (Reserved)           | --          | --     | 0       |
| 6           | --           | --       | (Reserved)           | --          | --     | 0       |
| 5           | --           | --       | (Reserved)           | --          | --     | 0       |
| 4           | --           | --       | (Reserved)           | --          | --     | 0       |
| 3           | --           | --       | (Reserved)           | --          | --     | 0       |
| 2           | --           | --       | (Reserved)           | --          | --     | 0       |
| 1           | --           | --       | (Reserved)           | --          | --     | 0       |
| 0           | --           | --       | (Reserved)           | --          | --     | 0       |

**Table 5. Additional Frequency Selections through Serial Data Interface Data Bytes**

| Input Conditions       |                    |                    | Output Frequency        |                  |
|------------------------|--------------------|--------------------|-------------------------|------------------|
| Data Byte 0, Bit 3 = 1 |                    |                    | CPU, SDRAM Clocks (MHz) | PCI Clocks (MHz) |
| Bit 6<br>BYT0_SEL2     | Bit 5<br>BYT0_SEL1 | Bit 4<br>BYT0_SEL0 |                         |                  |
| 0                      | 0                  | 0                  | 50                      | 25               |
| 0                      | 0                  | 1                  | 75.0                    | 32               |
| 0                      | 1                  | 0                  | 83.3                    | 41.65            |
| 0                      | 1                  | 1                  | 68.5                    | 34.25            |
| 1                      | 0                  | 0                  | 55.0                    | 27.5             |
| 1                      | 0                  | 1                  | 75.0                    | 37.5             |
| 1                      | 1                  | 0                  | 60.0                    | 30.0             |
| 1                      | 1                  | 1                  | 66.8                    | 33.4             |

**Table 6. Select Function for Data Byte 0, Bits 0:1**

| Function         | Input Conditions |       | Output Conditions   |                   |                |           |
|------------------|------------------|-------|---------------------|-------------------|----------------|-----------|
|                  | Data Byte 0      |       | CPU0:3,<br>SRAM0:11 | PCI_F,<br>PCI0:5  | REF0:1, IOAPIC | 48/24MHZ  |
|                  | Bit 1            | Bit 0 |                     |                   |                |           |
| Normal Operation | 0                | 0     | Note 3              | Note 3            | 14.318 MHz     | 48/24 MHz |
| Test Mode        | 0                | 1     | X1/2                | X1/4              | X1             | Note 4    |
| Spread Spectrum  | 1                | 0     | Note 3<br>SS±0.5%   | Note 3<br>SS±0.5% | 14.318 MHz     | 48/24 MHz |
| Three-state      | 1                | 1     | Hi-Z                | Hi-Z              | Hi-Z           | Hi-Z      |

**Note:**

3. CPU, SDRAM, and PCI frequency selections are listed in *Table 1* and *Table 5*.
4. In Test Mode, the 48/24MHz clock outputs are:
  - X1/2 for 48-MHz output.
  - X1/4 for 24-MHz output.

## How To Use the Serial Data Interface

### Electrical Requirements

Figure 5 illustrates electrical characteristics for the serial interface bus used with the W48S87-04. Devices send data over the bus with an open drain logic output that can (a) pull the bus line LOW, or (b) let the bus default to logic 1. The pull-up resistors on the bus (both clock and data lines) establish a default logic 1. All bus devices generally have logic inputs to receive data.

Although the W48S87-04 is a receive-only device (no data write-back capability), it does transmit an “acknowledge” data pulse after each byte is received. Thus, the SDATA line can both transmit and receive data.

The pull-up resistor should be sized to meet the rise and fall times specified in AC parameters, taking into consideration total bus line capacitance.

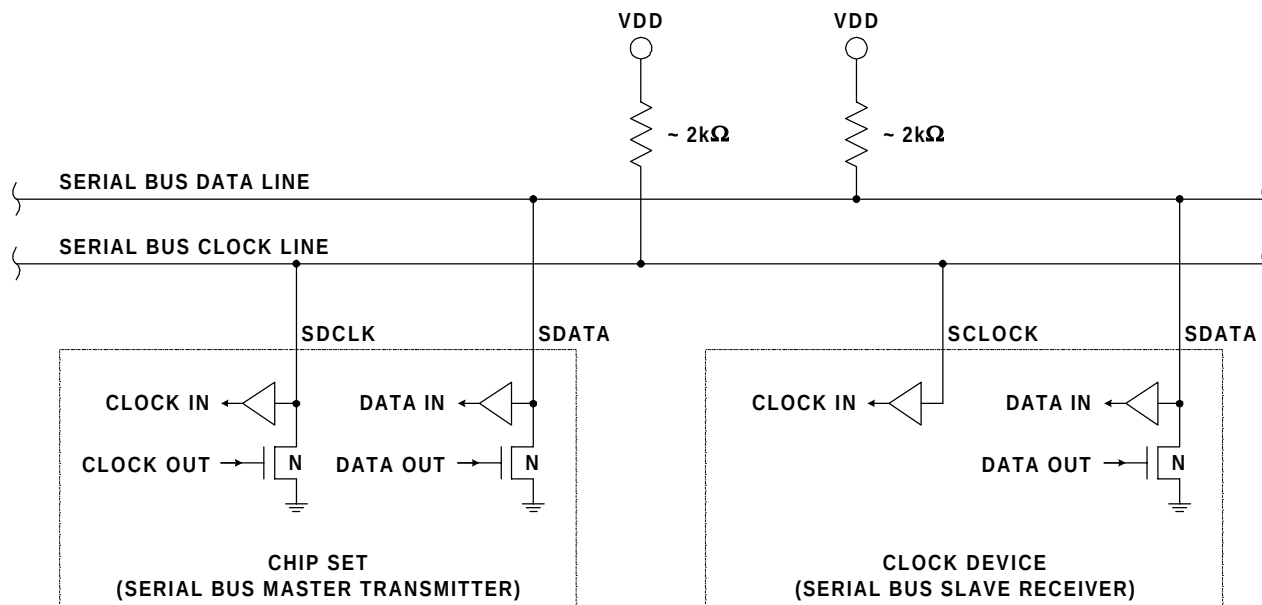


Figure 5. Serial Interface Bus Electrical Characteristics

### Signaling Requirements

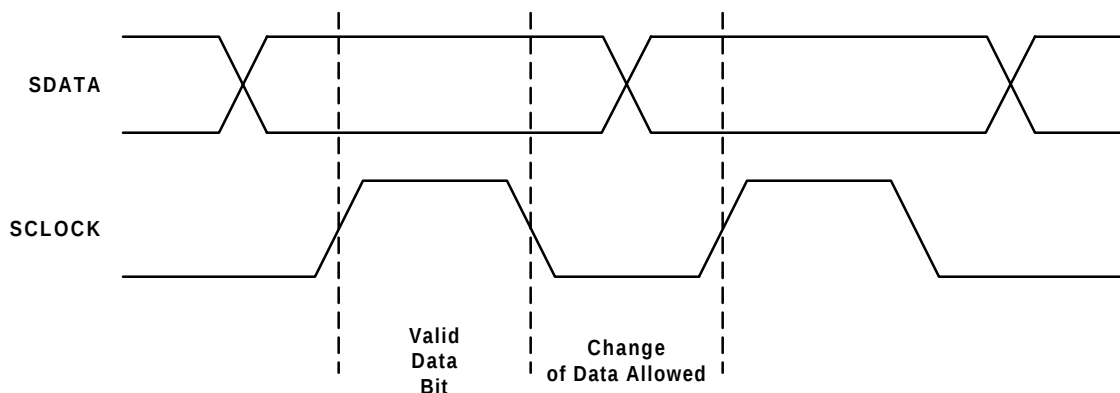
As shown in *Figure 6*, valid data bits are defined as stable logic 0 or 1 condition on the data line during a clock HIGH (logic 1) pulse. A transitioning data line during a clock HIGH pulse may be interpreted as a start or stop pulse (it will be interpreted as a start or stop pulse if the start/stop timing parameters are met).

A write sequence is initiated by a “start bit” as shown in *Figure 7*. A “stop bit” signifies that a transmission has ended.

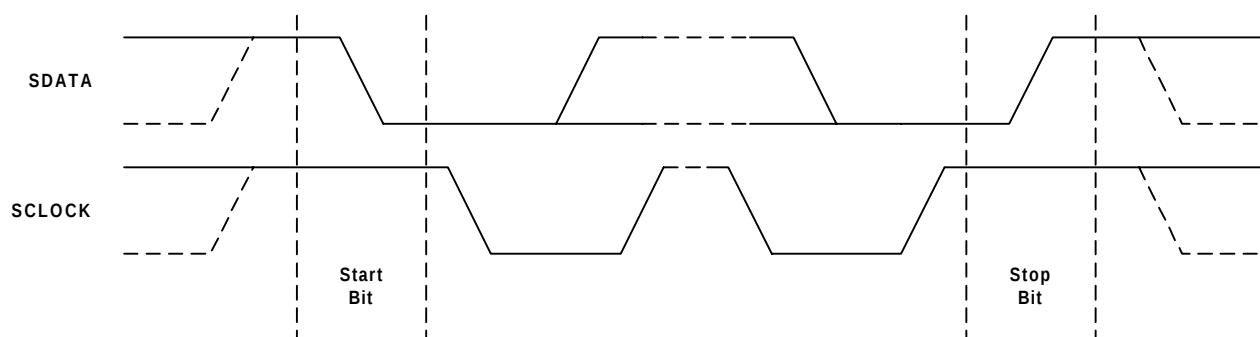
As stated previously, the W48S87-04 sends an “acknowledge” pulse after receiving eight data bits in each byte as shown in *Figure 8*.

### Sending Data to the W48S87-04

The device accepts data once it has detected a valid start bit and address byte sequence. Device functionality is changed upon the receipt of each data bit (registers are not double buffered). Partial transmission is allowed meaning that a transmission can be truncated as soon as the desired data bits are transmitted (remaining registers will be unmodified). Transmission is truncated with either a stop bit or new start bit (restart condition).



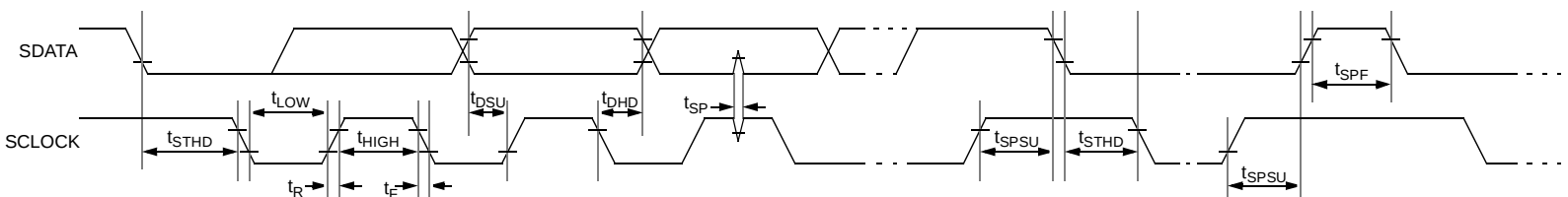
**Figure 6. Serial Data Bus Valid Data Bit**



**Figure 7. Serial Data Bus Start and Stop Bit**



### Figure 9. Serial Data Bus Timing Diagram



### Figure 9. Serial Data Bus Timing Diagram

## Absolute Maximum Ratings

Stresses greater than those listed in this table may cause permanent damage to the device. These represent a stress rating only. Operation of the device at these or any other conditions

above those specified in the operating sections of this specification is not implied. Maximum conditions for extended periods may affect reliability.

| Parameter        | Description                            | Rating       | Unit |
|------------------|----------------------------------------|--------------|------|
| $V_{DD}, V_{IN}$ | Voltage on any pin with respect to GND | -0.5 to +7.0 | V    |
| $T_{STG}$        | Storage Temperature                    | -65 to +150  | °C   |
| $T_A$            | Operating Temperature                  | 0 to +70     | °C   |
| $T_B$            | Ambient Temperature under Bias         | -55 to +125  | °C   |
| $ESD_{PROT}$     | Input ESD Protection                   | 2 (min.)     | kV   |

## Crystal Oscillator

| Parameter   | Description                                                  | Test Condition     | Min. | Typ. | Max. | Unit |
|-------------|--------------------------------------------------------------|--------------------|------|------|------|------|
| $V_{TH}$    | X1 Input Threshold Voltage <sup>[5]</sup>                    |                    |      | 1.65 |      | V    |
| $C_{LOAD}$  | Load Capacitance, Imposed on External Crystal <sup>[6]</sup> |                    |      | 20   |      | pF   |
| $C_{IN,X1}$ | X1 Input Capacitance <sup>[7]</sup>                          | Pin X2 unconnected |      | 40   |      | pF   |

## 3.3V DC Electrical Characteristics (CPU3.3#\_2.5 Input = 0)

$T_A = 0^{\circ}\text{C}$  to  $+70^{\circ}\text{C}$ ,  $V_{DD1:3} = V_{DDL1:2} = 3.3\text{V} \pm 5\%$  (3.135–3.465V)

| Parameter                                                 | Description                       |                        | Test Condition                                    | Min. | Typ. | Max. | Unit |
|-----------------------------------------------------------|-----------------------------------|------------------------|---------------------------------------------------|------|------|------|------|
| Supply Current                                            |                                   |                        |                                                   |      |      |      |      |
| I <sub>DD</sub>                                           | Combined 3.3V Supply Current      |                        | CPU0:3 =66.8 MHz<br>Outputs Loaded <sup>[8]</sup> |      |      | 160  | mA   |
| Logic Inputs (All referenced to V <sub>DDQ3</sub> = 3.3V) |                                   |                        |                                                   |      |      |      |      |
| V <sub>IL</sub>                                           | Input Low Voltage                 |                        |                                                   |      |      | 0.8  | V    |
| V <sub>IH</sub>                                           | Input High Voltage                |                        |                                                   | 2.0  |      |      | V    |
| I <sub>IL</sub>                                           | Input Low Current <sup>[9]</sup>  |                        |                                                   |      |      | 10   | μA   |
| I <sub>IH</sub>                                           | Input High Current <sup>[9]</sup> |                        |                                                   |      |      | 10   | μA   |
| Clock Outputs                                             |                                   |                        |                                                   |      |      |      |      |
| V <sub>OL</sub>                                           | Output Low Voltage                |                        | I <sub>OL</sub> = 1 mA                            |      |      | 50   | mV   |
| V <sub>OH</sub>                                           | Output High Voltage               |                        | I <sub>OH</sub> = −1 mA                           | 3.1  |      |      | V    |
| I <sub>OL</sub>                                           | Output Low Current                | CPU0:3 <sup>[10]</sup> | V <sub>OL</sub> = 1.5V                            | 55   | 75   | 105  | mA   |
|                                                           |                                   | SDRAM0:11              |                                                   | 80   | 110  | 155  |      |
|                                                           |                                   | PCI_F, PCI0:5          |                                                   | 55   | 75   | 105  |      |
|                                                           |                                   | IOAPIC                 |                                                   | 100  | 135  | 190  |      |
|                                                           |                                   | REF0                   |                                                   | 60   | 75   | 90   |      |
|                                                           |                                   | REF1                   |                                                   | 45   | 60   | 75   |      |
|                                                           |                                   | 48/24MHZ               |                                                   | 55   | 75   | 105  |      |

### Notes:

- X1 input threshold voltage (typical) is  $V_{DD}/2$ .
- The W48S87-04 contains an internal crystal load capacitor between pin X1 and ground and another between pin X2 and ground. Total load placed on crystal is 20 pF; this includes typical stray capacitance of short PCB traces to crystal.
- X1 input capacitance is applicable when driving X1 with an external clock source (X2 is left unconnected).
- All clock outputs loaded with maximum lump capacitance test load specified in AC Electrical Characteristics section.
- W48S87-04 logic inputs have internal pull-up devices.
- CPU0:3 loaded by 60Ω, 6-inch long transmission lines ending with 20-pF capacitors.

**3.3V DC Electrical Characteristics (CPU3.3#\_2.5 Input = 0) (continued)**
 $T_A = 0^{\circ}\text{C to } +70^{\circ}\text{C}$ ,  $V_{DD1:3} = V_{DDL1:2} = 3.3\text{V} \pm 5\%$  (3.135–3.465V)

| Parameter                  | Description                                             |                        | Test Condition                       | Min.               | Typ. | Max.               | Unit |
|----------------------------|---------------------------------------------------------|------------------------|--------------------------------------|--------------------|------|--------------------|------|
| I <sub>OH</sub>            | Output High Current                                     | CPU0:3 <sup>[10]</sup> | V <sub>OH</sub> = 1.5V               | 55                 | 85   | 125                | mA   |
|                            |                                                         | SDRAM0:11              |                                      | 80                 | 120  | 175                |      |
|                            |                                                         | PCI_F, PCI0:5          |                                      | 55                 | 85   | 125                |      |
|                            |                                                         | IOAPIC                 |                                      | 100                | 150  | 220                |      |
|                            |                                                         | REF0                   |                                      | 60                 | 85   | 110                |      |
|                            |                                                         | REF1                   |                                      | 45                 | 65   | 90                 |      |
|                            |                                                         | 48/24MHZ               |                                      | 55                 | 85   | 125                |      |
| Pin Capacitance/Inductance |                                                         |                        |                                      |                    |      |                    |      |
| C <sub>IN</sub>            | Input Pin Capacitance                                   |                        | Except X1 and X2                     |                    |      | 5                  | pF   |
| C <sub>OUT</sub>           | Output Pin Capacitance                                  |                        |                                      |                    |      | 6                  | pF   |
| L <sub>IN</sub>            | Input Pin Inductance                                    |                        |                                      |                    |      | 7                  | nH   |
| Serial Input Port          |                                                         |                        |                                      |                    |      |                    |      |
| V <sub>IL</sub>            | Input Low Voltage                                       |                        | V <sub>DD</sub> = 3.3V               |                    |      | 0.3V <sub>DD</sub> | V    |
| V <sub>IH</sub>            | Input High Voltage                                      |                        | V <sub>DD</sub> = 3.3V               | 0.7V <sub>DD</sub> |      |                    | V    |
| I <sub>IL</sub>            | Input Low Current                                       |                        | No internal pull-up/down on SCLOCK   |                    |      | 10                 | μA   |
| I <sub>IH</sub>            | Input High Current                                      |                        | No internal pull-up/down on SCLOCK   |                    |      | 10                 | μA   |
| I <sub>OL</sub>            | Sink Current into SDATA, Open Drain N-Channel Device On |                        | I <sub>OL</sub> = 0.3V <sub>DD</sub> | 6                  |      |                    | mA   |
| C <sub>IN</sub>            | Input Capacitance of SDATA and SCLOCK                   |                        |                                      |                    |      | 10                 | pF   |
| C <sub>SDATA</sub>         | Total Capacitance of SDATA Bus                          |                        |                                      |                    |      | 400                | pF   |
| C <sub>SCLOCK</sub>        | Total Capacitance of SCLOCK Bus                         |                        |                                      |                    |      | 400                | pF   |

**2.5V DC Electrical Characteristics (CPU3.3#\_2.5 Input = 1)**
 $T_A = 0^{\circ}\text{C to } +70^{\circ}\text{C}$ ,  $V_{DD1:3} = 3.3\text{V} \pm 5\%$  (3.135–3.456V),  $V_{DDL1:2} = 2.5\text{V} \pm 5\%$  (2.375–2.625V)

| Parameter             | Description                       | Test Condition                                     | Min. | Typ. | Max. | Unit          |
|-----------------------|-----------------------------------|----------------------------------------------------|------|------|------|---------------|
| <b>Supply Current</b> |                                   |                                                    |      |      |      |               |
| $I_{DD-3.3V}$         | 3.3V Supply Current               | CPU0:3 = 66.4 MHz<br>Outputs Loaded <sup>[8]</sup> |      |      | 300  | mA            |
| $I_{DD-2.5}$          | 2.5V Supply Current               | CPU0:3 = 66.4 MHz<br>Outputs Loaded <sup>[8]</sup> |      |      | 50   | mA            |
| <b>Logic Inputs</b>   |                                   |                                                    |      |      |      |               |
| $V_{IL}$              | Input Low Voltage                 |                                                    |      |      | 0.8  | V             |
| $V_{IH}$              | Input High Voltage                |                                                    | 2.0  |      |      | V             |
| $I_{IL}$              | Input Low Current <sup>[9]</sup>  |                                                    |      |      | 10   | $\mu\text{A}$ |
| $I_{IH}$              | Input High Current <sup>[9]</sup> |                                                    |      |      | 10   | $\mu\text{A}$ |

**2.5V DC Electrical Characteristics (CPU3.3#\_2.5 Input = 1) (continued)**
 $T_A = 0^{\circ}\text{C to } +70^{\circ}\text{C}$ ,  $V_{DD1:3} = 3.3\text{V} \pm 5\%$  (3.135–3.456V),  $V_{DDL1:2} = 2.5\text{V} \pm 5\%$  (2.375–2.625V)

| Parameter                  | Description            |                        | Test Condition          | Min.               | Typ. | Max.               | Unit |
|----------------------------|------------------------|------------------------|-------------------------|--------------------|------|--------------------|------|
| Clock Outputs              |                        |                        |                         |                    |      |                    |      |
| V <sub>OL</sub>            | Output Low Voltage     |                        | I <sub>OL</sub> = 1 mA  |                    |      | 50                 | mV   |
| V <sub>OH</sub>            | Output High Voltage    |                        | I <sub>OH</sub> = −1 mA | 2.2                |      |                    | V    |
| I <sub>OL</sub>            | Output Low Current     | CPU0:3 <sup>[10]</sup> | V <sub>OL</sub> = 1.25V | 45                 | 70   | 105                | mA   |
|                            |                        | IOAPIC                 | V <sub>OL</sub> = 1.25V | 55                 | 85   | 130                |      |
| I <sub>OH</sub>            | Output High Current    | CPU0:3 <sup>[10]</sup> | V <sub>OH</sub> = 1.25V | 40                 | 65   | 95                 | mA   |
|                            |                        | IOAPIC                 | V <sub>OH</sub> = 1.25V | 50                 | 80   | 120                |      |
| Pin Capacitance/Inductance |                        |                        |                         |                    |      |                    |      |
| C <sub>IN</sub>            | Input Pin Capacitance  |                        | Except X1 and X2        |                    |      | 5                  | pF   |
| C <sub>OUT</sub>           | Output Pin Capacitance |                        |                         |                    |      | 6                  | pF   |
| L <sub>IN</sub>            | Input Pin Inductance   |                        |                         |                    |      | 7                  | nH   |
| Serial Input Port          |                        |                        |                         |                    |      |                    |      |
| V <sub>IL</sub>            | Input Low Voltage      |                        | V <sub>DD</sub> = 2.5V  |                    |      | 0.3V <sub>DD</sub> | V    |
| V <sub>IH</sub>            | Input High Voltage     |                        | V <sub>DD</sub> = 2.5V  | 0.7V <sub>DD</sub> |      |                    | V    |

**3.3V AC Electrical Characteristics (CPU3.3#\_2.5 Input = 0)**
 $T_A = 0^{\circ}\text{C to } +70^{\circ}\text{C}$ ,  $V_{DD1:3} = 3.3\text{V} \pm 5\%$  (3.135–3.465V),  $f_{XTL} = 14.31818\text{ MHz}$ 
**Spread Spectrum function turned off**

AC clock parameters are tested and guaranteed over stated operating conditions using the stated lump capacitive load at the clock output.

**CPU Clock Outputs, CPU0:3 (Lump Capacitance Test Load = 20 pF)**

| Parameter | Description                                        | Test Condition/Comments                                                                                             | CPU = 66.8 MHz |      |      | CPU = 60 MHz |      |      | Unit     |
|-----------|----------------------------------------------------|---------------------------------------------------------------------------------------------------------------------|----------------|------|------|--------------|------|------|----------|
|           |                                                    |                                                                                                                     | Min.           | Typ. | Max. | Min.         | Typ. | Max. |          |
| $t_P$     | Period                                             | Measured on rising edge at 1.5V                                                                                     | 15             |      |      | 16.7         |      |      | ns       |
| $f$       | Frequency, Actual                                  | Determined by PLL divider ratio                                                                                     | 66.8           |      |      | 59.876       |      |      | MHz      |
| $t_H$     | High Time                                          | Duration of clock cycle above 2.4V                                                                                  | 5.2            |      |      | 6            |      |      | ns       |
| $t_L$     | Low Time                                           | Duration of clock cycle below 0.4V                                                                                  | 5              |      |      | 5.8          |      |      | ns       |
| $t_R$     | Output Rise Edge Rate                              | Measured from 0.4V to 2.4V                                                                                          | 1              |      | 4    | 1            |      | 4    | V/ns     |
| $t_F$     | Output Fall Edge Rate                              | Measured from 2.4V to 0.4V                                                                                          | 1              |      | 4    | 1            |      | 4    | V/ns     |
| $t_D$     | Duty Cycle                                         | Measured on rising and falling edge at 1.5V                                                                         | 45             |      | 55   | 45           |      | 55   | %        |
| $t_{JC}$  | Jitter, Cycle-to-Cycle                             | Measured on rising edge at 1.5V. Maximum difference of cycle time between two adjacent cycles.                      |                |      | 250  |              |      | 250  | ps       |
| $t_{SK}$  | Output Skew                                        | Measured on rising edge at 1.5V                                                                                     |                |      | 250  |              |      | 250  | ps       |
| $f_{ST}$  | Frequency Stabilization from Power-up (cold start) | Assumes full supply voltage reached within 1 ms from power-up. Short cycles exist prior to frequency stabilization. |                |      | 3    |              |      | 3    | ms       |
| $Z_0$     | AC Output Impedance                                | Average value during switching transition. Used for determining series termination value.                           | 15             | 20   | 30   | 15           | 20   | 30   | $\Omega$ |

**3.3V AC Electrical Characteristics (CPU3.3#\_2.5 Input = 0) (continued)**
**SDRAM Clock Outputs, SDRAM0:11 (Lump Capacitance Test Load = 30 pF)**

| Parameter       | Description                                        | Test Condition/Comments                                                                                             | CPU = 66.8 MHz |      |      | CPU = 60 MHz |      |      | Unit |
|-----------------|----------------------------------------------------|---------------------------------------------------------------------------------------------------------------------|----------------|------|------|--------------|------|------|------|
|                 |                                                    |                                                                                                                     | Min.           | Typ. | Max. | Min.         | Typ. | Max. |      |
| t <sub>P</sub>  | Period                                             | Measured on rising edge at 1.5V                                                                                     | 15             |      |      | 16.7         |      |      | ns   |
| f               | Frequency, Actual                                  | Determined by PLL divider ratio                                                                                     | 66.8           |      |      | 59.876       |      |      | MHz  |
| t <sub>R</sub>  | Output Rise Edge Rate                              | Measured from 0.4V to 2.4V                                                                                          | 1              |      | 4    | 1            |      | 4    | V/ns |
| t <sub>F</sub>  | Output Fall Edge Rate                              | Measured from 2.4V to 0.4V                                                                                          | 1              |      | 4    | 1            |      | 4    | V/ns |
| t <sub>D</sub>  | Duty Cycle                                         | Measured on rising and falling edge at 1.5V                                                                         | 45             |      | 55   | 45           |      | 55   | %    |
| t <sub>JC</sub> | Jitter, Cycle-to-Cycle                             | Measured on rising edge at 1.5V. Maximum difference of cycle time between two adjacent cycles.                      |                |      | 250  |              |      | 250  | ps   |
| t <sub>SK</sub> | Output Skew                                        | Measured on rising edge at 1.5V                                                                                     |                | 100  |      |              | 100  |      | ps   |
| t <sub>SK</sub> | CPU to SDRAM Clock Skew                            | Covers all CPU/SDRAM outputs. Measured on rising edge at 1.5V.                                                      |                |      | 500  |              |      | 500  | ps   |
| f <sub>ST</sub> | Frequency Stabilization from Power-up (cold start) | Assumes full supply voltage reached within 1 ms from power-up. Short cycles exist prior to frequency stabilization. |                |      | 3    |              |      | 3    | ms   |
| Z <sub>O</sub>  | AC Output Impedance                                | Average value during switching transition. Used for determining series termination value.                           | 10             | 15   | 20   | 10           | 15   | 20   | Ω    |

**PCI Clock Outputs, PCI\_F and PCI0:5 (Lump Capacitance Test Load = 30 pF)**

| Parameter       | Description                                        | Test Condition/Comments                                                                                             | CPU = 66.8 MHz |      |      | CPU = 60 MHz |      |      | Unit |
|-----------------|----------------------------------------------------|---------------------------------------------------------------------------------------------------------------------|----------------|------|------|--------------|------|------|------|
|                 |                                                    |                                                                                                                     | Min.           | Typ. | Max. | Min.         | Typ. | Max. |      |
| t <sub>P</sub>  | Period                                             | Measured on rising edge at 1.5V                                                                                     | 30             |      |      | 33.3         |      |      | ns   |
| f               | Frequency, Actual                                  | Determined by PLL divider ratio                                                                                     | 33.4           |      |      | 29.938       |      |      | MHz  |
| t <sub>H</sub>  | High Time                                          | Duration of clock cycle above 2.4V                                                                                  | 12             |      |      | 13.3         |      |      | ns   |
| t <sub>L</sub>  | Low Time                                           | Duration of clock cycle below 0.4V                                                                                  | 12             |      |      | 13.3         |      |      | ns   |
| t <sub>R</sub>  | Output Rise Edge Rate                              | Measured from 0.4V to 2.4V                                                                                          | 1              |      | 4    | 1            |      | 4    | V/ns |
| t <sub>F</sub>  | Output Fall Edge Rate                              | Measured from 2.4V to 0.4V                                                                                          | 1              |      | 4    | 1            |      | 4    | V/ns |
| t <sub>D</sub>  | Duty Cycle                                         | Measured on rising and falling edge at 1.5V                                                                         | 45             |      | 55   | 45           |      | 55   | %    |
| t <sub>JC</sub> | Jitter, Cycle-to-Cycle                             | Measured on rising edge at 1.5V. Maximum difference of cycle time between two adjacent cycles.                      |                |      | 250  |              |      | 250  | ps   |
| t <sub>SK</sub> | Output Skew                                        | Measured on rising edge at 1.5V                                                                                     |                |      | 250  |              |      | 250  | ps   |
| t <sub>O</sub>  | CPU to PCI Clock Skew                              | Covers all CPU/PCI outputs. Measured on rising edge at 1.5V. CPU leads PCI output.                                  | 1              |      | 4    | 1            |      | 4    | ns   |
| f <sub>ST</sub> | Frequency Stabilization from Power-up (cold start) | Assumes full supply voltage reached within 1 ms from power-up. Short cycles exist prior to frequency stabilization. |                |      | 3    |              |      | 3    | ms   |
| Z <sub>O</sub>  | AC Output Impedance                                | Average value during switching transition. Used for determining series termination value.                           | 15             | 20   | 30   | 15           | 20   | 30   | Ω    |

**3.3V AC Electrical Characteristics (CPU3.3#\_2.5 Input = 0) (continued)**
**IOAPIC Clock Output (Lump Capacitance Test Load = 20 pF)**

| Parameter       | Description                                        | Test Condition/Comments                                                                                             | CPU = 60/66.8 MHz |      |      | Unit |
|-----------------|----------------------------------------------------|---------------------------------------------------------------------------------------------------------------------|-------------------|------|------|------|
|                 |                                                    |                                                                                                                     | Min.              | Typ. | Max. |      |
| f               | Frequency, Actual                                  | Frequency generated by crystal oscillator                                                                           | 14.31818          |      |      | MHz  |
| t <sub>R</sub>  | Output Rise Edge Rate                              | Measured from 0.4V to 2.4V                                                                                          | 1                 |      | 4    | V/ns |
| t <sub>F</sub>  | Output Fall Edge Rate                              | Measured from 2.4V to 0.4V                                                                                          | 1                 |      | 4    | V/ns |
| t <sub>D</sub>  | Duty Cycle                                         | Measured on rising and falling edge at 1.5V                                                                         | 45                |      | 55   | %    |
| f <sub>ST</sub> | Frequency Stabilization from Power-up (cold start) | Assumes full supply voltage reached within 1 ms from power-up. Short cycles exist prior to frequency stabilization. |                   |      | 1.5  | ms   |
| Z <sub>0</sub>  | AC Output Impedance                                | Average value during switching transition. Used for determining series termination value.                           | 8                 | 12   | 15   | Ω    |

**REF0 Clock Output (Lump Capacitance Test Load = 45 pF)**

| Parameter       | Description                                        | Test Condition/Comments                                                                                             | CPU = 60/66.8 MHz |      |      | Unit |
|-----------------|----------------------------------------------------|---------------------------------------------------------------------------------------------------------------------|-------------------|------|------|------|
|                 |                                                    |                                                                                                                     | Min.              | Typ. | Max. |      |
| f               | Frequency, Actual                                  | Frequency generated by crystal oscillator                                                                           | 14.31818          |      |      | MHz  |
| t <sub>R</sub>  | Output Rise Edge Rate                              | Measured from 0.4V to 2.4V                                                                                          | 1                 |      | 4    | V/ns |
| t <sub>F</sub>  | Output Fall Edge Rate                              | Measured from 2.4V to 0.4V                                                                                          | 1                 |      | 4    | V/ns |
| t <sub>D</sub>  | Duty Cycle                                         | Measured on rising and falling edge at 1.5V                                                                         | 40                |      | 60   | %    |
| f <sub>ST</sub> | Frequency Stabilization from Power-up (cold start) | Assumes full supply voltage reached within 1 ms from power-up. Short cycles exist prior to frequency stabilization. |                   |      | 1.5  | ms   |
| Z <sub>0</sub>  | AC Output Impedance                                | Average value during switching transition. Used for determining series termination value.                           | 17                | 20   | 25   | Ω    |

**REF1 Clock Output (Lump Capacitance Test Load = 20 pF)**

| Parameter       | Description                                        | Test Condition/Comments                                                                                             | CPU = 60/66.8 MHz |      |      | Unit |
|-----------------|----------------------------------------------------|---------------------------------------------------------------------------------------------------------------------|-------------------|------|------|------|
|                 |                                                    |                                                                                                                     | Min.              | Typ. | Max. |      |
| f               | Frequency, Actual                                  | Frequency generated by crystal oscillator                                                                           | 14.31818          |      |      | MHz  |
| t <sub>R</sub>  | Output Rise Edge Rate                              | Measured from 0.4V to 2.4V                                                                                          | 1                 |      | 4    | V/ns |
| t <sub>F</sub>  | Output Fall Edge Rate                              | Measured from 2.4V to 0.4V                                                                                          | 1                 |      | 4    | V/ns |
| t <sub>D</sub>  | Duty Cycle                                         | Measured on rising and falling edge at 1.5V                                                                         | 40                |      | 55   | %    |
| f <sub>ST</sub> | Frequency Stabilization from Power-up (cold start) | Assumes full supply voltage reached within 1 ms from power-up. Short cycles exist prior to frequency stabilization. |                   |      | 1.5  | ms   |
| Z <sub>0</sub>  | AC Output Impedance                                | Average value during switching transition. Used for determining series termination value.                           | 20                | 25   | 35   | Ω    |

**3.3V AC Electrical Characteristics (CPU3.3#\_2.5 Input = 0) (continued)**
**48-/24-MHz Clock Outputs (Lump Capacitance Test Load = 20 pF)**

| Parameter       | Description                                        | Test Condition/Comments                                                                                             | CPU = 60/66.8 MHz |      |      | Unit |
|-----------------|----------------------------------------------------|---------------------------------------------------------------------------------------------------------------------|-------------------|------|------|------|
|                 |                                                    |                                                                                                                     | Min.              | Typ. | Max. |      |
| f               | Frequency, Actual                                  | Determined by PLL divider ratio (see n/m below)                                                                     | 48.008/24.004     |      |      | MHz  |
| f <sub>D</sub>  | Deviation from 48 MHz                              | (48.008 – 48)/48                                                                                                    | +167              |      |      | ppm  |
| m/n             | PLL Ratio                                          | (14.31818 MHz x 57/17 = 48.008 MHz)                                                                                 | 57/17             |      |      |      |
| t <sub>R</sub>  | Output Rise Edge Rate                              | Measured from 0.4V to 2.4V                                                                                          | 1                 |      | 4    | V/ns |
| t <sub>F</sub>  | Output Fall Edge Rate                              | Measured from 2.4V to 0.4V                                                                                          | 1                 |      | 4    | V/ns |
| t <sub>D</sub>  | Duty Cycle                                         | Measured on rising and falling edge at 1.5V                                                                         | 40                |      | 55   | %    |
| t <sub>JC</sub> | Jitter, Cycle-to-Cycle                             | Measured on rising edge at 1.5V. Maximum difference of cycle time between two adjacent cycles.                      |                   |      | 500  | ps   |
| f <sub>ST</sub> | Frequency Stabilization from Power-up (cold start) | Assumes full supply voltage reached within 1 ms from power-up. Short cycles exist prior to frequency stabilization. |                   |      | 3    | ms   |
| Z <sub>0</sub>  | AC Output Impedance                                | Average value during switching transition. Used for determining series termination value.                           | 15                | 20   | 30   | Ω    |

**Serial Input Port**

| Parameter           | Description                                    | Test Condition                                                                           | Min. | Typ. | Max. | Unit |
|---------------------|------------------------------------------------|------------------------------------------------------------------------------------------|------|------|------|------|
| f <sub>SCLOCK</sub> | SCLOCK Frequency                               | Normal Mode                                                                              | 0    |      | 100  | kHz  |
| t <sub>STHD</sub>   | Start Hold Time                                |                                                                                          | 4.0  |      |      | μs   |
| t <sub>LOW</sub>    | SCLOCK Low Time                                |                                                                                          | 4.7  |      |      | μs   |
| t <sub>HIGH</sub>   | SCLOCK High Time                               |                                                                                          | 4.0  |      |      | μs   |
| t <sub>DSU</sub>    | Data Setup Time                                |                                                                                          | 250  |      |      | ns   |
| t <sub>DHD</sub>    | Data Hold Time                                 | (Transmitter should provide a 300-ns hold time to ensure proper timing at the receiver.) | 0    |      |      | ns   |
| t <sub>R</sub>      | Rise Time, SDATA and SCLOCK                    | From 0.3V <sub>DD</sub> to 0.7V <sub>DD</sub>                                            |      |      | 1000 | ns   |
| t <sub>F</sub>      | Fall Time, SDATA and SCLOCK                    | From 0.7V <sub>DD</sub> to 0.3V <sub>DD</sub>                                            |      |      | 300  | ns   |
| t <sub>STSU</sub>   | Stop Setup Time                                |                                                                                          | 4.0  |      |      | μs   |
| t <sub>SPF</sub>    | Bus Free Time between Stop and Start Condition |                                                                                          | 4.7  |      |      | μs   |
| t <sub>SP</sub>     | Allowable Noise Spike Pulse Width              |                                                                                          |      |      | 50   | ns   |

**2.5V AC Electrical Characteristics (CPU3.3#\_2.5 Input = 1)**
 $T_A = 0^{\circ}\text{C to } +70^{\circ}\text{C}$ ,  $V_{DD1:3} = 3.3\text{V} \pm 5\%$  (3.135–3.465V),  $V_{DDL1:2} = 2.5\text{V} \pm 5\%$  (2.375–2.625V),

 $f_{XTL} = 14.31818 \text{ MHz}$ 

Spread Spectrum function turned off

AC clock parameters are tested and guaranteed over stated operating conditions using the stated lump capacitive load at the clock output.

**CPU Clock Outputs, CPU0:3 (Lump Capacitance Test Load = 20 pF)**

| Parameter | Description                                        | Test Condition/Comments                                                                                             | CPU = 66.8 MHz |      |      | CPU = 60 MHz |      |      | Unit     |
|-----------|----------------------------------------------------|---------------------------------------------------------------------------------------------------------------------|----------------|------|------|--------------|------|------|----------|
|           |                                                    |                                                                                                                     | Min.           | Typ. | Max. | Min.         | Typ. | Max. |          |
| $t_P$     | Period                                             | Measured on rising edge at 1.25V                                                                                    | 15             |      |      | 16.7         |      |      | ns       |
| $f$       | Frequency, Actual                                  | Determined by PLL divider ratio                                                                                     | 66.8           |      |      | 59.876       |      |      | MHz      |
| $t_H$     | High Time                                          | Duration of clock cycle above 2.0V                                                                                  | 5.2            |      |      | 6            |      |      | ns       |
| $t_L$     | Low Time                                           | Duration of clock cycle below 0.4V                                                                                  | 5              |      |      | 5.8          |      |      | ns       |
| $t_R$     | Output Rise Edge Rate                              | Measured from 0.4V to 2.0V                                                                                          | 0.8            |      | 3    | 0.8          |      | 3    | V/ns     |
| $t_F$     | Output Fall Edge Rate                              | Measured from 2.0V to 0.4V                                                                                          | 0.8            |      | 3    | 0.8          |      | 3    | V/ns     |
| $t_D$     | Duty Cycle                                         | Measured on rising and falling edge at 1.25V                                                                        | 45             |      | 55   | 45           |      | 55   | %        |
| $t_{JC}$  | Jitter, Cycle-to-Cycle                             | Measured on rising edge at 1.25V. Maximum difference of cycle time between two adjacent cycles.                     |                |      | 250  |              |      | 250  | ps       |
| $t_{SK}$  | Output Skew                                        | Measured on rising edge at 1.25V                                                                                    |                |      | 250  |              |      | 250  | ps       |
| $f_{ST}$  | Frequency Stabilization from Power-up (cold start) | Assumes full supply voltage reached within 1 ms from power-up. Short cycles exist prior to frequency stabilization. |                |      | 3    |              |      | 3    | ms       |
| $Z_o$     | AC Output Impedance                                | Average value during switching transition. Used for determining series termination value.                           | 12             | 20   | 30   | 12           | 20   | 30   | $\Omega$ |

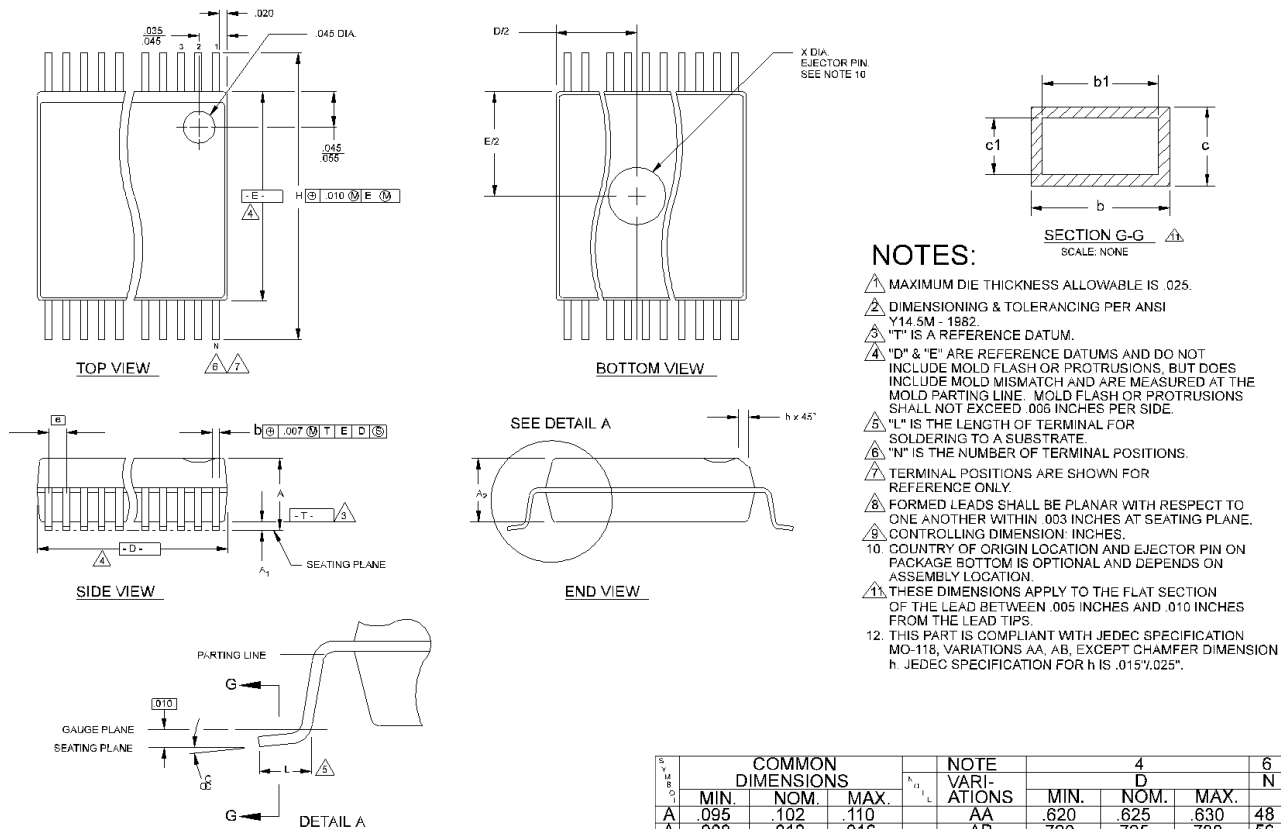
**IOAPIC Clock Output (Lump Capacitance Test Load = 20 pF)**

| Parameter | Description                                        | Test Condition/Comments                                                                                             | CPU = 60/66.8 MHz |      |      | Unit     |
|-----------|----------------------------------------------------|---------------------------------------------------------------------------------------------------------------------|-------------------|------|------|----------|
|           |                                                    |                                                                                                                     | Min.              | Typ. | Max. |          |
| $f$       | Frequency, Actual                                  | Frequency generated by crystal oscillator                                                                           | 14.31818          |      |      | MHz      |
| $t_R$     | Output Rise Edge Rate                              | Measured from 0.4V to 2.0V                                                                                          | 1                 |      | 4    | V/ns     |
| $t_F$     | Output Fall Edge Rate                              | Measured from 2.0V to 0.4V                                                                                          | 1                 |      | 4    | V/ns     |
| $t_D$     | Duty Cycle                                         | Measured on rising and falling edge at 1.25V                                                                        | 45                |      | 55   | %        |
| $f_{ST}$  | Frequency Stabilization from Power-up (cold start) | Assumes full supply voltage reached within 1 ms from power-up. Short cycles exist prior to frequency stabilization. |                   |      | 1.5  | ms       |
| $Z_o$     | AC Output Impedance                                | Average value during switching transition. Used for determining series termination value.                           | 10                | 15   | 25   | $\Omega$ |

**Ordering Information**

| Ordering Code | Freq. Mask Code | Package Name | Package Type           |
|---------------|-----------------|--------------|------------------------|
| W48S87        | 04              | H            | 48-pin SSOP (300 mils) |

Document #: 38-00859

**Package Diagram**
**48-Pin Small Shrink Outline Package (SSOP, 300 mils)**

**Summary of nominal dimensions in inches:**

**Body Width: 0.296**  
**Lead Pitch: 0.025**  
**Body Length: 0.625**  
**Body Height: 0.102**

| SYMBOL | COMMON DIMENSIONS |      |       | NOTE VARIATIONS | 4 D  |      |      | 6 N |
|--------|-------------------|------|-------|-----------------|------|------|------|-----|
|        | MIN.              | NOM. | MAX.  |                 | MIN. | NOM. | MAX. | N   |
|        |                   |      |       |                 |      |      |      |     |
| A      | .095              | .102 | .110  | AA              | .620 | .625 | .630 | 48  |
| A1     | .008              | .012 | .016  | AB              | .720 | .725 | .730 | 56  |
| A2     | .088              | .090 | .092  |                 |      |      |      |     |
| b      | .008              | .010 | .0135 |                 |      |      |      |     |
| b1     | .008              | .010 | .012  |                 |      |      |      |     |
| c      | .005              | -    | .010  |                 |      |      |      |     |
| c1     | .005              | .006 | .0085 |                 |      |      |      |     |
| D      | SEE VARIATIONS    |      |       | 4               |      |      |      |     |
| E      | .292              | .296 | .299  |                 |      |      |      |     |
| e      | .025 BSC          |      |       |                 |      |      |      |     |
| H      | .400              | .406 | .410  |                 |      |      |      |     |
| h      | .010              | .013 | .016  |                 |      |      |      |     |
| L      | .024              | .032 | .040  |                 |      |      |      |     |
| N      | SEE VARIATIONS    |      |       | 6               |      |      |      |     |
| X      | .085              | .093 | .100  | 10              |      |      |      |     |
| α      | 0°                | 5°   | 8°    |                 |      |      |      |     |

THIS TABLE IN INCHES

| SYMBOL | COMMON DIMENSIONS |       |       | NOTE VARIATIONS | 4 D   |       |       | 6 N |
|--------|-------------------|-------|-------|-----------------|-------|-------|-------|-----|
|        | MIN.              | NOM.  | MAX.  |                 | MIN.  | NOM.  | MAX.  | N   |
|        |                   |       |       |                 |       |       |       |     |
| A      | 2.41              | 2.59  | 2.79  | AA              | 15.75 | 15.88 | 16.00 | 48  |
| A1     | 0.20              | 0.31  | 0.41  | AB              | 18.29 | 18.42 | 18.54 | 56  |
| A2     | 2.24              | 2.29  | 2.34  |                 |       |       |       |     |
| b      | 0.203             | 0.254 | 0.343 |                 |       |       |       |     |
| b1     | 0.203             | 0.254 | 0.305 |                 |       |       |       |     |
| c      | 0.127             | -     | 0.254 |                 |       |       |       |     |
| c1     | 0.127             | 0.152 | 0.216 |                 |       |       |       |     |
| D      | SEE VARIATIONS    |       |       | 4               |       |       |       |     |
| E      | 7.42              | 7.52  | 7.59  |                 |       |       |       |     |
| e      | 0.635 BSC         |       |       |                 |       |       |       |     |
| H      | 10.16             | 10.31 | 10.41 |                 |       |       |       |     |
| h      | 0.25              | 0.33  | 0.41  |                 |       |       |       |     |
| L      | 0.61              | 0.81  | 1.02  |                 |       |       |       |     |
| N      | SEE VARIATIONS    |       |       | 6               |       |       |       |     |
| X      | 2.16              | 2.36  | 2.54  | 10              |       |       |       |     |
| α      | 0°                | 5°    | 8°    |                 |       |       |       |     |

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### Офис по работе с юридическими лицами:

105318, г.Москва, ул.Щербаковская д.3, офис 1107, 1118, ДЦ «Щербаковский»

Телефон: +7 495 668-12-70 (многоканальный)

Факс: +7 495 668-12-70 (доб.304)

E-mail: [info@moschip.ru](mailto:info@moschip.ru)

Skype отдела продаж:

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