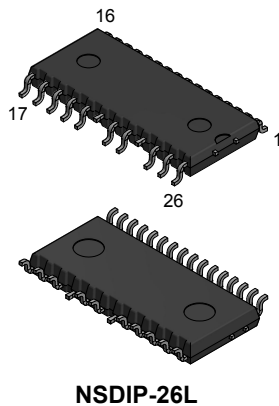


## SLLIMM™-nano IPM, 3 A, 600 V, 3-phase IGBT inverter bridge



**NSDIP-26L**

### Features

- IPM 3 A, 600 V, 3-phase IGBT inverter bridge including control ICs for gate driving and freewheeling diodes
- Optimized for low electromagnetic interference
- $V_{CE(sat)}$  negative temperature coefficient
- 3.3 V, 5 V, 15 V CMOS/TTL inputs comparators with hysteresis and pull-down/pull-up resistors
- Undervoltage lockout
- Internal bootstrap diode
- Interlocking function
- Comparator for fault protection against overtemperature and overcurrent
- Op-amp for advanced current sensing
- Optimized pinout for easy board layout
- NTC for temperature control (UL 1434 CA 2 and 4)
- Moisture sensitivity level (MSL) 3 for SMD package

### Applications

- 3-phase inverters for motor drives
- Roller shutters, dish washers, refrigerator compressors, heating systems, airconditioning fans, draining and recirculation pumps

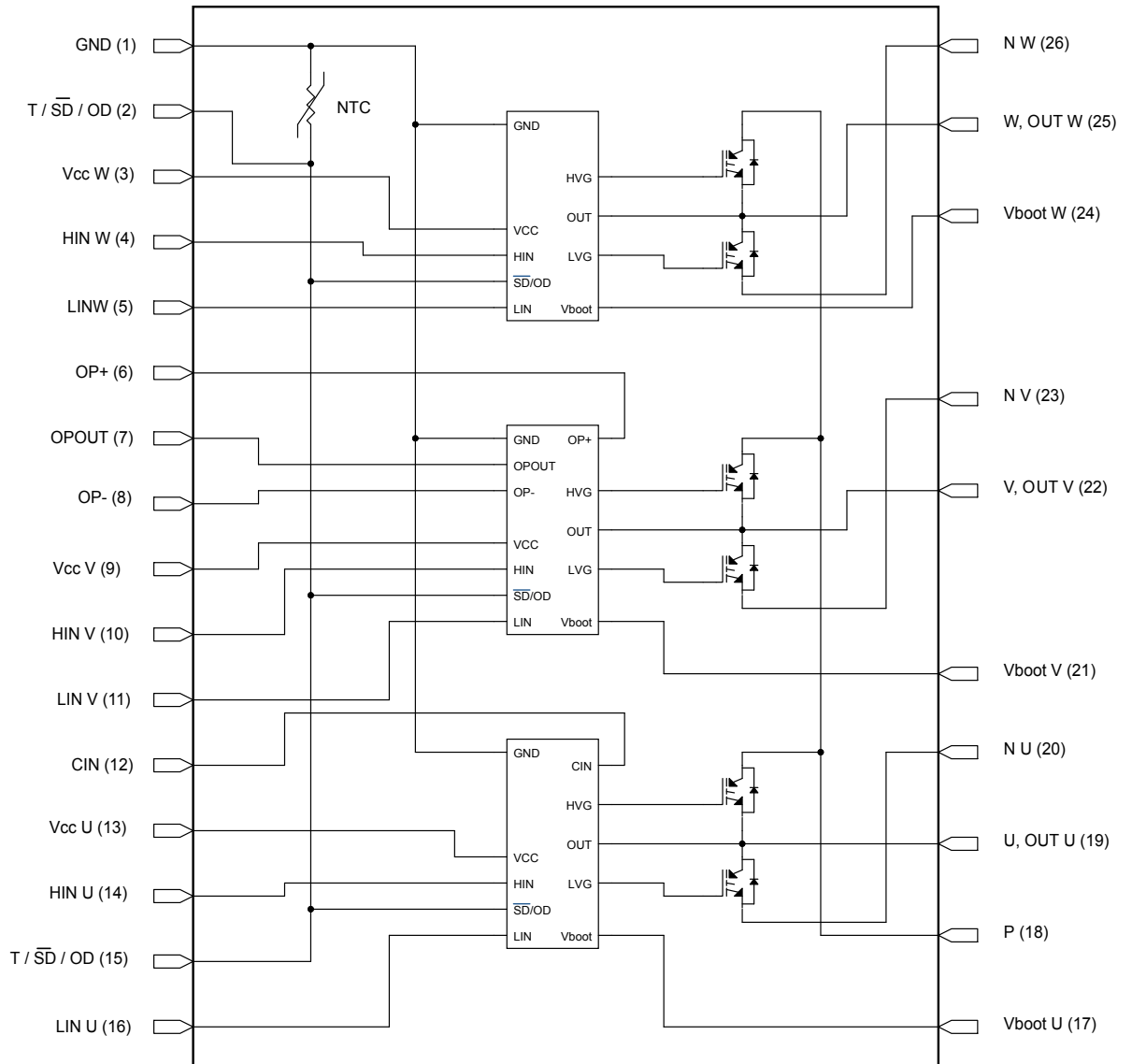
### Description

This SLLIMM (small low-loss intelligent molded module) nano provides a compact, high-performance AC motor drive in a simple, rugged design. It is composed of six IGBTs and three half-bridge HVICs for gate driving, providing low electromagnetic interference (EMI) characteristics with optimized switching speed. The package is optimized for thermal performance and compactness in built-in motor applications, or other low power applications where assembly space is limited. This IPM includes an operational amplifier, completely uncommitted, and a comparator that can be used to design a fast and efficient protection circuit. SLLIMM™ is a trademark of STMicroelectronics.

Product status	
STGIPNS3H60T-H	
Device summary	
<b>Order code</b>	STGIPNS3H60T-H
<b>Marking</b>	GIPNS3H60T-H
<b>Package</b>	NSDIP-26L
<b>Packing</b>	Tape and reel

# 1 Internal schematic diagram and pin configuration

Figure 1. Internal schematic diagram

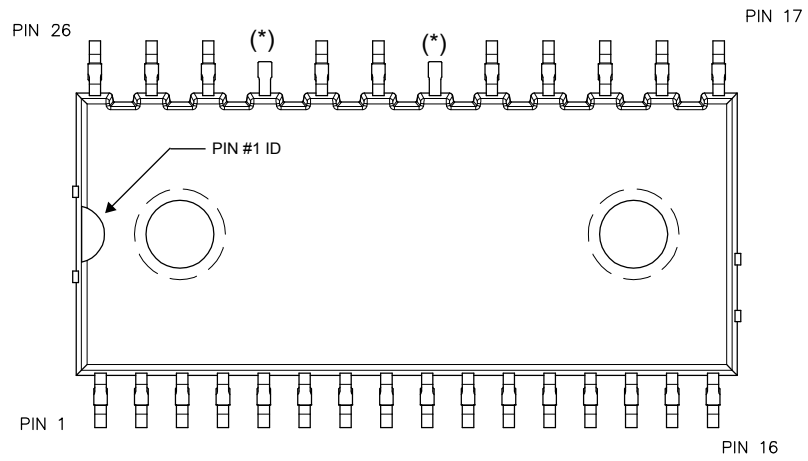


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**Table 1. Pin description**

Pin	Symbol	Description
1	GND	Ground
2	T/SD/ OD	NTC thermistor terminal / shutdown logic input (active low) / open-drain (comparator output)
3	V <sub>CC</sub> W	Low voltage power supply W phase
4	HIN W	High-side logic input for W phase
5	LIN W	Low-side logic input for W phase
6	OP+	Op-amp non inverting input
7	OP <sub>OUT</sub>	Op-amp output
8	OP-	Op-amp inverting input
9	V <sub>CC</sub> V	Low voltage power supply V phase
10	HIN V	High-side logic input for V phase
11	LIN V	Low-side logic input for V phase
12	CIN	Comparator input
13	V <sub>CC</sub> U	Low voltage power supply for U phase
14	HIN U	High-side logic input for U phase
15	T/SD/OD	NTC thermistor terminal / shutdown logic input (active low) / open-drain (comparator output)
16	LIN U	Low-side logic input for U phase
17	V <sub>BOOT</sub> U	Bootstrap voltage for U phase
18	P	Positive DC input
19	U, OUT <sub>U</sub>	U phase output
20	N <sub>U</sub>	Negative DC input for U phase
21	V <sub>BOOT</sub> V	Bootstrap voltage for V phase
22	V, OUT <sub>V</sub>	V phase output
23	N <sub>V</sub>	Negative DC input for V phase
24	V <sub>BOOT</sub> W	Bootstrap voltage for W phase
25	W, OUT <sub>W</sub>	W phase output
26	N <sub>W</sub>	Negative DC input for W phase

**Figure 2. Pin layout (top view)**



(\* Dummy pin internally connected to P (positive DC input).

## 2 Electrical ratings

### 2.1 Absolute maximum ratings

**Table 2. Inverter part**

Symbol	Parameter	Value	Unit
V <sub>CES</sub>	Each IGBT collector emitter voltage (V <sub>IN</sub> <sup>(1)</sup> = 0 V)	600	V
±I <sub>C</sub> <sup>(2)</sup>	Each IGBT continuous collector current (T <sub>C</sub> = 25 °C)	3	A
±I <sub>CP</sub> <sup>(3)</sup>	Each IGBT pulsed collector current (less than 1 ms)	18	A
P <sub>TOT</sub>	Each IGBT total dissipation (T <sub>C</sub> = 25 °C)	6.6	W

1. Applied among HIN<sub>i</sub>, LIN<sub>i</sub> and GND for i = U, V, W
2. Calculated according to the iterative formula:

$$I_C(T_C) = \frac{T_{j(max)} - T_C}{R_{thj-c} \cdot V_{CE(sat)(max)}(T_{j(max)}, I_C(T_C))}$$

3. Pulse width limited by max junction temperature.

**Table 3. Control part**

Symbol	Parameter	Min.	Max.	Unit
V <sub>OUT</sub>	Output voltage applied among OUT <sub>U</sub> , OUT <sub>V</sub> , OUT <sub>W</sub> - GND	V <sub>boot</sub> - 21	V <sub>boot</sub> + 0.3	V
V <sub>CC</sub>	Low voltage power supply	- 0.3	21	V
V <sub>CIN</sub>	Comparator input voltage	- 0.3	V <sub>CC</sub> + 0.3	V
V <sub>op+</sub>	Op-amp non-inverting input	- 0.3	V <sub>CC</sub> + 0.3	V
V <sub>op-</sub>	Op-amp inverting input	- 0.3	V <sub>CC</sub> + 0.3	V
V <sub>boot</sub>	Bootstrap voltage	- 0.3	620	V
V <sub>IN</sub>	Logic input voltage applied among HIN, LIN and GND	- 0.3	15	V
V <sub>T/SD/OD</sub>	Open-drain voltage	- 0.3	15	V
dv <sub>out</sub> /dt	Allowed output slew rate		50	V/ns

**Table 4. Total system**

Symbol	Parameter	Value	Unit
V <sub>ISO</sub>	Isolation withstand voltage applied between each pin and heatsink plate (AC voltage, t = 60 s)	1000	V
T <sub>J</sub>	Power chips operating junction temperature	-40 to 150	°C
T <sub>C</sub>	Module case operation temperature	-40 to 125	°C

## 2.2 Thermal data

**Table 5. Thermal data**

Symbol	Parameter	Value	Unit
$R_{thJA}$	Thermal resistance junction-ambient	44	°C/W

### 3 Electrical characteristics

#### 3.1 Inverter part

$T_J = 25\text{ °C}$  unless otherwise specified

**Table 6. Static**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{CE(sat)}$	Collector-emitter saturation voltage	$V_{CC} = V_{boot} = 15\text{ V}$ , $V_{IN}^{(1)} = 0\text{ to }5\text{ V}$ , $I_C = 1\text{ A}$	-	2.15	2.6	V
		$V_{CC} = V_{boot} = 15\text{ V}$ , $V_{IN}^{(1)} = 0\text{ to }5\text{ V}$ , $I_C = 1\text{ A}$ , $T_J = 125\text{ °C}$	-	1.65		
$I_{CES}$	Collector-cut off current ( $V_{IN}^{(1)} = 0$ "logic state")	$V_{CE} = 550\text{ V}$ , $V_{CC} = 15\text{ V}$ , $V_{BS} = 15\text{ V}$	-		250	$\mu\text{A}$
$V_F$	Diode forward voltage	$V_{IN}^{(1)} = 0$ "logic state", $I_C = 1\text{ A}$	-		1.7	V

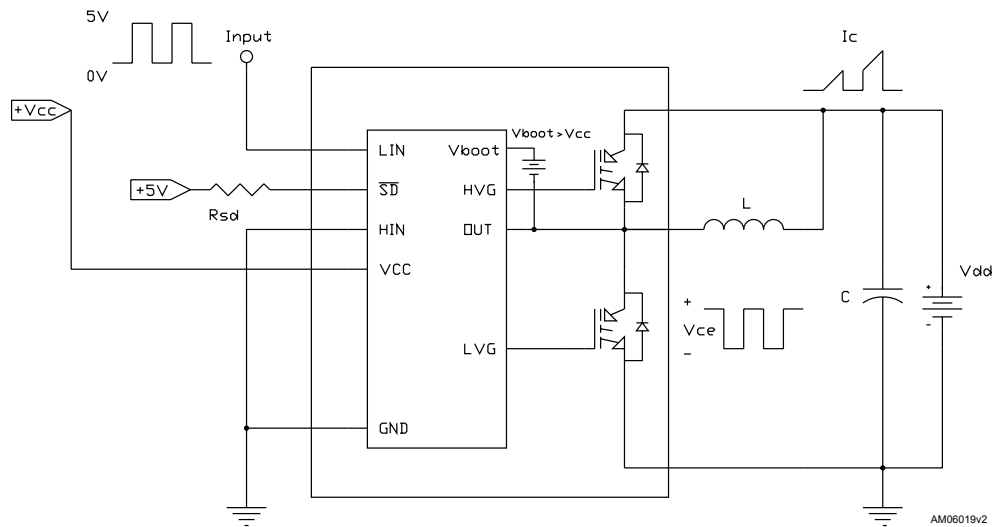
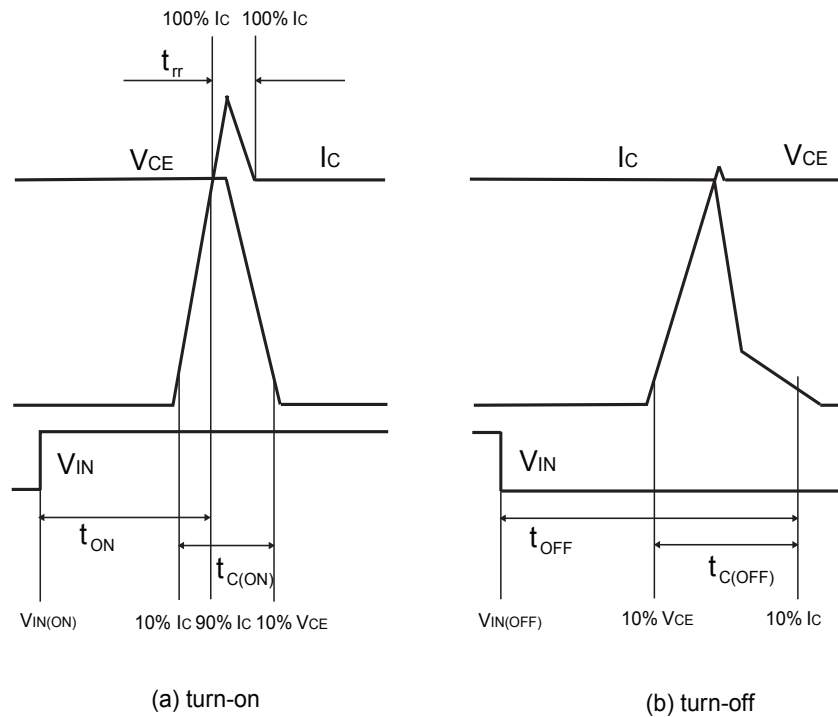
1. Applied among  $HIN_i$ ,  $LIN_i$  and GND for  $i = U, V, W$ .

**Table 7. Inductive load switching time and energy**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{on}^{(1)}$	Turn-on time	$V_{DD} = 300\text{ V}$ , $V_{CC} = V_{boot} = 15\text{ V}$ , $V_{IN}^{(2)} = 0\text{ to }5\text{ V}$ , $I_C = 1\text{ A}$ (see Figure 4. Switching time definition)	-	275	-	ns
$t_{c(on)}^{(1)}$	Crossover time (on)		-	90	-	
$t_{off}^{(1)}$	Turn-off time		-	890	-	
$t_{c(off)}^{(1)}$	Crossover time (off)		-	125	-	
$t_{rr}$	Reverse recovery time		-	50	-	
$E_{on}$	Turn-on switching energy		-	18	-	$\mu\text{J}$
$E_{off}$	Turn-off switching energy		-	13	-	

1.  $t_{ON}$  and  $t_{OFF}$  include the propagation delay time of the internal drive.  $t_{C(ON)}$  and  $t_{C(OFF)}$  are the switching times of IGBT itself under the internally given gate driving condition.

2. Applied among  $HIN_i$ ,  $LIN_i$  and GND for  $i = U, V, W$ .

**Figure 3. Switching time test circuit**

**Figure 4. Switching time definition**


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Figure 4. Switching time definition refers to HIN, LIN inputs (active high).



### 3.2 Control part

$V_{CC} = 15\text{ V}$  unless otherwise specified

**Table 8. Low voltage power supply**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{CC\_hys}$	$V_{CC}$ UV hysteresis		1.2	1.5	1.8	V
$V_{CC\_thON}$	$V_{CC}$ UV turn ON threshold		11.5	12	12.5	V
$V_{CC\_thOFF}$	$V_{CC}$ UV turn OFF threshold		10	10.5	11	V
$I_{qccu}$	Undervoltage quiescent supply current	$V_{CC} = 10\text{ V}$ , $T/\overline{SD}/OD = 5\text{ V}$ , $LIN = 0\text{ V}$ , $HIN = 0\text{ V}$ , $CIN = 0\text{ V}$			150	$\mu\text{A}$
$I_{qcc}$	Quiescent current	$V_{CC} = 15\text{ V}$ , $T/\overline{SD}/OD = 5\text{ V}$ , $LIN = 0\text{ V}$ , $HIN = 0\text{ V}$ , $CIN = 0\text{ V}$			1	mA
$V_{ref}$	Internal comparator (CIN) reference voltage		0.5	0.54	0.58	V

**Table 9. Bootstrapped voltage**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{BS\_hys}$	$V_{BS}$ UV hysteresis		1.2	1.5	1.8	V
$V_{BS\_thON}$	$V_{BS}$ UV turn ON threshold		11.1	11.5	12.1	V
$V_{BS\_thOFF}$	$V_{BS}$ UV turn OFF threshold		9.8	10	10.6	V
$I_{QBSU}$	Undervoltage $V_{BS}$ quiescent current	$V_{BS} < 9\text{ V}$ , $T/\overline{SD}/OD = 5\text{ V}$ , $LIN = 0\text{ V}$ and $HIN = 5\text{ V}$ , $CIN = 0\text{ V}$		70	110	$\mu\text{A}$
$I_{QBS}$	$V_{BS}$ quiescent current	$V_{BS} = 15\text{ V}$ , $T/\overline{SD}/OD = 5\text{ V}$ , $LIN = 0\text{ V}$ and $HIN = 5\text{ V}$ , $CIN = 0\text{ V}$		200	300	$\mu\text{A}$
$R_{DS(on)}$	Bootstrap driver on-resistance	LVG ON		120		$\Omega$

**Table 10. Logic inputs**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{il}$	Low logic level voltage				0.8	V
$V_{ih}$	High logic level voltage		2.25			V
$I_{HINh}$	HIN logic "1" input bias current	$HIN = 15\text{ V}$	20	40	100	$\mu\text{A}$
$I_{HINl}$	HIN logic "0" input bias current	$HIN = 0\text{ V}$			1	$\mu\text{A}$
$I_{LINl}$	LIN logic "0" input bias current	$LIN = 0\text{ V}$			1	$\mu\text{A}$
$I_{LINh}$	LIN logic "1" input bias current	$LIN = 15\text{ V}$	20	40	100	$\mu\text{A}$

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SDh}$	$\overline{SD}$ logic "0" input bias current	$\overline{SD} = 15\text{ V}$	220	295	370	$\mu\text{A}$
$I_{SDl}$	$\overline{SD}$ logic "1" input bias current	$\overline{SD} = 0\text{ V}$			3	$\mu\text{A}$
Dt	Dead time	(see Figure 9. Dead time and interlocking waveform definitions)		180		ns

**Table 11. Op-amp characteristics**

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$V_{io}$	Input offset voltage	$V_{ic} = 0\text{ V}, V_o = 7.5\text{ V}$			6	mV
$I_{io}$	Input offset current	$V_{ic} = 0\text{ V}, V_o = 7.5\text{ V}$		4	40	nA
$I_{ib}$	Input bias current <sup>(1)</sup>			100	200	nA
$V_{OL}$	Low level output voltage	$R_L = 10\text{ k}\Omega$ to $V_{CC}$		75	150	mV
$V_{OH}$	High level output voltage	$R_L = 10\text{ k}\Omega$ to GND	14	14.7		V
$I_o$	Output short-circuit current	Source, $V_{id} = +1\text{ V}, V_o = 0\text{ V}$	16	30		mA
		Sink, $V_{id} = -1\text{ V}, V_o = V_{CC}$	50	80		mA
SR	Slew rate	$V_i = 1 - 4\text{ V}, C_L = 100\text{ pF}$ , unity gain	2.5	3.8		V/ $\mu\text{s}$
GBWP	Gain bandwidth product	$V_o = 7.5\text{ V}$	8	12		MHz
$A_{vd}$	Large signal voltage gain	$R_L = 2\text{ k}\Omega$	70	85		dB
SVR	Supply voltage rejection ratio	vs. $V_{CC}$	60	75		dB
CMRR	Common mode rejection ratio		55	70		dB

1. The direction of input current is out of the IC.

**Table 12. Sense comparator characteristics**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{ib}$	Input bias current	$V_{CIN} = 1\text{ V}$			1	$\mu\text{A}$
$V_{od}$	Open-drain low level output voltage	$I_{od} = 3\text{ mA}$			0.5	V
$R_{ON\_OD}$	Open-drain low level output	$I_{od} = 3\text{ mA}$		166		$\Omega$
$R_{PD\_SD}$	$\overline{SD}$ pull-down resistor <sup>(1)</sup>			125		k $\Omega$
$t_{d\_comp}$	Comparator delay	$T/\overline{SD}/OD$ pulled to 5 V through 100 k $\Omega$ resistor		90	130	ns
SR	Slew rate	$C_L = 180\text{ pF}; R_{pu} = 5\text{ k}\Omega$		60		V/ $\mu\text{s}$
$t_{sd}$	Shutdown to high- / low-side driver propagation delay	$V_{OUT} = 0, V_{boot} = V_{CC}$ , $V_{IN} = 0$ to 3.3 V	50	125	200	ns
$t_{isd}$	Comparator triggering to high- / low-side driver turn-off propagation delay	Measured applying a voltage step from 0 V to 3.3 V to pin CIN	50	200	250	

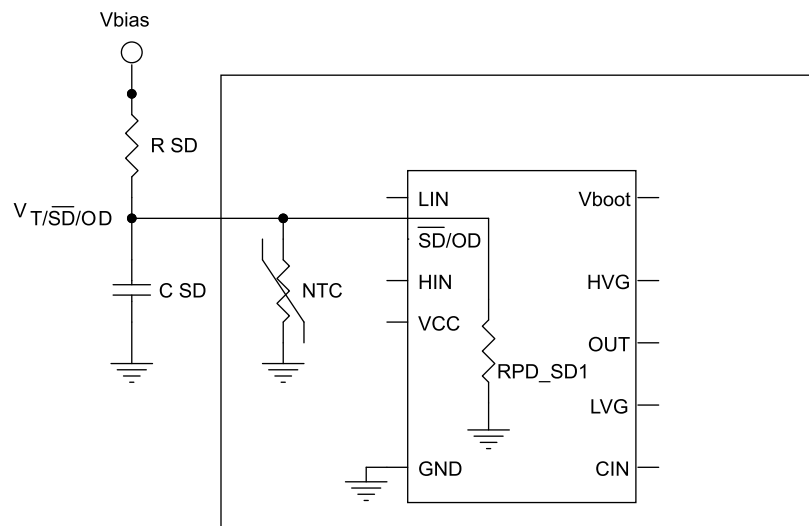
1. Equivalent value derived from the resistances of three drivers in parallel.

**Table 13. Truth table**

Condition	Logic input (V <sub>I</sub> )			Output	
	T/ $\overline{\text{SD}}$ /OD	LIN	HIN	LVG	HVG
Shutdown enable half-bridge tri-state	L	X <sup>(1)</sup>	X <sup>(1)</sup>	L	L
Interlocking half-bridge tri-state	H	H	H	L	L
0 "logic state" half-bridge tri-state	H	L	L	L	L
1 "logic state" low- side direct driving	H	H	L	H	L
1 "logic state" high- side direct driving	H	L	H	L	H

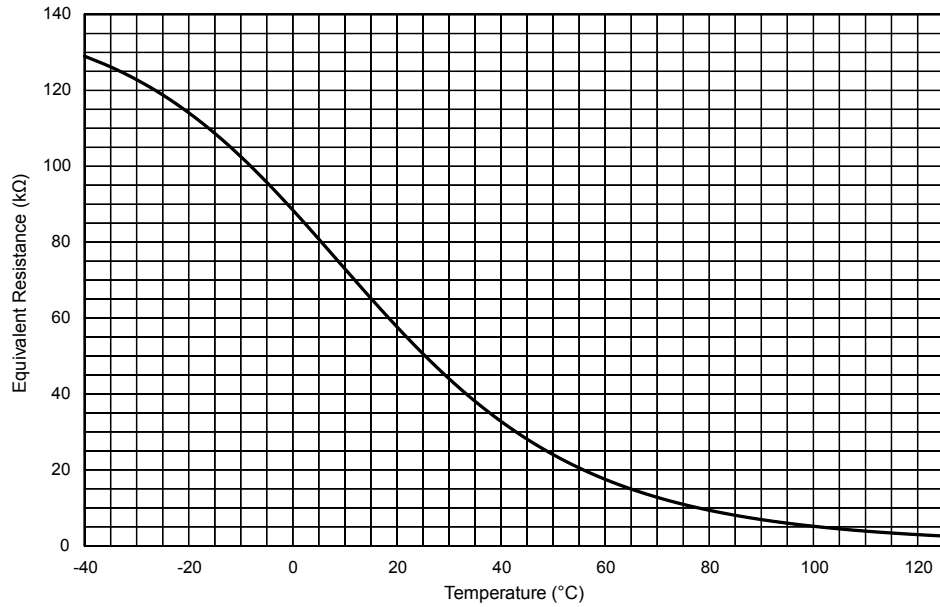
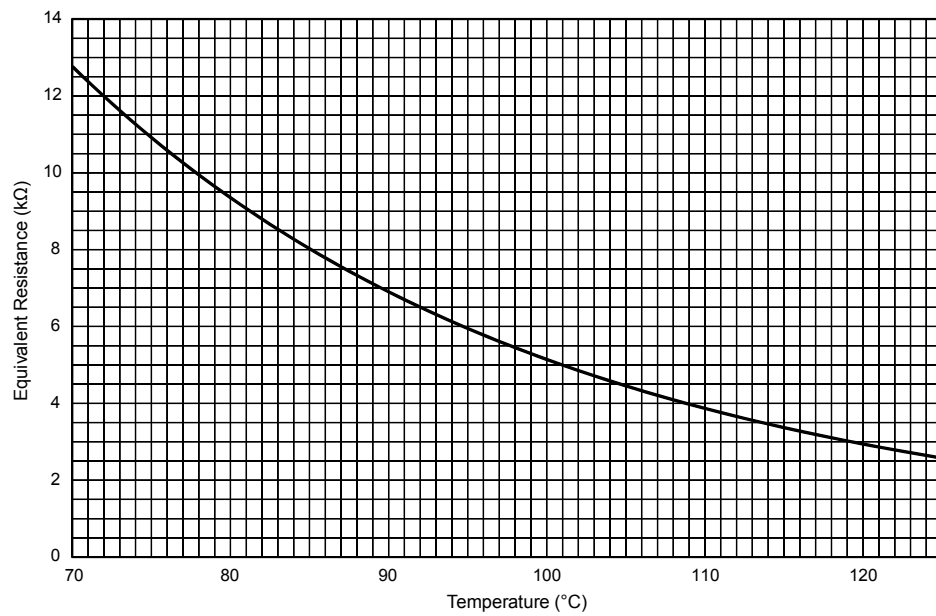
1. X: don't care.

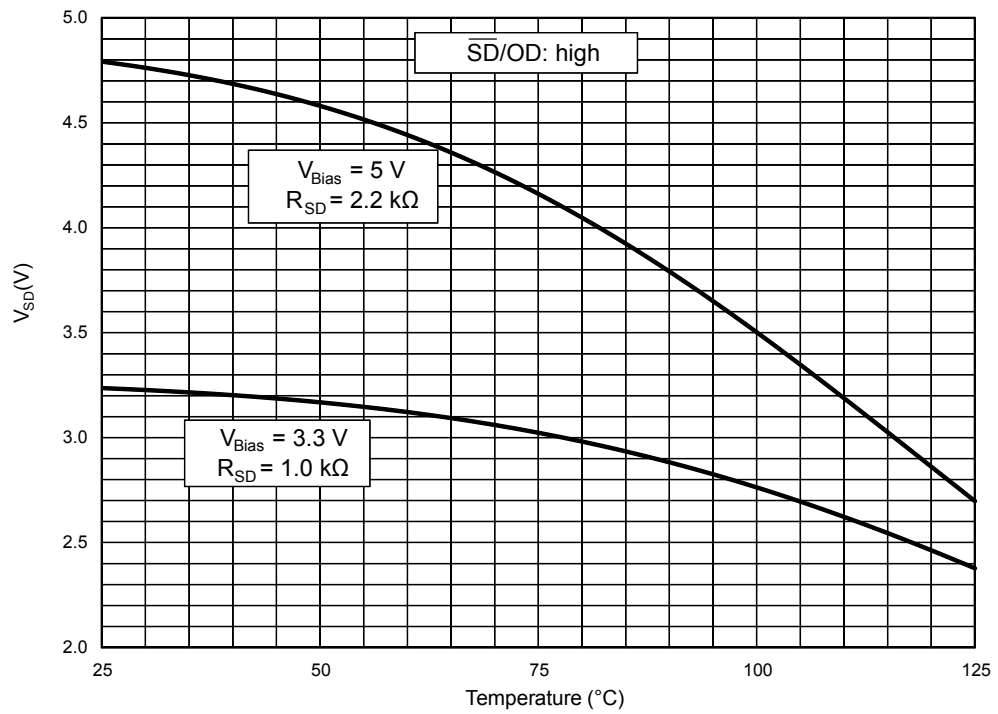
### 3.2.1 NTC thermistor

**Figure 5. Internal structure of  $\overline{\text{SD}}$  and NTC**


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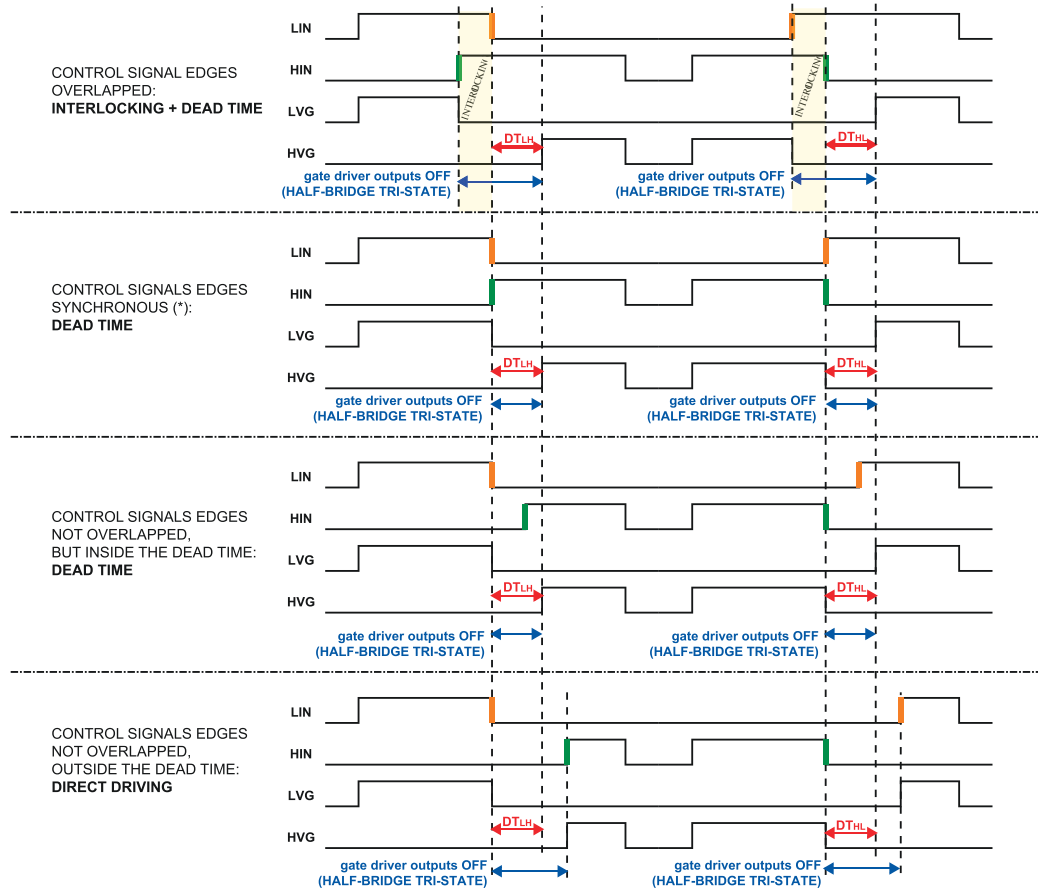
$R_{\text{PD\_SD}}$ : equivalent value as result of resistances of three drivers in parallel.

**Figure 6. Equivalent resistance (NTC//R<sub>PD\_SD</sub>)**

**Figure 7. Equivalent resistance (NTC//R<sub>PD\_SD</sub>) zoom**


**Figure 8. Voltage of T/ $\overline{\text{SD}}$ /OD pin according to NTC temperature**


### 3.3 Waveform definitions

Figure 9. Dead time and interlocking waveform definitions



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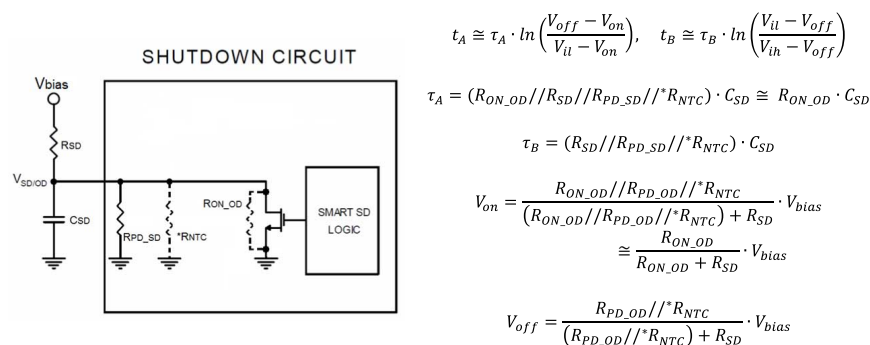
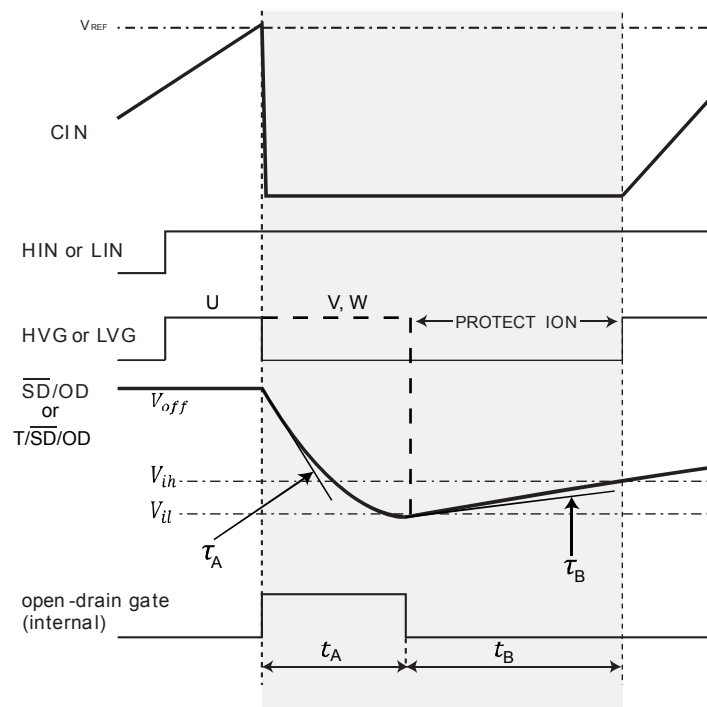
## 4 Shutdown function

The device is equipped with three half-bridge IC gate drivers and integrates a comparator for fault detection. The comparator has an internal voltage reference  $V_{REF}$  connected to the inverting input, while the non-inverting input pin (CIN) can be connected to an external shunt resistor for current monitoring.

Since the comparator is embedded in the U IC gate driver, in case of fault it disables directly the U outputs, whereas the shutdown of V and W IC gate drivers depends on the RC value of the external SD circuitry, which fix the disabling time.

For an effective design of the shutdown circuit, please refer to the AN4966.

**Figure 10. Shutdown timing waveforms**



$R_{SD}$  and  $C_{SD}$  external circuitry must be designed to ensure  $V_{on} < V_{il}$  &  $V_{off} > V_{ih}$

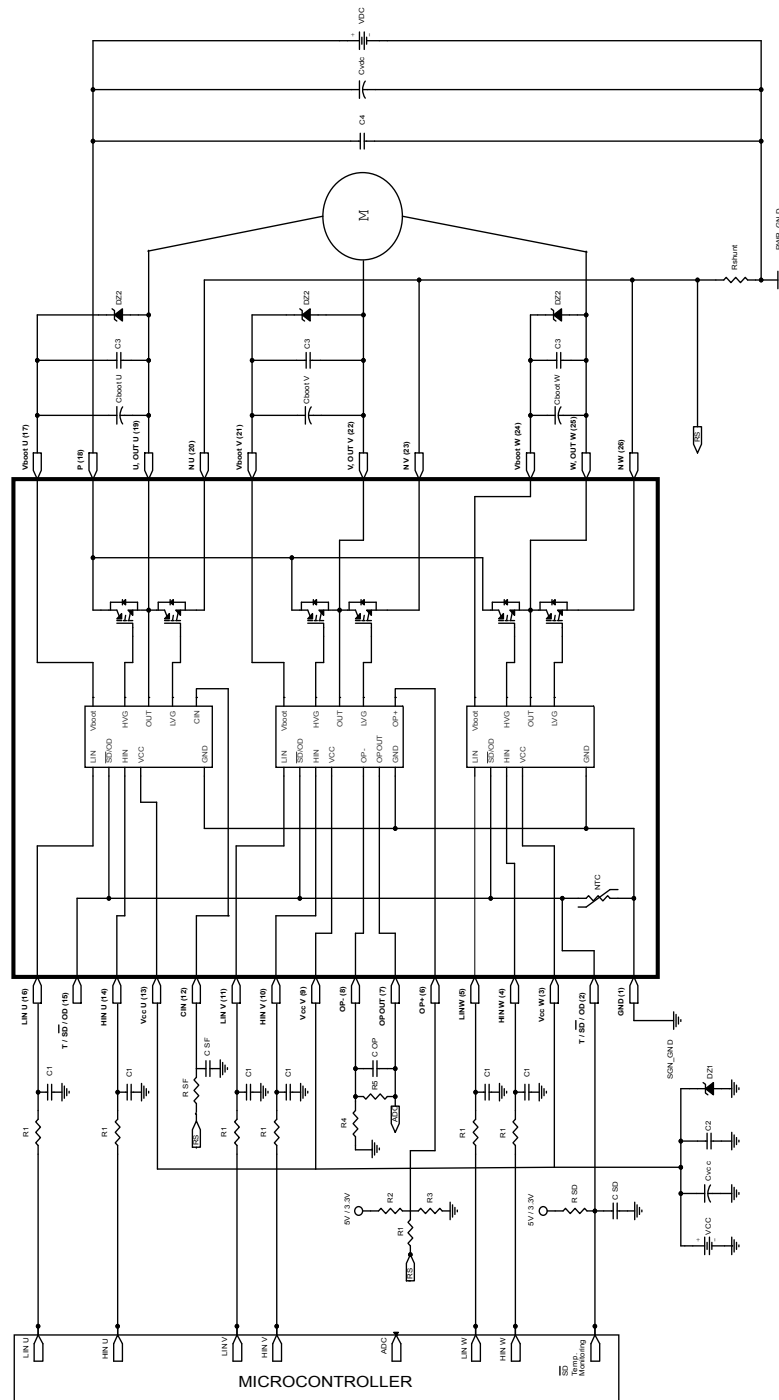
Please refer to AN4966 for further details.

\*  $R_{NTC}$  to be considered only when the NTC is internally connected to the T/SD/OD pin.

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## 5 Application circuit example

Figure 11. Application circuit example



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Application designers are free to use a different scheme according to the device specifications.



## 5.1 Guidelines

- The HIN, LIN input signals are active-high logic. A 375 k $\Omega$  (typ.) pull-down resistor is built-in for each input. To prevent input signal oscillation, the wiring of each input should be as short as possible and the use of RC filters ( $R_1$ ,  $C_1$ ) on each input signal is suggested. The filters should be made with a time constant of about 100 ns and placed as close as possible to the IPM input pins.
- The use of an (aluminum or tantalum) bypass capacitor  $C_{VCC}$  can help to reduce the transient circuit demand on the power supply. Also, to reduce any high-frequency switching noise distributed on the power lines, it is suggested to place a decoupling capacitor  $C_2$  (100 to 220 nF, with low ESR and low ESL) as close as possible to the Vcc pin and in parallel with the bypass capacitor.
- It is recommended to use of an RC filter ( $R_{SF}$ ,  $C_{SF}$ ) for preventing protection circuit malfunction. The time constant ( $R_{SF} \times C_{SF}$ ) should be set to 1  $\mu$ s and the filter must be placed as close as possible to the CIN pin.
- The  $\overline{SD}$  is an input/output pin (open-drain type if used as output). A built-in thermistor NTC is internally connected between the  $\overline{SD}$  pin and GND. The  $V_{SD}$ -GND voltage decreases as the temperature increases due to the pull-up  $R_{SD}$  resistor. In order to keep the voltage always higher than the high-level logic threshold, the pull-up resistor is suggested to be set at 1 k $\Omega$  or 2.2 k $\Omega$  for 3.3 V or 5 V MCU power supply respectively. The  $C_{SD}$  capacitor of the filter on SD should be fixed no higher than 3.3 nF in order to assure an  $\overline{SD}$  activation time of  $T_A \leq 500$  ns; in addition, the filter should be placed as close as possible to the  $\overline{SD}$  pin.
- The  $C_3$  decoupling capacitor (from 100 to 220 nF, ceramic with low ESR and low ESL), placed in parallel with each  $C_{boot}$ , is useful to filter high-frequency disturbance. Both  $C_{boot}$  and  $C_3$  (if present) should be placed as close as possible to the U, V, W and  $V_{boot}$  pins. Bootstrap negative electrodes should be connected to the U, V, W terminals directly and separated from the main output wires.
- To prevent overvoltage on the Vcc pin, a Zener diode (Dz1) can be used. Similarly on the  $V_{boot}$  pin, a Zener diode (Dz2) can be placed in parallel with each  $C_{boot}$ .
- The use of the  $C_4$  decoupling capacitor (100 to 220 nF, with low ESR and low ESL) in parallel with the electrolytic capacitor  $C_{vdc}$  is useful to prevent surge destruction. Both the  $C_4$  and  $C_{vdc}$  capacitors should be placed as close as possible to the IPM ( $C_4$  has priority over  $C_{vdc}$ ).
- By integrating an application-specific type HVIC inside the module, it is possible to perform direct coupling to the MCU terminals without an opto-coupler.
- Use low inductance shunt resistors for phase leg current sensing.
- To avoid malfunctions, the wiring between the N pins, the shunt resistor and PWR\_GND should be as short as possible.
- The connection of SGN\_GND to PWR\_GND at only one point (close to the shunt resistor terminal) can help to reduce the impact of power ground fluctuation.

These guidelines ensure the device specifications for application designs. For further details, please refer to the relevant application note.

**Table 14. Recommended operating conditions**

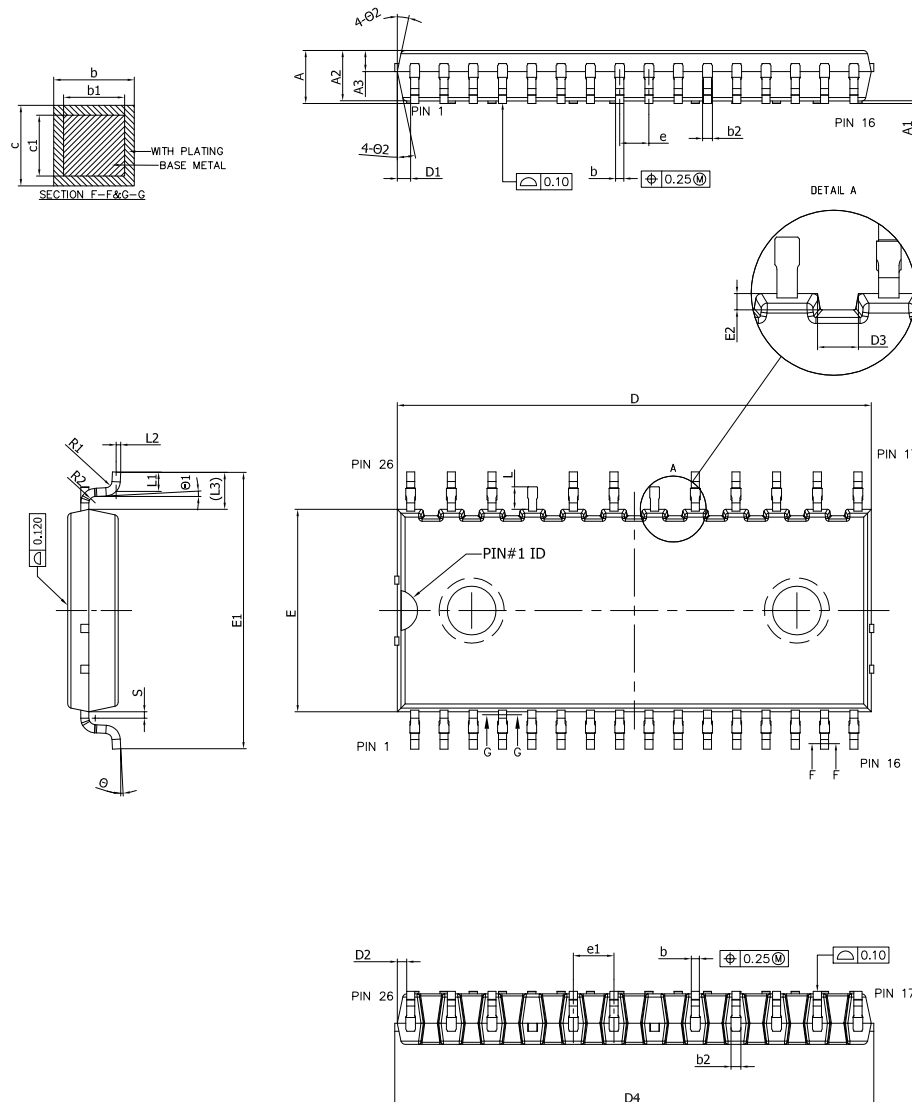
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{PN}$	Supply voltage	Applied among P-Nu, Nv, Nw		300	500	V
$V_{CC}$	Control supply voltage	Applied to $V_{CC}$ -GND	13.5	15	18	V
$V_{BS}$	High-side bias voltage	Applied to $V_{BOOTx}$ -OUT for x = U, V, W	13		18	V
$t_{dead}$	Blanking time to prevent arm-short	For each input signal	1.5			$\mu$ s
$f_{PWM}$	PWM input signal	-40 $^{\circ}$ C < Tc < 100 $^{\circ}$ C -40 $^{\circ}$ C < Tj < 125 $^{\circ}$ C			25	kHz
$T_C$	Case operation temperature				100	$^{\circ}$ C

## 6 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK® is an ST trademark.

### 6.1 NSDIP-26L package information

Figure 12. NSDIP-26L package outline

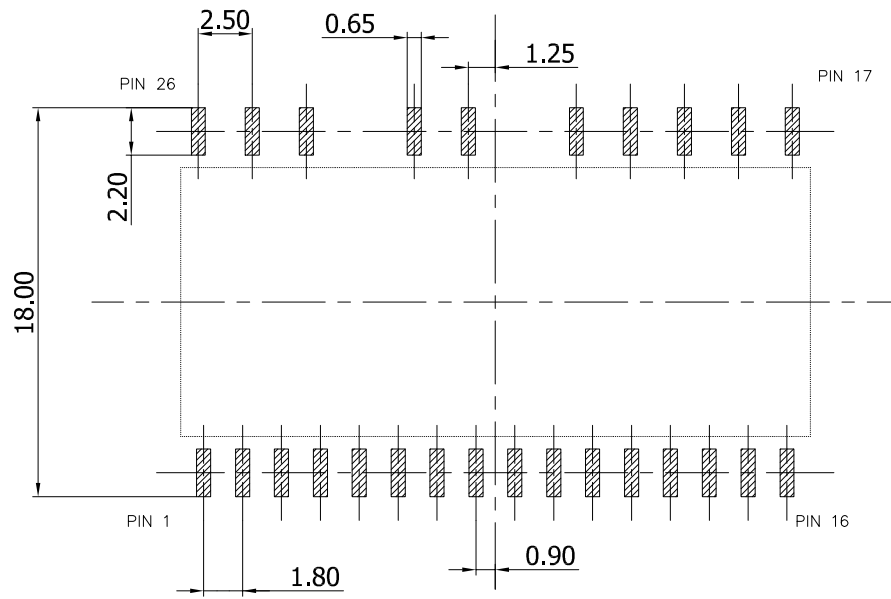


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**Table 15. NSDIP-26L package mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A			3.45
A1	0.10		0.25
A2	3.00	3.10	3.20
A3	1.70	1.80	1.90
b	0.47		0.57
b1	0.45	0.50	0.55
b2	0.63		0.67
c	0.47		0.57
c1	0.45	0.50	0.55
D	29.05	29.15	29.25
D1	0.70		
D2	0.45		
D3	0.90		
D4			29.65
E	12.35	12.45	12.55
E1	16.70	17.00	17.30
E2	0.35		
e	1.70	1.80	1.90
e1	2.40	2.50	2.60
L	1.24	1.39	1.54
L1	1.00	1.15	1.30
L2	0.25 BSC		
L3	2.275 REF		
R1	0.25	0.40	0.55
R2	0.25	0.40	0.55
S		0.39	0.55
θ	0°		8°
θ1	3° BSC		
θ2	10°	12°	14°

Figure 13. NSDIP-26L recommended footprint (dimensions are in mm)



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## Revision history

**Table 16. Document revision history**

Date	Revision	Changes
19-Apr-2017	1	Initial release
09-Jan-2018	2	Datasheet promoted from preliminary data to production data. Modified features on cover page. Modified Figure 2: "Pin layout (top view)", Table 3: "Inverter part", Table 5: "Total system", Table 6: "Thermal data", Table 9: "Low voltage power supply", Table 10: "Bootstrapped voltage", Table 13: "Sense comparator characteristics". Updated Section 6.1: "NSDIP-26L package information". Minor text changes.
03-Apr-2018	3	Removed maturity status indication from cover page. Modified <a href="#">Table 2. Inverter part</a> , <a href="#">Table 3. Control part</a> . Modified <a href="#">Section 4 Shutdown function</a> . Added <a href="#">Table 14. Recommended operating conditions</a> . Minor text changes.

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