

## Features

- Temperature ranges
  - Industrial:  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$
  - Automotive-E:  $-40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$
- Pin and function compatible with CY7C199C
- High speed
  - $t_{AA} = 10\text{ ns}$  (Industrial)
- Low active power
  - $I_{CC} = 80\text{ mA}$  at  $10\text{ ns}$
- Low CMOS standby power
  - $I_{SB2} = 3\text{ mA}$
- 2.0V Data Retention
- Automatic power down when deselected
- CMOS for optimum speed/power
- TTL-compatible inputs and outputs
- Easy memory expansion with  $\overline{CE}$  and  $\overline{OE}$  features
- Available in Pb-free 28-pin 300-Mil wide Molded SOJ, 28-pin 300-Mil wide SOIC and 28-pin TSOP I packages

## Functional Description

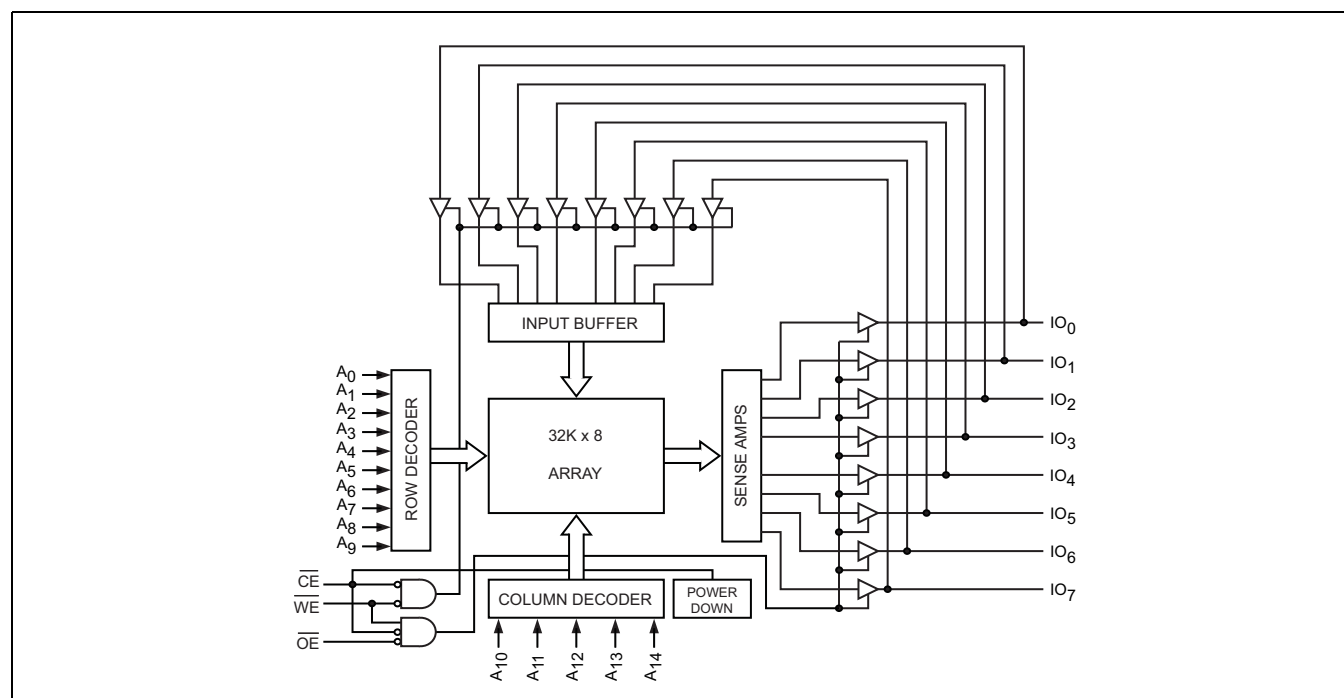
The CY7C199D is a high performance CMOS static RAM organized as 32,768 words by 8 bits. Easy memory expansion is provided by an active LOW Chip Enable ( $\overline{CE}$ ), an active LOW Output Enable ( $\overline{OE}$ ) and tri-state drivers. This device has an automatic power down feature, reducing the power consumption when deselected. The input and output pins ( $IO_0$  through  $IO_7$ ) are placed in a high impedance state when the device is deselected ( $\overline{CE}$  HIGH), the outputs are disabled ( $\overline{OE}$  HIGH), or during a write operation ( $\overline{CE}$  LOW and  $\overline{WE}$  LOW).

Write to the device by taking Chip Enable ( $\overline{CE}$ ) and Write Enable ( $\overline{WE}$ ) inputs LOW. Data on the eight IO pins ( $IO_0$  through  $IO_7$ ) is then written into the location specified on the address pins ( $A_0$  through  $A_{14}$ ).

Read from the device by taking Chip Enable ( $\overline{CE}$ ) and Output Enable ( $\overline{OE}$ ) LOW while forcing Write Enable ( $\overline{WE}$ ) HIGH. Under these conditions, the contents of the memory location specified by the address pins appears on the IO pins.

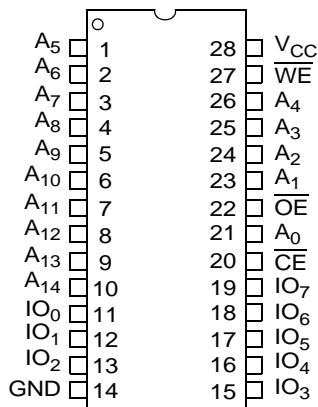
For best practice recommendations, refer to the Cypress application note [AN1064, SRAM System Guidelines](#).

## Logic Block Diagram

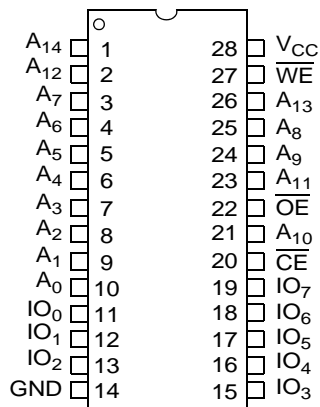


## Pin Configuration

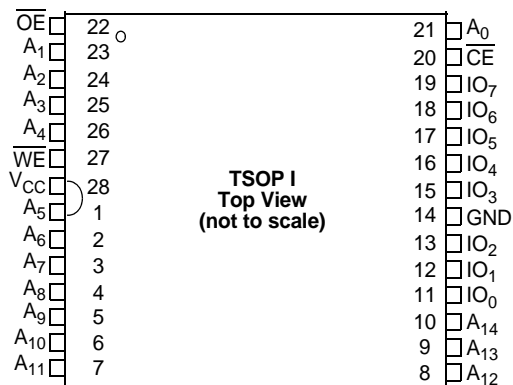
**Figure 1. 28-Pin SOJ  
(Top View)**



**Figure 2. 28-Pin SOIC  
(Top View)**



**Figure 3. 28-Pin TSOP I  
(Top View)**



## Selection Guide

Description	-10 (Industrial)	-25 (Automotive) <sup>[1]</sup>	Unit
Maximum Access Time	10	25	ns
Maximum Operating Current	80	63	mA
Maximum CMOS Standby Current	3	15	mA

**Note:**

1. Automotive product information is preliminary

## Maximum Ratings

Exceeding the maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage Temperature .....  $-65^{\circ}\text{C}$  to  $+150^{\circ}\text{C}$

Ambient Temperature with

Power Applied .....  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$

Supply Voltage on  $V_{CC}$  to Relative GND <sup>[2]</sup> .....  $-0.5\text{V}$  to  $+6.0\text{V}$

DC Voltage Applied to Outputs

in High Z State <sup>[2]</sup> .....  $-0.5\text{V}$  to  $V_{CC} + 0.5\text{V}$

DC Input Voltage <sup>[2]</sup> .....  $-0.5\text{V}$  to  $V_{CC} + 0.5\text{V}$

Output Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage .....  $> 2,001\text{V}$   
(per MIL-STD-883, Method 3015)

Latch-up Current .....  $> 200\text{ mA}$

## Operating Range

Range	Ambient Temperature	$V_{CC}$	Speed
Industrial	$-40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$	$5\text{V} \pm 0.5\text{V}$	10 ns
Automotive-E	$-40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$	$5\text{V} \pm 0.5\text{V}$	25 ns

## Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions	7C199D-10		7C199D-25		Unit
			Min	Max	Min	Max	
$V_{OH}$	Output HIGH Voltage	$I_{OH} = -4.0\text{ mA}$	2.4		2.4		V
$V_{OL}$	Output LOW Voltage	$I_{OL} = 8.0\text{ mA}$		0.4		0.4	V
$V_{IH}$	Input HIGH Voltage <sup>[2]</sup>		2.2	$V_{CC} + 0.5$	2.2	$V_{CC} + 0.5$	V
$V_{IL}$	Input LOW Voltage <sup>[2]</sup>		$-0.5$	0.8	$-0.5$	0.8	V
$I_{IX}$	Input Leakage Current	$\text{GND} \leq V_I \leq V_{CC}$	$-1$	$+1$	$-5$	$+5$	$\mu\text{A}$
$I_{OZ}$	Output Leakage Current	$\text{GND} \leq V_O \leq V_{CC}$ , Output Disabled	$-1$	$+1$	$-5$	$+5$	$\mu\text{A}$
$I_{CC}$	$V_{CC}$ Operating Supply Current	$V_{CC} = \text{Max}$ , $I_{OUT} = 0\text{ mA}$ , $f = f_{\text{max}} = 1/t_{RC}$	100 MHz	80		—	mA
			83 MHz	72		—	mA
			66 MHz	58		—	mA
			40 MHz	37		63	mA
$I_{SB1}$	Automatic CE Power down Current—TTL Inputs	Max $V_{CC}$ , $\overline{CE} \geq V_{IH}$ , $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$ , $f = f_{\text{max}}$		10		50	mA
$I_{SB2}$	Automatic CE Power down Current—CMOS Inputs	Max $V_{CC}$ , $\overline{CE} \geq V_{CC} - 0.3\text{V}$ , $V_{IN} \geq V_{CC} - 0.3\text{V}$ or $V_{IN} \leq 0.3\text{V}$ , $f = 0$		3		15	mA

**Note:**

2.  $V_{IL}(\text{min}) = -2.0\text{V}$  and  $V_{IH}(\text{max}) = V_{CC} + 1\text{V}$  for pulse durations of less than 5 ns.

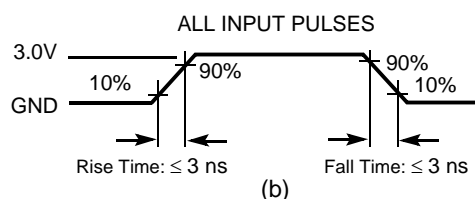
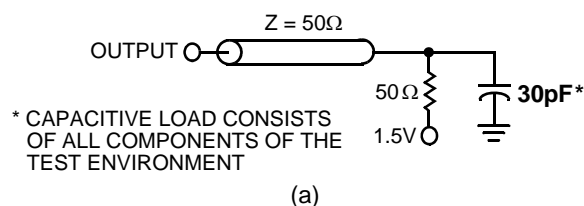
## Capacitance <sup>[3]</sup>

Parameter	Description	Test Conditions	Max	Unit
$C_{IN}$	Input Capacitance	$T_A = 25^\circ\text{C}$ , $f = 1\text{ MHz}$ , $V_{CC} = 5.0\text{V}$	8	pF
$C_{OUT}$	Output Capacitance		8	pF

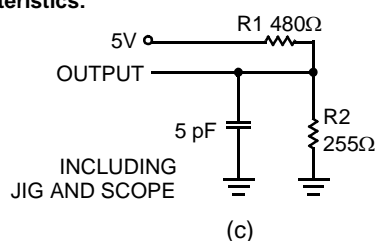
## Thermal Resistance <sup>[3]</sup>

Parameter	Description	Test Conditions	SOJ	TSOP I	SOIC	Unit
$\Theta_{JA}$	Thermal Resistance (Junction to Ambient)	Still Air, soldered on a 3 x 4.5 inch, four-layer printed circuit board	59.16	54.65	TBD	$^\circ\text{C/W}$
$\Theta_{JC}$	Thermal Resistance (Junction to Case)		40.84	21.49	TBD	$^\circ\text{C/W}$

## AC Test Loads and Waveforms <sup>[4]</sup>



### High Z characteristics:



### Notes:

- Tested initially and after any design or process changes that may affect these parameters.
- AC characteristics (except High Z) are tested using the load conditions shown in Figure (a). High Z characteristics are tested for all speeds using the test load shown in Figure (c).

**Switching Characteristics** (Over the Operating Range) <sup>[5]</sup>

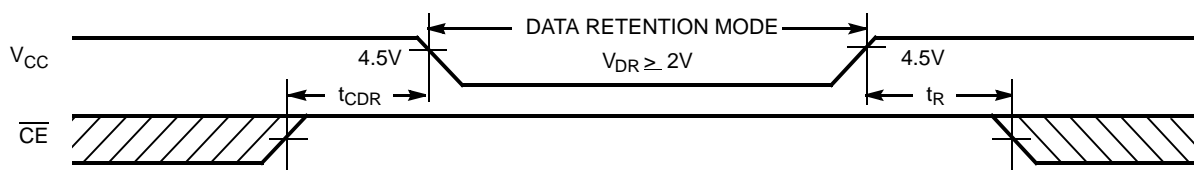
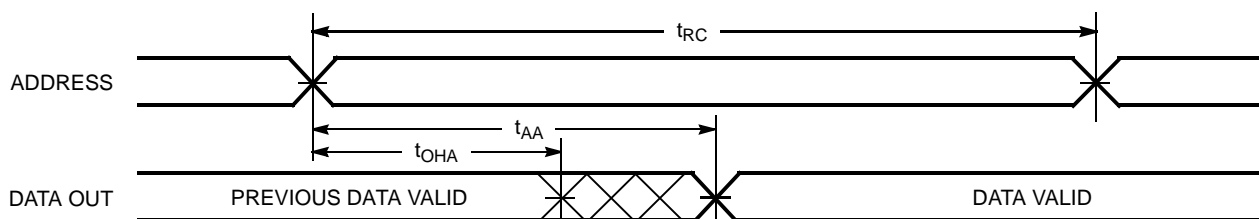
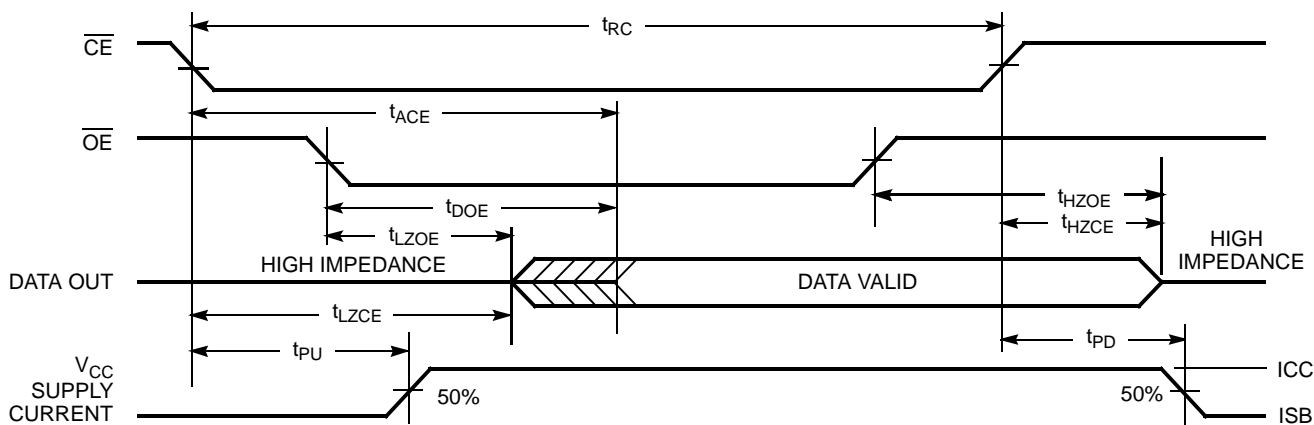
Parameter	Description	7C199D-10		7C199D-25		Unit
		Min	Max	Min	Max	
Read Cycle						
t <sub>power</sub> <sup>[6]</sup>	V <sub>CC</sub> (typical) to the first access	100		100		μs
t <sub>RC</sub>	Read Cycle Time	10		25		ns
t <sub>AA</sub>	Address to Data Valid		10		25	ns
t <sub>OHA</sub>	Data Hold from Address Change	3		3		ns
t <sub>ACE</sub>	$\overline{\text{CE}}$ LOW to Data Valid		10		25	ns
t <sub>DOE</sub>	$\overline{\text{OE}}$ LOW to Data Valid		5		10	ns
t <sub>LZOE</sub> <sup>[7]</sup>	$\overline{\text{OE}}$ LOW to Low Z	0		0		ns
t <sub>HZOE</sub> <sup>[7, 8]</sup>	$\overline{\text{OE}}$ HIGH to High Z		5		11	ns
t <sub>LZCE</sub> <sup>[7]</sup>	$\overline{\text{CE}}$ LOW to Low Z	3		3		ns
t <sub>HZCE</sub> <sup>[7, 8]</sup>	$\overline{\text{CE}}$ HIGH to High Z		5		11	ns
t <sub>PU</sub> <sup>[9]</sup>	$\overline{\text{CE}}$ LOW to Power up	0		0		ns
t <sub>PD</sub> <sup>[9]</sup>	$\overline{\text{CE}}$ HIGH to Power down		10		25	ns
Write Cycle <sup>[10, 11]</sup>						
t <sub>WC</sub>	Write Cycle Time	10		25		ns
t <sub>SCE</sub>	$\overline{\text{CE}}$ LOW to Write End	7		18		ns
t <sub>AW</sub>	Address Setup to Write End	7		18		ns
t <sub>HA</sub>	Address Hold from Write End	0		0		ns
t <sub>SA</sub>	Address Setup to Write Start	0		0		ns
t <sub>PWE</sub>	$\overline{\text{WE}}$ Pulse Width	7		18		ns
t <sub>SD</sub>	Data Setup to Write End	6		12		ns
t <sub>HD</sub>	Data Hold from Write End	0		0		ns
t <sub>HZWE</sub> <sup>[7]</sup>	$\overline{\text{WE}}$ LOW to High Z		5		11	ns
t <sub>LZWE</sub> <sup>[7, 8]</sup>	$\overline{\text{WE}}$ HIGH to Low Z	3		3		ns

**Notes:**

- Test conditions assume signal transition time of 3 ns or less for all speeds, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified  $I_{\text{OL}}/I_{\text{OH}}$  and 30-pF load capacitance.
- $t_{\text{POWER}}$  gives the minimum amount of time that the power supply should be at typical  $V_{\text{CC}}$  values until the first memory access can be performed.
- At any given temperature and voltage condition,  $t_{\text{HZCE}}$  is less than  $t_{\text{LZCE}}$ ,  $t_{\text{HZOE}}$  is less than  $t_{\text{LZOE}}$ , and  $t_{\text{HZWE}}$  is less than  $t_{\text{LZWE}}$  for any given device.
- $t_{\text{HZOE}}$ ,  $t_{\text{HZCE}}$ , and  $t_{\text{HZWE}}$  are specified with  $C_{\text{L}} = 5 \text{ pF}$  as in part (b) of "AC Test Loads and Waveforms" <sup>[4]</sup> on page 4. Transition is measured  $\pm 200 \text{ mV}$  from steady-state voltage.
- This parameter is guaranteed by design and is not tested.
- The internal write time of the memory is defined by the overlap of  $\overline{\text{CE}}$  LOW and  $\overline{\text{WE}}$  LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.
- The minimum write cycle time for Write Cycle No. 3 ( $\overline{\text{WE}}$  controlled,  $\overline{\text{OE}}$  LOW) is the sum of  $t_{\text{HZWE}}$  and  $t_{\text{SD}}$ .

**Data Retention Characteristics** (Over the Operating Range)

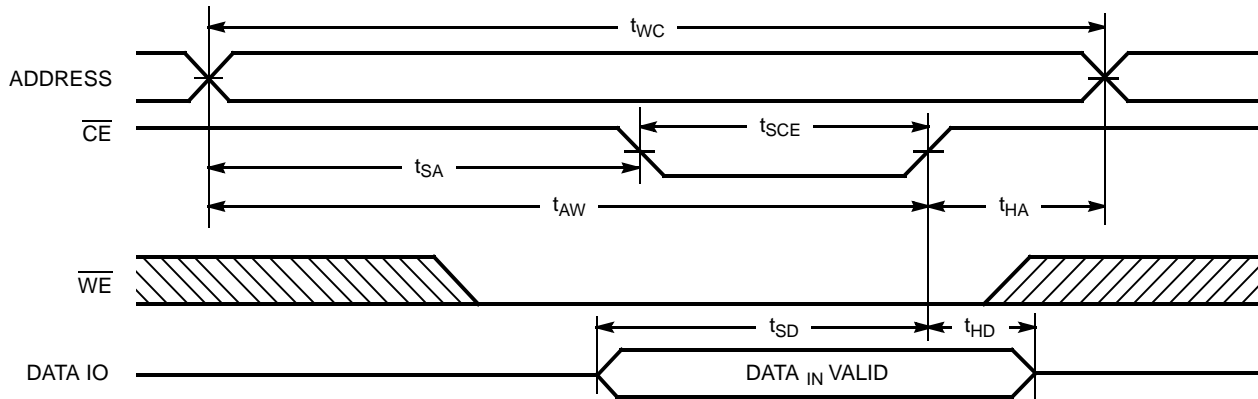
Parameter	Description	Conditions	Min	Max	Unit
$V_{DR}$	$V_{CC}$ for Data Retention		2.0		V
$I_{CCDR}$	Data Retention Current	$V_{CC} = V_{DR} = 2.0V$ , $\overline{CE} \geq V_{CC} - 0.3V$ , $V_{IN} \geq V_{CC} - 0.3V$ or $V_{IN} \leq 0.3V$	Industrial	3	mA
			Automotive-E	15	mA
$t_{CDR}^{[3]}$	Chip Deselect to Data Retention Time		0		ns
$t_R^{[12]}$	Operation Recovery Time		$t_{RC}$		ns

**Data Retention Waveform**

**Switching Waveforms**
**Read Cycle No. 1 (Address Transition Controlled)** [13, 14]

**Read Cycle No. 2 ( $\overline{OE}$  Controlled)** [14, 15]

**Notes:**

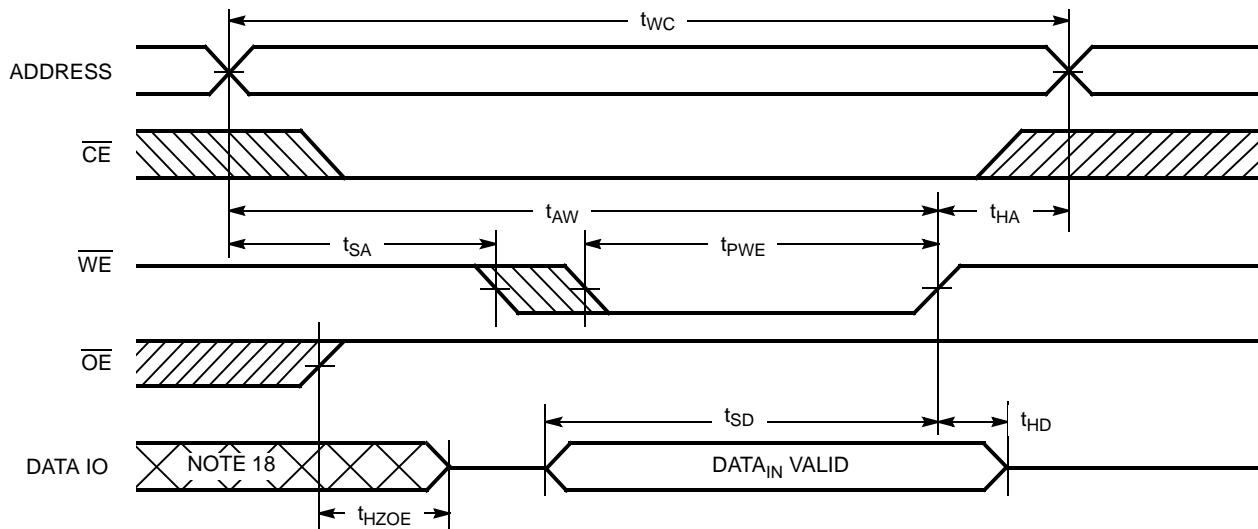
12. Full device operation requires linear  $V_{CC}$  ramp from  $V_{DR}$  to  $V_{CC(min)} \geq 50 \mu s$  or stable at  $V_{CC(min)} \geq 50 \mu s$ .
13. Device is continuously selected.  $\overline{OE}, \overline{CE} = V_{IL}$ .
14.  $\overline{WE}$  is HIGH for read cycle.
15. Address valid prior to or coincident with  $\overline{CE}$  transition LOW.

## Switching Waveforms (continued)

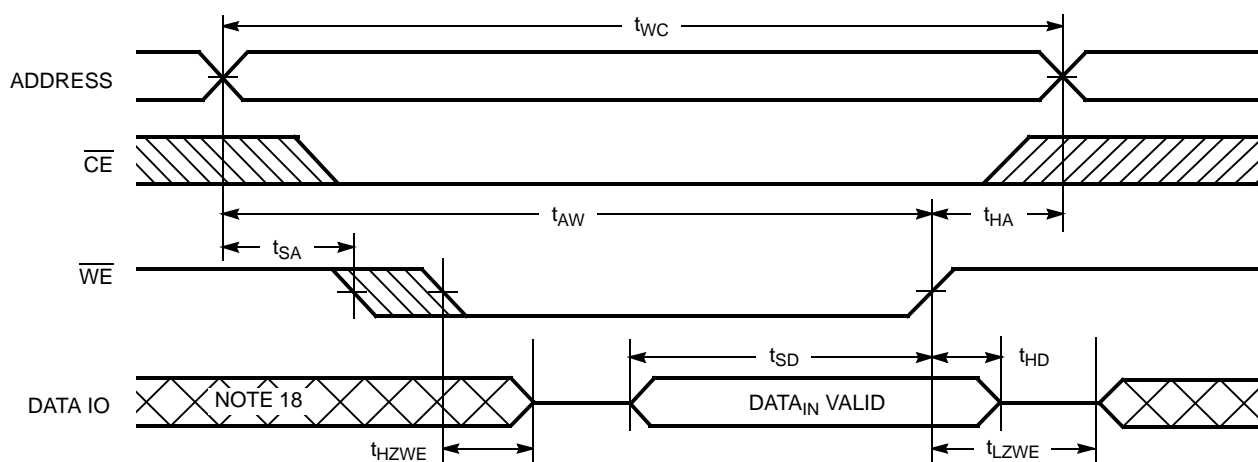
### Write Cycle No. 1 ( $\overline{\text{CE}}$ Controlled) [10, 16, 17]



### Write Cycle No. 2 ( $\overline{\text{WE}}$ Controlled) [10, 16, 17]



### Write Cycle No. 3 ( $\overline{\text{WE}}$ Controlled, $\overline{\text{OE}}$ LOW) [11, 17]



#### Notes:

16. Data IO is high impedance if  $\overline{\text{OE}} = V_{IH}$ .
17. If  $\overline{\text{CE}}$  goes HIGH simultaneously with  $\overline{\text{WE}}$  HIGH, the output remains in a high-impedance state.
18. During this period the IOs are in the output state and input signals should not be applied.

### Truth Table

$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	Inputs/Outputs	Mode	Power
H	X	X	High Z	Deselect/Power down	Standby ( $I_{SB}$ )
L	H	L	Data Out	Read	Active ( $I_{CC}$ )
L	L	X	Data In	Write	Active ( $I_{CC}$ )
L	H	H	High Z	Deselect, Output disabled	Active ( $I_{CC}$ )

### Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
10	CY7C199D-10VXI	51-85031	28-pin (300-Mil) Molded SOJ (Pb-Free)	Industrial
	CY7C199D-10ZXI	51-85071	28-pin TSOP Type I (Pb-free)	
25	CY7C199D-25SXE	51-85026	28-pin (300-Mil) SOIC (Pb-Free)	Automotive-E

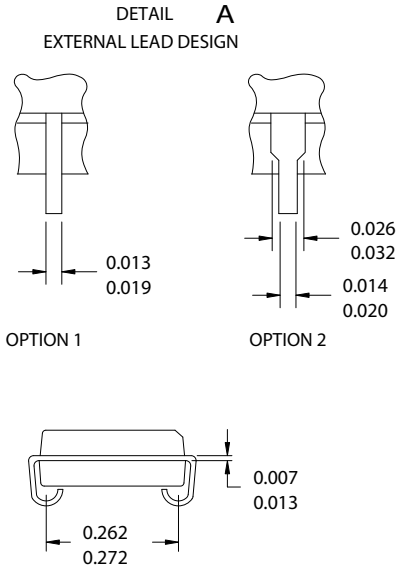
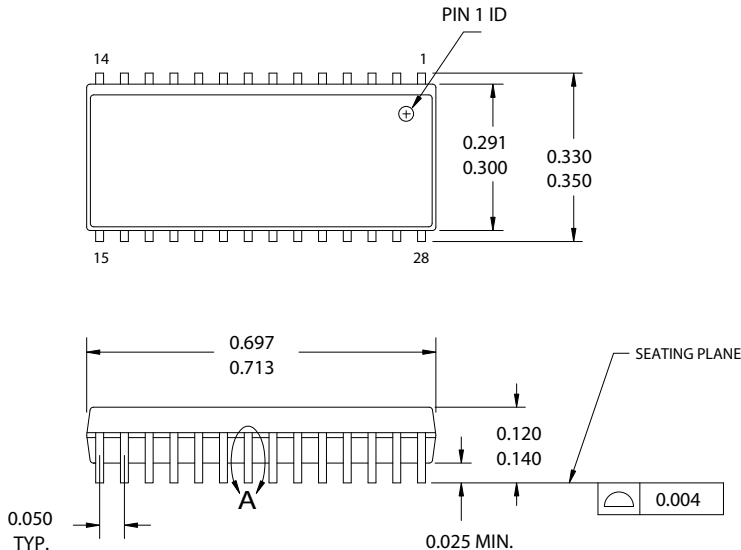
Please contact your local Cypress sales representative for availability of these parts.

### Package Diagrams

Figure 4. 28-Pin (300-Mil) Molded SOJ

NOTE :

1. JEDEC STD REF MO088
2. BODY LENGTH DIMENSION DOES NOT INCLUDE MOLD PROTRUSION/END FLASH  
MOLD PROTRUSION/END FLASH SHALL NOT EXCEED 0.006 in (0.152 mm) PER SIDE
3. DIMENSIONS IN INCHES  
MIN.  
MAX.

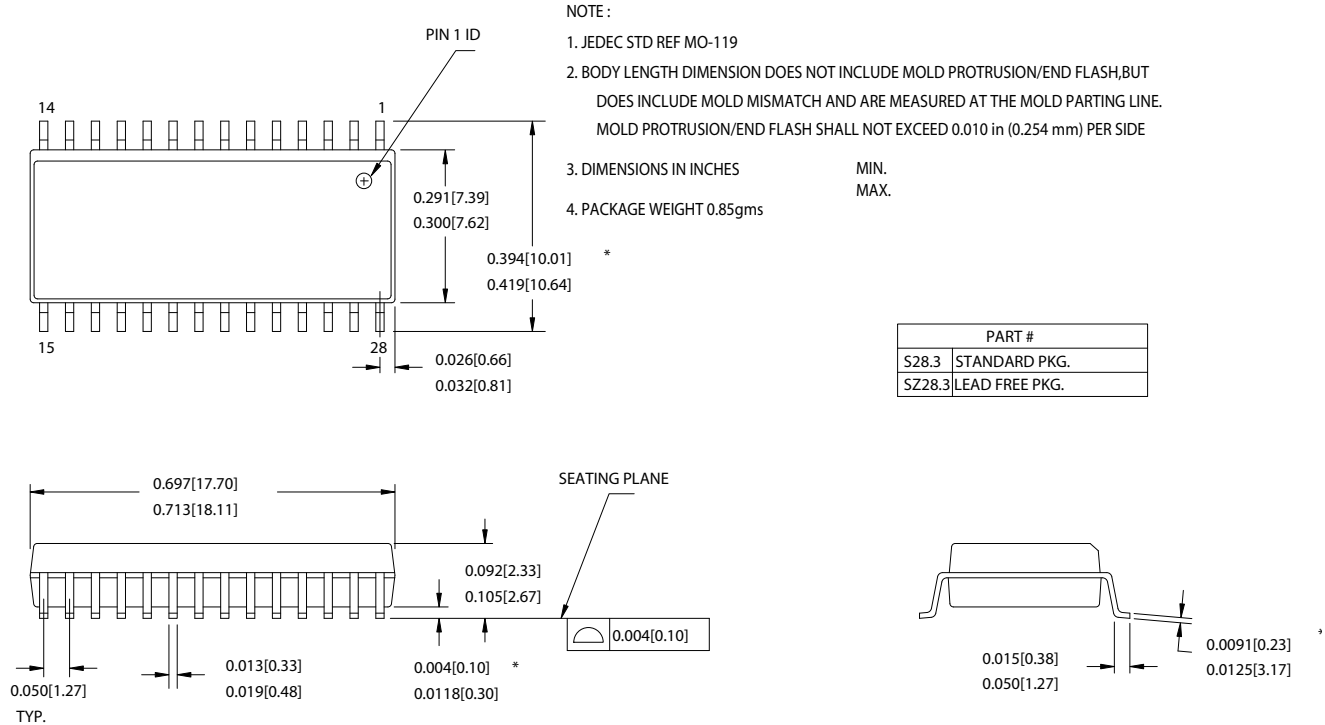


51-85031-°C



**Package Diagrams** (continued)

**Figure 5. 28-Pin (300-Mil) SOIC**

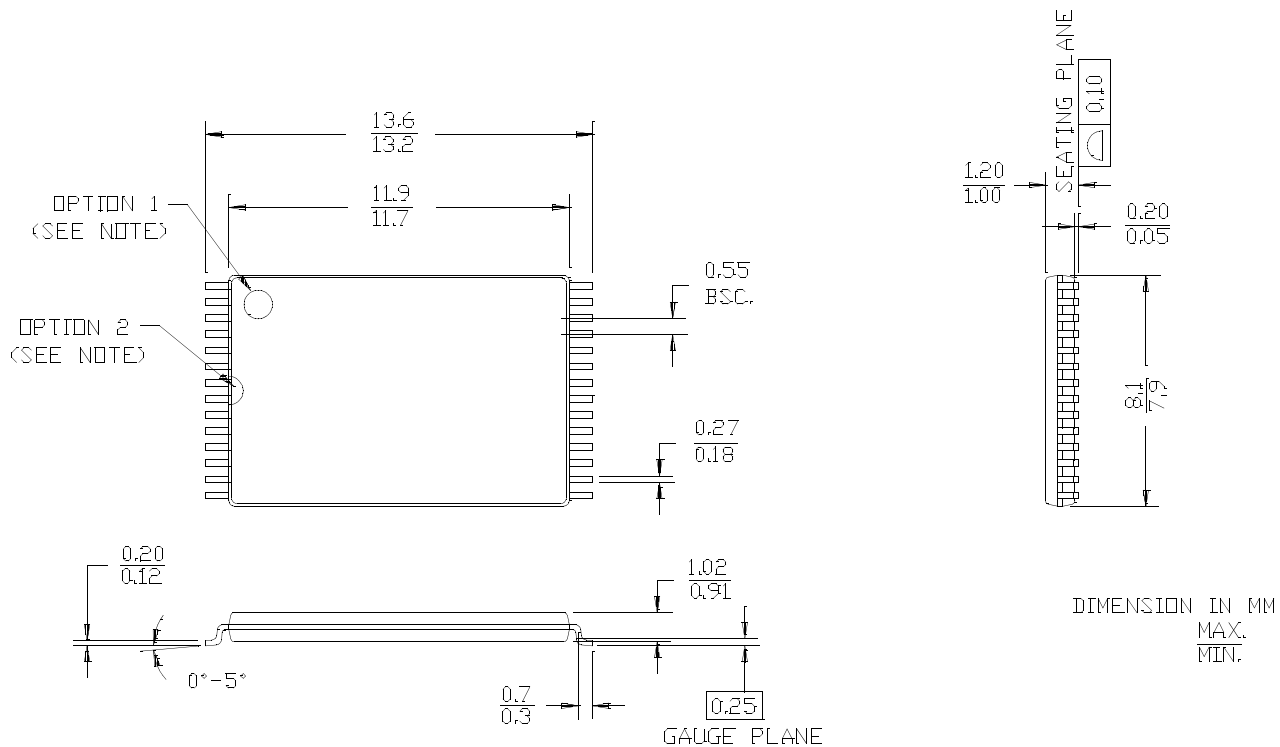


51-85026-\*D

## Package Diagrams (continued)

**Figure 6. 28-Pin Thin Small Outline Package Type 1 (8x13.4 mm)**

NOTE: ORIENTATION I.D MAY BE LOCATED EITHER AS SHOWN IN OPTION 1 OR OPTION 2



51-85071-°G

## Document History Page

Document Title: CY7C199D 256K (32K x 8) Static RAM Document Number: 38-05471				
Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	201560	SWI	See ECN	Advance Information datasheet for C9 IPP
*A	233728	RKF	See ECN	DC parameters modified as per EROS (Spec # 01-02165) Pb-free Offering in Ordering Information
*B	262950	RKF	See ECN	Removed 28-LCC Pinout and Package Diagrams Added Data Retention Characteristics table Added T <sub>power</sub> Spec in Switching Characteristics table Shaded Ordering Information
*C	307594	RKF	See ECN	Reduced Speed bins to -10, -12 and -15 ns
*D	820660	VKN	See ECN	Converted from Preliminary to Final Removed 12 ns and 15 ns speed bin Removed Commercial Operating range Removed "L" part Removed 28-pin PDIP and 28-pin SOIC package Changed Overshoot spec from V <sub>CC</sub> +2V to V <sub>CC</sub> +1V in footnote #2 Changed I <sub>CC</sub> spec from 60 mA to 80 mA for 100 MHz speed bin Added I <sub>CC</sub> specs for 83 MHz, 66 MHz and 40 MHz speed bins Updated Thermal Resistance table Updated Ordering Information Table
*E	2745093	VKN	See ECN	Included 28-Pin SOIC package Changed V <sub>IH</sub> level from 2.0V to 2.2V For Industrial grade, changed t <sub>SD</sub> from 5 ns to 6 ns, and t <sub>HZWE</sub> from 6 ns to 5 ns Included Automotive-E information

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