

N-Channel 20-V (D-S) MOSFET

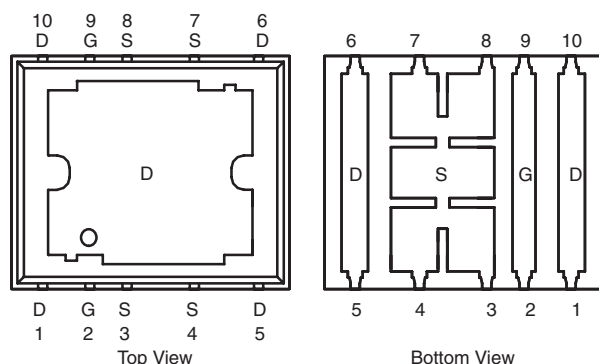
PRODUCT SUMMARY

V _{DS} (V)	R _{DS(on)} (Ω) ^e	I _D (A) ^a		Q _g (Typ.)
		Silicon Limit	Package Limit	
20	0.0016 at V _{GS} = 10 V	220	60	46 nC
	0.0025 at V _{GS} = 4.5 V	117	60	

Package Drawing

www.vishay.com/doc?72945

PolarPAK



Top surface is connected to pins 1, 5, 6, and 10

Ordering Information: SiE808DF-T1-E3 (Lead (Pb)-free)
SiE808DF-T1-GE3 (Lead (Pb)-free and Halogen-free)

FEATURES

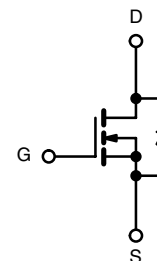
- Halogen-free According to IEC 61249-2-21 Definition
- TrenchFET[®] Gen II Power MOSFET
- Ultra Low Thermal Resistance Using Top-Exposed PolarPAK[®] Package for Double-Sided Cooling
- Leadframe-Based New Encapsulated Package
 - Die Not Exposed
 - Same Layout Regardless of Die Size
- Low Q_{gd}/Q_{gs} Ratio Helps Prevent Shoot-Through
- 100 % R_g and UIS Tested
- Compliant to RoHS directive 2002/95/EC



RoHS
COMPLIANT
HALOGEN
FREE
Available

APPLICATIONS

- VRM
- DC/DC Conversion: Low-Side
- Synchronous Rectification



N-Channel MOSFET

For Related Documents
www.vishay.com/ppg?73739

ABSOLUTE MAXIMUM RATINGS T_A = 25 °C, unless otherwise noted

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V _{DS}	20	V
Gate-Source Voltage	V _{GS}	± 20	
Continuous Drain Current (T _J = 150 °C)	I _D	220 (Silicon Limit)	A
		60 ^a (Package Limit)	
		60 ^a	
		45 ^{b, c}	
Pulsed Drain Current	I _{DM}	100	
Continuous Source-Drain Diode Current	I _S	60 ^a	A
		4.3 ^{b, c}	
Single Pulse Avalanche Current	I _{AS}	35	
Avalanche Energy	E _{AS}	61	mJ
Maximum Power Dissipation	P _D	125	W
		80	
		5.2 ^{b, c}	
		3.3 ^{b, c}	
Operating Junction and Storage Temperature Range	T _J , T _{stg}	- 55 to 150	°C
Soldering Recommendations (Peak Temperature) ^{d, e}		260	

Notes:

a. Package limited is 60 A.

b. Surface Mounted on 1" x 1" FR4 board.

c. t = 10 s.

d. See Solder Profile (www.vishay.com/doc?73257). The PolarPAK is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.

e. Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.

THERMAL RESISTANCE RATINGS

Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^{a, b}	$t \leq 10$ s	R_{thJA}	20	24	°C/W
Maximum Junction-to-Case (Drain Top)	Steady State	R_{thJC} (Drain)	0.8	1	
Maximum Junction-to-Case (Source) ^{a, c}		R_{thJC} (Source)	2.2	2.7	

Notes:

a. Surface Mounted on 1" x 1" FR4 board.

b. Maximum under Steady State conditions is 68 °C/W.

c. Measured at source pin (on the side of the package).

SPECIFICATIONS $T_J = 25$ °C, unless otherwise noted

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0 V, I _D = 250 μA	20			V
V _{DS} Temperature Coefficient	ΔV _{DS} /T _J	I _D = 250 μA		26.5		mV/°C
V _{GS(th)} Temperature Coefficient	ΔV _{GS(th)} /T _J			- 7.3		
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	1.5	2.3	3	V
Gate-Source Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 20 V			± 100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 20 V, V _{GS} = 0 V			1	μA
		V _{DS} ≥ 20 V, V _{GS} = 0 V, T _J = 55 °C			10	
On-State Drain Current ^a	I _{D(on)}	V _{DS} ≥ 5 V, V _{GS} = 10 V	25			A
Drain-Source On-State Resistance ^a	R _{DS(on)}	V _{GS} = 10 V, I _D = 25 A		0.0013	0.0016	Ω
		V _{GS} = 4.5 V, I _D = 25 A		0.0021	0.0025	
Forward Transconductance ^a	g _{fs}	V _{DS} = 10 V, I _D = 25 A		95		S
Dynamic ^b						
Input Capacitance	C _{iss}	V _{DS} = 10 V, V _{GS} = 0 V, f = 1 MHz		8800		pF
Output Capacitance	C _{oss}			1600		
Reverse Transfer Capacitance	C _{rss}			600		
Total Gate Charge	Q _g	V _{DS} = 10 V, V _{GS} = 10 V, I _D = 25 A		102	155	nC
		V _{DS} = 10 V, V _{GS} = 4.5 V, I _D = 20 A		46	70	
Gate-Source Charge	Q _{gs}			26		
Gate-Drain Charge	Q _{gd}			8		
Gate Resistance	R _g	f = 1 MHz		0.9	1.35	Ω
Turn-On Delay Time	t _{d(on)}	V _{DD} = 10 V, R _L = 1 Ω I _D ≅ 10 A, V _{GEN} = 4.5 V, R _g = 1 Ω		180	270	ns
Rise Time	t _r			215	325	
Turn-Off Delay Time	t _{d(off)}			50	75	
Fall Time	t _f			15	25	
Turn-On Delay Time	t _{d(on)}	V _{DD} = 10 V, R _L = 1 Ω I _D ≅ 10 A, V _{GEN} = 10 V, R _g = 1 Ω		25	40	
Rise Time	t _r			55	85	
Turn-Off Delay Time	t _{d(off)}			55	85	
Fall Time	t _f			10	15	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I _S	T _C = 25 °C			60	A
Pulse Diode Forward Current ^a	I _{SM}				100	
Body Diode Voltage	V _{SD}	I _S = 10 A		0.8	1.2	V
Body Diode Reverse Recovery Time	t _{rr}	I _F = 10 A, di/dt = 100 A/μs, T _J = 25 °C		56	85	ns
Body Diode Reverse Recovery Charge	Q _{rr}			60	90	nC
Reverse Recovery Fall Time	t _a			26		ns
Reverse Recovery Rise Time	t _b			30		

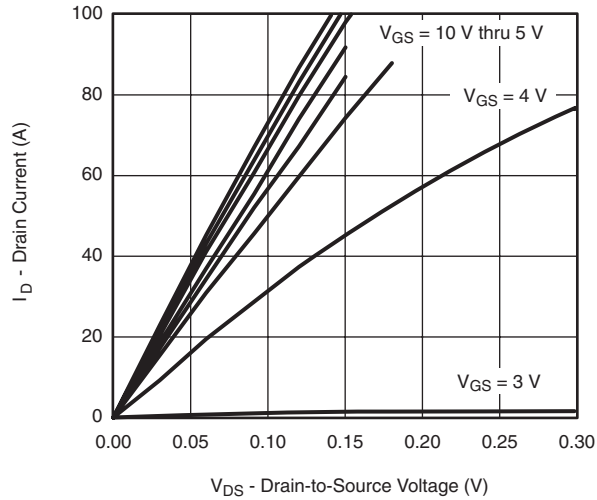
Notes:

a. Pulse test; pulse width ≤ 300 μ s, duty cycle ≤ 2 %.

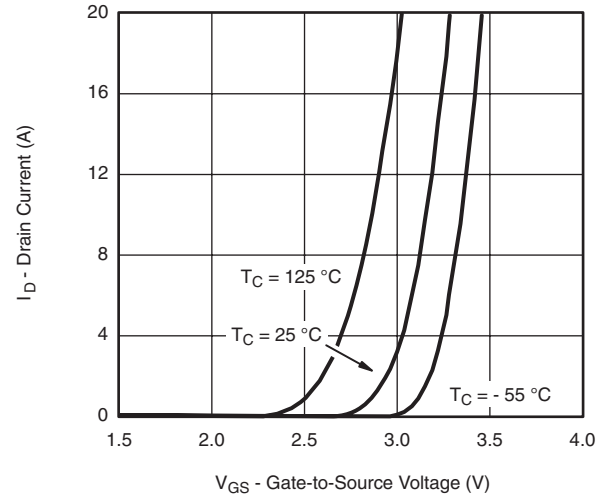
b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

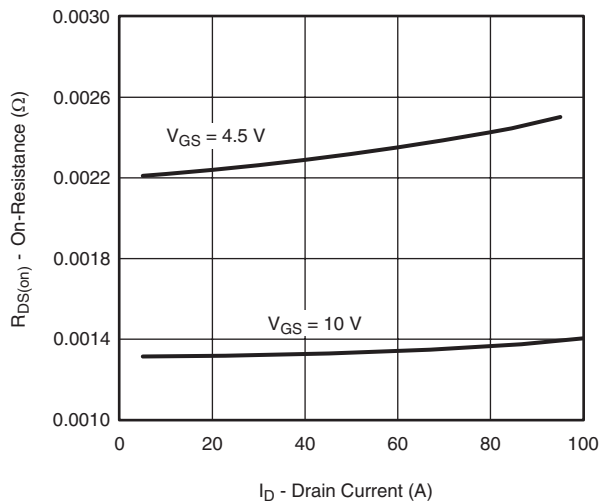
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



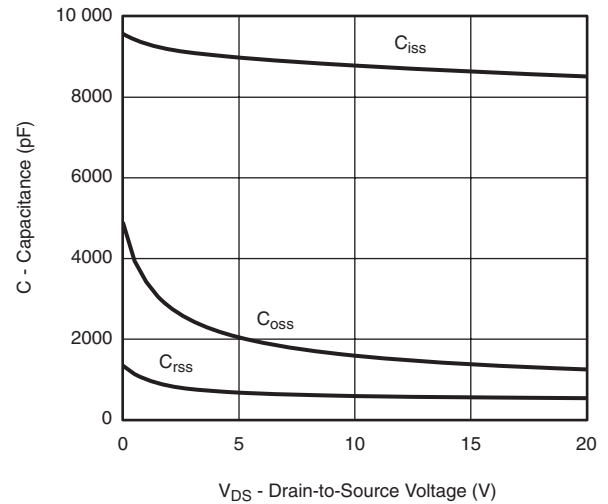
Output Characteristics



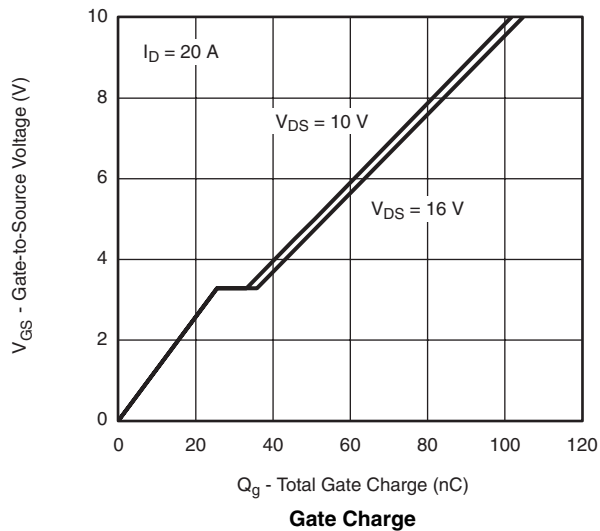
Transfer Characteristics



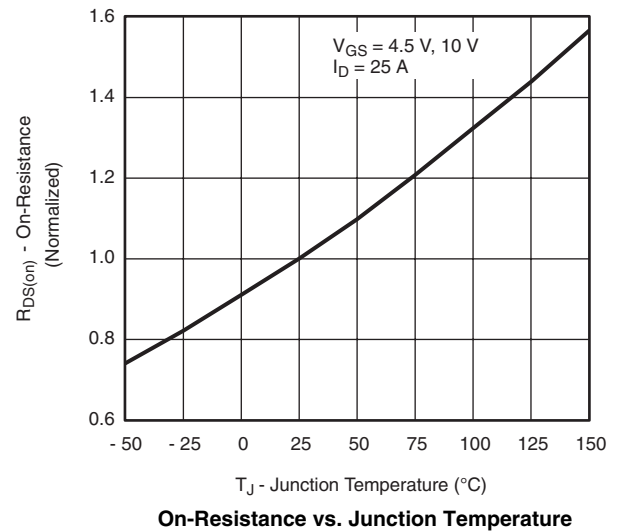
On-Resistance vs. Drain Current and Gate Voltage



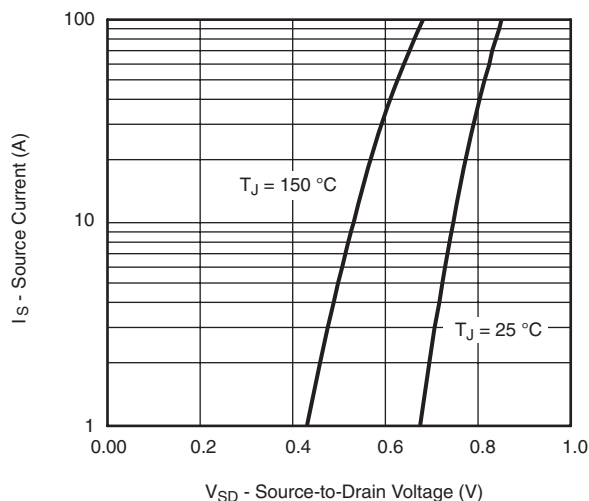
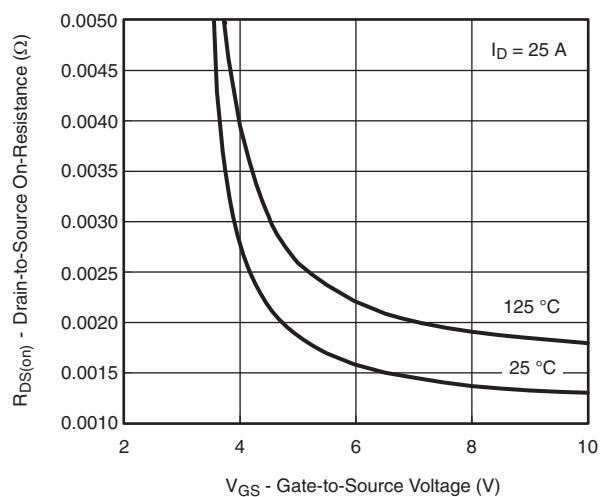
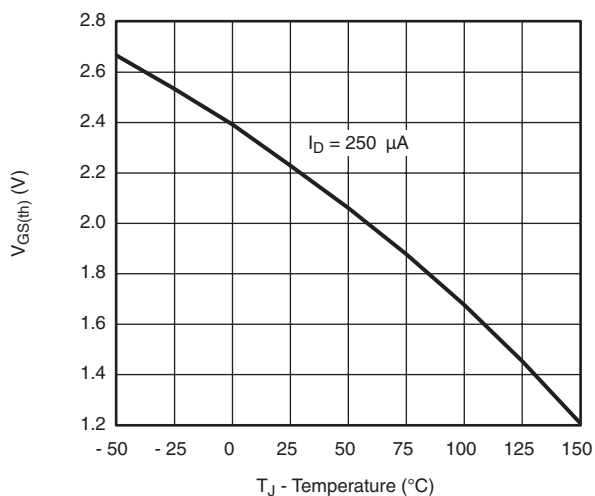
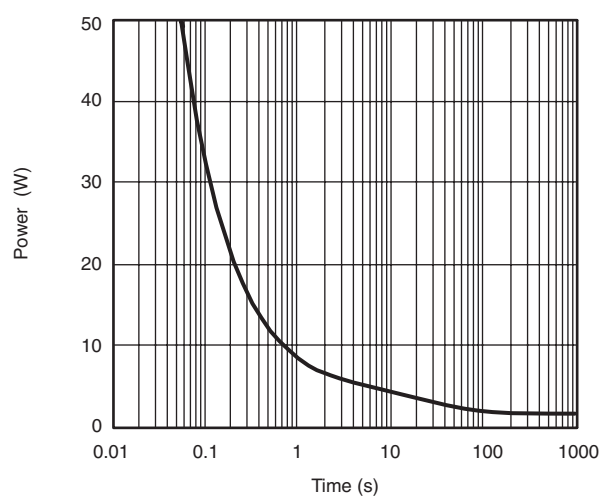
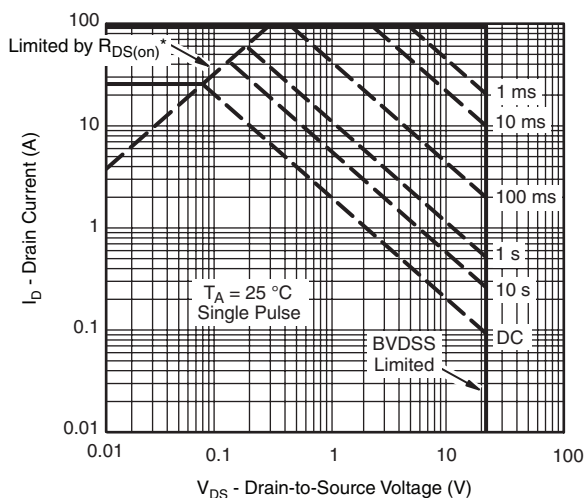
Capacitance



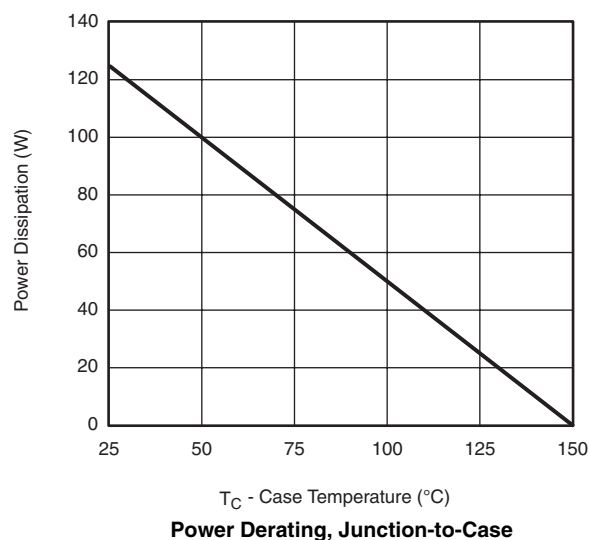
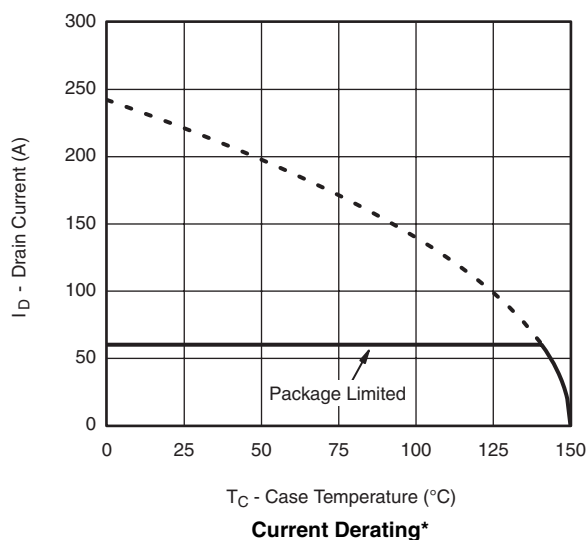
Gate Charge



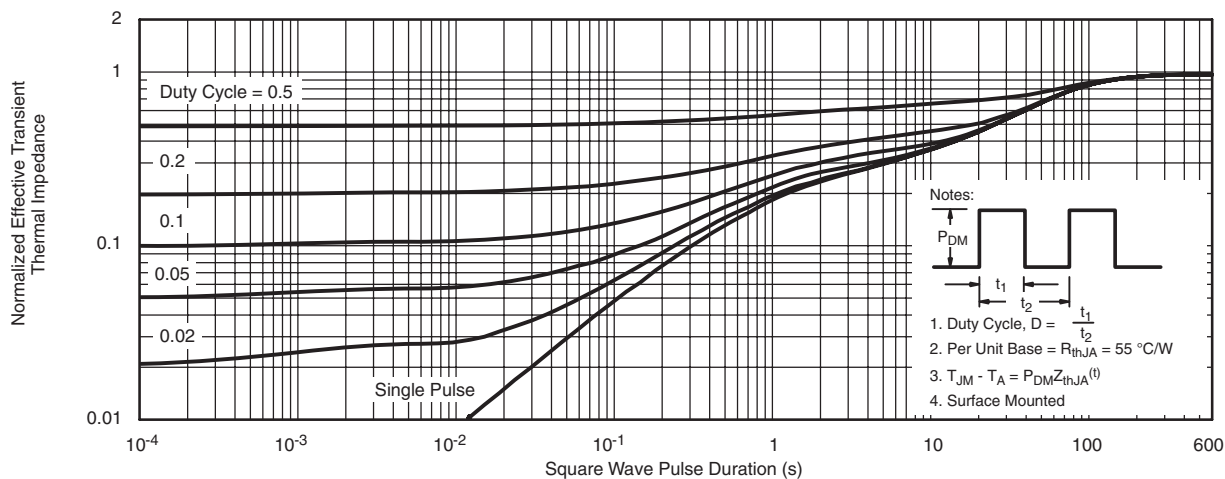
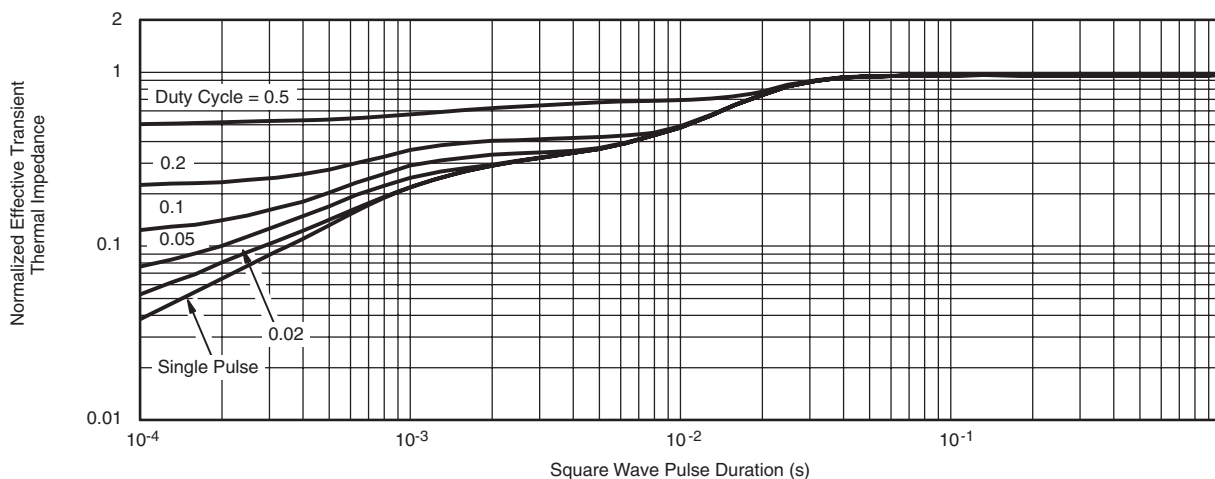
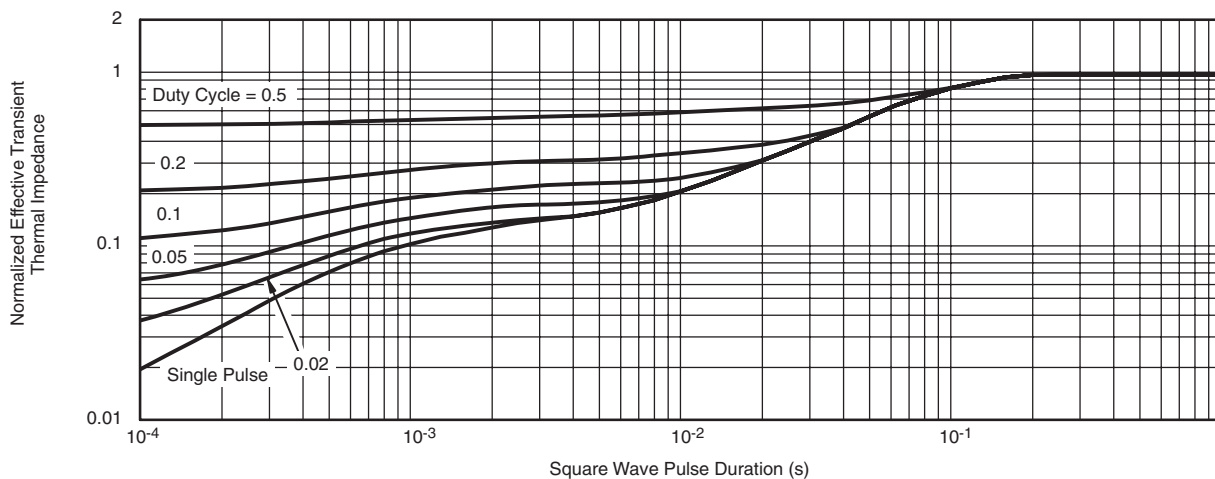
On-Resistance vs. Junction Temperature

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted**Source-Drain Diode Forward Voltage****On-Resistance vs. Gate-to-Source Voltage****Threshold Voltage****Single Pulse Power, Junction-to-Ambient*** $V_{DS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified**Safe Operating Area, Junction-to-Ambient**

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

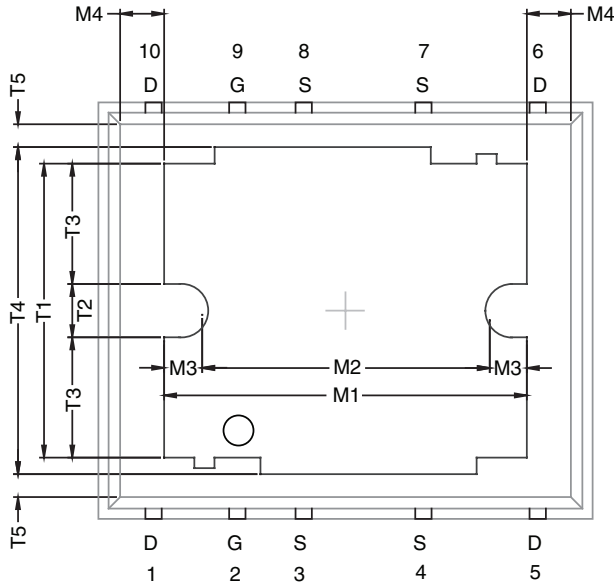


* The power dissipation P_D is based on $T_{J(max)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

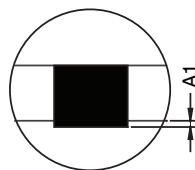
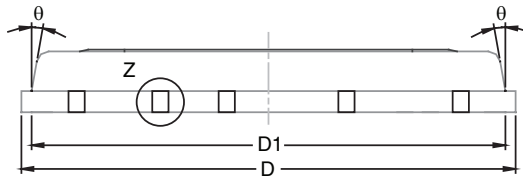
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted**Normalized Thermal Transient Impedance, Junction-to-Ambient****Normalized Thermal Transient Impedance, Junction-to-Case (Drain Top)****Normalized Thermal Transient Impedance, Junction-to-Source**

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?73739.

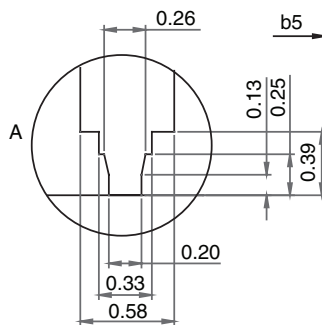
POLARPAK™ OPTION L



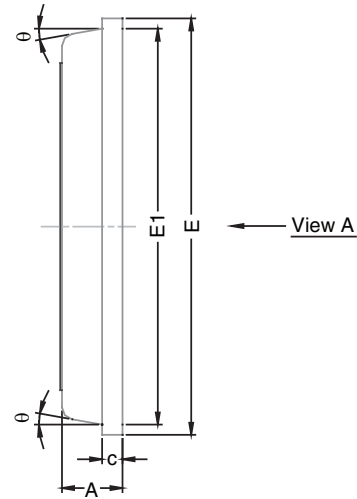
(Top View)



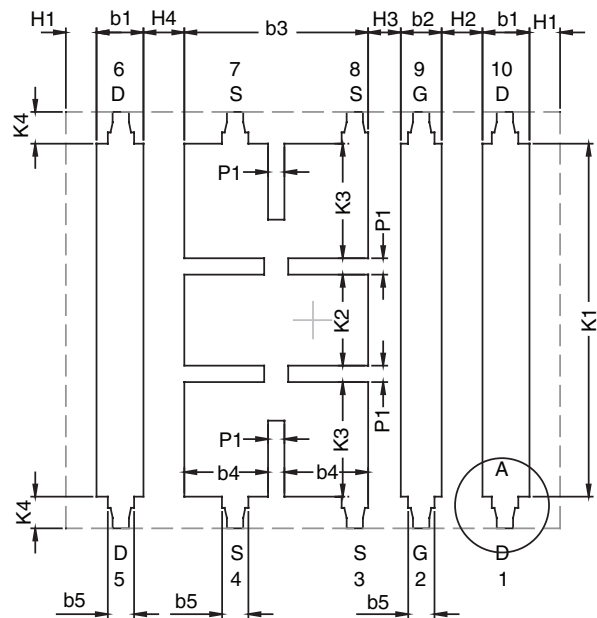
DETAIL Z



Product datasheet/information page contain links to applicable package drawing.



View A



View A
(Bottom View)

Package Information

Vishay Siliconix

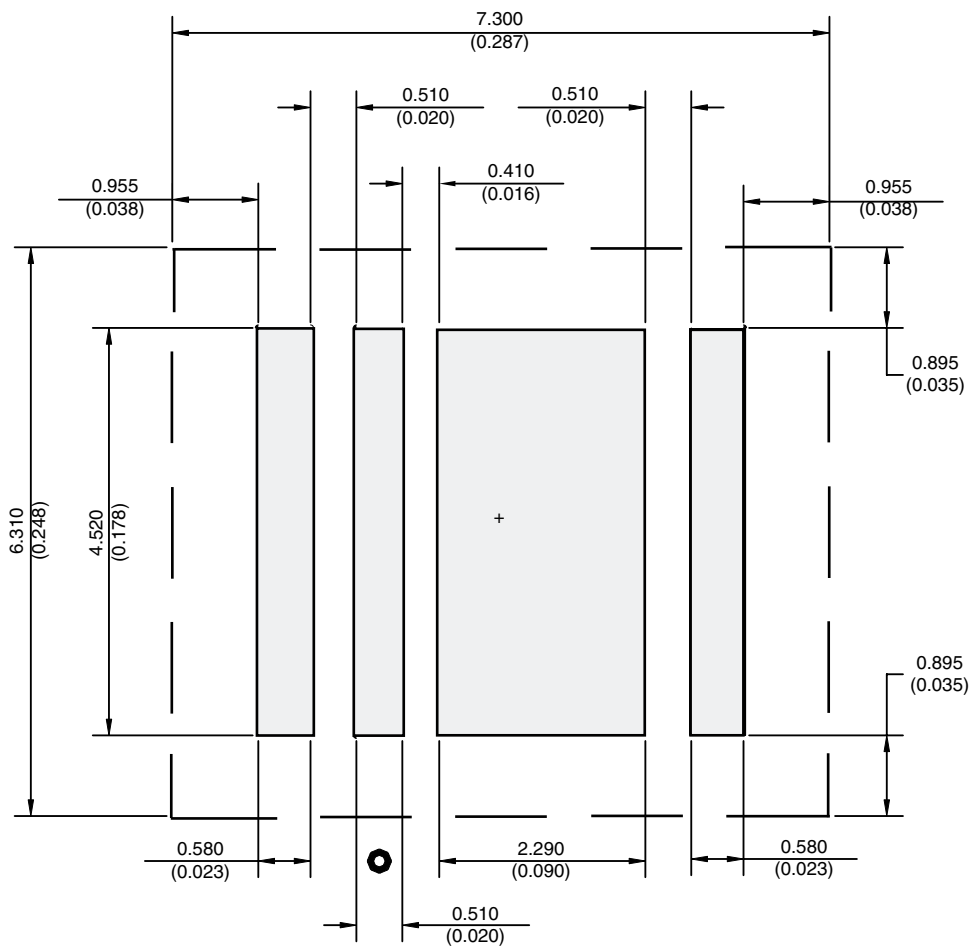


DIM	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.75	0.80	0.85	0.030	0.031	0.033
A1	0.00	-	0.05	0.000	-	0.002
b1	0.48	0.58	0.68	0.019	0.023	0.027
b2	0.41	0.51	0.61	0.016	0.020	0.024
b3	2.19	2.29	2.39	0.086	0.090	0.094
b4	0.89	1.04	1.19	0.035	0.041	0.047
b5	0.23	0.33	0.43	0.009	0.013	0.017
c	0.20	0.25	0.30	0.008	0.010	0.012
D	6.00	6.15	6.30	0.236	0.242	0.248
D1	5.74	5.89	6.04	0.226	0.232	0.238
E	5.01	5.16	5.31	0.197	0.203	0.209
E1	4.75	4.90	5.05	0.187	0.193	0.199
H1	0.23	-	-	0.009	-	-
H2	0.45	-	0.56	0.018	-	0.022
H3	0.31	0.41	0.51	0.012	0.016	0.020
H4	0.45	-	0.56	0.018	-	0.022
K1	4.22	4.37	4.52	0.166	0.172	0.178
K2	1.08	1.13	1.18	0.043	0.044	0.046
K3	1.37	-	-	0.054	-	-
K4	0.24	-	-	0.009	-	-
M1	4.30	4.50	4.70	0.169	0.177	0.185
M2	3.43	3.58	3.73	0.135	0.141	0.147
M3	0.22	-	-	0.009	-	-
M4	0.05	-	-	0.002	-	-
P1	0.15	0.20	0.25	0.006	0.008	0.010
T1	3.48	3.64	4.10	0.137	0.143	0.161
T2	0.56	0.76	0.95	0.022	0.030	0.037
T3	1.20	-	-	0.047	-	-
T4	3.90	-	-	0.153	-	-
T5	0	0.18	0.36	0.000	0.007	0.014
θ	0°	10°	12°	0°	10°	12°
ECN: T-08441-Rev. C, 11-Aug-08 DWG: 5946						

Notes

Millimeters govern over inches.

RECOMMENDED MINIMUM PADS FOR PolarPAK® Option L and S



Recommended Minimum for PolarPAK Option L and S
 Dimensions in mm/(Inches)
 No External Traces within Broken Lines
 Dot indicates Gate Pin (Part Marking)



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Material Category Policy

Vishay Intertechnology, Inc. hereby certifies that all its products that are identified as RoHS-Compliant fulfill the definitions and restrictions defined under Directive 2011/65/EU of The European Parliament and of the Council of June 8, 2011 on the restriction of the use of certain hazardous substances in electrical and electronic equipment (EEE) - recast, unless otherwise specified as non-compliant.

Please note that some Vishay documentation may still make reference to RoHS Directive 2002/95/EC. We confirm that all the products identified as being compliant to Directive 2002/95/EC conform to Directive 2011/65/EU.

Vishay Intertechnology, Inc. hereby certifies that all its products that are identified as Halogen-Free follow Halogen-Free requirements as per JEDEC JS709A standards. Please note that some Vishay documentation may still make reference to the IEC 61249-2-21 definition. We confirm that all the products identified as being compliant to IEC 61249-2-21 conform to JEDEC JS709A standards.

Данный компонент на территории Российской Федерации

Вы можете приобрести в компании MosChip.

Для оперативного оформления запроса Вам необходимо перейти по данной ссылке:

<http://moschip.ru/get-element>

Вы можете разместить у нас заказ для любого Вашего проекта, будь то серийное производство или разработка единичного прибора.

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Нашей специализацией является поставка электронной компонентной базы двойного назначения, продукции таких производителей как XILINX, Intel (ex.ALTERA), Vicor, Microchip, Texas Instruments, Analog Devices, Mini-Circuits, Amphenol, Glenair.

Сотрудничество с глобальными дистрибьюторами электронных компонентов, предоставляет возможность заказывать и получать с международных складов практически любой перечень компонентов в оптимальные для Вас сроки.

На всех этапах разработки и производства наши партнеры могут получить квалифицированную поддержку опытных инженеров.

Система менеджмента качества компании отвечает требованиям в соответствии с ГОСТ Р ИСО 9001, ГОСТ РВ 0015-002 и ЭС РД 009

Офис по работе с юридическими лицами:

105318, г.Москва, ул.Щербаковская д.3, офис 1107, 1118, ДЦ «Щербаковский»

Телефон: +7 495 668-12-70 (многоканальный)

Факс: +7 495 668-12-70 (доб.304)

E-mail: info@moschip.ru

Skype отдела продаж:

moschip.ru

moschip.ru_4

moschip.ru_6

moschip.ru_9