ANALOG DEVICES

HMC373LP3 / 373LP3E

v04.1119

GaAs PHEMT MMIC LOW NOISE AMPLIFIER w/ BYPASS MODE, 700 - 1000 MHz

Typical Applications

The HMC373LP3 / HMC373LP3E is ideal for basestation receivers:

- GSM, GPRS & EDGE
- CDMA & W-CDMA
- Private Land Mobile Radio

Features

Noise Figure: 0.9 dB

Output IP3: +35 dBm

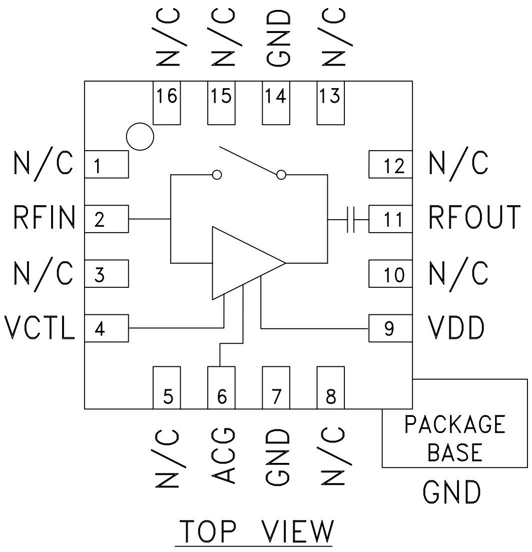
Gain: 14 dB

Low Loss LNA Bypass Path

Single Supply: +5V @ 90 mA

50 Ohm Matched Output

Functional Diagram



General Description

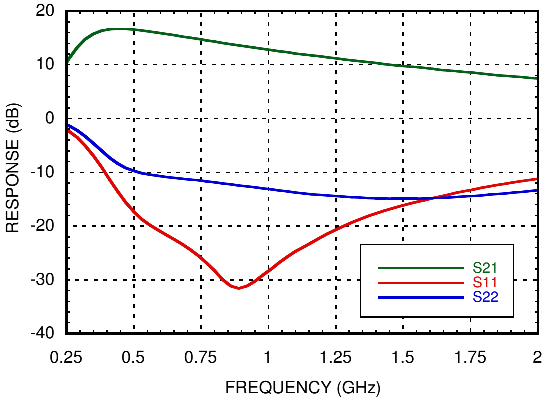
The HMC373LP3 / HMC373LP3E are versatile, high dynamic range GaAs MMIC Low Noise Amplifiers that integrates a low loss LNA bypass mode on the IC. The amplifier is ideal for GSM & CDMA cellular basestation front-end receivers operating between 700 and 1000 MHz and provides 0.9 dB noise figure, 14 dB of gain and +35 dBm IP3 from a single supply of +5V @ 90 mA. Input and output return losses are 28 and 12 dB respectively with the LNA requiring minimal external components to optimize the RF input match, RF ground and DC bias. By presenting an open or short circuit to a single control line, the LNA can be switched into a low 2.0 dB loss bypass mode reducing the current consumption to 10 µA. For applications which require improved noise figure, please see the HMC668LP3(E).

Electrical Specifications, T_A = +25° C, Vdd = +5V

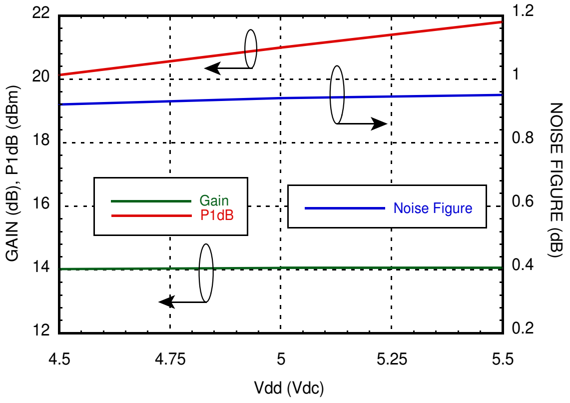
Parameter	LNA Mode			LNA Mode			Bypass Mode			Units
	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Frequency Range	810 - 960			700 - 1000			700 - 1000			MHz
Gain	11.5	13.5		10.5	14		-2.8	-2.0		dB
Gain Variation Over Temperature		0.008	0.015		0.008	0.015		0.002	0.004	dB / °C
Noise Figure		0.9	1.3		1.0	1.4				dB
Input Return Loss		28			25			30		dB
Output Return Loss		12			11			25		dB
Reverse Isolation		20			19					dB
Power for 1dB Compression (P1dB)*	18	21		17	20			30		dBm
Saturated Output Power (Psat)		22.5			22					dBm
Third Order Intercept (IP3)* (-20 dBm Input Power per tone, 1 MHz tone spacing)		35.5			35			50		dBm
Supply Current (Idd)		90			90			0.01		mA

** P1dB and IP3 for LNA Mode are referenced to RFOUT while P1dB and IP3 for Bypass Mode are referenced to RFIN.*

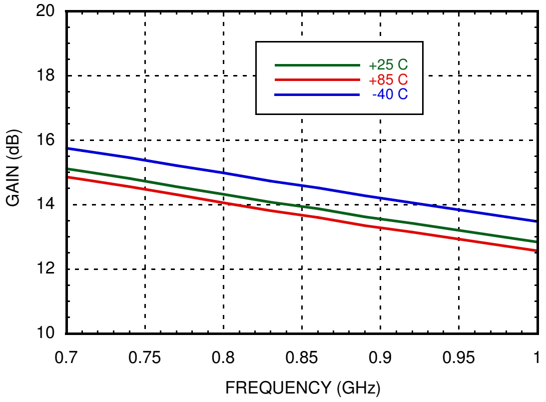
LNA Broadband Gain & Return Loss



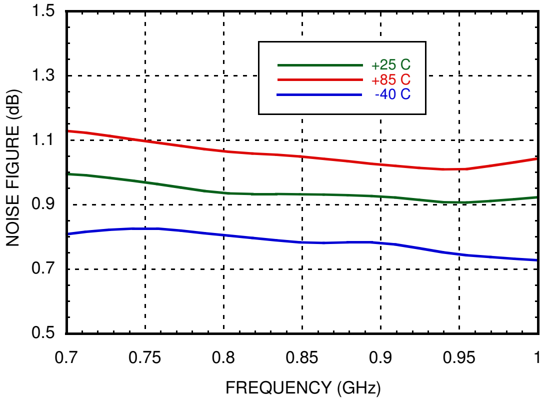
LNA – Gain, Noise Figure & Power vs. Supply Voltage @ 850 MHz



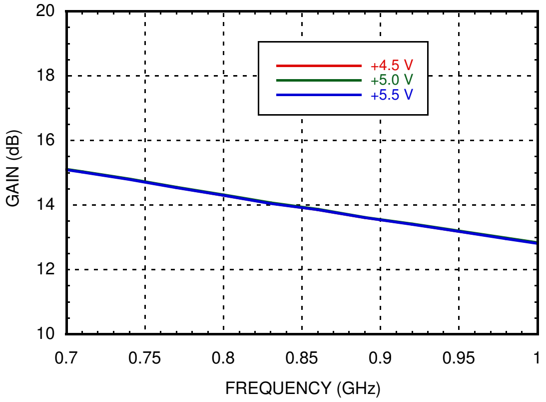
LNA Gain vs. Temperature



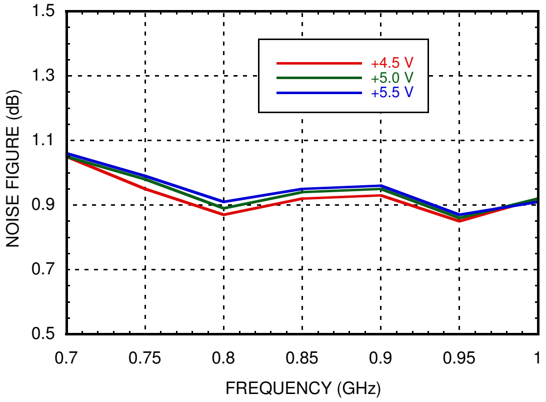
LNA Noise Figure vs. Temperature



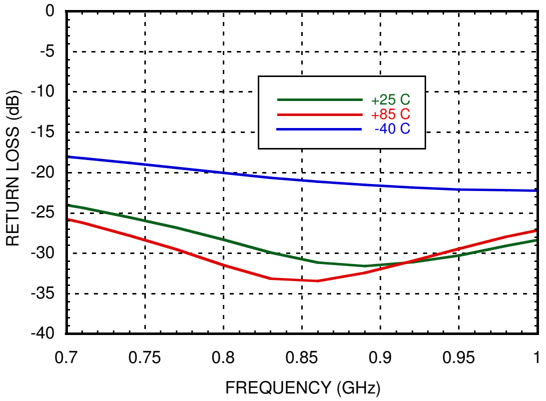
LNA Gain vs. Vdd



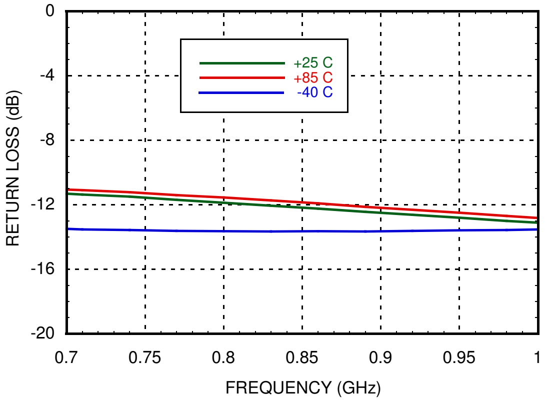
LNA Noise Figure vs. Vdd



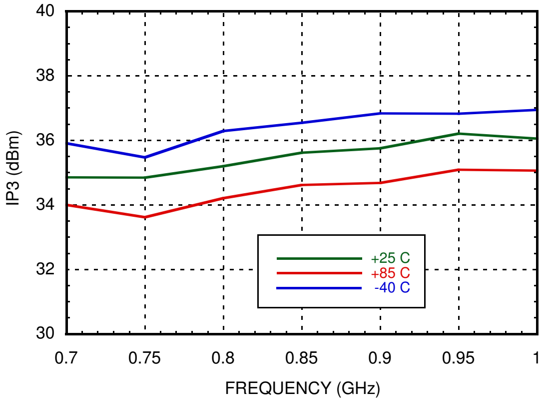
LNA Input Return Loss vs. Temperature



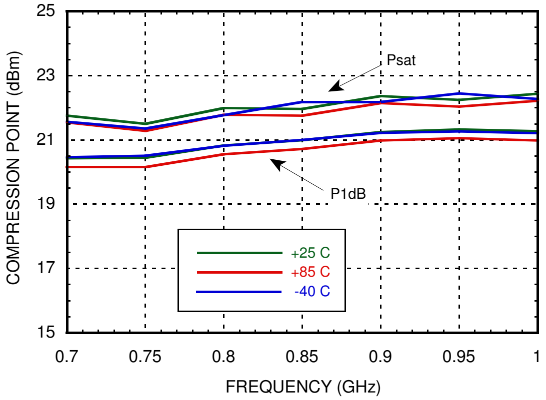
LNA Output Return Loss vs. Temperature



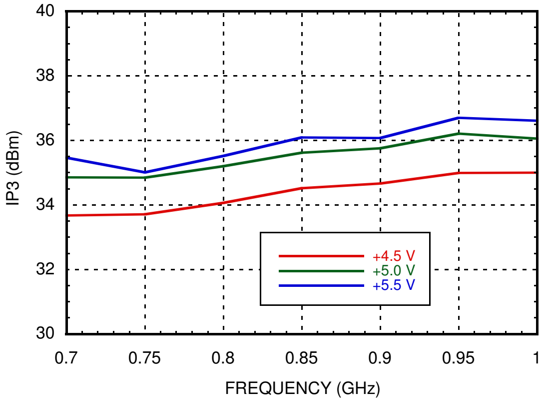
LNA Output IP3 vs. Temperature



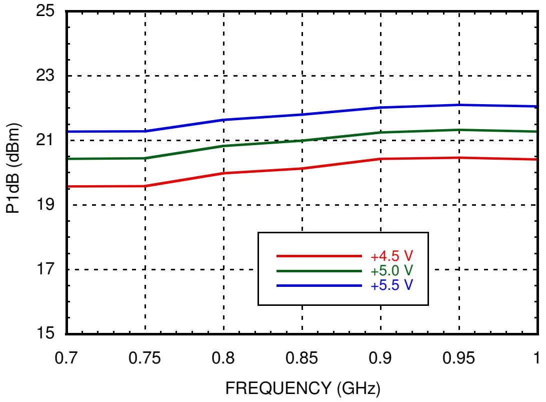
LNA P1dB & Psat vs. Temperature



LNA Output IP3 vs. Vdd

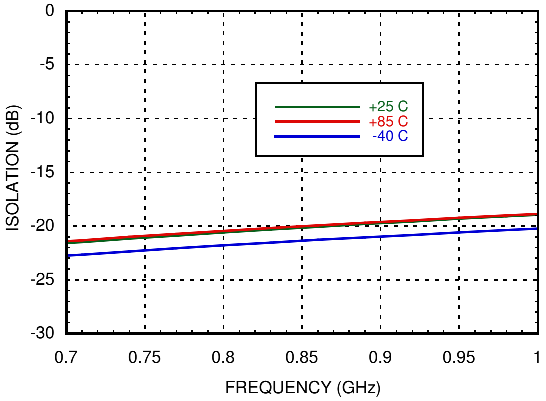


LNA P1dB vs. Vdd

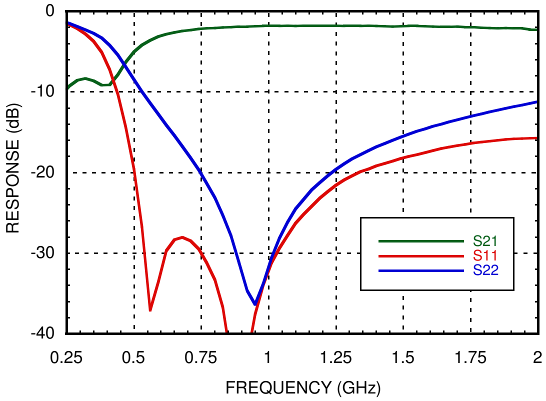


GaAs PHEMT MMIC LOW NOISE AMPLIFIER w/ BYPASS MODE, 700 - 1000 MHz

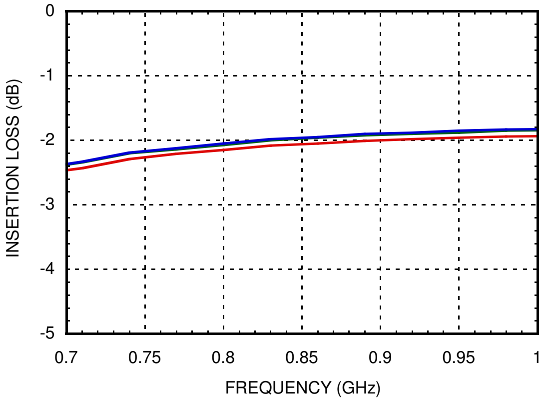
LNA Reverse Isolation vs. Temperature



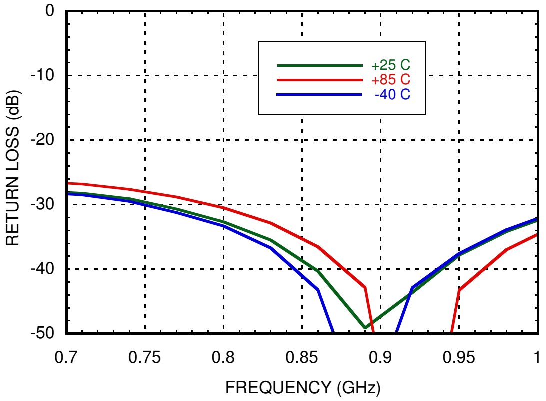
Bypass Mode Broadband Insertion Loss & Return Loss



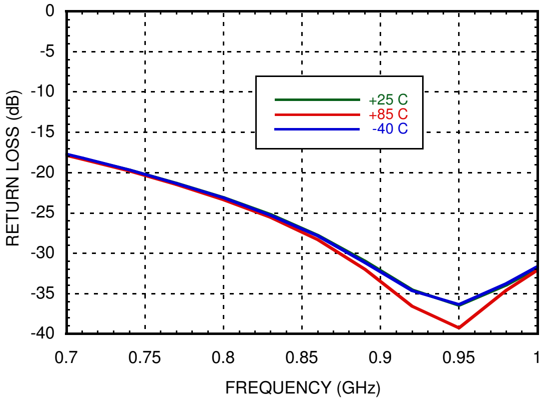
Bypass Mode Insertion Loss vs. Temperature



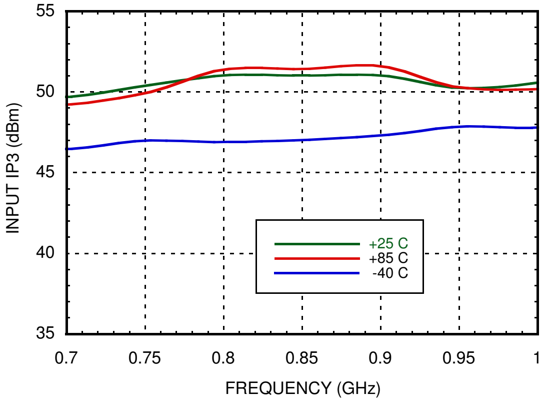
Bypass Mode Input Return Loss vs. Temperature



Bypass Mode Output Return Loss vs. Temperature



Bypass Mode Input IP3 vs. Temperature



Absolute Maximum Ratings

Drain Bias Voltage (Vdd)	+8.0 Vdc
RF Input Power (RFIN) LNA Mode (Vdd = +5.0 Vdc) Bypass Mode	+15 dBm +30 dBm
Channel Temperature	150 °C
Continuous Pdiss (T = 85 °C) (derate 13.5 mW/°C above 85 °C)	0.878 W
Thermal Resistance (channel to ground paddle)	74.1 °C/W
Storage Temperature	-65 to +150° C
Operating Temperature	-40 to +85° C

Typical Supply Current vs. Vdd

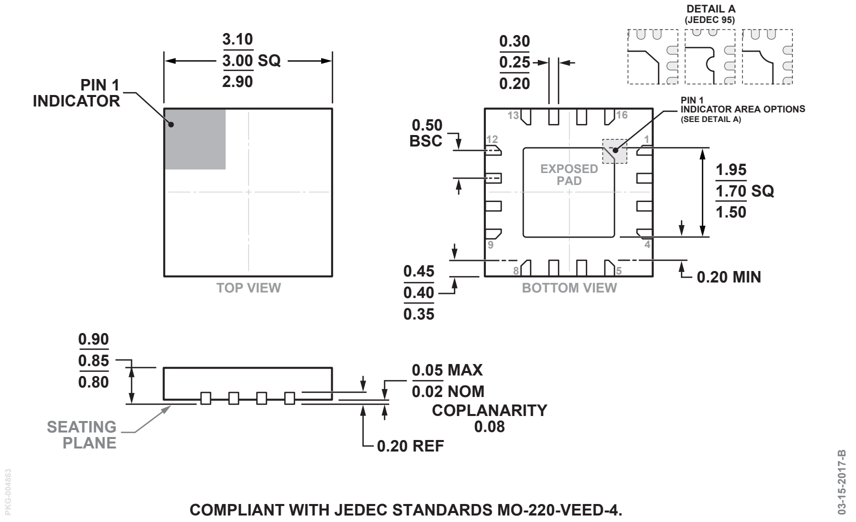
Vdd (Vdc)	Idd (mA)
+4.5	87
+5.0	90
+5.5	93

Truth Table

LNA Mode	Vctl= Short Circuit to DC Ground
Bypass Mode	Vctl= Open Circuit

ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

Outline Drawing



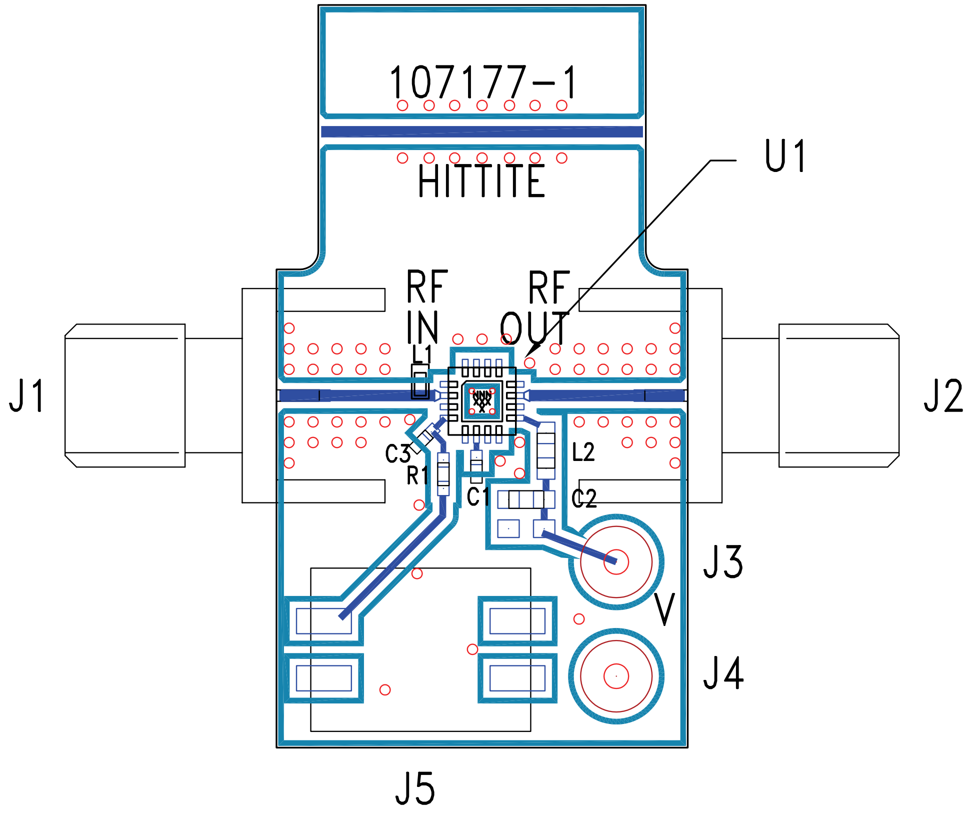
16-Lead Lead Frame Chip Scale Package [LFCSP]
3 mm × 3 mm Body and 0.85 mm Package Height
(HCP-16-1)
Dimensions shown in millimeters

Package Information

Part Number	Package Body Material	Lead Finish	MSL Rating [1]	Package Marking [2]
HMC373LP3E	RoHS-compliant Low Stress Injection Molded Plastic	100% matte Sn	MSL3	373 XXXX
HMC373LP3ETR	RoHS-compliant Low Stress Injection Molded Plastic	100% matte Sn	MSL3	373 XXXX

[1] Max peak reflow temperature of 260 °C
[2] 4-Digit lot number XXXX

Evaluation PCB



List of Materials for Evaluation PCB 107220 [1]

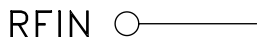
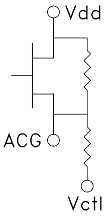
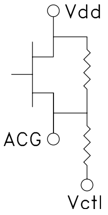
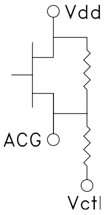
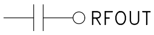
Item	Description
J1 - J2	PCB Mount SMA RF Connector
J3 - J4	DC Pin
J5	2 Pos DIP Switch
C1	10000 pF Capacitor, 0402 Pkg.
C2	10000 pF Capacitor, 0603 Pkg.
C3	1000 pF Capacitor, 0402 Pkg.
L1	19 nH Inductor, 0402 Pkg.
L2	18 nH Inductor, 0603 Pkg.
R1	2 Ohm Resistor, 0402 Pkg.
U1	HMC373LP3 / HMC373LP3E Amplifier
PCB [2]	107177 Evaluation Board

[1] Reference this number when ordering complete evaluation PCB

[2] Circuit Board Material: Rogers 4350

The circuit board used in the application should use RF circuit design techniques. Signal lines should have 50 Ohm impedance while the package ground leads and exposed paddle should be connected directly to the ground plane similar to that shown. A sufficient number of via holes should be used to connect the top and bottom ground planes. The evaluation circuit board shown is available from Analog Devices upon request.

Pin Descriptions

Pin Number	Function	Description	Interface Schematic
1, 3, 5, 8, 10, 12, 13, 15, 16	N/C	No connection necessary. These pins may be connected to RF/DC ground.	
2	RFIN	This pin is matched to 50 Ohms with a 19 nH inductor to ground. See Application Circuit.	
4	Vctl	DC ground return. LNA is in high gain mode when a short circuit is introduced to this pin through an external switch. LNA is in bypass mode when open circuit is introduced	
6	ACG	An external capacitor of 0.01µF to ground is required for low frequency bypassing. See Application Circuit for further details.	
7, 14	GND	These pins must be connected to RF/DC ground.	
9	Vdd	Power supply voltage. Choke inductor and bypass capacitor are required. See application circuit.	
11	RFOUT	This pin is AC coupled and matched to 50 Ohms.	

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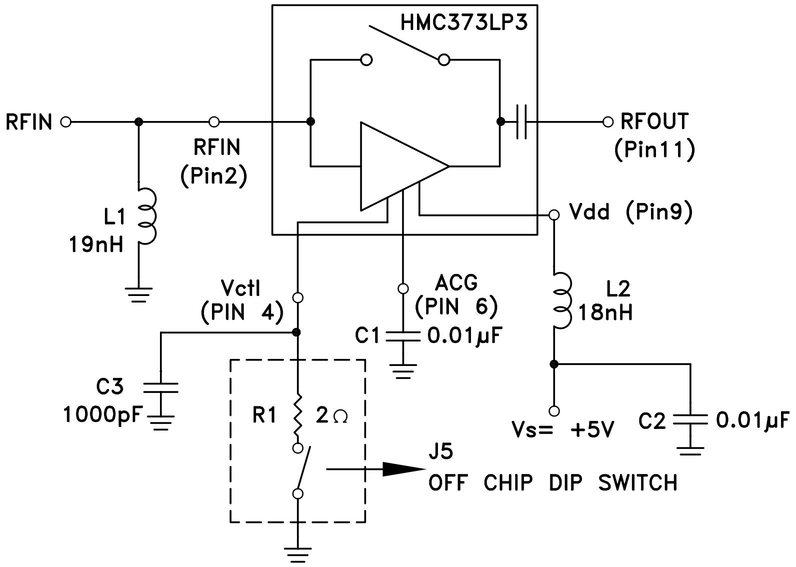
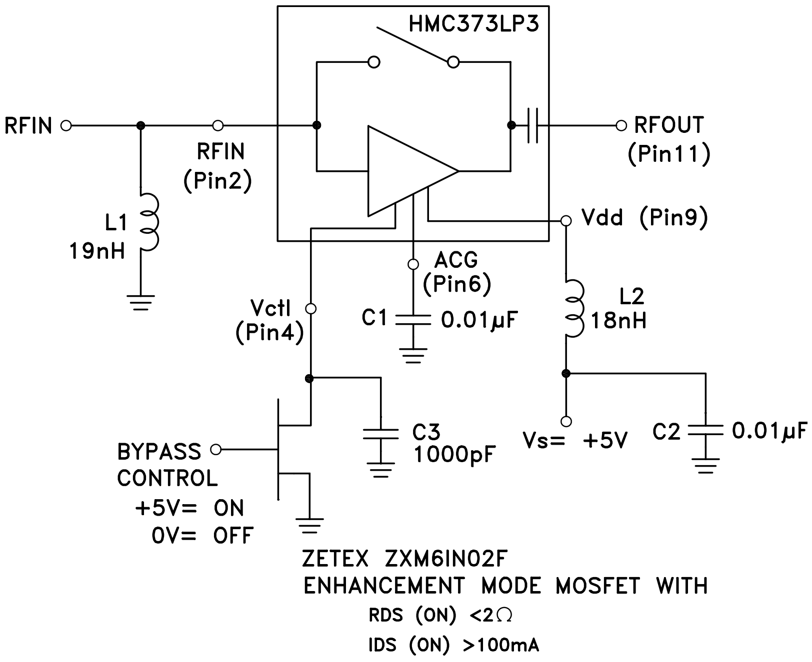
Evaluation Board Circuit



Application Circuit



Note 1: Choose value of capacitor C1 for low frequency bypassing. A 0.01 µF ±10% capacitor is recommended.

Note 2: Pin 4 (Vctl) is the DC ground return for the circuit. The LNA is in the high gain mode when a short circuit is introduced to this pin through an external switch. The LNA is in bypass mode when an open circuit is introduced. For the data presented, switching is done through a two position DIP switch (J5) in series with a 2 Ohm resistor (to account for the Ron of an electrical switch).

Note 3: L1, L2 and C1 should be located as close to pins as possible.

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+7 495 668 12 70
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Общество с ограниченной ответственностью «МосЧип» ИНН 7719860671 / КПП 771901001
Адрес: 105318, г.Москва, ул.Щербаковская д.3, офис 1107

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Офис по работе с юридическими лицами:

105318, г.Москва, ул.Щербаковская д.3, офис 1107, 1118, ДЦ «Щербаковский»

Телефон: +7 495 668-12-70 (многоканальный)

Факс: +7 495 668-12-70 (доб.304)

E-mail: info@moschip.ru

Skype отдела продаж:

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