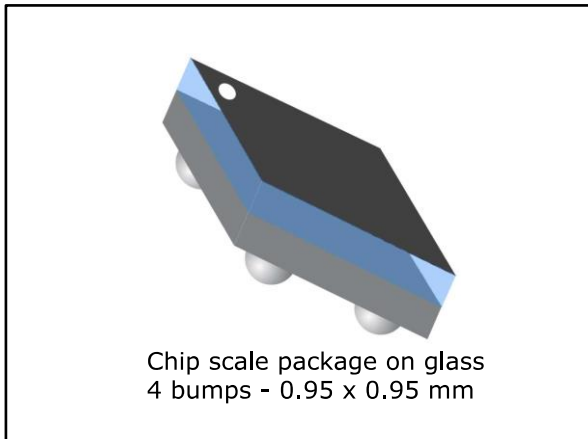


50 Ω / conjugate match to WILC1000 transformer balun

Datasheet - production data



Features

- 2.45 GHz Balun with integrated matching network
- Matching optimized for ATMEL WILC1000
- Low insertion loss
- Low amplitude imbalance
- Coated Flip-Chip on glass
- Small footprint < 0.90 mm²

Benefits

- Very low profile
- High RF performance
- PCB space saving versus discrete solution
- BOM count reduction
- Efficient manufacturability

Description

This device is an ultra-miniature matched balun. Matching impedance has been optimized for the ATMEL SmartConnect WILC1000 Wireless Link Controller. It is using STMicroelectronics IPD technology on non-conductive glass substrate which optimizes RF performance.

Figure 1: Pin configuration (bump view)

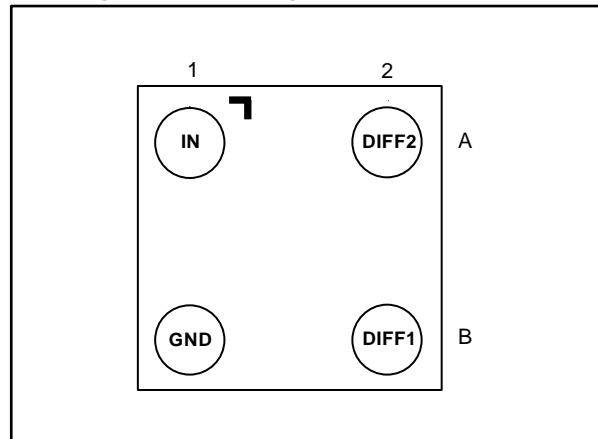
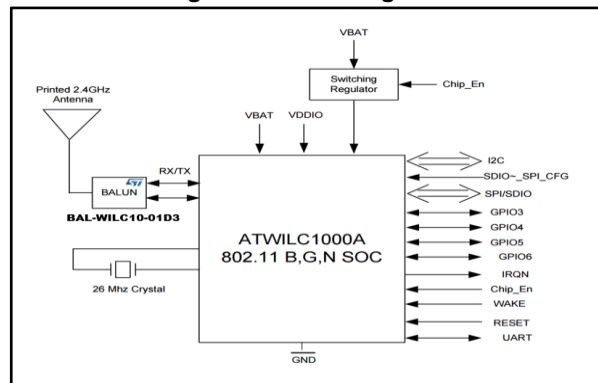


Figure 2: Block diagram



1 Characteristics

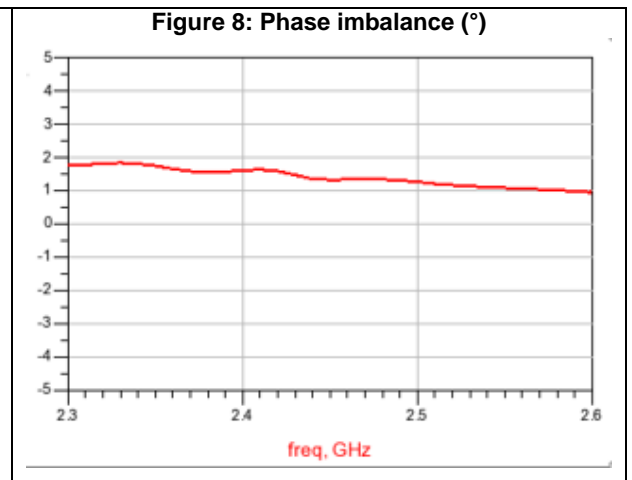
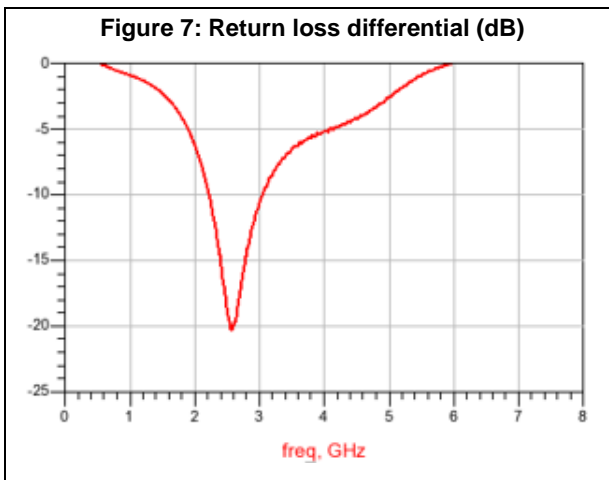
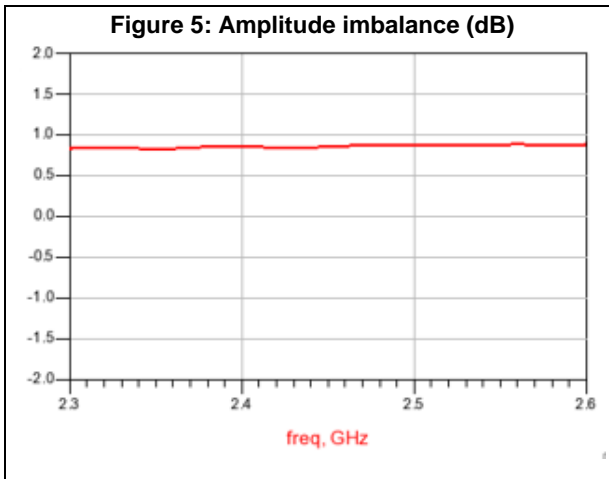
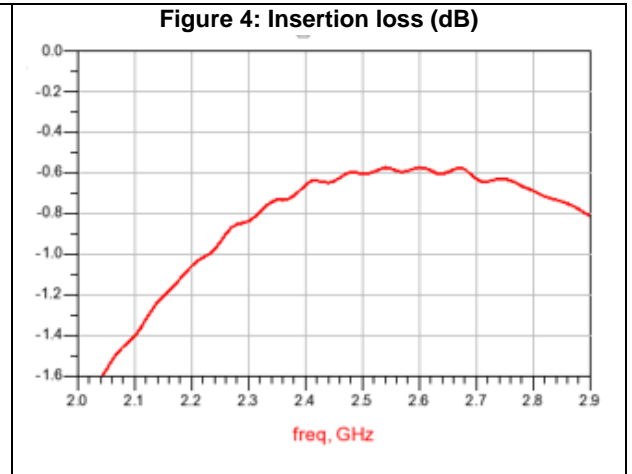
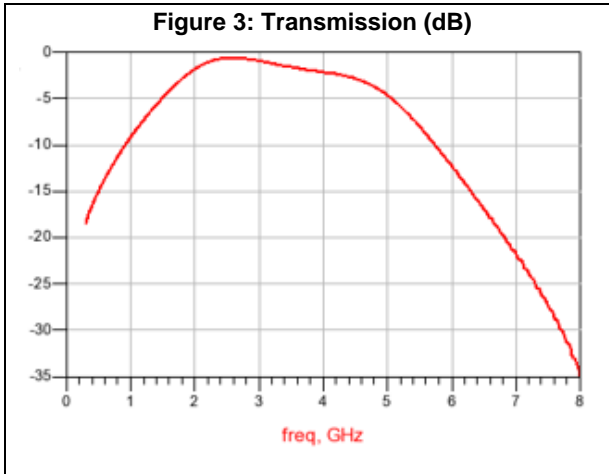
Table 1: Absolute maximum ratings (limiting values)

Symbol	Parameter	Value	Unit
P _{IN}	Input power R _{FIN}	20	dBm
V _{ESD}	ESD ratings MIL STD 883C (HBM: C = 100pF, R = 1.5kΩ, air discharge)	2000	V
	ESD ratings machine model (MM: C = 200pF, R = 25 Ω, L = 500 nH)	500	
	ESD ratings charged device model (CDM, JESD22-C101D)	500	
T _{OP}	Operating temperature	-40 to +105	°C

Table 2: Electrical characteristics (values, T_{amb} = 25 °C)

Symbol	Parameter	Value			Unit
		Min.	Typ.	Max.	
Z _{OUT}	Nominal differential output impedance	Conjugate match to WILC1000			Ω
Z _{IN}	Nominal input impedance	-	50	-	Ω
f	Frequency range (bandwidth)	2400		2500	MHz
I _L	Insertion loss in bandwidth		0.65	0.8	dB
R _{L_SE}	Single ended return loss in bandwidth		-16	-15	
R _{L_DIFF}	Differential return loss in bandwidth		-17	-15	
H ₂	Second harmonic rejection (differential mode)			-3.8	
H ₃	Third harmonic rejection (differential mode)			-23	
Φ _{imb}	Phase imbalance	-2	1.3	2	°
A _{imb}	Amplitude imbalance	-0.9	0.8	0.9	dB

1.1 RF measurements



2 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

2.1 Flip-Chip package information

Figure 9: Flip-Chip 4 bumps CSPG 0.4 package outline

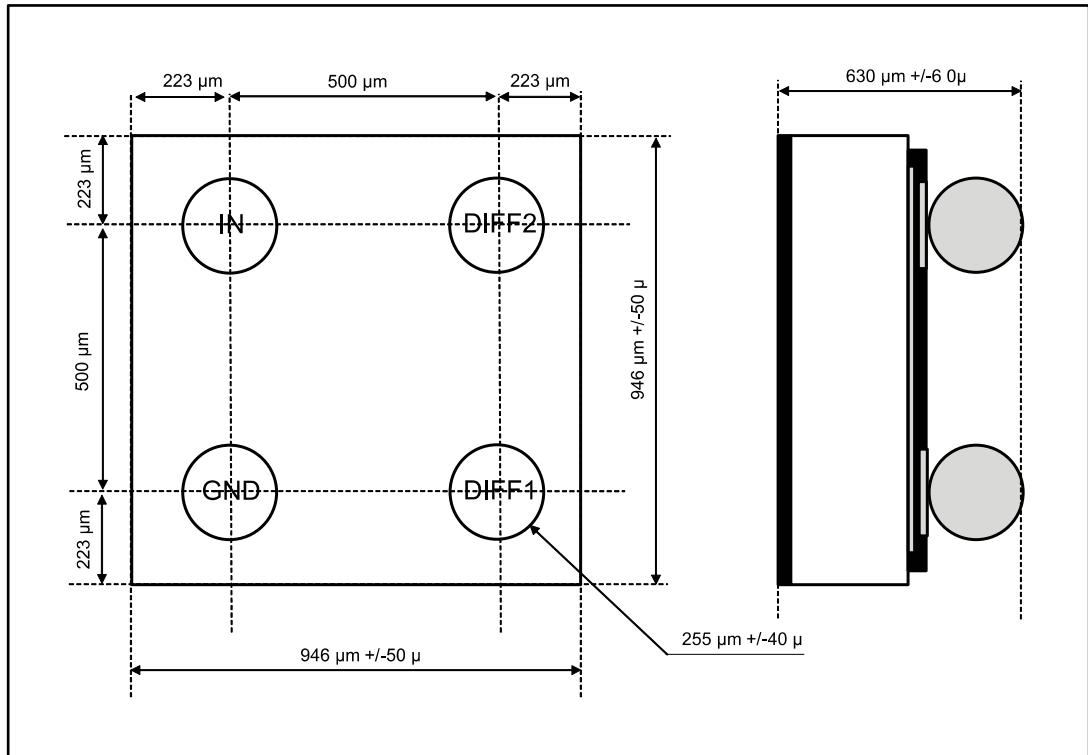
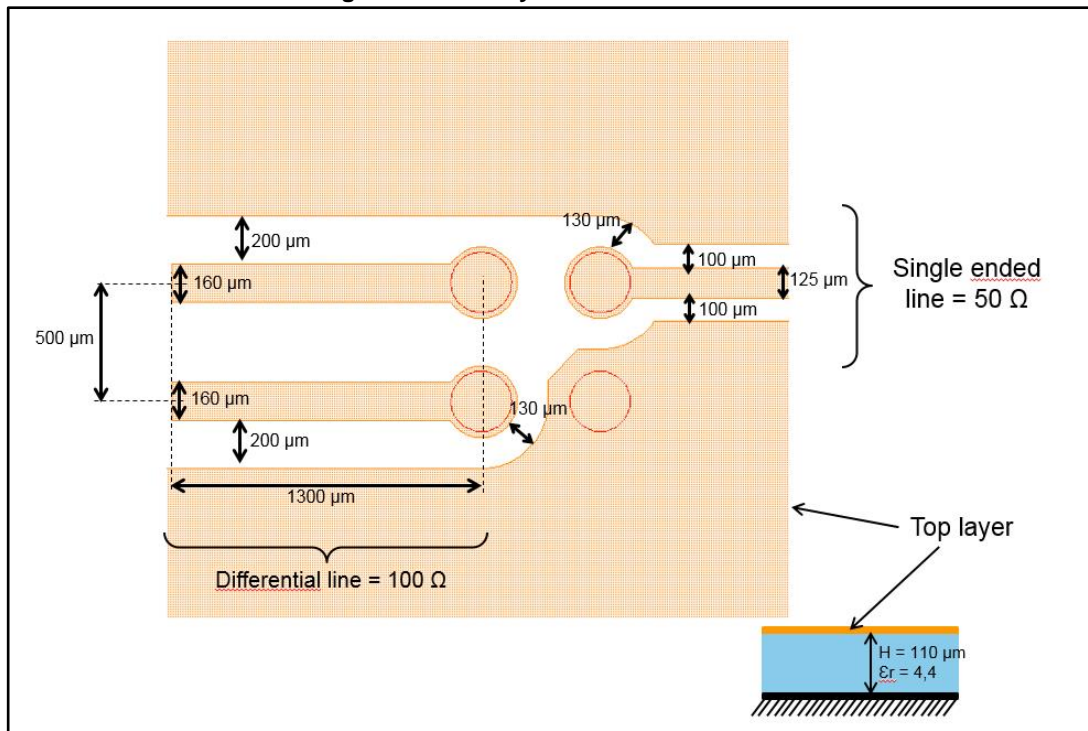
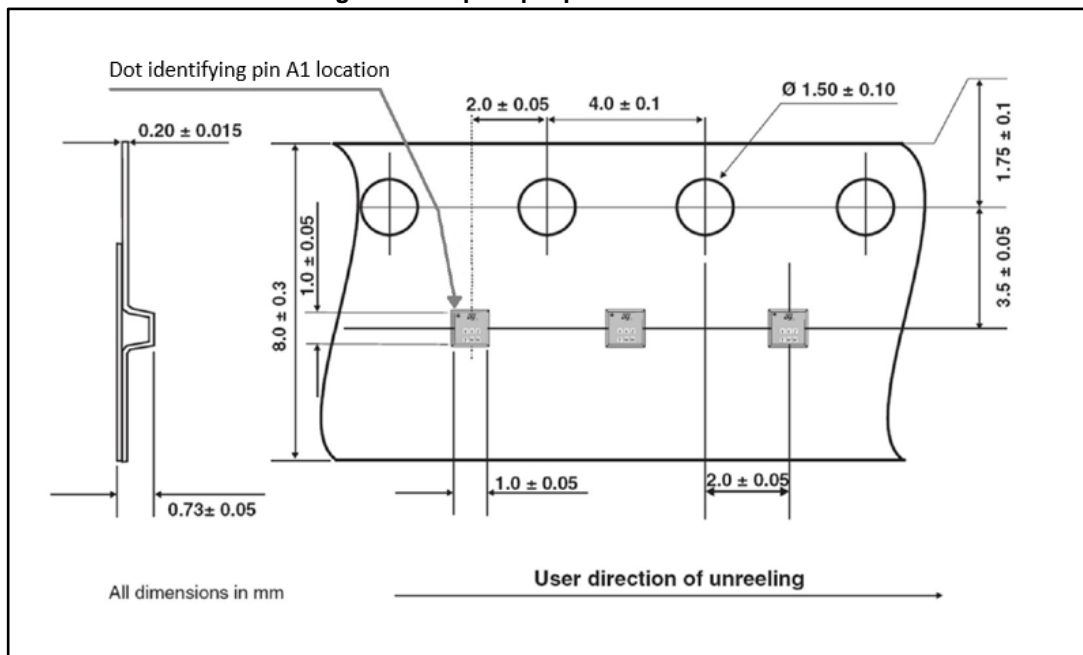


Figure 10: PCB layout recommendation



2.2 Flip-chip 4 bumps CSPG packing information

Figure 11: Flip-chip tape and reel outline



More information is available in the application note AN2348: "Flip Chip: Package description and recommendations for use"

Figure 12: Marking

Dot, ST logo
 ■ ECOPACK grade
 xx = marking
 z = manufacturing location
 yww = datecode

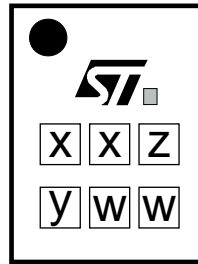


Figure 13: Footprint - non solder mask defined

Copper pad diameter:
 220µm recommended
 180µm minimum
 260µm maximum

Solder mask opening:
 320µm recommended
 300µm minimum
 340µm maximum

Solder stencil opening:
 220µm recommended

Line to connect copper pad on solder mask opening should be smaller than copper pad diameter

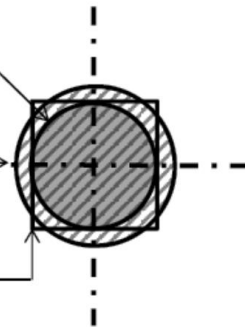
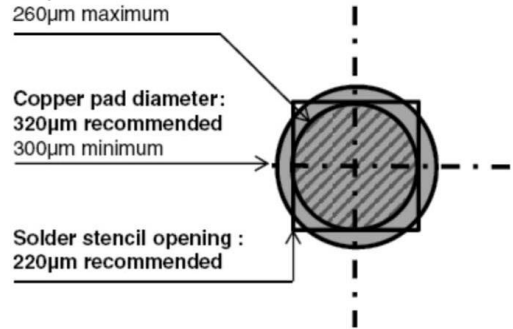


Figure 14: Footprint - solder mask defined

Solder mask opening:
 220µm recommended
 180µm minimum
 260µm maximum

Copper pad diameter:
 320µm recommended
 300µm minimum

Solder stencil opening :
 220µm recommended



3 Ordering information

Table 3: Ordering information

Order code	Marking	Package	Weight	Base qty.	Delivery mode
BAL-WILC10-01D3	L	WLCSP	1.084 mg	5000	Tape and reel (7")

4 Revision history

Table 4: Document revision history

Date	Revision	Changes
31-Mar-2017	1	Initial release.

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