**NXP Semiconductors**
Data sheet: Technical Data

Document Number: MC34716
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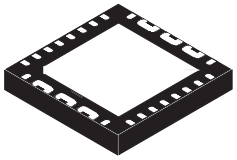
# 1.0 MHz dual switch-mode DDR power supply

**34716**

**DUAL SWITCH-MODE DDR POWER SUPPLY**



**EP SUFFIX**
**98ASA00702D**
**26-PIN QFN**

The 34716 is a highly integrated, space-efficient, low cost, dual synchronous buck switching regulator with integrated N-channel power MOSFETs. It is a high performance point-of-load (PoL) power supply with its second output having the ability to track an external reference voltage. it provides a full power supply solution for Double-Data-Rate (DDR) Memories.

Channel one provides a source only, 5.0 A drive capability, while channel two can sink and source up to 3.0 A. With its high current drive capability, channel one can be used to supply the VDDQ to the memory chipset. The second channel's ability to track a reference voltage provides an ideal means of supporting the termination voltage (VTT) required by modern data buses such as Double-Data-Rate (DDR) memory buses, including, but not limited to DDR, DDR2, DDR3 and Low power DDR3/DDR4 memories. Both channels are highly efficient with tight output regulation. The 34716 also provides a buffered output reference voltage (VREFOUT) to the memory chipset.

The 34716 SMARTMOS device offers a variety of control, supervisory and protection functions that simplify the implementation of complex designs. It is housed in a Pb-free, thermally enhanced and space efficient 26-pin exposed pad QFN.

Features

- 50 mΩ integrated N-channel power MOSFETs
- Input voltage operating range from 3.0 to 6.0 V
- ±1% accurate output voltages, ranging from 0.6 to 3.6 V
- The second output tracks 1/2 an external reference voltage
- ±1% accurate buffered reference output voltage
- Programmable switching frequency range from 200 kHz to 1.0 MHz
- Programmable soft start timing for channel one
- Over-current limit and short-circuit protection on both channels
- Thermal shutdown
- Output over-voltage and under-voltage detection
- Active low power good output signal
- Active low standby and shutdown inputs

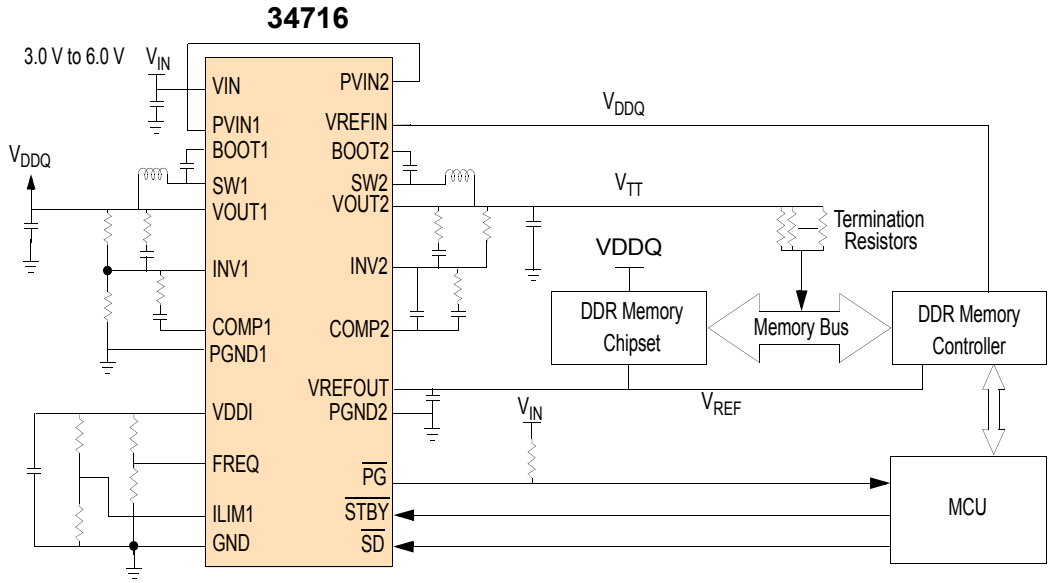



**Figure 1. Simplified application diagram**

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# 1 Orderable parts

**Table 1. Orderable part variations**

| Part number | Notes | Temperature ($T_A$) | Package |
|---|---|---|---|
| MC34716EP | (1) | -40 °C to 85 °C | 26 pin QFN |

Notes

1. To order parts in Tape & Reel, add the R2 suffix to the part number.

# 2 Internal block diagram

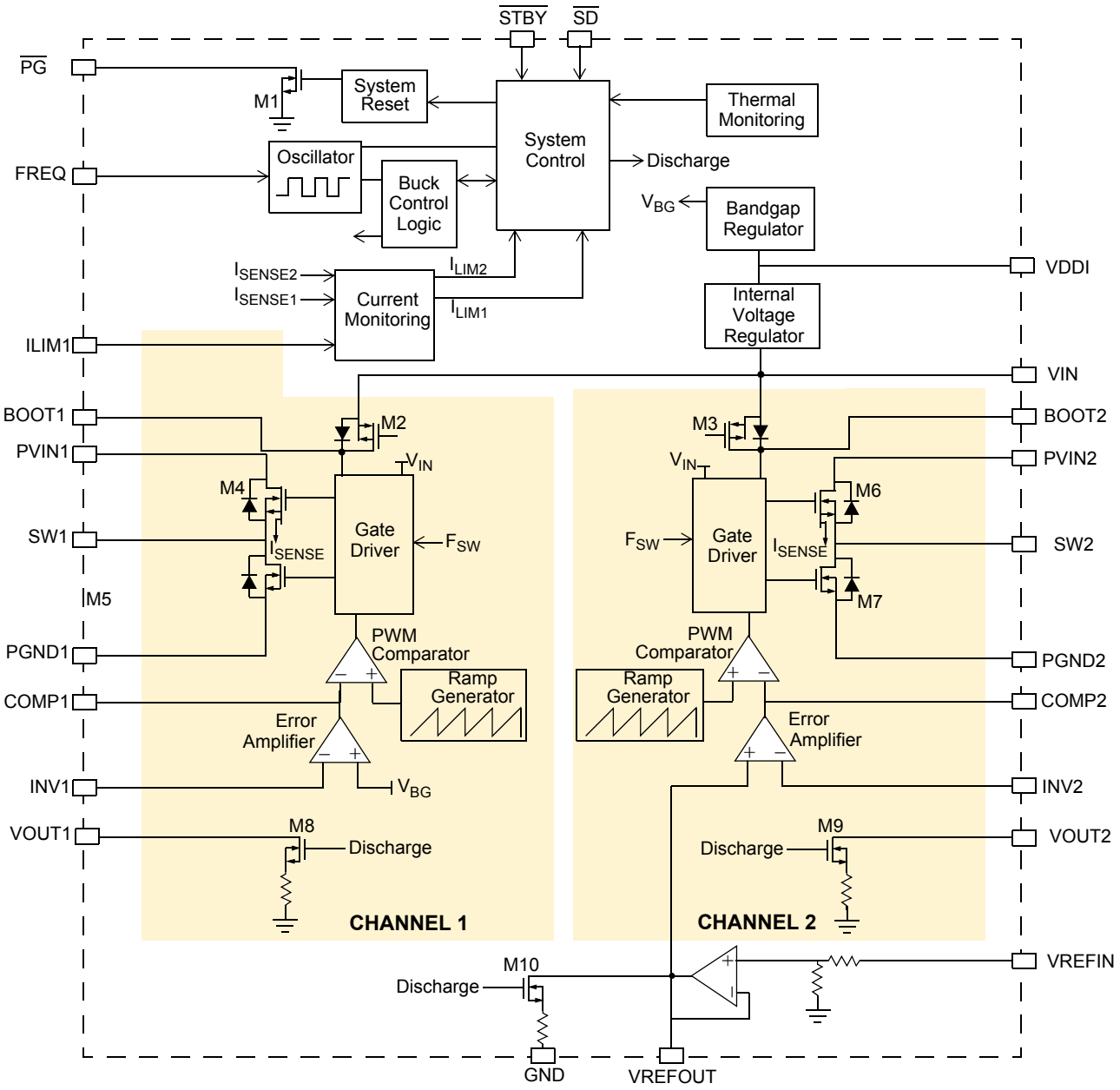



**Figure 2. Simplified internal block diagram**

34716

# 3 Pin connections

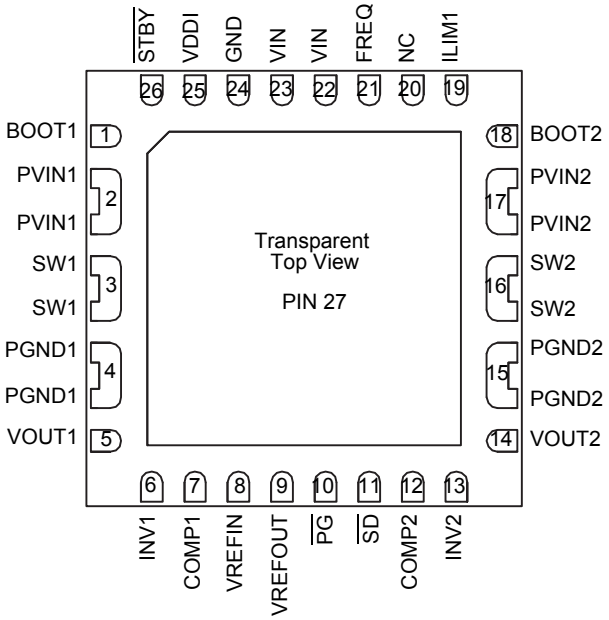



**Figure 3. Pin connections**

Section 5.2. "Functional pin description", page 14 provides a functional description of each pin.

**Table 2. Pin definitions**

| Pin number | Pin name | Pin function | Formal name | Definition |
|---|---|---|---|---|
| 1 | BOOT1 | Passive | Bootstrap | Channel 1 Bootstrap capacitor input pin |
| 2 | PVIN1 | Supply | Power Input Voltage | Channel 1 Buck converter power input |
| 3 | SW1 | Output | Switching Node | Channel 1 Buck converter switching node |
| 4 | PGND1 | Ground | Power Ground | Channel 1 Buck converter and discharge MOSFETs power ground |
| 5 | VOUT1 | Output | Output Voltage Discharge Path | Channel 1 Buck converter output voltage discharge pin |
| 6 | INV1 | Input | Error Amplifier Inverting Input | Channel 1 Buck converter error amplifier inverting input |
| 7 | COMP1 | Input | Buck Convertor Compensation Input | Channel 1 Buck converter external compensation network input |
| 8 | VREFIN | Input | Reference Voltage Input | Voltage tracking reference voltage input |
| 9 | VREFOUT | Output | Reference Voltage Output | This is a buffered reference voltage output |
| 10 | $\overline{PG}$ | Output | Power Good Output Signal | It is an active low open drain power good status reporting output |
| 11 | $\overline{SD}$ | Input | Shutdown Input | Shutdown mode input control pin |
| 12 | COMP2 | Input | Buck Convertor Compensation Input | Channel 2 Buck converter external compensation network input |
| 13 | INV2 | Input | Error Amplifier Inverting Input | Channel 2 Buck converter error amplifier inverting input |
| 14 | VOUT2 | Output | Output Voltage Discharge Path | Channel 2 Buck converter output voltage discharge pin |
| 15 | PGND2 | Ground | Power Ground | Channel 2 Buck converter and discharge MOSFETs power ground |

**Table 2. Pin definitions (continued)**

| Pin number | Pin name | Pin function | Formal name | Definition |
|---|---|---|---|---|
| 16 | SW2 | Output | Switching Node | Channel 2 Buck converter switching node |
| 17 | PVIN2 | Power | Power Input Voltage | Channel 2 Buck converter power input |
| 18 | BOOT2 | Input | Bootstrap Input | Channel 2 Bootstrap capacitor input pin |
| 19 | ILIM1 | Input | Soft Start Adjustment Input | Channel 1 soft start adjustment |
| 20 | NC | None | No Connect | No internal connections to this pin |
| 21 | FREQ | Input | Frequency Adjustment Input | The buck converters switching frequency adjustment input |
| 22,23 | VIN | Power | Input Supply Voltage | Power supply voltage of the IC |
| 24 | GND | Ground | Signal Ground | Analog ground of the IC |
| 25 | VDDI | Output | Internal Supply Voltage | Internal supply voltage output |
| 26 | $\overline{\text{STBY}}$ | Input | Standby Input | Standby mode input control pin |
| 27 | GND | Ground | Thermal Pad | Thermal pad for heat transfer. Connect the thermal pad to the analog ground and the ground plane for heat sinking. |

# 4 Electrical characteristics

## 4.1 Maximum ratings

**Table 3. Maximum ratings**

All voltages are with respect to ground unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

| Symbol | Ratings | Value | Unit | Notes |
|---|---|---|---|---|
| **Electrical ratings** | | | | |
| $V_{IN}$ | Input supply voltage (VIN) pin | −0.3 to 7.0 | V | |
| $P_{VIN}$ | High-side MOSFET drain voltage (PVIN1, PVIN2) pins | −0.3 to 7.0 | V | |
| $V_{SW}$ | Switching Node (SW1, SW2) Pins | −0.3 to 7.0 | V | |
| $V_{BOOT}$ - $V_{SW}$ | BOOT1, BOOT2 pins (referenced to SW1, SW2 pins respectively) | −0.3 to 7.0 | V | |
| - | $\overline{PG}$, VOUT1, VOUT2, $\overline{SD}$, and $\overline{STBY}$ pins | −0.3 to 7.0 | V | |
| - | VDDI, FREQ, ILIM1, INV1, INV2, COMP1, COMP2, VREFIN, and VREFOUT pins | −0.3 to 3.0 | V | |
| $I_{OUT1}$ | Channel 1 continuous output current | +5.0 | A | (2) |
| $I_{OUT2}$ | Channel 2 continuous output current | ±3.0 | A | (2) |
| $V_{ESD1}$<br>$V_{ESD2}$<br>$V_{ESD3}$ | ESD voltage<br>• Human body model<br>• Machine model (MM)<br>• Charge device model | <br>±2000<br>±200<br>±750 | V | (3) |
| **Thermal ratings** | | | | |
| $T_A$ | Operating ambient temperature | −40 to 85 | °C | (4) |
| $T_{STG}$ | Storage temperature | −65 to +150 | °C | |
| $T_{PPRT}$ | Peak package reflow temperature during reflow | Note 6 | °C | (5),(6) |
| $T_{J(MAX)}$ | Maximum junction temperature | +150 | °C | |
| $P_D$ | Power dissipation ($T_A$ = 85 °C) | 2.03 | W | (7) |

Notes

2. Continuous output current capability so long as $T_J$ is $\leq T_{J(MAX)}$.
3. ESD testing is performed in accordance with the Human Body Model (HBM) ($C_{ZAP}$ = 100 pF, $R_{ZAP}$ = 1500 Ω), the Machine Model (MM) ($C_{ZAP}$ = 200 pF, $R_{ZAP}$ = 0 Ω), and the Charge Device Model (CDM), Robotic ($C_{ZAP}$ = 4.0 pF).
4. The limiting factor is junction temperature, taking into account power dissipation, thermal resistance, and heatsinking.
5. Pin soldering temperature limit is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause malfunction or permanent damage to the device.
6. NXP's Package Reflow capability meets Pb-free requirements for JEDEC standard J-STD-020C. For Peak Package Reflow Temperature and Moisture Sensitivity Levels (MSL), Go to www.NXP.com, search by part number [e.g. remove prefixes/suffixes and enter the core ID to view all orderable parts. (i.e. MC33xxxD enter 33xxx), and review parametrics.
7. Maximum power dissipation at indicated ambient temperature.

**Table 3. Maximum ratings *(continued)***

All voltages are with respect to ground unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

| Symbol | Ratings | Value | Unit | Notes |
|---|---|---|---|---|
| **Thermal resistance** [8] | | | | |
| $R_{\theta JA}$ | Thermal resistance, junction to ambient, single-layer board (1s) | 93 | °C/W | (9) |
| $R_{\theta JMA}$ | Thermal resistance, junction to ambient, four-layer board (2s2p) | 32 | °C/W | (10) |
| $R_{QJB}$ | Thermal resistance, junction to board | 13.6 | °C/W | (11) |

Notes

8. The PVIN, SW, and PGND pins comprise the main heat conduction paths.
9. Per SEMI G38-87 and JEDEC JESD51-2 with the single-layer board (JESD51-3) horizontal.
10. Per JEDEC JESD51-6 with the board (JESD51-7) horizontal. There are thermal vias connecting the package to the two planes in the board. (per JESD51-5)
11. Thermal resistance between the device and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

# 4.2 Static electrical characteristics

**Table 4. Static electrical characteristics**

Characteristics noted under conditions 3.0 V ≤ $V_{IN}$ ≤ 6.0 V, −40 °C ≤ $T_A$ ≤ 85 °C, GND = 0 V, unless otherwise noted. Typical values noted reflect the approximate parameter means at $T_A$ = 25 °C under nominal conditions, unless otherwise noted.

| Symbol | Characteristic | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| **IC input supply voltage (VIN)** | | | | | | |
| $V_{IN}$ | Input supply voltage operating range | 3.0 | - | 6.0 | V | |
| $I_{IN}$ | Input DC supply current<br>(Normal mode: $\overline{SD}$ = 1 & $\overline{STBY}$ = 1, unloaded outputs) | - | - | 35 | mA | (12) |
| $I_{INQ}$ | Input DC supply current<br>(Standby mode, $\overline{SD}$ = 1 & $\overline{STBY}$ = 0) | - | - | 25 | mA | (12) |
| $I_{INOFF}$ | Input DC supply current<br>(Shutdown mode, $\overline{SD}$ = 0 & $\overline{STBY}$ = X) | - | - | 100 | µA | (12) |
| **Internal supply voltage output (VDDI)** | | | | | | |
| $V_{DDI}$ | Internal supply voltage range | 2.35 | 2.5 | 2.65 | V | |
| **Channel 1 buck converter (PVIN1, SW1, PGND1, BOOT1, INV1, COMP1, ILIM1)** | | | | | | |
| $P_{VIN}$ | CH 1 high-side MOSFET drain voltage range | 2.5 | - | 6.0 | V | |
| $V_{OUTHI1}$ | Output voltage adjustment range | 0.7 | - | 3.6 | V | (13) |
| - | Output voltage accuracy | 1.0 | - | 1.0 | % | (13), (14), (15) |
| $REG_{LN1}$ | Line regulation<br>(Normal operation, $V_{IN}$ = 3.0 V to 6.0 V, $I_{OUT1}$ = +5.0 A) | −1.0 | - | 1.0 | % | (13) |
| $REG_{LD1}$ | Load regulation<br>(Normal operation, $I_{OUT1}$ = 0.0 A to 5.0 A) | −1.0 | - | 1.0 | % | (13) |
| $V_{REF1}$ | Error amplifier reference voltage | - | 0.7 | - | V | (13) |
| $V_{UVR1}$ | Output undervoltage threshold | −8.0 | - | −1.5 | % | |
| $V_{OVR1}$ | Output overvoltage threshold | 1.5 | - | 8.0 | % | |
| $I_{OUT1}$ | Continuous output current | - | - | 5.0 | A | |
| $I_{LIM1}$ | Overcurrent limit | - | 6.5 | - | A | |
| $V_{ILIM1}$ | Soft start adjusting reference voltage range | 1.25 | - | $V_{DDI}$ | V | |
| $I_{SHORT1}$ | Short-circuit current limit | - | 8.5 | - | A | |

**Table 4. Static electrical characteristics (continued)**

Characteristics noted under conditions 3.0 V ≤ $V_{IN}$ ≤ 6.0 V, –40 °C ≤ $T_A$ ≤ 85 °C, GND = 0 V, unless otherwise noted. Typical values noted reflect the approximate parameter means at $T_A$ = 25 °C under nominal conditions, unless otherwise noted.

| Symbol | Characteristic | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| $R_{DS(on)HS1}$ | High-side N-CH power MOSFET (M4) $R_{DS(on)}$ ($I_{OUT1}$ = 1.0 A, $V_{BOOT1}$ - $V_{SW1}$= 3.3 V) | 10 | - | 50 | mΩ | (13) |
| $R_{DS(on)LS1}$ | Low-side N-CH power MOSFET (M5) $R_{DS(on)}$ ($I_{OUT1}$ = 1.0 A, $V_{IN}$ = 3.3 V) | 10 | - | 50 | mΩ | (13) |
| $R_{DS(on)M2}$ | M2 $R_{DS(on)}$ ($V_{IN}$ = 3.3 V, M2 is on) | 2.0 | - | 4.0 | Ω | |
| $I_{SW}$ | SW1 leakage current (standby and shutdown modes) | –10 | - | 10 | µA | |
| $I_{PVIN1}$ | PVIN1 pin leakage current (Shutdown mode) | –10 | - | 10 | µA | |
| $A_{EA}$ | Error amplifier DC gain | - | 150 | - | dB | (13) |
| $UGBW_{EA}$ | Error amplifier unit gain bandwidth | - | 3.0 | - | MHz | (13) |

Notes
12. Section “Modes of operation”, Page 18 has a detailed description of the different operating modes of the 34716
13. Design information only, this parameter is not production tested.
14. Overall output accuracy is directly affected by the accuracy of the external feedback network, 1% feedback resistors are recommended.
15. ±1% is assured at room temperature.

**Channel 1 buck converter (PVIN1, SW1, PGND1, BOOT1, INV1, COMP1, ILIM1) (continued)**

| | | | | | | |
|---|---|---|---|---|---|---|
| $SR_{EA}$ | Error amplifier slew rate | - | 7.0 | - | V/µs | (16) |
| $OFFSET_{EA}$ | Error amplifier input offset | –3.0 | 0 | 3.0 | mV | (16) |
| $I_{INV1}$ | INV1 pin leakage current | –1.0 | - | 1.0 | µA | |
| $T_{SDFET1}$ | Thermal shutdown threshold | - | 170 | - | °C | (16) |
| $T_{SDHYFET1}$ | Thermal shutdown hysteresis | - | 25 | - | °C | (16) |

**Channel 2 buck converter (PVIN2, SW2, PGND2, BOOT2, INV2, COMP2)**

| | | | | | | |
|---|---|---|---|---|---|---|
| $P_{VIN}$ | CH 2 high-side MOSFET drain voltage range | 2.5 | - | 6.0 | V | |
| $V_{OUTHI2}$ | Output voltage adjustment range | 0.6 | - | 1.35 | V | (16),(20) |
| - | Output voltage accuracy | –1.0 | - | 1.0 | % | (16), (17), (18) |
| $REG_{LN2}$ | Line regulation (normal operation, $V_{IN}$ = 3.0 to 6.0 V, $I_{OUT2}$ = ±3.0 A) | –1.0 | - | 1.0 | % | (16) |
| $REG_{LD2}$ | Load regulation (normal operation, $I_{OUT2}$ = -3.0 to 3.0 A) | –1.0 | - | 1.0 | % | (16) |
| $V_{REF2}$ | Error amplifier common mode voltage range | 0.0 | - | 1.35 | V | (16), (19) |
| $V_{UVR2}$ | Output undervoltage threshold | –8.0 | - | –1.5 | % | |
| $V_{OVR2}$ | Output overvoltage threshold | 1.5 | - | 8.0 | % | |
| $I_{OUT2}$ | Continuous output current | –3.0 | - | 3.0 | A | |
| $I_{LIM2}$ | Overcurrent Limit (sinking and sourcing) | - | 4.0 | - | A | |
| $I_{SHORT2}$ | Short-circuit current limit (sinking and sourcing) | - | 6.5 | - | A | |
| $R_{DS(on)HS2}$ | High-side N-CH power MOSFET (M6) $R_{DS(on)}$ • ($I_{OUT2}$ = 1.0 A, $V_{BOOT2}$ - $V_{SW2}$= 3.3 V) | 10 | - | 50 | mΩ | (16) |
| $R_{DS(on)LS2}$ | Low-side N-CH power MOSFET (M7) $R_{DS(on)}$ • ($I_{OUT2}$ = 1.0 A, $V_{IN}$ = 3.3 V) | 10 | - | 50 | mΩ | (16) |
| $R_{DS(on)M3}$ | M3 $R_{DS(on)}$ • ($V_{IN}$ = 3.3 V, M3 is on) | 2.0 | - | 4.0 | Ω | |
| $I_{SW}$ | SW2 leakage current (standby and shutdown modes) | –10 | - | 10 | A | |
| $I_{PVIN2}$ | PVIN2 pin leakage current (standby and shutdown modes) | –10 | - | 10 | µA | |

**Table 4. Static electrical characteristics (continued)**

Characteristics noted under conditions 3.0 V ≤ $V_{IN}$ ≤ 6.0 V, –40 °C ≤ $T_A$ ≤ 85 °C, GND = 0 V, unless otherwise noted. Typical values noted reflect the approximate parameter means at $T_A$ = 25 °C under nominal conditions, unless otherwise noted.

| Symbol | Characteristic | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| $A_{EA}$ | Error amplifier DC gain | - | 150 | - | dB | (16) |
| $UGBW_{EA}$ | Error amplifier unit gain bandwidth | - | 3.0 | - | MHz | (16) |
| $SR_{EA}$ | Error amplifier slew rate | - | 7.0 | - | V/µs | (16) |
| $OFFSET_{EA}$ | Error amplifier input offset | –3.0 | 0 | 3.0 | mV | (16) |
| $I_{INV2}$ | INV2 pin leakage current | –1.0 | - | 1.0 | µA | |
| $T_{SDFET2}$ | Thermal shutdown threshold | - | 170 | - | °C | (16) |
| $T_{SDHYFET2}$ | Thermal shutdown hysteresis | - | 25 | - | °C | (16) |

Notes

16. Design information only, this parameter is not production tested.
17. Overall output accuracy is directly affected by the accuracy of the external feedback network. 1% feedback resistors are recommended
18. ±1% is assured at room temperature
19. The 1% output voltage regulation is only guaranteed for a common mode voltage range greater than or equal to 0.6 V at room temperature
20. If a $V_{OUT}$ =0.6 V is desired, make sure $V_{IN}$ is kept below 3.6 V and the switching frequency FSW is lower than 500 kHz to allow enough room for output regulation

**Table 4. Static electrical characteristics (continued)**

Characteristics noted under conditions 3.0 V ≤ $V_{IN}$ ≤ 6.0 V, −40 °C ≤ $T_A$ ≤ 85 °C, GND = 0 V, unless otherwise noted. Typical values noted reflect the approximate parameter means at $T_A$ = 25 °C under nominal conditions, unless otherwise noted.

| Symbol | Characteristic | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| **Oscillator (FREQ)** | | | | | | |
| $V_{FREQ}$ | Oscillator frequency adjusting reference voltage range | 0.0 | - | $V_{DDI}$ | V | |
| **Tracking (VREFIN, VREFOUT, VOUT1, VOUT2)** | | | | | | |
| $V_{REFIN}$ | VREFIN external reference voltage range | 0.0 | - | 2.7 | V | (21) |
| $V_{REFOUT}$ | VREFOUT buffered reference voltage range | 0.0 | - | 1.35 | V | |
| - | VREFOUT buffered reference voltage accuracy | −1.0 | - | 1.0 | % | (22) |
| $I_{REFOUT}$ | VREFOUT buffered reference voltage current capability | 0.0 | - | 8.0 | mA | |
| $I_{REFOUTLIM}$ | VREFOUT buffered reference voltage overcurrent limit | - | 11 | - | mA | |
| $R_{TDR(M10)}$ | VREFOUT total discharge resistance | - | 50 | - | Ω | (21) |
| $R_{TDR(M8)}$ | VOUT1 total discharge resistance | - | 50 | - | Ω | (21) |
| $R_{TDR(M9)}$ | VOUT2 total discharge resistance | - | 50 | - | Ω | (21) |
| $I_{VOUTLKG2}$ | VOUT2 pin leakage current (standby mode, $V_{OUT2}$ = 3.6 V) | −1.0 | - | 1.0 | μA | |
| **Control and supervisory ($\overline{\text{STBY}}$, $\overline{\text{SD}}$, $\overline{\text{PG}}$)** | | | | | | |
| $V_{STBYHI}$ | $\overline{\text{STBY}}$ high level input voltage | 2.0 | - | - | V | |
| $V_{STBYLO}$ | $\overline{\text{STBY}}$ low level input voltage | - | - | 0.4 | V | |
| $R_{STBYUP}$ | $\overline{\text{STBY}}$ pin internal pull-up resistor | 1.0 | - | 2.0 | MΩ | |
| $V_{SDHI}$ | $\overline{\text{SD}}$ high level input voltage | 2.0 | - | - | V | |
| $V_{SDLO}$ | $\overline{\text{SD}}$ low level input voltage | - | - | 0.4 | V | |
| $R_{SDUP}$ | $\overline{\text{SD}}$ pin internal pull-up resistor | 1.0 | - | 2.0 | MΩ | |
| $V_{PGLO}$ | $\overline{\text{PG}}$ low level output voltage ($I_{PG}$ = 3.0 mA) | - | - | 0.4 | V | |
| $I_{PGLKG}$ | $\overline{\text{PG}}$ pin leakage current (M1 is off, Pulled up to VIN) | - | - | 1.0 | μA | |

Notes

21. Design information only, this parameter is not production tested.
22. The 1% accuracy is only guaranteed for $V_{REFOUT}$ greater than or equal to 0.6 V at room temperature.

## 4.3 Dynamic electrical characteristics

**Table 5. Dynamic electrical characteristics**

Characteristics noted under conditions 3.0 V ≤ $V_{IN}$ ≤ 6.0 V, –40 °C ≤ $T_A$ ≤ 85 °C, GND = 0 V, unless otherwise noted. Typical values noted reflect the approximate parameter means at $T_A$ = 25 °C under nominal conditions, unless otherwise noted.

| Symbol | Characteristic | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| **Channel 1 buck converter (PVIN1, SW1, PGND1, BOOT1, INV1, COMP1, ILIM1)** | | | | | | |
| $t_{RISE1}$ | Switching node (SW1) rise time ($P_{VIN}$ = 3.3 V, IOUT1 = 5.0 A) | - | 8.0 | - | ns | (23) |
| $t_{FALL1}$ | Switching node (SW1) fall time ($P_{VIN}$ = 3.3 V, IOUT1 = 5.0 A) | - | 5.0 | - | ns | (23) |
| $t_{OFFMIN}$ | Minimum off time | - | 150 | - | ns | |
| $t_{ONMIN}$ | Minimum on time | - | 0 | - | ns | (24) |
| $t_{SS1}$ | Soft start duration (normal mode)<br>ILIM1: 1.25 to 1.49 V<br>1.5 to 1.81 V<br>1.82 to 2.13 V<br>2.14 to 2.5 V | <br>-<br>-<br>-<br>- | <br>3.2<br>1.6<br>0.8<br>0.4 | <br>-<br>-<br>-<br>- | ms | |
| $t_{LIM1}$ | Overcurrent limit timer | - | 10 | - | ms | |
| $t_{TIMEOUT1}$ | Overcurrent limit retry timeout period | 80 | - | 120 | ms | |
| $t_{FILTER1}$ | Output undervoltage/overvoltage filter delay timer | 5.0 | - | 25 | µs | |
| **Channel 2 buck converter (PVIN2, SW2, PGND2, BOOT2, INV2, COMP2)** | | | | | | |
| $t_{RISE2}$ | Switching node (SW2) rise time ($P_{VIN}$ = 3.3 V, $I_{OUT2}$ = ±3.0 A) | - | 28 | - | ns | (23) |
| $t_{FALL2}$ | Switching node (SW2) fall time ($P_{VIN}$ = 3.3 V, $I_{OUT2}$ = ±3.0 A) | - | 12.0 | - | ns | (23) |
| $t_{OFFMIN}$ | Minimum off time | - | 150 | - | ns | |
| $t_{ONMIN}$ | Minimum on time | - | 180 | - | ns | |
| $t_{SS2}$ | Soft start duration (normal mode) | - | 1.6 | - | ms | |
| $t_{LIM2}$ | Overcurrent limit timer | - | 10 | - | ms | |
| $t_{TIMEOUT2}$ | Overcurrent limit retry timeout period | 80 | - | 120 | ms | |
| $t_{FILTER2}$ | Output undervoltage/overvoltage filter delay timer | 5.0 | - | 25 | µs | |
| **Oscillator (FREQ)** (25) | | | | | | |
| $f_{SW}$ | Oscillator default switching frequency (FREQ = GND) | - | 1.0 | - | MHz | |
| $f_{SW}$ | Oscillator switching frequency range | 200 | - | 1000 | kHz | |
| **Control and supervisory ($\overline{\text{STBY}}$, $\overline{\text{SD}}$, $\overline{\text{PG}}$)** | | | | | | |
| $t_{PGRESET}$ | $\overline{\text{PG}}$ reset delay | 8.0 | - | 12 | ms | |
| $t_{TIMEOUT}$ | Thermal shutdown retry timeout period | 80 | - | 120 | ms | (23) |
| $t_{OFFMIN}$ | Minimum off time | - | 150 | - | ns | |
| $t_{ONMIN}$ | Minimum on time | - | 100 | - | ns | |

Notes

23. Design information only, this parameter is not production tested.
24. The regulator has the ability to enter into pulse skip mode when the inductor current ripple reaches the threshold for the LS zero detect, which has a typical value of 500 mA.
25. Oscillator frequency tolerance is ±10%.

## 4.4 Electrical performance curves

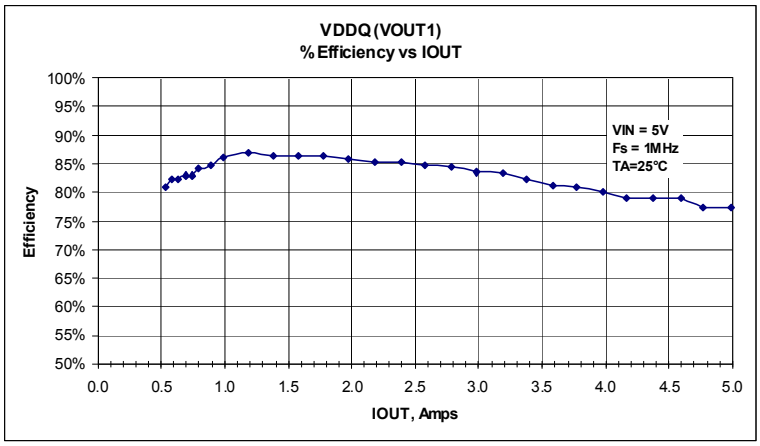



**Figure 4. % Efficiency vs. $I_{OUT}$**

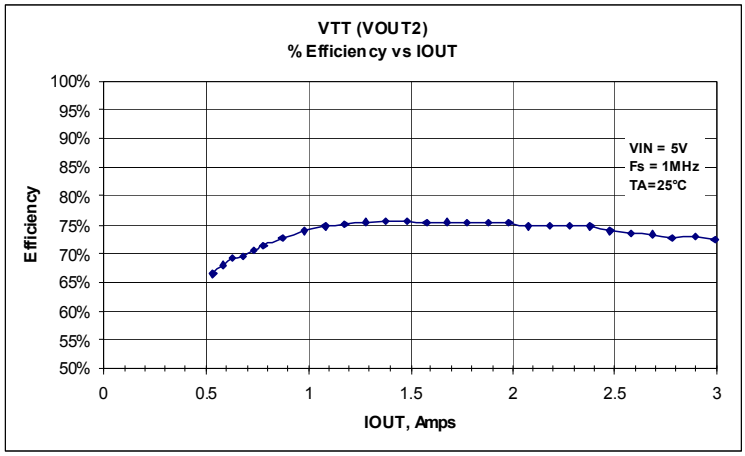



**Figure 5. % Efficiency vs. $I_{OUT}$**

# 5 Functional description

## 5.1 Introduction

In modern microprocessor/memory applications, address command and control lines require system level termination to a voltage ($V_{TT}$) equal to 1/2 the memory supply voltage ($V_{DDQ}$). Having the termination voltage at the midpoint ensures that the power supply maintains symmetry when switching occurs. Also, the DDR SDRAM input receiver must have a reference voltage ($V_{REF}$) that is free of any noise or voltage variations. $V_{REF}$ is also equal to 1/2 $V_{DDQ}$. Varying the $V_{REF}$ voltage effects the setup and hold time of the memory. To comply with DDR requirements and to obtain the best performance, $V_{TT}$ and $V_{REF}$ must be tightly regulated to track 1/2 $V_{DDQ}$ across voltage, temperature and noise margins. $V_{TT}$ must track any variations in the DC $V_{REF}$ value ($V_{TT}$ = $V_{REF}$ ±40 mV), (See Figure 6) for a DDR system level diagram.

The 34716 supplies the $V_{DDQ}$, $V_{TT}$ and a buffered $V_{REF}$ output. To ensure compliance with DDR specifications, the $V_{DDQ}$ line is applied to the VREFIN pin and divided by 2 internally through a precision resistor divider. This internal voltage is then used as the reference voltage for the $V_{TT}$ output. The same internal voltage is also buffered so that the $V_{REF}$ voltage at the applications VREFOUT pin can be used without an external resistor divider. The 34716 offers tight voltage regulation and power sequencing/tracking along with the ability to handle DDR peak transient current requirements. It gives the user a complete DDR power supply solution with optimum performance. Buffering the $V_{REF}$ output provides enhanced immunity to noise and load changes.

The 34716 uses a voltage mode synchronous buck switching converter topology with integrated low $R_{DS(on)}$ (50 mΩ) N-channel power MOSFETs to provide an output voltage accuracy of less than ±2.0%. It has a programmable switching frequency that operates at up to 1.0 MHz. The 34716 supplies 5.0 A maximum from one output and sinks and sources up to 3.0 A of continuous current from the other output. It provides protection against output overcurrent, overvoltage, undervoltage and overtemperature conditions. It also protects the system from short-circuit events. A power good output signal alerts the host when a fault occurs.

For boards that support the suspend-to-RAM (S3) and the suspend-to-disk (S5) states, the 34716 offers the $\overline{\text{STBY}}$ and the $\overline{\text{SD}}$ pins respectively. Pulling any of these pins low, puts the IC in the corresponding state.

By integrating the control/supervisory circuitry along with the power MOSFET switches for the buck converter into a space-efficient package, the 34716 offers a complete, small-size, cost-effective and simple solution to satisfy the needs of DDR memory applications.

Besides DDR memory termination, the 34716 also supports supply termination for other active buses and graphics card memory. It can be used in Netcom/Telecom applications like servers and is suitable for desktop motherboards, game consoles, set top boxes, and high end high definition TVs.

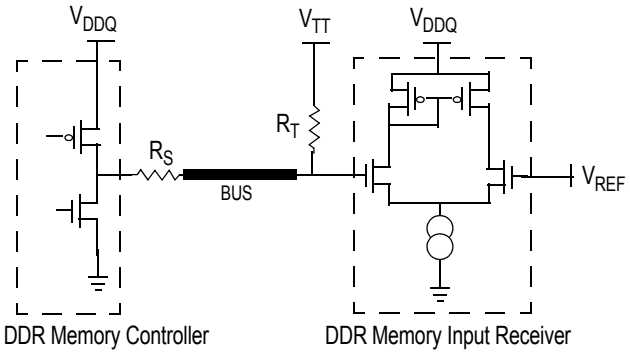



**Figure 6. DDR system level diagram**

## 5.2 Functional pin description

### 5.2.1 Bootstrap input (BOOT1, BOOT2)

Bootstrap capacitor input pin. Connect a capacitor (as discussed in 7.7Bootstrap capacitor 27) between this pin and the SW pin of the respective channel to enhance the gate of the high-side Power MOSFET during switching.

### 5.2.2 Power input voltage (PVIN1, PVIN2)

Buck converter power input voltage. This is the drain of the buck converter high-side power MOSFET.

### 5.2.3 Switching node (SW1, SW2)

Buck converter switching node. This pin is connected to the output inductor.

### 5.2.4 Power ground (PGND1, PGND2)

Buck converter and discharge MOSFETs power ground. It is the source of the buck converter low-side power MOSFET.

### 5.2.5 Compensation input (COMP1, COMP2)

Buck converter external compensation network connects to this pin. Use a type III compensation network.

### 5.2.6 Error amplifier inverting input (inv1, INV2)

Buck converter error amplifier inverting input. Connect the $V_{DDQ}$ voltage (channel 1) to INV1 pin through a resistor divider and connect the $V_{TT}$ voltage (channel 2) directly to INV2 pin.

### 5.2.7 Output voltage discharge path (VOUT1, VOUT2)

Buck converters output voltage are connected to these pins. It only serves as the output discharge path once the $\overline{SD}$ signal is asserted.

### 5.2.8 Internal supply voltage output (VDDI)

This is the output of the internal bias voltage regulator. Connect a 1.0 µF, 6.0 V low ESR ceramic filter capacitor between this pin and the GND pin. Filtering any spikes on this output is essential to the internal circuitry stable operation.

### 5.2.9 Signal ground (GND)

Analog ground of the IC. Internal analog signals are referenced to this pin voltage.

### 5.2.10 Input supply voltage (VIN)

IC power supply input voltage. Input filtering is required for the device to operate properly.

### 5.2.11 Power good output signal ($\overline{PG}$)

This is an active low open drain output that is used to report the status of the device to a host. This output activates after a successful power up sequence and stays active as long as the device is in normal operation and is not experiencing any faults. This output activates after a 10 ms delay and must be pulled up by an external resistor to a supply voltage like $V_{IN}$.

### 5.2.12 Standby input ($\overline{\text{STBY}}$)

If this pin is tied to the GND pin, the device is set to standby mode. If left unconnected or tied to the VIN pin, the device is set to normal mode. The pin has an internal pull-up of 1.5 MΩ. This input accepts the S3 (suspend-to-RAM) control signal.

### 5.2.13 Shutdown input ($\overline{\text{SD}}$)

If this pin is tied to the GND pin, the device is set to shutdown Mode. If left unconnected or tied to the vin pin, the device is set to normal mode. the pin has an internal pull-up of 1.5 mω. this input accepts the s5 (Suspend-To-Disk) control signal.

### 5.2.14 Reference voltage output (VREFOUT)

This is a buffered reference voltage output that is equal to 1/2 $V_{REFIN}$. It has a 10 mA current drive capability. This output is used as the $V_{REF}$ voltage rail and should be filtered against any noise. Connect a 0.1 µF, 6.0 V low ESR ceramic filter capacitor between this pin and the GND pin and between this pin and $V_{DDQ}$ rail. $V_{REFOUT}$ is also used as the reference voltage for the buck converter error amplifier.

### 5.2.15 Reference voltage input (VREFIN)

The output of channel two tracks 1/2 the voltage applied at this pin.

### 5.2.16 Frequency adjustment input (FREQ)

The buck converters switching frequency can be adjusted by connecting this pin to an external resistor divider between VDDI and GND pins. The default switching frequency (FREQ pin connected to ground, GND) is set at 1.0 MHz.

### 5.2.17 Channel 1 soft start adjustment input (ILIM1)

Channel one soft start can be adjusted by applying a voltage between 1.25 V and $V_{DDI}$.

## 5.3 Functional internal block description

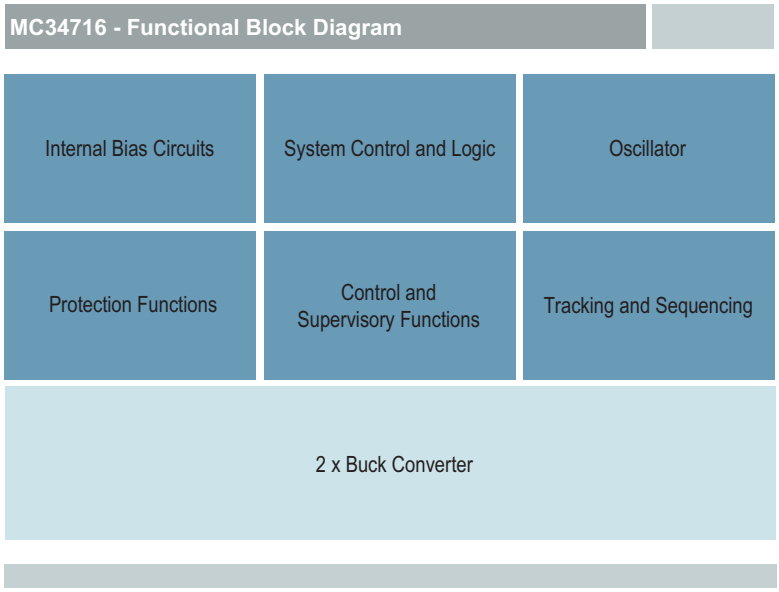



**Figure 7. Block illustration**

### 5.3.1 Internal bias circuits

This block contains all circuits that provide the necessary supply voltages and bias currents for the internal circuitry. It consists of:

- Internal voltage supply regulator: Supplies the $V_{DDI}$ voltage that is used to drive the digital/analog internal circuits. It is equipped with a Power-On-Reset (POR) circuit that watches for the right regulation levels. External filtering is needed on the VDDI pin. This block turns off during the shutdown mode.
- Internal bandgap reference voltage: Supplies the reference voltage to some of the internal circuitry.
- Bias circuit: Generates the bias currents necessary to run all of the blocks in the IC.

### 5.3.2 System control and logic

This block is the brains of the IC where the device processes data and reacts to it. Based on the status of the $\overline{\text{STBY}}$ and $\overline{\text{SD}}$ pins, the system control reacts accordingly and orders the device into the right status. It also takes inputs from all of the monitoring/protection circuits and initiates power-up or power-down commands. It communicates with the buck converter to manage the switching operation and protects it against any faults.

### 5.3.3 Oscillator

This block generates the clock cycles necessary to run the IC digital blocks. It also generates the buck converters switching frequency. The switching frequency can be programmed by connecting a resistor divider to the FREQ pin, between VDDI and GND pins (See Figure 1).

### 5.3.4 Protection functions

This block contains the following circuits:

- Overcurrent limit and short-circuit detection: Monitors the output of the buck converters for overcurrent conditions and short-circuit events and alerts the system control for further commands.
- Thermal limit detection: Monitors the temperature of the device for overheating events. If the temperature rises above the thermal shutdown threshold, this block alerts the system control for further commands.
- Output overvoltage and undervoltage monitoring: This Monitors the buck converters output voltages to ensure they are within regulation boundaries. If not, this block alerts the system control for further commands.

### 5.3.5 Control and supervisory functions

This block is used to interface with an outside host. It contains the following circuits:

- Standby control Input: An outside host can put the 34716 device into standby mode (S3 or suspend-to-RAM mode) by sending a logic “0” to the $\overline{\text{STBY}}$ pin.
- Shutdown control Input: An outside host can put the 34716 device into shutdown mode (S5 or suspend-to-disk mode) by sending a logic “0” to the $\overline{\text{SD}}$ pin.
- Power good output signal: The 34716 can communicate to an outside host that a fault has occurred by pulling the voltage on the $\overline{\text{PG}}$ pin high through a pull-up resistor.

### 5.3.6 Tracking and sequencing

This block allows the output of channel 2 of the 34716 to track 1/2 the voltage applied at the VREFIN pin. This allows the $V_{REF}$ and $V_{TT}$ voltages to track 1/2 $V_{DDQ}$ and assures that none of them are higher than $V_{DDQ}$ at any point during normal operating conditions. For power-down during a shutdown (S5) mode, the 34716 uses internal discharge MOSFETs (M8, M9, and M10 on Figure 2) to discharge $V_{DDQ}$, $V_{TT}$, and $V_{REF}$ respectively. These discharge MOSFETs are only active during shutdown mode. Using this block along with controlling the $\overline{\text{SD}}$ and $\overline{\text{STBY}}$ pins makes the device suitable for power sequencing by controlling when to turn the 34716 outputs on or off.

### 5.3.7 Buck converter

This block provides the main function of the 34716: DC to DC conversion from an un-regulated input voltage to a regulated output voltage used by the loads for reliable operation. The buck converter is a high performance, fixed frequency (externally adjustable), Synchronous buck PWM voltage-mode control with a minimum on time of 100ns. It drives integrated 50 mΩ N-channel power MOSFETs saving board space and enhancing efficiency. The switching regulator output voltage is adjustable with an accuracy of less than ±2% to meet DDR requirements. The regulator's voltage control loop is compensated using a type III compensation network, with external components to allow for optimizing the loop compensation, for a wide range of operating conditions. A typical Bootstrap circuit with an internal PMOS switch provides the voltage necessary to properly enhance the high-side MOSFET gate.

The 34716 is designed to address DDR memory power supplies. It provides a full power supply solution for DDR applications. The integrated converter has the ability to supply up to 5.0 A out of channel 1 and sink and source up to 3.0 A of continuous current from channel 2.

# 6 Functional device operation

## 6.1 Operational modes

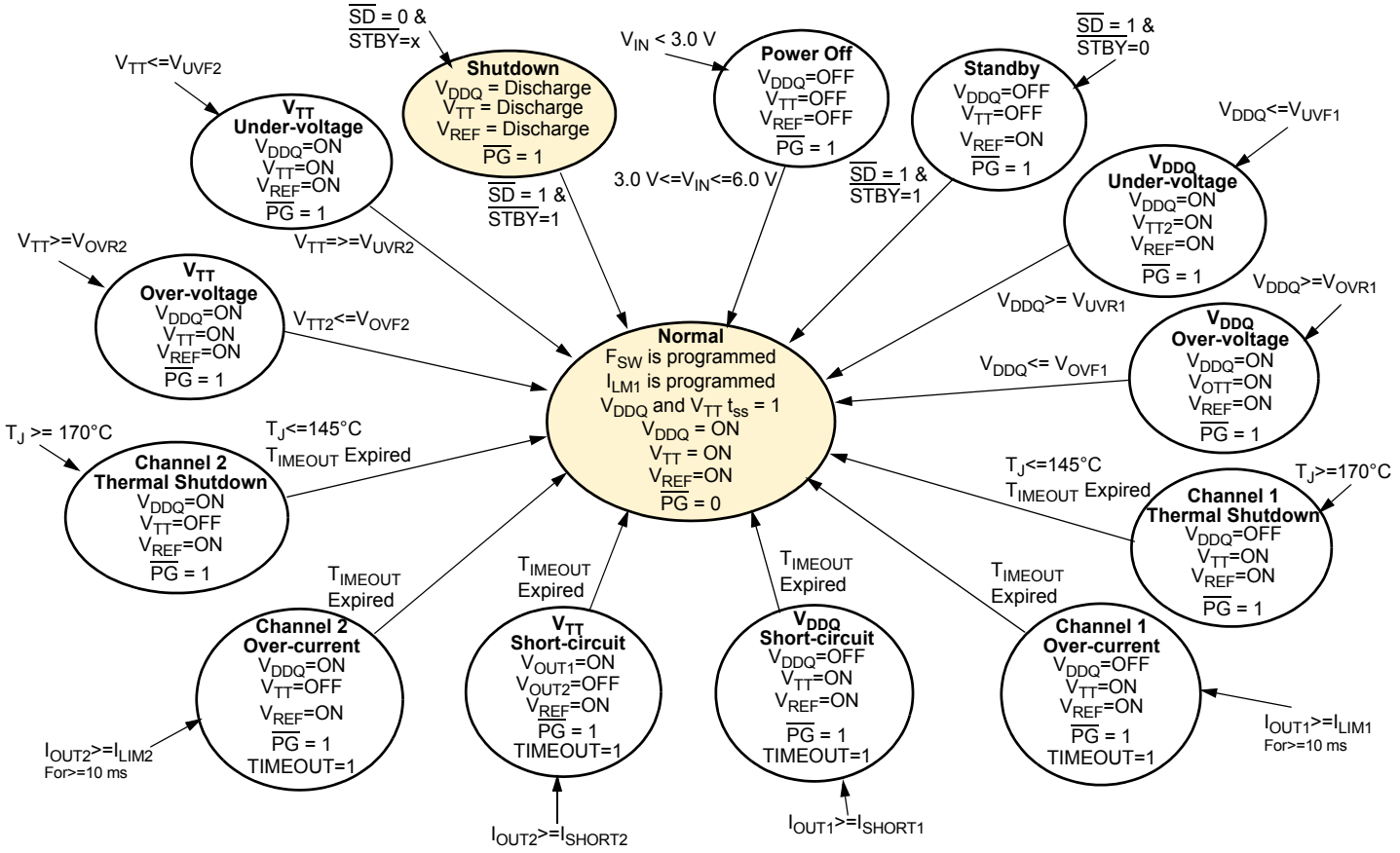



**Figure 8. Operation modes diagram**

### 6.1.1 Modes of operation

The 34716 has three primary modes of operation:

#### 6.1.1.1 Normal mode

In normal mode, all functions and outputs are fully operational. To be in this mode, the $V_{IN}$ must be within its operating range. Both shutdown and standby inputs must be pulled high, and there can be no faults present. This mode consumes the most amount of power.

#### 6.1.1.2 Standby mode

This mode is predominantly used in desktop memory solutions where the DDR supply must be ACPI compliant (advanced configuration and power interface). When this mode is activated by pulling the $\overline{STBY}$ pin low, $V_{TT}$ is put in high Z state, $I_{OUT2}$ = 0 A while $V_{DDQ}$ and $V_{REF}$ stay active. This is the S3 state suspend-to-RAM or self refresh mode and it is the lowest DRAM power state. In this mode, the DRAM preserves the data. While in this mode, the 34716 consumes less power than in the normal mode, because the buck converter and most of the internal blocks are disabled.

#### 6.1.1.3 Shutdown mode

In this mode, activated by pulling the $\overline{SD}$ pin low, the chip is in a shutdown state and the outputs are all disabled and discharged. This is the S4/S5 power state or suspend-to-disk state, where the DRAM loses all of its data content (no power supplied to the DRAM). The reason for discharging the $V_{TT}$ and $V_{REF}$ lines is to ensure that, upon exiting, the shutdown mode, $V_{TT}$ and $V_{REF}$ are lower than $V_{DDQ}$. Otherwise $V_{TT}$ could remain floating high and be higher than $V_{DDQ}$ upon powering up. In this mode, the 34716 consumes the least amount of power since almost all of the internal blocks are disabled.

### 6.1.2 Start-up sequence

When power is first applied, the 34716 checks the status of the $\overline{SD}$ and $\overline{STBY}$ pins. If the device is in a shutdown mode, no block powers up and the output does not attempt to ramp. If the device is in a standby mode, only the $V_{DDI}$ internal supply voltage and the bias currents are established and no further activities can occur. Once the $\overline{SD}$ and $\overline{STBY}$ pins are released to enable the device, the internal $V_{DDI}$ POR signal is also released. The rest of the internal blocks are enabled, and the buck converters switching frequency and the $V_{DDQ}$ Soft start values are determined by reading the FREQ and ILIM1 pins respectively. A soft start cycle is then initiated to ramp up the outputs. While channel 1 buck converter uses an internal reference, channel 2 converter error amplifier uses the voltage on the VREFOUT pin ($V_{REF}$) as its reference voltage. $V_{REF}$ is equal to 1/2 $V_{DDQ}$, where $V_{DDQ}$ is applied to the VREFIN pin. This way, the 34716 assures that $V_{REF}$ and $V_{TT}$ voltages track 1/2 $V_{DDQ}$ to meet DDR requirements.

Soft start is used to prevent the output voltage from overshooting during startup. At initial startup, the output capacitor is at zero volts; $V_{OUT}$ = 0 V. Therefore, the voltage across the inductor is $PV_{IN}$ during the capacitor charge phase which creates a very sharp di/dt ramp. Allowing the inductor current to rise too high can result in a large difference between the charging current and the actual load current. This could cause an undesired voltage spike once the capacitor is fully charged. The soft start is active each time the IC goes out of standby or shutdown mode, power is recycled or after a fault retry.

To fully take advantage of soft starting, enable the $V_{TT}$ output before introducing VDDQ on the VREFIN pin. If this happens after a soft start cycle expires and the VREFIN voltage has a high dv/dt, the output naturally tracks it immediately and ramp up with a fast dv/dt itself (which defeats the purpose of soft starting). For reliable operation, it is best to have the VDDQ voltage available before enabling the $V_{TT}$ output.

After a successful start-up cycle where the device is enabled, no faults have occurred and the output voltages have reached their regulation point, the 34716 pulls the power good output signal low after a 10 ms reset delay. This indicates to the host that the device is in normal operation.

### 6.1.3 Protection functions

The 34716 monitors the application for several fault conditions to protect the load from overstress. The reaction of the IC to these faults ranges from turning off the outputs to just alerting the host that something is wrong. In the following paragraphs, each fault condition is explained:

#### 6.1.3.1 Output overvoltage

An overvoltage condition occurs once the output voltage goes higher than the rising overvoltage threshold ($V_{OVR}$). In this case, the power good output signal is pulled high, alerting the host that a fault is present, but the outputs stay active. To avoid erroneous overvoltage conditions, a 20 µs filter is implemented. The buck converter uses its feedback loop to attempt to correct the fault. Once the output voltage falls below the falling overvoltage threshold ($V_{OVF}$), the fault is cleared and the power good output signal is pulled low. The device is then back in normal operation. The condition is the same for both outputs.

#### 6.1.3.2 Output undervoltage

An undervoltage condition occurs once the output voltage falls below the falling undervoltage threshold ($V_{UVF}$). In this case, the power good output signal is pulled high (alerting the host that a fault is present) ‘but the outputs stay active. To avoid erroneous undervoltage conditions, a 20 µs filter is implemented. The buck converter uses its feedback loop to attempt to correct the fault. Once the output voltage rises above the rising undervoltage threshold ($V_{UVR}$), the fault is cleared and the power good output signal is pulled low. The device is then back in normal operation. The condition is the same for both outputs.

### 6.1.3.3 Output overcurrent

This block detects overcurrent in the power MOSFETs of the buck converter. It is comprised of a sense MOSFET and a comparator for each channel. The sense MOSFET acts as a current detecting device by sampling a ratio of the load current. That sample is compared via the comparator with an internal reference to determine if the output is in overcurrent. If the peak current in the output inductor reaches the overcurrent limit ($I_{LIM}$), the converter starts a cycle-by-cycle operation to limit the current, and a 10 ms overcurrent limit timer ($t_{LIM}$) starts. The converter stays in this mode of operation until one of the following occurs:

- The current is reduced back to the normal level before $t_{LIM}$ expires. In this case normal operation is regained.
- $t_{LIM}$ expires without regaining normal operation, at which point the device turns off the output and the power good output signal is pulled high. At the end of a timeout period of 100 ms ($t_{TIMEOUT}$), the device attempts another soft start cycle.
- The device reaches the thermal shutdown limit ($T_{SDFET}$) and turns off the output. The power good ($\overline{PG}$) output signal is pulled high.
- The output current keeps increasing until it reaches the short-circuit current limit ($I_{SHORT}$). See below for more details.

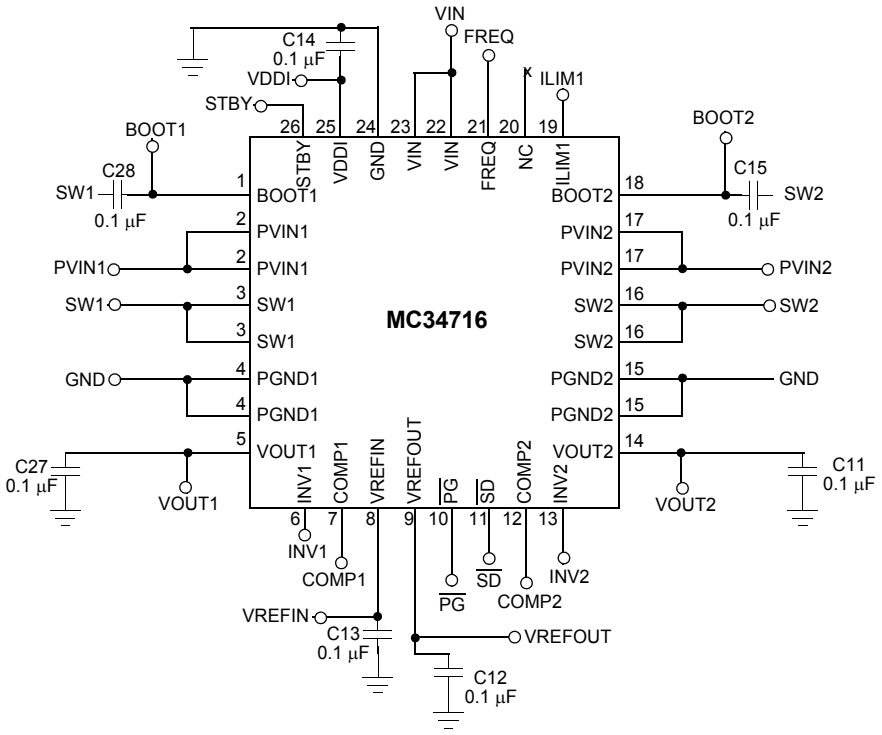
### 6.1.3.4 Short-circuit current limit

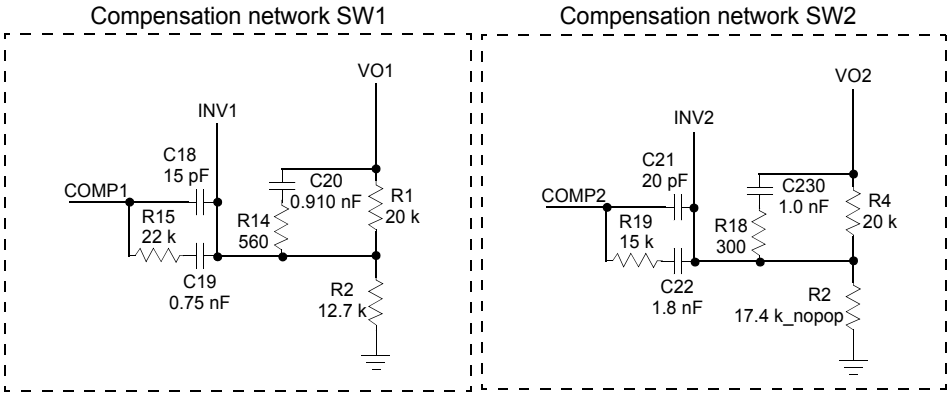
This block uses the same current detection mechanism as the overcurrent limit detection block. If the load current reaches the $I_{SHORT}$ value, the device reacts by shutting down the output immediately. This is necessary to prevent damage in case of a permanent short-circuit. Then, at the end of a timeout period of 100 ms ($t_{TIMEOUT}$), the device attempts another soft start cycle.

### 6.1.3.5 Thermal shutdown

Each channel has its own thermal shutdown block. Thermal limit detection block monitors the temperature of the device and protects against excessive heating. If the temperature reaches the thermal shutdown threshold ($T_{SDFET}$), the converter output switches off and the power good output signal indicates a fault by pulling high. The device stays in this state until the temperature has decreased by the hysteresis value and then after a timeout period ($t_{TIMEOUT}$) of 100 ms, the device automatically retries and the output goes through a soft start cycle. If successful normal operation is regained, the power good output signal is asserted low.

# 7 Typical applications



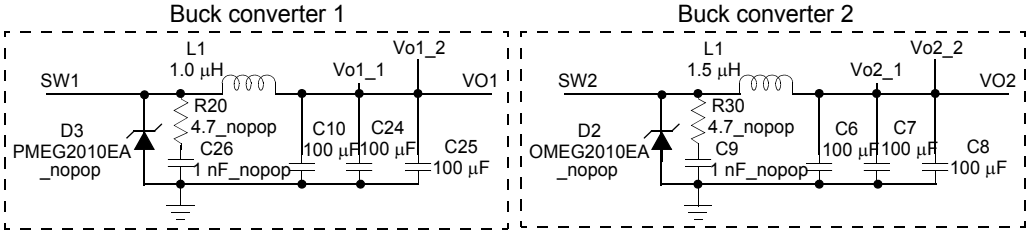




**Figure 9. Typical application**

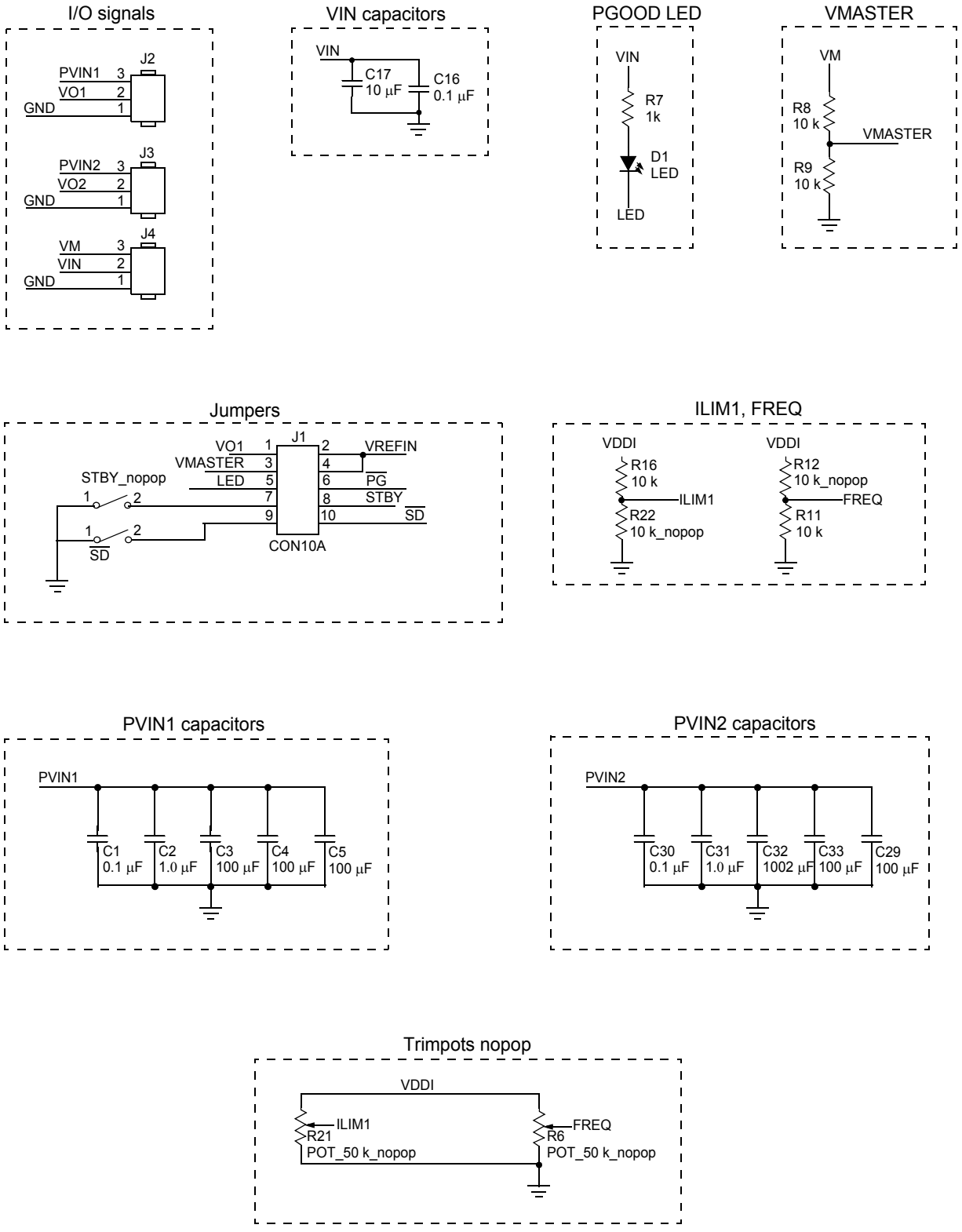



**Figure 10. Typical application**

## 7.1 Configuring the output voltage:

Channel 1 of the 34716 is a general purpose DC-DC converter. The resistor divider to the -INV1 node is responsible for setting the output voltage, according to the following equation:

$$V_{OUT} = V_{REF}\left(\frac{R1}{R2} + 1\right)$$

Where $V_{REF}$ is the internal $V_{BG}$=0.7 V.

Channel 2 is a DDR specific voltage power supply, and the output voltage is given by the equation:

$$V_{TT} = \frac{V_{REFIN}}{2}$$

Where $V_{REFIN}$ is equal to $V_{DDQ}$.

## 7.2 Switching frequency configuration

The switching frequency has a value of 1.0 MHz when the FREQ pin is connected to the GND. If the smallest frequency value of 200 kHz is desired, then connect the FREQ pin to VDDI. To program the switching frequency to another value, an external resistor divider must be connected to the FREQ pin to achieve the voltages given by Table 7.3.

## 7.3 Frequency selection

| Frequency | Voltage applied to pin FREQ |
|---|---|
| 200 | 2.341 – 2.500 |
| 253 | 2.185 – 2.340 |
| 307 | 2.029 – 2.184 |
| 360 | 1.873 – 2.028 |
| 413 | 1.717 – 1.872 |
| 466 | 1.561 – 1.716 |
| 520 | 1.405 – 1.560 |
| 573 | 1.249 – 1.404 |
| 627 | 1.093 – 1.248 |
| 680 | 0.936 – 1.092 |
| 733 | 0.781 – 0.936 |
| 787 | 0.625 – 0.780 |
| 840 | 0.469 – 0.624 |
| 893 | 0.313 – 0.468 |
| 947 | 0.157 – 0.312 |
| 1000 | 0.000 – 0.156 |

## 7.4 Soft start adjustment

Table 6 shows the voltage that should be applied to the ILIM1 pin to get the desired sort start timing on channel 1 only.

**Table 6. Soft start configurations**

| Soft start [ms] | Voltage applied to ILIM |
|---|---|
| 3.2 | 1.19 – 1.49 V |
| 1.6 | 1.50 – 1.81 V |
| 0.8 | 1.82 – 2.13 V |
| 0.4 | 2.14 – 2.50 V |

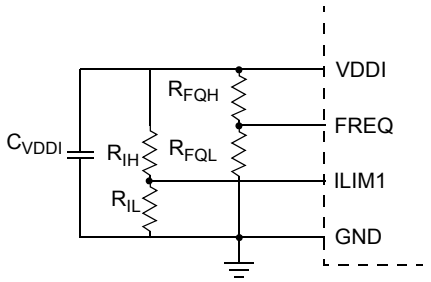



**Figure 11. Resistor divider for frequency and soft ftart adjustment**

## 7.5 Selecting inductor

Inductor calculation process is the same for both channels. The equation is the following:

$$L = D'_{MAX} * T * \frac{(V_{out} + I_{out} * (Rds(on)_ls + r_w))}{\Delta I_{out}}$$

| | |
|---|---|
| $D'_{MAX} = 1 - \frac{V_{out}}{Vin_\max}$ | Maximum Off Time Percentage |
| $T$ | Switching Period |
| $Rds(on)_ls$ | Drain – to – Source Resistance of FET |
| $r_w$ | Winding Resistance of Inductor |
| $\Delta I_{OUT} = 0.4 * I_{OUT}$ | Output Current Ripple |

If channel 1 is serving as the power supply for channel 2, locate the LC poles at different frequencies in order to ensure that the input impedance of the second converter is always higher than the output impedance of the first converter (thus ensuring system stability). This is achieved by selecting different values for L1 and L2 slightly higher than the calculated value.

## 7.6 Selecting the output filter capacitor

For the output capacitor, the following considerations are most important and not the actual Farad value: the physical size, the ESR of the capacitor and the voltage rating.

Calculate the minimum output capacitor using the following formula:

$$Co = \frac{I_{OUT} * dt_I_rise}{TR_V_dip}$$

Transient response percentage:
TR_%
(Use a recommended value of 2 to 4% to assure a good transient response.)

Maximum transient voltage:
TR_V_dip = $V_{OUT}$*TR_%

Maximum current step:

$$\Delta Iout_step = \frac{(Vin_\min - Vout) * D_\max}{Fsw * L}$$

Inductor current rise time:

$$dt_I_rise = \frac{T * I_{OUT}}{\Delta I_{OUT}_step}$$

The following formula are helpful for finding the maximum allowed ESR.

$$ESR_{\max} = \frac{\Delta V_{OUT} * Fsw * L}{V_{OUT}(1 - D\min)}$$

The effects of the ESR is often neglected by the designers and may present a hidden danger to the ultimate supply stability. Poor quality capacitors have widely disparate ESR values, which can make the closed loop response inconsistent.

## 7.7 Bootstrap capacitor

The bootstrap capacitor is needed to supply the gate voltage for the high-side MOSFET. This N-channel MOSFET needs a voltage difference between its gate and source to be able to turn on. The high-side MOSFET source is the SW node, so it is not at ground and it is floating and shifting in voltage. Applying a voltage directly to the gate of the high-side that is referenced to ground is not sufficient. Instead, the voltage must be referenced to the SW node. This is why the bootstrap capacitor is needed. This capacitor charges during the high- side off time. Since the low-side is on during that time, the SW node and the bottom of the bootstrap capacitor are connected to ground, and the top of the capacitor is connected to a voltage source. The capacitor charges up to that voltage source (for example 5.0 V). Now when the low- side MOSFET switches off and the high-side MOSFET switches on, the SW nodes rise to $V_{IN}$, and the voltage on the boot pin becomes $V_{CAP}$ + $V_{IN}$. The gate of the high-side has $V_{CAP}$ across it and can stay enhanced. A 0.1 μf capacitor is a good value for this bootstrap element.

## 7.8 Type III compensation network

To meet contemporary demands, power supplies must often offer accurate and tight output voltage regulation. A high DC gain is required to accomplish this. However, high gain increases the possibility of instability in the power supply. To minimize the threat of power supply instability, compensation is added to the internal error amplifier to counteract some of the gains and phases contained in the control-to-output transfer function. The Type III compensation network used for 34716 is comprised of two poles: One integrator and one high frequency to cancel the zero generated from the ESR of the output capacitor and two zeros to cancel the two poles generated from the LC filter as shown in Figure 12.

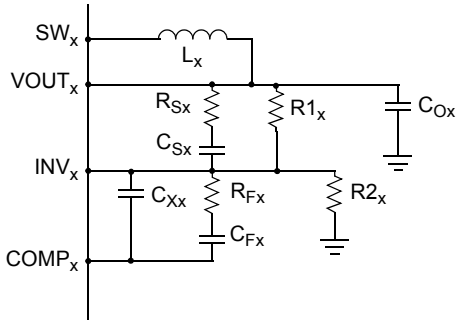



**Figure 12. Type III compensation network**

1. Choose a value for R1 (R2 only applies to channel 1).
2. Consider a crossover frequency of one tenth the switching frequency. Set the zero pole frequency to Fcross/10.

$$F_{P0} = \frac{1}{10} F_{CROSS} = \frac{1}{2\pi * R_1 C_F}$$

$$C_F = \frac{1}{2\pi * R_1 F_{PO}}$$

3. Knowing the LC frequency, the frequency of zero 1 and zero 2 in the compensation network is equal to $F_{LC}$.

$$F_{LC} = \frac{1}{2\pi\sqrt{L_X C_{OX}}} = F_{Z1} = F_{Z2}$$

$$F_{Z1} = \frac{1}{2\pi * R_F C_F} \qquad F_{Z2} = \frac{1}{2\pi * R_1 C_S}$$

This gives the following result:

$$R_F = \frac{1}{2\pi * C_F F_{Z1}} \qquad C_S = \frac{1}{2\pi * R_1 F_{Z2}}$$

4. Calculate $R_S$ by placing the first pole at the ESR zero frequency.

$$F_{ESR} = \frac{1}{2\pi * Co_X * ESR} = F_{P1}$$

$$F_{P1} = \frac{1}{2\pi * R_S C_S} \longrightarrow R_S = \frac{1}{2\pi * F_{P1} C_S}$$

5. Equating pole 2 to 5 times the crossover frequency to achieve a faster response and a proper phase margin:

$$5 \bullet F_{CROSS} = F_{P2} = \frac{1}{2\pi \bullet R_F \frac{C_F C_X}{C_F + C_x}} \longrightarrow$$

$$C_X = \frac{C_F}{2\pi * R_F C_F F_{P2} - 1}$$

## 7.9 Tracking configurations

The 34716 allows default Ratiometric tracking on channel 2 by connecting VDDQ to the VREFIN pin. It has an internal resistor divider that allows an output of VDDQ/2.

## 7.10 Layout guidelines

The layout of any switching regulator requires careful consideration. First, there are high di/dt signals present, and the traces carrying these signals need to be kept as short and as wide as possible to minimize the trace inductance and therefore reduce the voltage spikes they can create. To do this, requires an understanding of the major current carrying loops. See Figure 13. Place these loops and their associated components in a way that minimizes the loop size and prevents coupling to other parts of the circuit. Also, to minimize noise coupling, route the current-carrying power traces and their associated return traces so that they run adjacent to one another. If sensitive traces must cross the current carrying traces, place them perpendicular to one another to reduce field interaction.

Second, carefully consider the placement of small signal components that connect to sensitive nodes. The critical small signal components are the ones associated with the feedback circuit. The high-impedance input of the error amp is especially sensitive to noise, and the feedback. So place compensation components as far from the switch node and as close to the input of the error amplifier as possible. Other critical small signal components include the bypass capacitors for VIN, VREFIN, and VDDI. Locate the bypass capacitors as close to the pin as possible.

The use of a multi-layer printed circuit board is recommended. Dedicate one layer, usually the layer under the top layer, as a ground plane. Make all critical component ground connections with vias to this layer. Make sure that the power grounds (PGND1 and PGND2) are connected directly to the ground plane and not routed through the thermal pad or analog ground. Dedicate another layer as a power plane and split this plane into local areas for common voltage nets.

Use a dedicated trace to connect the IC input supply (VIN) to the input supply. This prevents noise on the buck regulator's power inputs (PVIN1 and PVIN2) from injecting switching noise into the IC’s analog circuitry.

In order to effectively transfer heat from the top layer to the ground plane and other layers of the printed circuit board, thermal vias must be used in the thermal pad design. Five to nine vias should be spaced evenly and have a finished diameter of 0.3 mm.

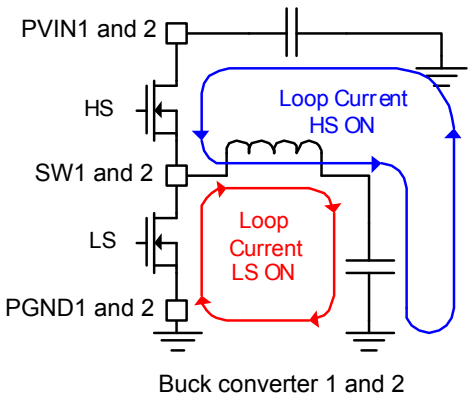
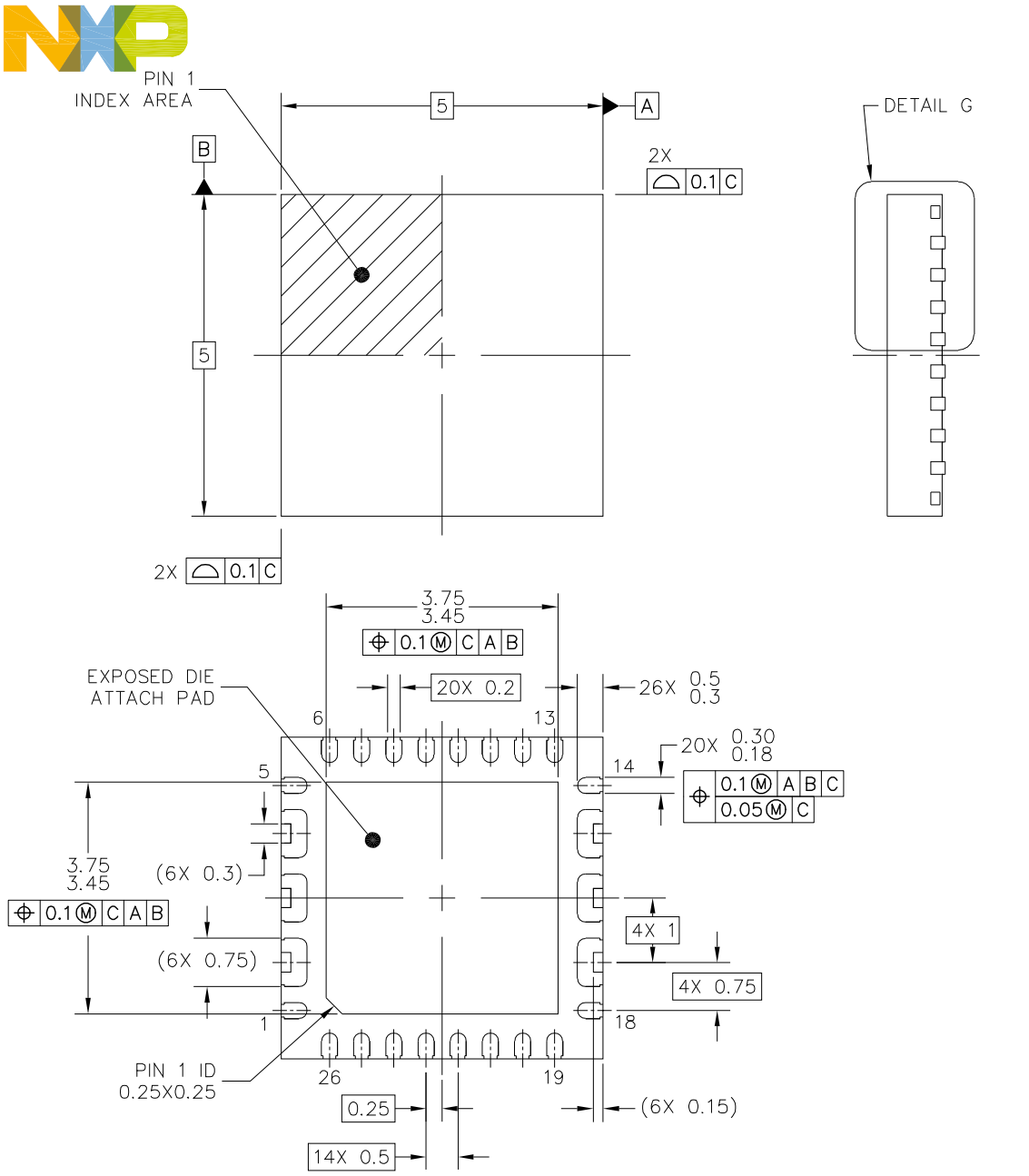



**Figure 13. Current loop**

# 8 Packaging

## 8.1 Packaging dimensions

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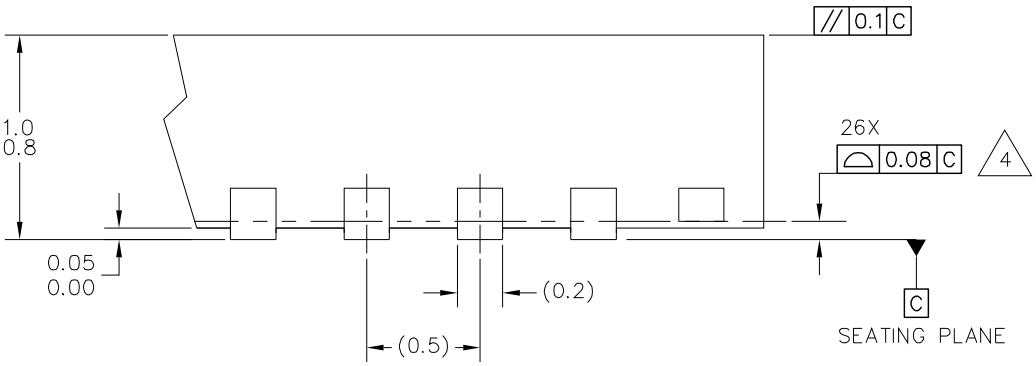


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NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. THIS IS A NON–JEDEC REGISTERED PACKAGE.
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**34716**

# 9 Revision history

| Revision | Date | Description of Changes |
|---|---|---|
| 1.0 | 2/2006 | • Pre-release version<br>• Implemented Revision History page |
| 2.0 | 2/2007 | • Initial release<br>• Converted format from Market Assessment to Product Preview<br>• Major updates to the data, form, and style |
| 3.0 | 5/2007 | • Changed Feature from 2% to 1%, relabeled to include soft start<br>• Change references for 45 mΩ Integrated N-Channel Power MOSFETs to 50 mΩ<br>• Removed Machine Model in Maximum ratings<br>• Changed Input DC supply current, Input DC supply current, and Input DC supply current<br>• Added CH 1 high-side MOSFET drain voltage range<br>• Changed Output voltage accuracy<br>• Changed Soft start adjusting reference voltage range and Short-circuit current limit<br>• Changed High-side N-CH power MOSFET (M4) RDS(on) and Low-side N-CH power MOSFET (M5) RDS(on)<br>• Changed M2 RDS(on) and PVIN1 pin leakage current<br>• Added CH 2 high-side MOSFET drain voltage range<br>• Changed Output voltage accuracy<br>• Changed Short-circuit current limit (sinking and sourcing)<br>• Changed High-side N-CH power MOSFET (M6) RDS(on) and Low-side N-CH power MOSFET (M7) RDS(on)<br>• Changed M3 RDS(on) and PVIN2 pin leakage current (standby and shutdown modes)<br>• Changed VREFOUT buffered reference voltage accuracy, VREFOUT buffered reference voltage current capability, and VREFOUT buffered reference voltage overcurrent limit<br>• Changed STBY pin internal pull-up resistor and SD pin internal pull-up resistor<br>• Changed Soft start duration (normal mode)<br>• Changed Overcurrent limit retry timeout period and Output undervoltage/overvoltage filter delay timer<br>• Changed Oscillator default switching frequency (FREQ = GND), PG reset delay, and Thermal shutdown retry timeout period<br>• Changed definition for Channel 1 soft start adjustment input (ILIM1)<br>• Changed drawings in Typical application<br>• Changed table for Soft start adjustment<br>• Removed PC34716EP/R2 from the ordering information and added MC34716EP/R2<br>• Changed data sheet status to Advance Information |
| 4.0 | 12/2008 | • Made changes to Switching Node (SW1, SW2) Pins, BOOT1, BOOT2 pins (referenced to SW1, SW2 pins respectively), Output undervoltage threshold, Output overvoltage threshold, Both channels of High-side N-CH power MOSFET (M4) RDS(on), Both channels of Low-side N-CH power MOSFET (M5) RDS(on), Charge device model<br>• Added Machine model (MM), Both channels of SW2 leakage current (standby and shutdown modes), Both channels of (Error amplifier DC gain, Error amplifier unit gain bandwidth, Error amplifier slew rate, Error amplifier input offset)<br>• Fixed drawing for Type III compensation network<br>• Added pin 27 to Figure 3 and the Pin definitions<br>• Added the section Layout guidelines |
| 5.0 | 4/2012 | • Changed typical for Minimum on time 11 |
| 6.0 | 12/2014 | • Updated case outline (changed 98ASA10728D to 98ASA00702D) as per PCN 16331 |
| 7.0 | 3/2015 | • Added note (19) to Static electrical characteristics |
| 8.0 | 4/2016 | • Minimum output voltage for Channel 2 extended to 0.6 V<br>• Updated document style and format |

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