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# **FDG6335N**

# 20V N-Channel PowerTrench® MOSFET

#### **General Description**

This N-Channel MOSFET has been designed specifically to improve the overall efficiency of DC/DC converters using either synchronous or conventional switching PWM controllers. It has been optimized use in small switching regulators, providing an extremely low  $R_{\text{DS}(\text{ON})}$  and gate charge  $(Q_{\text{G}})$  in a small package.

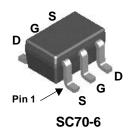
#### **Applications**

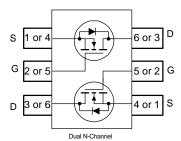
- DC/DC converter
- · Power management
- Loadswitch

#### **Features**

• 0.7 A, 20 V.  $R_{DS(ON)} = 300 \text{ m}\Omega \ @ \ V_{GS} = 4.5 \text{ V}$   $R_{DS(ON)} = 400 \text{ m}\Omega \ @ \ V_{GS} = 2.5 \text{ V}$ 

- Low gate charge (1.1 nC typical)
- High performance trench technology for extremely low  $R_{\mbox{\scriptsize DS(ON)}}$
- Compact industry standard SC70-6 surface mount package





The pinouts are symmetrical; pin 1 and pin 4 are interchangeable.

## Absolute Maximum Ratings T<sub>A</sub>=25°C unless otherwise noted

Symbol	Parameter		Ratings	Units
V <sub>DSS</sub>	Drain-Source Voltage		20	V
V <sub>GSS</sub>	Gate-Source Voltage		± 12	V
I <sub>D</sub>	Drain Current - Continuous	(Note 1)	0.7	А
	- Pulsed		2.1	
P <sub>D</sub>	Power Dissipation for Single Operation	(Note 1)	0.3	W
T <sub>J</sub> , T <sub>STG</sub>	Operating and Storage Junction Temperature Range		-55 to +150	°C

## **Thermal Characteristics**

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1)	415	°C/W
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**Package Marking and Ordering Information** 

Device Marking	Device	Reel Size	Tape width	Quantity
.35	FDG6335N	7"	8mm	3000 units

Symbol	Parameter	Test Conditions	Min	Тур	Max	Units
Off Char	acteristics		II.			l
BV <sub>DSS</sub>	Drain–Source Breakdown Voltage	$V_{GS} = 0 \text{ V}, \qquad I_D = 250  \mu\text{A}$	20			V
$\Delta BV_{DSS} \over \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D$ = 250 $\mu$ A, Referenced to 25°C		14		mV/°C
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> = 16 V, V <sub>GS</sub> = 0 V			1	μΑ
I <sub>GSSF</sub>	Gate-Body Leakage, Forward	$V_{GS} = 12 \text{ V},  V_{DS} = 0 \text{ V}$			100	nA
I <sub>GSSR</sub>	Gate-Body Leakage, Reverse	$V_{GS} = -12 \text{ V},  V_{DS} = 0 \text{ V}$			-100	nA
On Chara	acteristics (Note 2)		•		•	
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$ , $I_D = 250 \mu\text{A}$	0.6	1.1	1.5	V
$\Delta V_{GS(th)} \over \Delta T_J$	Gate Threshold Voltage Temperature Coefficient	$I_D = -250 \mu A$ , Referenced to 25°C		-2.8		mV/°C
R <sub>DS(on)</sub>	Static Drain–Source On–Resistance	$ \begin{array}{cccccccccccccccccccccccccccccccccccc$		180 293 247	300 400 442	mΩ
I <sub>D(on)</sub>	On-State Drain Current	$V_{GS} = 4.5 \text{ V},  I_D = 0.7 \text{ A}, T_J=125^{\circ}\text{C}$ $V_{GS} = 4.5 \text{ V},  V_{DS} = 5 \text{ V}$	1			Α
<b>g</b> FS	Forward Transconductance	$V_{DS} = 5 \text{ V}, \qquad I_{D} = 0.7 \text{ A}$		2.8		S
Dynamic	Characteristics					
C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> = 10 V, V <sub>GS</sub> = 0 V,		113		pF
Coss	Output Capacitance	f = 1.0 MHz		34		pF
C <sub>rss</sub>	Reverse Transfer Capacitance			16		pF
Switching	Characteristics (Note 2)					
t <sub>d(on)</sub>	Turn-On Delay Time	$V_{DD} = 10 \text{ V},  I_D = 1 \text{ A},$		5	10	ns
t <sub>r</sub>	Turn-On Rise Time	$V_{GS} = 4.5 \text{ V}, R_{GEN} = 6 \Omega$		7	15	ns
t <sub>d(off)</sub>	Turn-Off Delay Time			9	18	ns
t <sub>f</sub>	Turn-Off Fall Time			1.5	3	ns
$Q_g$	Total Gate Charge	$V_{DS} = 10 \text{ V},  I_{D} = 0.7 \text{ A},$		1.1	1.4	nC
Q <sub>gs</sub>	Gate-Source Charge	V <sub>GS</sub> = 4.5 V		0.24		nC
$Q_{gd}$	Gate-Drain Charge			0.3		nC
Drain-Sc	ource Diode Characteristics	and Maximum Ratings				
Is	Maximum Continuous Drain-Sour	<u> </u>			0.25	Α
$V_{SD}$	Drain–Source Diode Forward Voltage	$V_{GS} = 0 \text{ V}, \qquad I_S = 0.25 \text{ A} \text{ (Note 2)}$		0.74	1.2	V

#### Notes

<sup>1.</sup>  $R_{\theta JA}$  is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta JA}$  is determined by the user's board design.  $R_{\theta JA} = 415^{\circ}\text{C/W}$  when mounted on a minimum pad.

<sup>2.</sup> Pulse Test: Pulse Width < 300µs, Duty Cycle < 2.0%

## **Typical Characteristics**

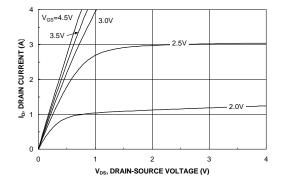


Figure 1. On-Region Characteristics.

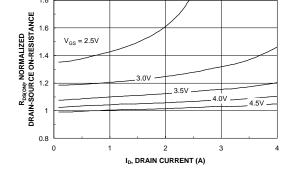


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

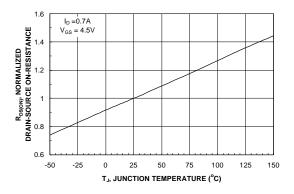


Figure 3. On-Resistance Variation with Temperature.

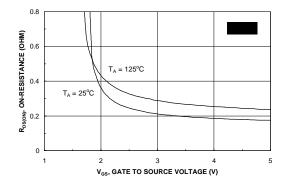


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

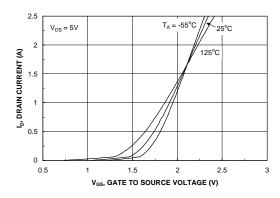


Figure 5. Transfer Characteristics.

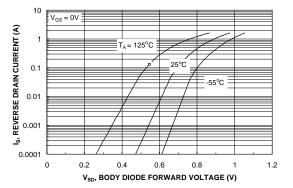
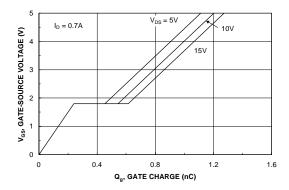


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

# **Typical Characteristics**



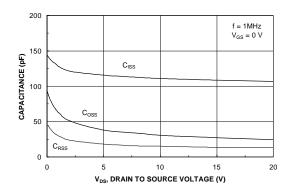
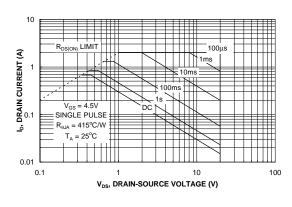


Figure 7. Gate Charge Characteristics.





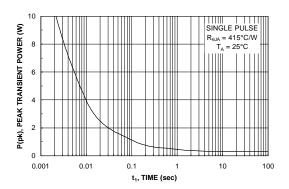


Figure 9. Maximum Safe Operating Area.

Figure 10. Single Pulse Maximum Power Dissipation.

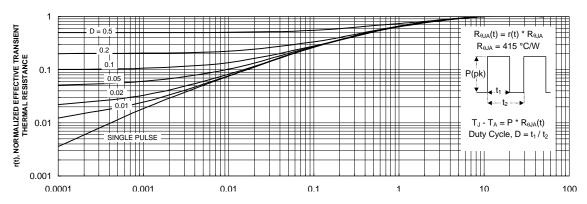


Figure 11. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1. Transient thermal response will change depending on the circuit board design.

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