

74AHC273-Q100; 74AHCT273-Q100

Octal D-type flip-flop with reset; positive-edge trigger

Rev. 1 — 27 March 2013

Product data sheet

1. General description

The 74AHC273-Q100; 74AHCT273-Q100 is a high-speed Si-gate CMOS device and is pin compatible with Low-power Schottky TTL (LSTTL). It is specified in compliance with JEDEC standard No. 7-A.

The 74AHC273-Q100; 74AHCT273-Q100 has eight edge-triggered, D-type flip-flops with individual D inputs and Q outputs.

The common clock (CP) and master reset (\overline{MR}) inputs, load and reset (clear) all flip-flops simultaneously. The state of each D input, one set-up time before the LOW-to-HIGH clock transition, is transferred to the corresponding output (Qn) of the flip-flop.

All outputs are forced LOW, independent of clock or data inputs, by a LOW on the \overline{MR} input.

The device is useful for applications where only the true output is required and the clock and master reset are common to all storage elements.

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 1) and is suitable for use in automotive applications.

2. Features and benefits

- Automotive product qualification in accordance with AEC-Q100 (Grade 1)
 - ◆ Specified from $-40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$ and from $-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$
- Balanced propagation delays
- All inputs have Schmitt-trigger actions
- Inputs accept voltages higher than V_{CC}
- Ideal buffer for MOS microcontroller or memory
- Common clock and master reset
- Input levels:
 - ◆ For 74AHC273-Q100: CMOS level
 - ◆ For 74AHCT273-Q100: TTL level
- ESD protection:
 - ◆ MIL-STD-883, method 3015 exceeds 2000 V
 - ◆ HBM JESD22-A114F exceeds 2000 V
 - ◆ MM JESD22-A115-A exceeds 200 V (C = 200 pF, R = 0 Ω)
- Multiple package options

3. Ordering information

Table 1. Ordering information

| Type number | Package | | | Version |
|-----------------------|-------------------|----------|--|----------|
| | Temperature range | Name | Description | |
| 74AHC273-Q100 | | | | |
| 74AHC273D-Q100 | -40 °C to +125 °C | SO20 | plastic small outline package; 20 leads; body width 7.5 mm | SOT163-1 |
| 74AHC273PW-Q100 | -40 °C to +125 °C | TSSOP20 | plastic thin shrink small outline package; 20 leads; body width 4.4 mm | SOT360-1 |
| 74AHC273BQ-Q100 | -40 °C to +125 °C | DHVQFN20 | plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 20 terminals; body 2.5 × 4.5 × 0.85 mm | SOT764-1 |
| 74AHCT273-Q100 | | | | |
| 74AHCT273D-Q100 | -40 °C to +125 °C | SO20 | plastic small outline package; 20 leads; body width 7.5 mm | SOT163-1 |
| 74AHCT273PW-Q100 | -40 °C to +125 °C | TSSOP20 | plastic thin shrink small outline package; 20 leads; body width 4.4 mm | SOT360-1 |
| 74AHCT273BQ-Q100 | -40 °C to +125 °C | DHVQFN20 | plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 20 terminals; body 2.5 × 4.5 × 0.85 mm | SOT764-1 |

4. Functional diagram



Fig 1. Logic symbol



Fig 2. IEC logic symbol



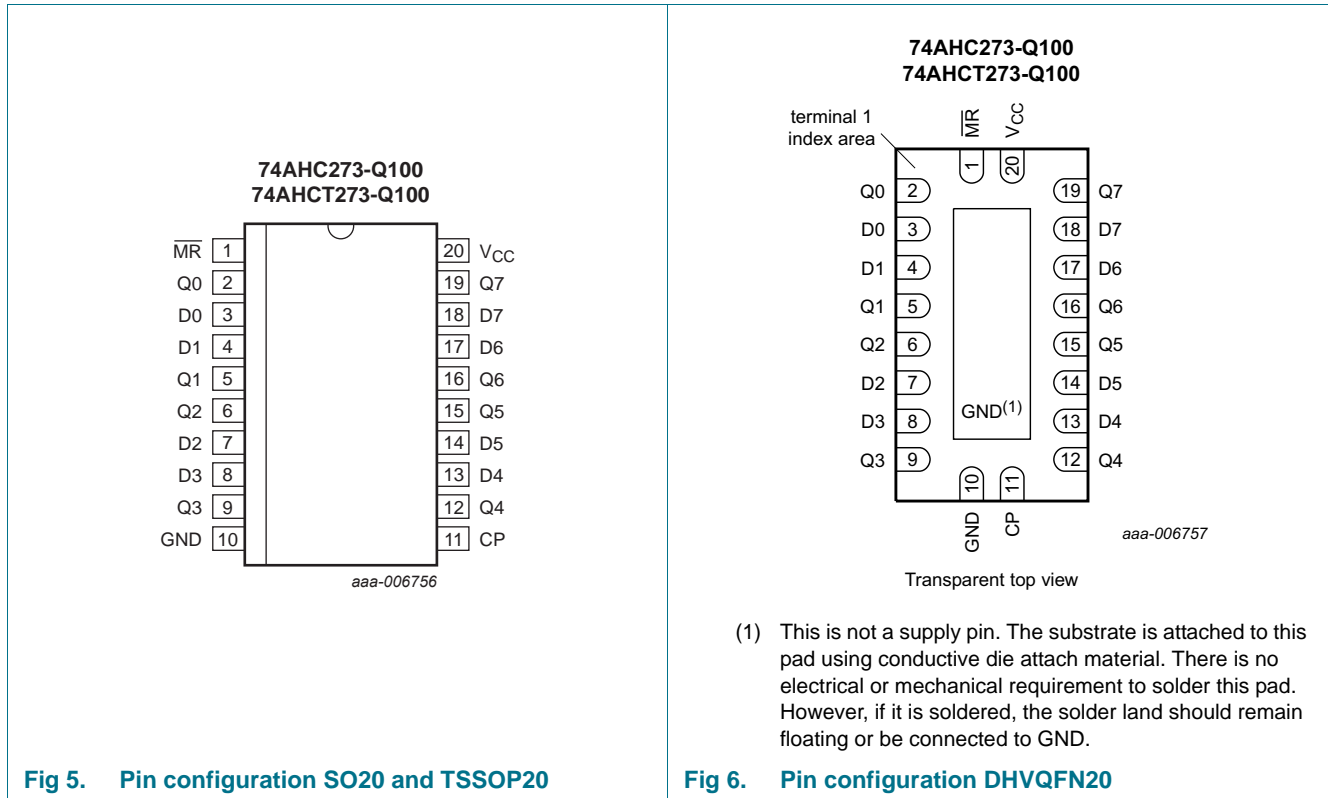
Fig 3. Logic diagram



Fig 4. Functional diagram

5. Pinning information

5.1 Pinning



5.2 Pin description

Table 2. Pin description

| Symbol | Pin | Description |
|--------------------------------|----------------------------|--|
| $\overline{\text{MR}}$ | 1 | master reset input (active LOW) |
| Q0, Q1, Q2, Q3, Q4, Q5, Q6, Q7 | 2, 5, 6, 9, 12, 15, 16, 19 | flip-flop output |
| D0, D1, D2, D3, D4, D5, D6, D7 | 3, 4, 7, 8, 13, 14, 17, 18 | data input |
| GND | 10 | ground (0 V) |
| CP | 11 | clock input (LOW-to-HIGH edge-triggered) |
| V _{CC} | 20 | supply voltage |

6. Functional description

Table 3. Function table^[1]

| Operating mode | Control | | Input | Output |
|----------------|------------------------|----|-------|--------|
| | $\overline{\text{MR}}$ | CP | Dn | Qn |
| Reset (clear) | L | X | X | L |
| Load '1' | H | ↑ | h | H |
| Load '0' | H | ↑ | l | L |

- [1] H = HIGH voltage level;
 h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition;
 L = LOW voltage level;
 l = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition;
 ↑ = LOW-to-HIGH;
 X = don't care.

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

| Symbol | Parameter | Conditions | Min | Max | Unit |
|-----------|-------------------------|--|--------------------|------|------|
| V_{CC} | supply voltage | | -0.5 | +7.0 | V |
| V_I | input voltage | | -0.5 | +7.0 | V |
| I_{IK} | input clamping current | $V_I < -0.5 \text{ V}$ | ^[1] -20 | - | mA |
| I_{OK} | output clamping current | $V_O < -0.5 \text{ V}$ or $V_O > V_{CC} + 0.5 \text{ V}$ | ^[1] -20 | +20 | mA |
| I_O | output current | $V_O = -0.5 \text{ V}$ to $(V_{CC} + 0.5 \text{ V})$ | -25 | +25 | mA |
| I_{CC} | supply current | | - | +75 | mA |
| I_{GND} | ground current | | -75 | - | mA |
| T_{stg} | storage temperature | | -65 | +150 | °C |
| P_{tot} | total power dissipation | $T_{amb} = -40 \text{ °C}$ to $+125 \text{ °C}$ | ^[2] - | 500 | mW |

- [1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

- [2] For SO20 packages: above 70 °C the value of P_{tot} derates linearly at 8 mW/K.
 For TSSOP20 packages: above 60 °C the value of P_{tot} derates linearly at 5.5 mW/K.
 For DHVQFN20 packages: above 60 °C the value of P_{tot} derates linearly at 4.5 mW/K.

8. Recommended operating conditions

Table 5. Operating conditions

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-----------------------|-------------------------------------|---|-----|-----|----------|------|
| 74AHC273-Q100 | | | | | | |
| V_{CC} | supply voltage | | 2.0 | 5.0 | 5.5 | V |
| V_I | input voltage | | 0 | - | 5.5 | V |
| V_O | output voltage | | 0 | - | V_{CC} | V |
| T_{amb} | ambient temperature | | -40 | +25 | +125 | °C |
| $\Delta t/\Delta V$ | input transition rise and fall rate | $V_{CC} = 3.0\text{ V to }3.6\text{ V}$ | - | - | 100 | ns/V |
| | | $V_{CC} = 4.5\text{ V to }5.5\text{ V}$ | - | - | 20 | ns/V |
| 74AHCT273-Q100 | | | | | | |
| V_{CC} | supply voltage | | 4.5 | 5.0 | 5.5 | V |
| V_I | input voltage | | 0 | - | 5.5 | V |
| V_O | output voltage | | 0 | - | V_{CC} | V |
| T_{amb} | ambient temperature | | -40 | +25 | +125 | °C |
| $\Delta t/\Delta V$ | input transition rise and fall rate | $V_{CC} = 4.5\text{ V to }5.5\text{ V}$ | - | - | 20 | ns/V |

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

| Symbol | Parameter | Conditions | 25 °C | | | -40 °C to +85 °C | | -40 °C to +125 °C | | Unit |
|----------------------|---|---|-------|------|------|------------------|------|-------------------|------|------|
| | | | Min | Typ | Max | Min | Max | Min | Max | |
| 74AHC273-Q100 | | | | | | | | | | |
| V_{IH} | HIGH-level input voltage | $V_{CC} = 2.0\text{ V}$ | 1.5 | - | - | 1.5 | - | 1.5 | - | V |
| | | $V_{CC} = 3.0\text{ V}$ | 2.1 | - | - | 2.1 | - | 2.1 | - | V |
| | | $V_{CC} = 5.5\text{ V}$ | 3.85 | - | - | 3.85 | - | 3.85 | - | V |
| V_{IL} | LOW-level input voltage | $V_{CC} = 2.0\text{ V}$ | - | - | 0.5 | - | 0.5 | - | 0.5 | V |
| | | $V_{CC} = 3.0\text{ V}$ | - | - | 0.9 | - | 0.9 | - | 0.9 | V |
| | | $V_{CC} = 5.5\text{ V}$ | - | - | 1.65 | - | 1.65 | - | 1.65 | V |
| V_{OH} | HIGH-level output voltage | $V_I = V_{IH}$ or V_{IL} | | | | | | | | |
| | | $I_O = -50\ \mu\text{A}; V_{CC} = 2.0\text{ V}$ | 1.9 | 2.0 | - | 1.9 | - | 1.9 | - | V |
| | | $I_O = -50\ \mu\text{A}; V_{CC} = 3.0\text{ V}$ | 2.9 | 3.0 | - | 2.9 | - | 2.9 | - | V |
| | | $I_O = -50\ \mu\text{A}; V_{CC} = 4.5\text{ V}$ | 4.4 | 4.5 | - | 4.4 | - | 4.4 | - | V |
| | | $I_O = -4.0\text{ mA}; V_{CC} = 3.0\text{ V}$ | 2.58 | - | - | 2.48 | - | 2.40 | - | V |
| | $I_O = -8.0\text{ mA}; V_{CC} = 4.5\text{ V}$ | 3.94 | - | - | 3.80 | - | 3.70 | - | V | |
| V_{OL} | LOW-level output voltage | $V_I = V_{IH}$ or V_{IL} | | | | | | | | |
| | | $I_O = 50\ \mu\text{A}; V_{CC} = 2.0\text{ V}$ | - | 0 | 0.1 | - | 0.1 | - | 0.1 | V |
| | | $I_O = 50\ \mu\text{A}; V_{CC} = 3.0\text{ V}$ | - | 0 | 0.1 | - | 0.1 | - | 0.1 | V |
| | | $I_O = 50\ \mu\text{A}; V_{CC} = 4.5\text{ V}$ | - | 0 | 0.1 | - | 0.1 | - | 0.1 | V |
| | | $I_O = 4.0\text{ mA}; V_{CC} = 3.0\text{ V}$ | - | - | 0.36 | - | 0.44 | - | 0.55 | V |
| | $I_O = 8.0\text{ mA}; V_{CC} = 4.5\text{ V}$ | - | - | 0.36 | - | 0.44 | - | 0.55 | V | |

Table 6. Static characteristics ...continued

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

| Symbol | Parameter | Conditions | 25 °C | | | -40 °C to +85 °C | | -40 °C to +125 °C | | Unit |
|-----------------------|---------------------------|---|-------|-----|------|------------------|------|-------------------|------|---------------|
| | | | Min | Typ | Max | Min | Max | Min | Max | |
| I_I | input leakage current | $V_I = 5.5 \text{ V}$ or GND; $V_{CC} = 0 \text{ V}$ to 5.5 V | - | - | 0.1 | - | 1.0 | - | 2.0 | μA |
| I_{CC} | supply current | $V_I = V_{CC}$ or GND; $I_O = 0 \text{ A}$; $V_{CC} = 5.5 \text{ V}$ | - | - | 4.0 | - | 40 | - | 80 | μA |
| C_I | input capacitance | | - | 3 | 10 | - | 10 | - | 10 | pF |
| C_O | output capacitance | | - | 4 | - | - | - | - | - | pF |
| 74AHCT273-Q100 | | | | | | | | | | |
| V_{IH} | HIGH-level input voltage | $V_{CC} = 4.5 \text{ V}$ to 5.5 V | 2.0 | - | - | 2.0 | - | 2.0 | - | V |
| V_{IL} | LOW-level input voltage | $V_{CC} = 4.5 \text{ V}$ to 5.5 V | - | - | 0.8 | - | 0.8 | - | 0.8 | V |
| V_{OH} | HIGH-level output voltage | $V_I = V_{IH}$ or V_{IL} ; $V_{CC} = 4.5 \text{ V}$ | | | | | | | | |
| | | $I_O = -50 \mu\text{A}$ | 4.4 | - | - | 4.4 | - | 4.4 | - | V |
| | | $I_O = -8.0 \text{ mA}$ | 3.94 | - | - | 3.80 | - | 3.70 | - | V |
| V_{OL} | LOW-level output voltage | $V_I = V_{IH}$ or V_{IL} ; $V_{CC} = 4.5 \text{ V}$ | | | | | | | | |
| | | $I_O = 50 \mu\text{A}$ | - | 0 | 0.1 | - | 0.1 | - | 0.1 | V |
| | | $I_O = 8.0 \text{ mA}$ | - | - | 0.36 | - | 0.44 | - | 0.55 | V |
| I_I | input leakage current | $V_I = 5.5 \text{ V}$ or GND; $V_{CC} = 0 \text{ V}$ to 5.5 V | - | - | 0.1 | - | 1.0 | - | 2.0 | μA |
| I_{CC} | supply current | $V_I = V_{CC}$ or GND; $I_O = 0 \text{ A}$; $V_{CC} = 5.5 \text{ V}$ | - | - | 4.0 | - | 40 | - | 80 | μA |
| ΔI_{CC} | additional supply current | per input pin; $V_I = V_{CC} - 2.1 \text{ V}$; other pins at V_{CC} or GND; $I_O = 0 \text{ A}$; $V_{CC} = 4.5 \text{ V}$ to 5.5 V | - | - | 1.35 | - | 1.5 | - | 1.5 | mA |
| C_I | input capacitance | | - | 3 | 10 | - | 10 | - | 10 | pF |
| C_O | output capacitance | | - | 4 | - | - | - | - | - | pF |

10. Dynamic characteristics

Table 7. Dynamic characteristics

 Voltages are referenced to GND (ground = 0 V); for test circuit see [Figure 10](#).

| Symbol | Parameter | Conditions | 25 °C | | | –40 °C to +85 °C | | –40 °C to +125 °C | | Unit |
|---|-------------------|--|-------------------|------------------------------|------|------------------|------|-------------------|------|------|
| | | | Min | Typ ^[1] | Max | Min | Max | Min | Max | |
| 74AHC273-Q100 | | | | | | | | | | |
| t_{pd} | propagation delay | CP to Qn; see Figure 7 ^[2] | | | | | | | | |
| | | $V_{CC} = 3.0\text{ V to }3.6\text{ V}$ | | | | | | | | |
| | | $C_L = 15\text{ pF}$ | - | 6.0 | 13.6 | 1.0 | 16.0 | 1.0 | 17.0 | ns |
| | | $C_L = 50\text{ pF}$ | - | 8.6 | 17.1 | 1.0 | 19.5 | 1.0 | 21.5 | ns |
| | | $V_{CC} = 4.5\text{ V to }5.5\text{ V}$ | | | | | | | | |
| | | $C_L = 15\text{ pF}$ | - | 4.2 | 9 | 1.0 | 10.5 | 1.0 | 11.5 | ns |
| | | $C_L = 50\text{ pF}$ | - | 6.0 | 11.0 | 1.0 | 12.5 | 1.0 | 14.0 | ns |
| | | MR to Qn; see Figure 8 ^[3] | | | | | | | | |
| | | $V_{CC} = 3.0\text{ V to }3.6\text{ V}$ | | | | | | | | |
| | | $C_L = 15\text{ pF}$ | - | 5.1 | 13.6 | 1.0 | 16.0 | 1.0 | 17.0 | ns |
| | | $C_L = 50\text{ pF}$ | - | 7.3 | 17.1 | 1.0 | 19.5 | 1.0 | 21.5 | ns |
| | | f_{max} | maximum frequency | see Figure 7 | | | | | | |
| $V_{CC} = 3.0\text{ V to }3.6\text{ V}$ | | | | | | | | | | |
| $C_L = 15\text{ pF}$ | 75 | | | 120 | - | 65 | - | 65 | - | MHz |
| $C_L = 50\text{ pF}$ | 50 | | | 75 | - | 45 | - | 45 | - | MHz |
| $V_{CC} = 4.5\text{ V to }5.5\text{ V}$ | | | | | | | | | | |
| $C_L = 15\text{ pF}$ | 120 | | | 165 | - | 100 | - | 100 | - | MHz |
| t_w | pulse width | CP HIGH or LOW; see Figure 7 | | | | | | | | |
| | | $V_{CC} = 3.0\text{ V to }3.6\text{ V}$ | 5.0 | - | - | 6.5 | - | 6.5 | - | ns |
| | | $V_{CC} = 4.5\text{ V to }5.5\text{ V}$ | 5.0 | - | - | 5.0 | - | 5.0 | - | ns |
| | | $\overline{\text{MR}}$ LOW; see Figure 8 | | | | | | | | |
| | | $V_{CC} = 3.0\text{ V to }3.6\text{ V}$ | 5.0 | - | - | 6.0 | - | 6.0 | - | ns |
| | | $V_{CC} = 4.5\text{ V to }5.5\text{ V}$ | 5.0 | - | - | 5.0 | - | 5.0 | - | ns |
| t_{su} | set-up time | Dn to CP; see Figure 9 | | | | | | | | |
| | | $V_{CC} = 3.0\text{ V to }3.6\text{ V}$ | 3.0 | - | - | 3.0 | - | 3.0 | - | ns |
| | | $V_{CC} = 4.5\text{ V to }5.5\text{ V}$ | 3.0 | - | - | 3.0 | - | 3.0 | - | ns |
| t_h | hold time | Dn to CP; see Figure 9 | | | | | | | | |
| | | $V_{CC} = 3.0\text{ V to }3.6\text{ V}$ | 1.0 | - | - | 1.0 | - | 1.0 | - | ns |
| | | $V_{CC} = 4.5\text{ V to }5.5\text{ V}$ | 1.0 | - | - | 1.0 | - | 1.0 | - | ns |

Table 7. Dynamic characteristics ...continuedVoltages are referenced to GND (ground = 0 V); for test circuit see [Figure 10](#).

| Symbol | Parameter | Conditions | 25 °C | | | -40 °C to +85 °C | | -40 °C to +125 °C | | Unit |
|--|-------------------------------|--|-------|--------------------|------|------------------|------|-------------------|------|------|
| | | | Min | Typ ^[1] | Max | Min | Max | Min | Max | |
| t _{rec} | recovery time | $\overline{\text{MR}}$ to CP; see Figure 8 | | | | | | | | |
| | | V _{CC} = 3.0 V to 3.6 V | 2.5 | - | - | 2.5 | - | 2.5 | - | ns |
| | | V _{CC} = 4.5 V to 5.5 V | 2.0 | - | - | 2.0 | - | 2.0 | - | ns |
| C _{PD} | power dissipation capacitance | f _i = 1 MHz; V _I = GND to V _{CC} ^[4] | - | 14 | - | - | - | - | - | pF |
| 74AHCT273-Q100; V_{CC} = 4.5 V to 5.5 V | | | | | | | | | | |
| t _{pd} | propagation delay | CP to Qn; see Figure 7 ^[2] | | | | | | | | |
| | | C _L = 15 pF | - | 4.0 | 7.5 | 1.0 | 8.8 | 1.0 | 9.5 | ns |
| | | C _L = 50 pF | - | 5.8 | 9.2 | 1.0 | 10.5 | 1.0 | 11.5 | ns |
| | | $\overline{\text{MR}}$ to Qn; see Figure 8 ^[3] | | | | | | | | |
| | | C _L = 15 pF | - | 3.9 | 10.0 | 1.0 | 11.6 | 1.0 | 12.5 | ns |
| | | C _L = 50 pF | - | 5.6 | 11.0 | 1.0 | 12.6 | 1.0 | 14.0 | ns |
| f _{max} | maximum frequency | see Figure 7 | | | | | | | | |
| | | C _L = 15 pF | 75 | 120 | - | 65 | - | 65 | - | MHz |
| | | C _L = 50 pF | 50 | 75 | - | 45 | - | 45 | - | MHz |
| t _W | pulse width | CP HIGH or LOW; see Figure 7 | 5.0 | - | - | 6.5 | - | 6.5 | - | ns |
| | | $\overline{\text{MR}}$ LOW; see Figure 8 | 5.0 | - | - | 6.0 | - | 6.0 | - | ns |
| t _{su} | set-up time | Dn to CP; see Figure 9 | 3.0 | - | - | 3.0 | - | 3.0 | - | ns |
| t _h | hold time | Dn to CP; see Figure 9 | 1.0 | - | - | 1.0 | - | 1.0 | - | ns |
| t _{rec} | recovery time | $\overline{\text{MR}}$ to CP; see Figure 8 | 2.5 | - | - | 2.5 | - | 2.5 | - | ns |
| C _{PD} | power dissipation capacitance | f _i = 1 MHz; V _I = GND to V _{CC} ^[4] | - | 18 | - | - | - | - | - | pF |

[1] Typical values are measured at nominal supply voltage (V_{CC} = 3.3 V and V_{CC} = 5.0 V).

[2] t_{pd} is the same as t_{PLH} and t_{PHL}.

[3] t_{pd} is the same as t_{PHL} only.

[4] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f_i = input frequency in MHz;

f_o = output frequency in MHz;

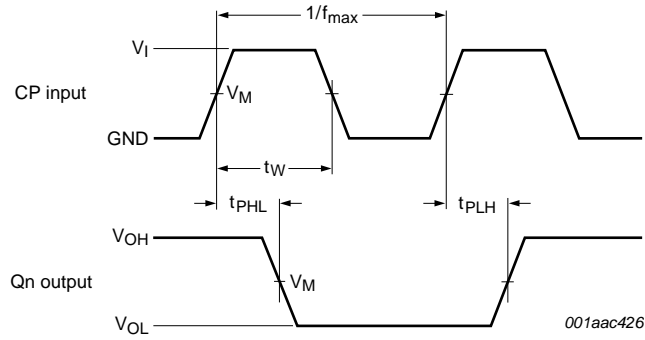
C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

N = number of inputs switching;

Σ(C_L × V_{CC}² × f_o) = sum of the outputs.

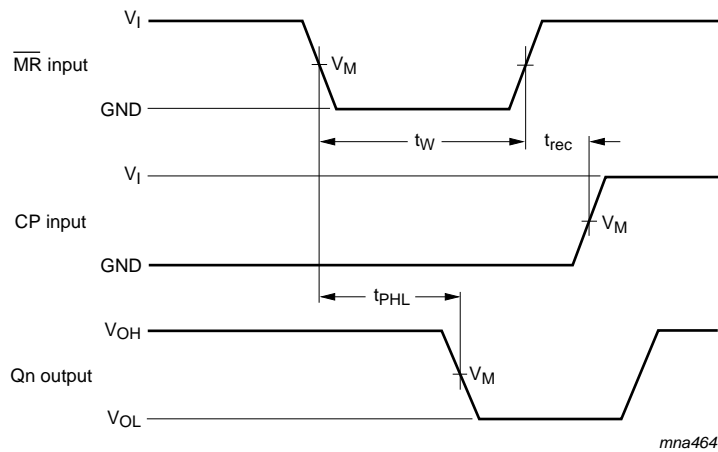
11. Waveforms



Measurement points are given in [Table 8](#).

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

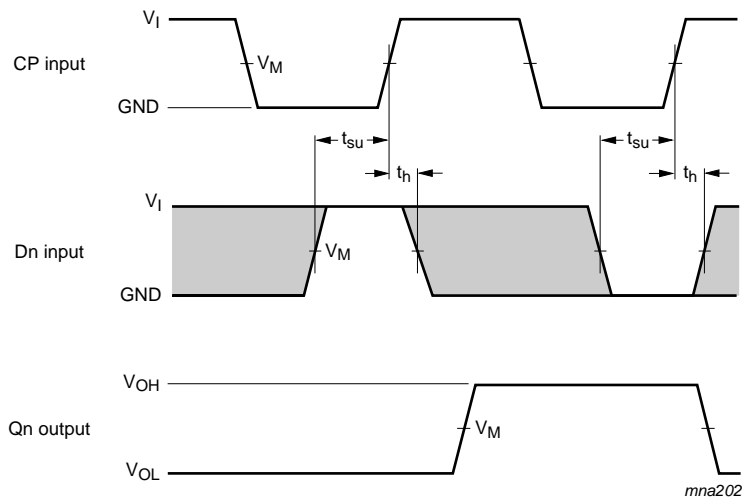
Fig 7. Clock pulse width, maximum frequency and input to output propagation delays



Measurement points are given in [Table 8](#).

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig 8. Master reset pulse width, recovery time and propagation delay



Measurement points are given in [Table 8](#).

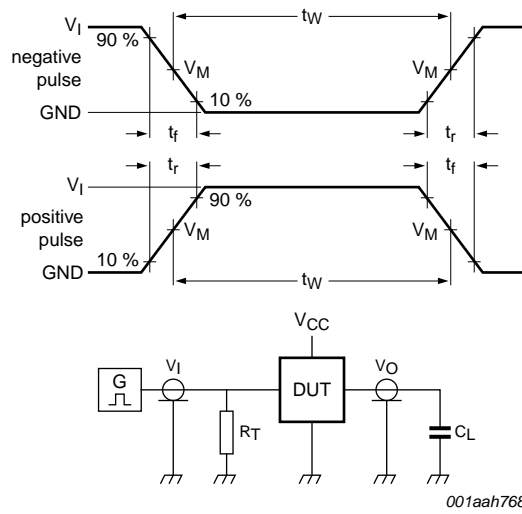
The shaded areas indicate when the input is permitted to change for predictable output performance.

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig 9. Data set-up and hold times

Table 8. Measurement points

| Type | Input | Output |
|----------------|---------------------|---------------------|
| | V_M | V_M |
| 74AHC273-Q100 | $0.5 \times V_{CC}$ | $0.5 \times V_{CC}$ |
| 74AHCT273-Q100 | 1.5 V | $0.5 \times V_{CC}$ |



Test data is given in [Table 9](#).

Definitions test circuit:

R_T = termination resistance should be equal to output impedance Z_o of the pulse generator.

C_L = load capacitance including jig and probe capacitance.

Fig 10. Test circuit for measuring switching times

Table 9. Test data

| Type | Input | | Load | Test |
|----------------|----------|---------------|--------------|--------------------|
| | V_I | t_r, t_f | C_L | |
| 74AHC273-Q100 | V_{CC} | ≤ 3.0 ns | 15 pF, 50 pF | t_{PLH}, t_{PHL} |
| 74AHCT273-Q100 | 3.0 V | ≤ 3.0 ns | 15 pF, 50 pF | t_{PLH}, t_{PHL} |

12. Package outline

SO20: plastic small outline package; 20 leads; body width 7.5 mm

SOT163-1



Fig 11. Package outline SOT163-1 (SO20)

TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm

SOT360-1



Fig 12. Package outline SOT360-1 (TSSOP20)

DHVQFN20: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 20 terminals; body 2.5 x 4.5 x 0.85 mm

SOT764-1



Fig 13. Package outline SOT764-1 (DHVQFN20)

13. Abbreviations

Table 10. Abbreviations

| Acronym | Description |
|---------|--|
| CDM | Charged Device Model |
| CMOS | Complementary Metal-Oxide Semiconductor |
| DUT | Device Under Test |
| ESD | ElectroStatic Discharge |
| HBM | Human Body Model |
| LSTTL | Low-power Schottky Transistor-Transistor Logic |
| MM | Machine Model |
| MIL | Military |
| MOS | Metal-Oxide Semiconductor |

14. Revision history

Table 11. Revision history

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|------------------------|--------------|--------------------|---------------|------------|
| 74AHC_AHCT273_Q100 v.1 | 20130327 | Product data sheet | - | - |

15. Legal information

15.1 Data sheet status

| Document status ^{[1][2]} | Product status ^[3] | Definition |
|-----------------------------------|-------------------------------|---|
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