NXP Semiconductors
Data Sheet

Document Number: WCT1011DS

Rev. 0 09/2016

WCT1011DS

Features

- Compliant with the latest version Wireless Power Consortium (WPC) power class 0 specification power transmitter design
- Supports wide transmitter DC input voltage ranging from 4.2 V, typically 12 V and 19 V
- Integrated digital demodulation
- Supports two-way communication, transmitter to receiver by FSK and receiver to transmitter by ASK
- Supports all types of receiver modulation strategies (AC capacitor, AC resistor, and DC resistor)
- Supports Q factor detection and calibrated power loss based Foreign Object Detection (FOD) Framework
- Supports low standby power
- Supports various power control techniques: operation frequency control, duty cycle control, phase difference control and topology switch
- LED for system status indication
- Over-voltage/current/temperature protection
- Software-based solution to provide maximum design freedom and product differentiation
- FreeMASTER GUI tool to enable configuration, calibration, and debugging

Applications

- Extended Power Profile Power Transmitter

  Extended power profile consumer power transmitter solution with operation frequency and duty cycle control, phase difference control, and topology switch (WPC MP-Ax types or customer properties)

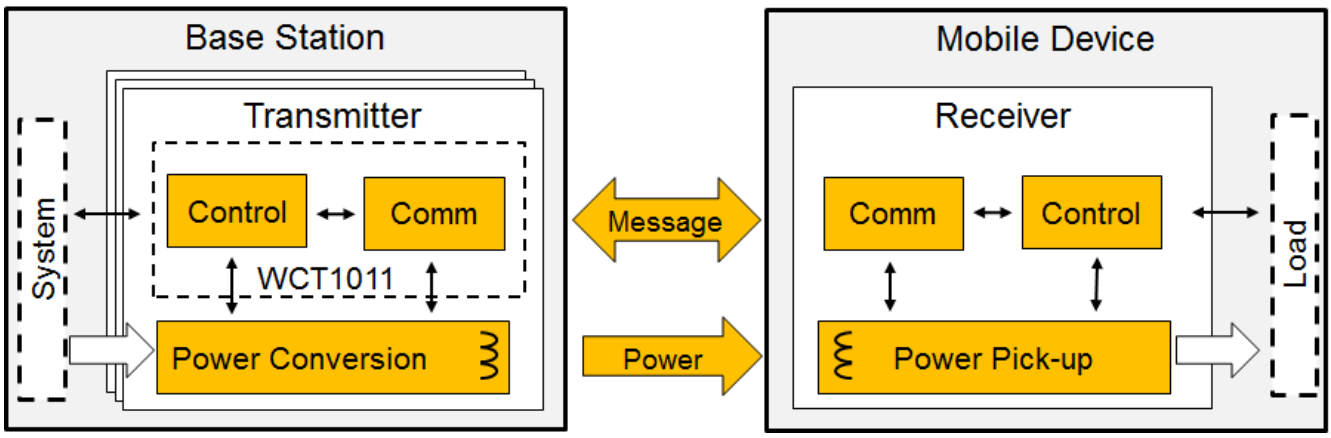
Overview Description

The WCT1011 is a wireless power transmitter controller that integrates all required functions for the WPC “Qi” compliant wireless power transmitter design. It is an intelligent device that works with the NXP touch sensing technology or uses periodically analog PING to detect a mobile device for charging while gaining super low standby power. Once the mobile device is detected, the WCT1011 controls the power transfer by adjusting the operation frequency and duty cycle, or switching topology, or adjusting the phase difference of the power stage according to message packets sent by mobile device.

In order to maximize the design freedom and product differentiation, the WCT1011 supports the extended power profile consumer power transmitter design (WPC MP-Ax types or customization) by using operation frequency and duty cycle control, phase difference control, and topology switch by software based solutions, which can support wireless charging with both extended power profile power receiver and baseline power profile power receiver. In addition, the easy-to-use FreeMASTER GUI tool has configuration, calibration, and debugging functions to provide the user-friendly design experience and reduce time-to-market.

The WCT1011 includes a digital demodulation module to reduce the external components, an FSK modulation module to support two-way communication, a protection module to handle the over-voltage/current/temperature protection, and an FOD module to protect from overheating by misplaced metallic foreign objects. It also handles any abnormal condition and operational status and provides comprehensive indicator outputs for robust system design.

Wireless Charging System Functional Diagram



Contents

1 Absolute Maximum Ratings

1.1 Electrical operating ratings

Table 1 Absolute maximum electrical ratings (V_{SS} = 0 V, V_{SSA} = 0 V)

Characteristic	Symbol	Notes[1]	Min.	Max.	Unit
Supply Voltage Range	V_{DD}		–0.3	4.0	V
Analog Supply Voltage Range	V_{DDA}		–0.3	4.0	V
ADC High Voltage Reference	V_{REFHx}		–0.3	4.0	V
Voltage difference V_{DD} to V_{DDA}	ΔV_{DD}		–0.3	0.3	V
Voltage difference V_{SS} to V_{SSA}	ΔV_{ss}		–0.3	0.3	V
Digital Input Voltage Range	V_{IN}	Pin Group 1	–0.3	5.5	V
RESET Input Voltage Range	V_{IN_RESET}	Pin Group 2	–0.3	4.0	V
Analog Input Voltage Range	V_{INA}	Pin Group 3	–0.3	4.0	V
Input clamp current, per pin ($V_{IN} < V_{SS}$ - 0.3 V)[2, 3]	V_{IC}		–	–5.0	mA
Output clamp current, per pin[4]	V_{OC}		–	±20.0	mA
Contiguous pin DC injection current—regional limit sum of 16 contiguous pins	I_{ICont}		–25	25	mA
Output Voltage Range (normal push-pull mode)	V_{OUT}	Pin Group 1,2	–0.3	4.0	V
Output Voltage Range (open drain mode)	V_{OUTOD}	Pin Group 1	–0.3	5.5	V
$\overline{\text{RESET}}$ Output Voltage Range	V_{OUTOD_RESET}	Pin Group 2	–0.3	4.0	V
Ambient Temperature	T_A		–40	85	°C
Storage Temperature Range (Extended Industrial)	T_{STG}		–55	150	°C

1. Default Mode:
   - Pin Group 1: GPIO, TDI, TDO, TMS, TCK
   - Pin Group 2: $\overline{\text{RESET}}$
   - Pin Group 3: ADC and Comparator Analog Inputs
2. Continuous clamp current.
3. All 5 volt tolerant digital I/O pins are internally clamped to VSS through an ESD protection diode. There is no diode connection to VDD. If VIN greater than VDIO_MIN (= VSS–0.3 V) is observed, then there is no need to provide current limiting resistors at the pads. If this limit cannot be observed, then a current limiting resistor is required.
4. I/O is configured as push-pull mode.

1.2 Thermal handling ratings

Table 2 Thermal handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
T_{STG}	Storage temperature	–55	150	°C	1
T_{SDR}	Solder temperature, lead-free	–	260	°C	2

1. Determined according to JEDEC Standard JESD22-A103, *High Temperature Storage Life.*
2. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices.*

1.3 ESD handling ratings

Table 3 ESD handling ratings

Characteristic[1]	Min.	Max.	Unit
ESD for Human Body Model (HBM)	-2000	+2000	V
ESD for Machine Model (MM)	-200	+200	V
ESD for Charge Device Model (CDM)	-500	+500	V
Latch-up current at TA= 85°C (I_{LAT})	-100	+100	mA

1. Parameter is achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted.

1.4 Moisture handling ratings

Table 4 Moisture handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
MSL	Moisture sensitivity level	–	3	–	1

1. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices.*

2 Electrical Characteristics

2.1 General characteristics

Table 5 General electrical characteristics

Recommended operating conditions (V_{REFLx} = 0 V, V_{SSA} = 0 V, V_{SS} = 0 V)							
Characteristic	**Symbol**	**Notes**	**Min.**	**Typ.**	**Max.**	**Unit**	**Test conditions**
Supply Voltage[2]	V_{DD} ,V_{DDA}		2.7	3.3	3.6	V	-
ADC Reference Voltage High	V_{REFHA} V_{REFHB}		V_{DDA} -0.6		V_{DDA}	V	-
Voltage difference V_{DD} to V_{DDA}	ΔV_{DD}		-0.1	0	0.1	V	-
Voltage difference V_{SS} to V_{SSA}	ΔV_{ss}		-0.1	0	0.1	V	-
Input Voltage High (digital inputs)	V_{IH}	1 (Pin Group 1)	0.7×V_{DD}		5.5	V	-
$\overline{\text{RESET}}$ Voltage High	V_{IH_RESET}	1 (Pin Group 2)	0.7×V_{DD}	-	V_{DD}	V	-
Input Voltage Low (digital inputs)	V_{IL}	1 (Pin Group 1,2)			0.35×V_{DD}	V	-
Output Source Current High (at V_{OH} min.) [3,4] • Programmed for low drive strength • Programmed for high drive strength	I_{OH}	 1 (Pin Group 1) 1 (Pin Group 1)	 - -		 -2 -9	mA	
Output Source Current High (at V_{OL} max.) [3,4] • Programmed for low drive strength • Programmed for high drive strength	I_{OL}	 1 (Pin Group 1,2) 1 (Pin Group 1,2)	 - -		 2 9	mA	-
Output Voltage High	V_{OH}	1 (Pin Group 1)	V_{DD} -0.5	-	-	V	I_{OH} = I_{OHmax}
Output Voltage Low	V_{OL}	1 (Pin Group 1,2)	-	-	0.5	V	I_{OL} = I_{OLmax}
Digital Input Current High	I_{IH}	1 (Pin Group 1)	-	0	+/-2.5	µA	V_{IN} = 2.4 V to 5.5 V

pull-up enabled or disabled		1 (Pin Group 2)					V_{IN} = 2.4 V to V_{DD}
Comparator Input Current High	I_{IHC}	1 (Pin Group 3)		0	+/-2	µA	$V_{IN} = V_{DDA}$
Internal Pull-Up Resistance	$R_{Pull-Up}$		20	-	50	kΩ	-
Internal Pull-Down Resistance	$R_{Pull-Down}$		20	-	50	kΩ	-
Comparator Input Current Low	I_{ILC}	1 (Pin Group 3)	-	0	+/-2	µA	V_{IN} = 0V
Output Current[1] High Impedance State	I_{OZ}	1 (Pin Group 1,2)	-	0	+/-1	µA	-
Schmitt Trigger Input Hysteresis	V_{HYS}	1 (Pin Group 1,2)	0.06×V_{DD}	-	-	V	-
Input capacitance	C_{IN}		-	10	-	pF	-
Output capacitance	C_{OUT}		-	10	-	pF	-
GPIO pin interrupt pulse width[5]	T_{INT_Pulse}	6	1.5	-	-	Bus clock	-
Port rise and fall time (high drive strength). Slew disabled.	$T_{Port\_H\_DIS}$	7	5.5	-	15.1	ns	2.7 ≤ VDD ≤ 3.6V
Port rise and fall time (high drive strength). Slew enabled.	$T_{Port\_H\_EN}$	7	1.5	-	6.8	ns	2.7 ≤ VDD ≤ 3.6V
Port rise and fall time (low drive strength). Slew disabled.	$T_{Port\_L\_DIS}$	8	8.2	-	17.8	ns	2.7 ≤ VDD ≤ 3.6V
Port rise and fall time (low drive strength). Slew enabled.	$T_{Port\_L\_EN}$	8	3.2	-	9.2	ns	2.7 ≤ VDD ≤ 3.6V
Device (system and core) clock frequency	f_{SYSCLK}		0.001	-	100	MHz	-
Bus clock	f_{BUS}		-	-	50	MHz	-

1. Default Mode
   - Pin Group 1: GPIO, TDI, TDO, TMS, TCK
   - Pin Group 2: $\overline{\text{RESET}}$
   - Pin Group 3: ADC and Comparator Analog Inputs
2. ADC specifications are not guaranteed when VDDA is below 3.0 V.
3. Total chip source or sink current cannot exceed 75mA.
4. Contiguous pin DC injection current of regional limit—including sum of negative injection currents or sum of positive injection currents of 16 contiguous pins—is 25mA.
5. Applies to a pin only when it is configured as GPIO and configured to cause an interrupt by appropriately programming GPIOn_IPOLR and GPIOn_IENR.
6. The greater synchronous and asynchronous timing must be met.
7. 75 pF load
8. 15 pF load

2.2 Device characteristics

Table 6 General device characteristics

Power mode transition behavior					
Symbol	**Description**	**Min.**	**Max.**	**Unit**	**Notes**
T_{POR}	After a POR event, the amount of delay from when VDD reaches 2.7 V to when the first instruction executes (over the operating temperature range).	199	225	µs	
T_{S2R}	STOP mode to RUN mode	6.79	7.27	µs	1
$T_{LPS2LPR}$	LPS mode to LPRUN mode	240.9	551	µs	2
Reset and interrupt timing					
Symbol	**Characteristic**	**Min.**	**Max.**	**Unit**	**Notes**
t_{RA}	Minimum $\overline{\text{RESET}}$ Assertion Duration	16	-	ns	3
t_{RDA}	$\overline{\text{RESET}}$ desertion to First Address Fetch	865 × T_{OSC} + 8 × T_{SYSCLK}	-	ns	4
t_{IF}	Delay from Interrupt Assertion to Fetch of first instruction (exiting STOP mode)	361.3	570.9	ns	
PMC Low-Voltage Detection (LVD) and Power-On Reset (POR) parameters					
Symbol	**Characteristic**	**Min.**	**Typ.**	**Max.**	**Unit**
V_{POR_A}	POR Assert Voltage[5]	-	2.0	-	V
V_{POR_R}	POR Release Voltage[6]	-	2.7	-	V
V_{LVI_2p7}	LVI_2p7 Threshold Voltage	-	2.73	-	V
V_{LVI_2p2}	LVI_2p2 Threshold Voltage	-	2.23	-	V
JTAG timing					
Symbol	**Description**	**Min.**	**Max.**	**Unit**	**Notes**
f_{OP}	TCK frequency of operation	DC	$f_{SYSCLK}/8$	MHz	
t_{PW}	TCK clock pulse width	50	-	ns	
t_{DS}	TMS, TDI data set-up time	5	-	ns	
t_{DH}	TMS, TDI data hold time	5	-	ns	
t_{DV}	TCK low to TDO data valid	-	30	ns	
t_{TS}	TCK low to TDO tri-state	-	30	ns	

Regulator 1.2 V parameters					
Symbol	**Characteristic**	**Min.**	**Typ.**	**Max.**	**Unit**
V_{CAP}	Output Voltage[7]	-	1.22	-	V
I_{SS}	Short Circuit Current[8]	-	600	-	mA
T_{RSC}	Short Circuit Tolerance (VCAP shorted to ground)	-	-	30	Mins
V_{REF}	Reference Voltage (after trim)	-	1.21	-	V
Phase-locked loop timing					
Symbol	**Characteristic**	**Min.**	**Typ.**	**Max.**	**Unit**
f_{Ref_PLL}	PLL input reference frequency[9]	8	8	16	MHz
f_{OP_PLL}	PLL output frequency[10]	200	-	400	MHz
t_{Lock_PLL}	PLL lock time[11]	35.5	-	73.2	µs
t_{DC_PLL}	Allowed Duty Cycle of input reference	40	50	60	%
Relaxation oscillator electrical specifications					
Symbol	**Characteristic**	**Min.**	**Typ.**	**Max.**	**Unit**
f_{ROSC_8M}	8 MHz Output Frequency[12] RUN Mode • 0°C to 105°C • -40°C to 105°C Standby Mode (IRC trimmed @ 8 MHz) • -40°C to 105°C	 7.84 7.76 -	 8 8 405	 8.16 8.24 -	 MHz MHz kHz
$f_{ROSC\_8M\_Delta}$	8 MHz Frequency Variation over 25°C RUN Mode Due to temperature • 0°C to 105°C • -40°C to 105°C	 - -	 +/-1.5 +/-1.5	 +/-2 +/-3	 % %
f_{ROSC_200k}	200 kHz Output Frequency[13] RUN Mode • -40°C to 105°C	 194	 200	 206	 kHz
$f_{ROSC\_200k\_Delta}$	200 kHz Output Frequency Variation over 25°C RUN Mode Due to temperature • 0°C to 85°C • -40°C to 105°C	 - -	 +/-1.5 +/-1.5	 +/-2 +/-3	 % %
t_{Stab}	Stabilization Time • 8 MHz output[14] • 200 kHz output[15]	 - -	 0.12 10	 - -	 µs µs
t_{DC_ROSC}	Output Duty Cycle	48	50	52	%
Flash specifications					
Symbol	**Description**	**Min.**	**Typ.**	**Max.**	**Unit**
t_{hvpgm4}	Longword Program high-voltage time	-	7.5	18	µs

$t_{hversscr}$	Sector Erase high-voltage time[16]	-	13	113	ms
$t_{hversall}$	Erase All high-voltage time[16]	-	52	452	ms
$t_{rd1sec1k}$	Read 1s Section execution time (flash sector)[17]	-	-	60	µs
t_{pgmchk}	Program Check execution time[17]	-	-	45	µs
t_{rdrsrc}	Read Resource execution time[17]	-	-	30	µs
t_{pgm4}	Program Longword execution time	-	65	145	µs
t_{ersscr}	Erase Flash Sector execution time[18]	-	14	114	ms
t_{rd1all}	Read 1s All Blocks execution time	-	-	0.9	ms
t_{rdonce}	Read Once execution time[17]	-	-	25	µs
$t_{pgmonce}$	Program Once execution time	-	65	-	µs
t_{ersall}	Erase All Blocks execution time[18]	-	70	575	ms
t_{vfykey}	Verify Backdoor Access Key execution time[17]	-	-	30	µs
$t_{flashretp10k}$	Data retention after up to 10 K cycles	5	50[19]	-	years
$t_{flashretp1k}$	Data retention after up to 1 K cycles	20	100[19]	-	years
$n_{flashcyc}$	Cycling endurance[20]	10 K	50 K[19]	-	cycles

12-bit ADC electrical specifications

Symbol	Characteristic	Min.	Typ.	Max.	Unit
V_{DDA}	Supply voltage[21]	3	3.3	3.6	V
f_{ADCCLK}	ADC conversion clock[22]	0.1	-	10	MHz
R_{ADC}	Conversion range with single-ended/unipolar[23]	V_{REFL}	-	V_{REFH}	V
V_{ADCIN}	Input voltage range (per input) with internal reference[24]	0	-	V_{DDA}	V
t_{ADC}	Conversion time[25]	-	8	-	t_{ADCCLK}
t_{ADCPU}	ADC power-up time (from adc_pdn)	-	13	-	t_{ADCCLK}
I_{ADCRUN}	ADC RUN current (per ADC block)	-	1.8	-	mA
INL_{ADC}	Integral non-linearity[26]	-	+/- 1.5	+/- 2.2	LSB[27]
DNL_{ADC}	Differential non-linearity[26]	-	+/- 0.5	+/- 0.8	LSB[27]
E_{GAIN}	Gain Error	-	0.996 to 1.004	0.99 to 1.101	-
ENOB	Effective number of bits	-	10.6	-	bits
I_{INJ}	Input injection current[28]	-	-	+/-3	mA
C_{ADCI}	Input sampling capacitance	-	4.8	-	pF

Comparator and 6-bit DAC electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit
V_{DD}	Supply voltage	2.7	-	3.6	V
I_{DDHS}	Supply current, High-speed mode(EN=1, PMODE=1)	-	300	-	µA
I_{DDLS}	Supply current, Low-speed mode(EN=1, PMODE=0)	-	36	-	µA

V_{AIN}	Analog input voltage	V_{ss}	-	V_{DD}	V
V_{AIO}	Analog input offset voltage	-	-	20	mV
V_H	Analog comparator hysteresis[29] • CR0[HYSTCTR]=00 • CR0[HYSTCTR]=01 • CR0[HYSTCTR]=10 • CR0[HYSTCTR]=11	- - - -	5 25 55 80	13 48 105 148	mV mV mV mV
V_{CMPOh}	Output high	V_{DD} -0.5	-	-	V
V_{CMPOl}	Output low	-	-	0.5	V
t_{DHS}	Propagation delay, high-speed mode (EN=1, PMODE=1)[30]	-	25	50	ns
t_{DLS}	Propagation delay, low-speed mode (EN=1, PMODE=0) [30]	-	60	200	ns
t_{DInit}	Analog comparator initialization delay[31]	-	40	-	µs
I_{DAC6b}	6-bit DAC current adder (enabled)	-	7	-	µA
R_{DAC6b}	6-bit DAC reference inputs	V_{DDA}	-	V_{DD}	V
INL_{DAC6b}	6-bit DAC integral non-linearity	-0.5	-	0.5	LSB[32]
DNL_{DAC6b}	6-bit DAC differential non-linearity	-0.3	-	0.3	LSB

PWM timing parameters

Symbol	Characteristic	Min.	Typ.	Max.	Unit
f_{PWM}	PWM clock frequency[33,34]	-	100	-	MHz
S_{PWMNEP}	NanoEdge Placement (NEP) step size	-	312	-	ps
t_{DFLT}	Delay for fault input activating to PWM output deactivated	1	-	-	ns
t_{PWMPU}	Power-up time[35]	-	25	-	µs

Timer timing

Symbol	Characteristic	Min.	Max.	Unit	Notes
P_{IN}	Timer input period	$2T_{timer}$ + 6	-	ns	36
P_{INHL}	Timer input high/low period	$1T_{timer}$ + 3	-	ns	36
P_{OUT}	Timer output period	$2T_{timer}$ - 2	-	ns	36
P_{OUTHL}	Timer output high/low period	$1T_{timer}$ - 2	-	ns	36

SCI timing

Symbol	Characteristic	Min.	Max.	Unit	Notes
BR_{SCI}	Baud rate	-	(f_{MAX_SCI} /16)	Mbit/s	37
PW_{RXD}	RXD pulse width	$0.965/BR_{SCI}$	$1.04/BR_{SCI}$	µs	

PW_{TXD}	TXD pulse width	$0.965/BR_{SCI}$	$1.04/BR_{SCI}$	µs	

IIC timing

Symbol	Characteristic	Min.		Max.		Unit	Notes
		Min.	Max.	Min.	Max.		
f_{SCL}	SCL clock frequency	0	100	0	400	kHz	
t_{HD_STA}	Hold time (repeated) START condition. After this period, the first clock pulse is generated.	4	-	0.6	-	µs	
t_{SCL_LOW}	LOW period of the SCL clock	4.7	-	1.3	-	µs	
t_{SCL_HIGH}	HIGH period of the SCL clock	4	-	0.6	-	µs	
t_{SU_STA}	Set-up time for a repeated START condition	4.7	-	0.6	-	µs	
t_{HD_DAT}	Data hold time for IIC bus devices	0[38]	3.45[39]	0[40]	0.9[38]	µs	
t_{SU_DAT}	Data set-up time	250[41]	-	100[42]	-	ns	
t_r	Rise time of SDA and SCL signals	-	1000	$20 + 0.1C_b$	300	ns	43
t_f	Fall time of SDA and SCL signals	-	300	$20 + 0.1C_b$	300	ns	42, 43
t_{SU_STOP}	Set-up time for STOP condition	4	-	0.6	-	µs	
t_{BUS_Free}	Bus free time between STOP and START condition	4.7	-	1.3	-	µs	
t_{SP}	Pulse width of spikes that must be suppressed by the input filter	N/A	N/A	0	50	ns	

1. Clock configuration: CPU and system clocks= 100 MHz; Bus Clock = 100 MHz.
2. CPU clock = 200 kHz and 8 MHz IRC on standby.
3. If the $\overline{\text{RESET}}$ pin filter is enabled by setting the RST_FLT bit in the SIM_CTRL register to 1, the minimum pulse assertion must be greater than 21 ns.
4. TOSC means oscillator clock cycle; TSYSCLK means system clock cycle.
5. During 3.3 V VDD power supply ramp down
6. During 3.3 V VDD power supply ramp up (gated by LVI_2p7)
7. Value is after trim
8. Guaranteed by design
9. An externally supplied reference clock should be as free as possible from any phase jitter for the PLL to work correctly. The PLL is optimized for 8 MHz input.
10. The frequency of the core system clock cannot exceed 50 MHz. If the NanoEdge PWM is available, the PLL output must be set to 400 MHz.
11. This is the time required after the PLL is enabled to ensure reliable operation.
12. Frequency after application of 8 MHz trimmed.
13. Frequency after application of 200 kHz trimmed.
14. Standby to run mode transition.
15. Power down to run mode transition.
16. Maximum time based on expectations at cycling end-of-life.
17. Assumes 25 MHz flash clock frequency.
18. Maximum times for erase parameters based on expectations at cycling end-of-life.
19. Typical data retention values are based on measured response accelerated at high temperature and derated to a constant 25°C use profile. Engineering Bulletin EB618 does not apply to this technology. Typical endurance defined in Engineering Bulletin EB619.
20. Cycling endurance represents number of program/erase cycles at -40°C ≤ Tj ≤ 125°C.
21. The ADC functions up to VDDA = 2.7 V. When VDDA is below 3.0 V, ADC specifications are not guaranteed.
22. ADC clock duty cycle is 45% ~ 55%.
23. Conversion range is defined for x1 gain setting. For x2 and x4 the range is 1/2 and 1/4, respectively.

24. In unipolar mode, positive input must be ensured to be always greater than negative input.
25. First conversion takes 10 clock cycles.
26. INLADC/DNLADC is measured from VADCIN = VREFL to VADCIN = VREFH using Histogram method at x1 gain setting.
27. Least Significant Bit = 0.806 mV at 3.3 V VDDA, x1 gain setting.
28. The current that can be injected into or sourced from an unselected ADC input without affecting the performance of the ADC.
29. Typical hysteresis is measured with input voltage range limited to 0.6 to VDD-0.6V.
30. Signal swing is 100 mV.
31. Comparator initialization delay is defined as the time between software writes to change control inputs (Writes to DACEN, VRSEL, PSEL, MSEL, VOSEL) and the comparator output settling to a stable level.
32. 1 LSB = Vreference/64.
33. Reference IPbus clock of 100 MHz in NanoEdge Placement mode.
34. Temperature and voltage variations do not affect NanoEdge Placement step size.
35. Powerdown to NanoEdge mode transition.
36. Ttimer = Timer input clock cycle. For 100 MHz operation, Ttimer = 10 ns.
37. fMAX_SCI is the frequency of operation of the SCI clock in MHz, which can be selected as the bus clock (max. 50 MHz depending on part number) or 2x bus clock (max. 100 MHz) for the device.
38. The master mode I2C deasserts ACK of an address byte simultaneously with the falling edge of SCL. If no slaves acknowledge this address byte, then a negative hold time can result, depending on the edge rates of the SDA and SCL lines.
39. The maximum tHD_DAT must be met only if the device does not stretch the LOW period (tSCL_LOW) of the SCL signal.
40. Input signal Slew = 10 ns and Output Load = 50 pF
41. Set-up time in slave-transmitter mode is 1 IPBus clock period, if the TX FIFO is empty.
42. A Fast mode IIC bus device can be used in a Standard mode IIC bus system, but the requirement tSU_DAT ≥ 250 ns must then be met. This occurs when the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, then it must output the next data bit to the SDA line trmax + tSU_DAT = 1000 + 250 = 1250ns (according to the Standard mode I2C bus specification) before the SCL line is released.
43. Cb = total capacitance of the one bus line in pF.

2.3 Thermal operating characteristics

Table 7 General thermal characteristics

Symbol	Description	Min	Max	Unit
T_J	Die junction temperature	-40	125	°C
T_A	Ambient temperature	-40	85	°C

3 Typical Performance Characteristics

3.1 System efficiency

The maximum system efficiency (RX output power vs. TX input power) on WCT-15W1COILTX solution with MP Qi Receiver (RX) Simulator is more than 75%.

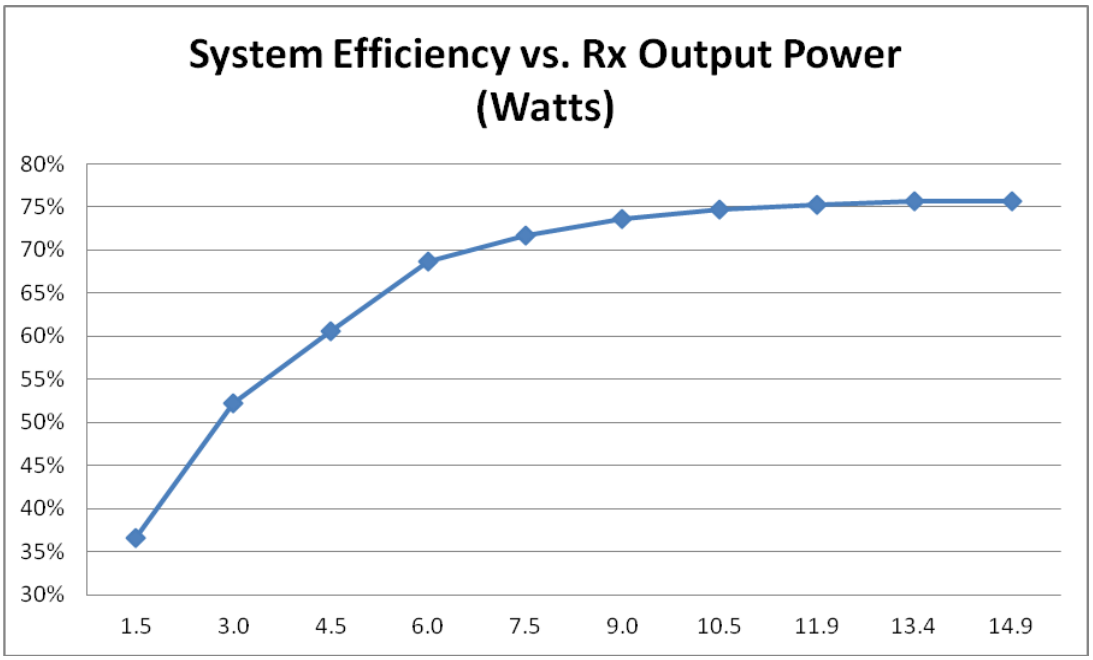


Figure 1 System efficiency on the WCT-15W1COILTX solution

Note: Power components are the main factor to determine the system efficiency, such as drivers and MOSFETs. The efficiency data in Figure 1 is obtained on the NXP reference solution with MP TX WCT-15W1COILTX configuration.

3.2 Standby power

The WCT1011 solution only consumes very low standby power with special low power control method, and can further achieve ultra low standby power by using the touch sensor technology.

It is recommended that the power consumption of the transmitter in standby mode meets the relative regional regulations especially for “No-load power consumption”.

Transmitter (TX) power consumption in standby mode with analog PING: < 8mA (96 mW with 12 V DC input)

3.3 Digital demodulation

The WCT1011 solution employs digital demodulation algorithm to communicate with RX. This method can achieve high performance, low cost, very simple coil signal sensing circuit with less component number.

3.4 Two-way communication

The WCT1011 solution supports two-way communication and uses FSK to send messages to RX. This method allows TX to negotiate with RX to establish advanced power transfer contract, and calibrate power loss for more precise FOD protection.

3.5 Foreign object detection

The WCT1011 solution supports power class 0 FOD framework, which is based on calibrated power loss method and quality factor (Q factor) method.

4 Device Information

4.1 Functional block diagram

From Figure 2, the low power feature with NXP touch technology is optional according to user requirements for minimizing standby power. When this function is not deployed, its pin can be configured for other purpose of use. Besides, 10 pins (dashed) are also configurable for different design requirements to provide design freedom and differentiation.

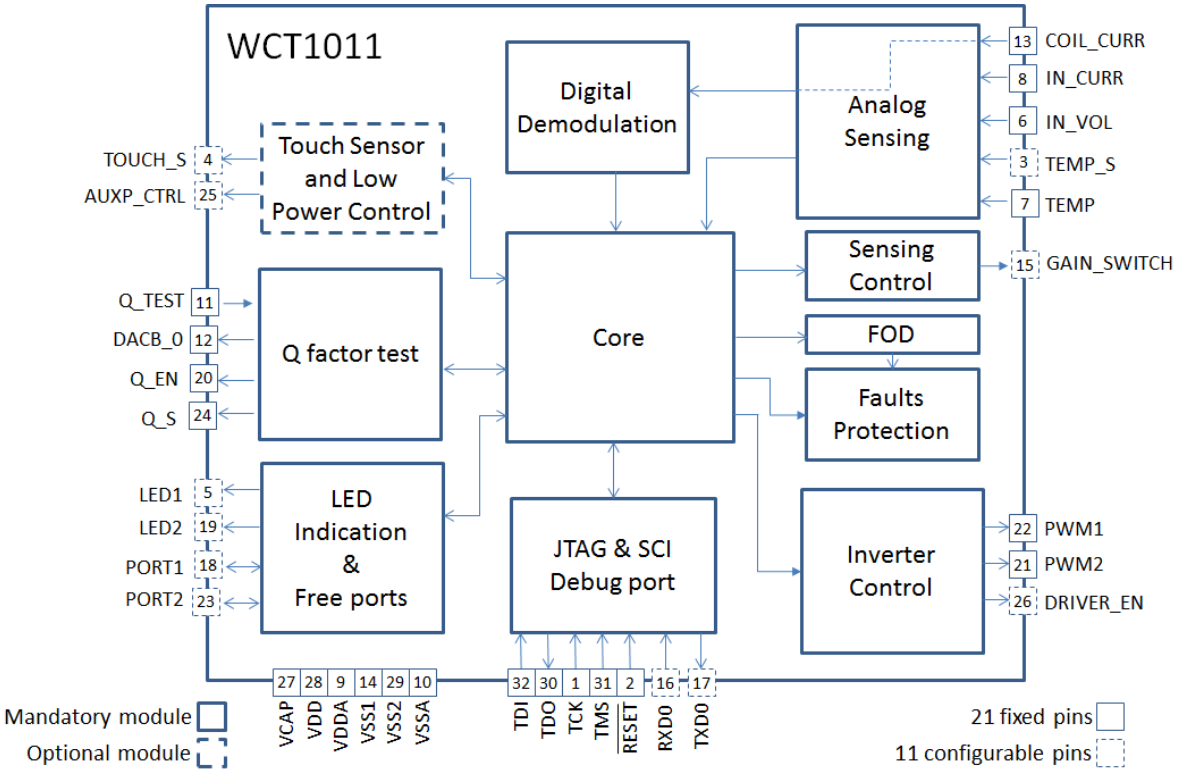


Figure 2 WCT1011 functional block diagram

4.2 Pinout diagram

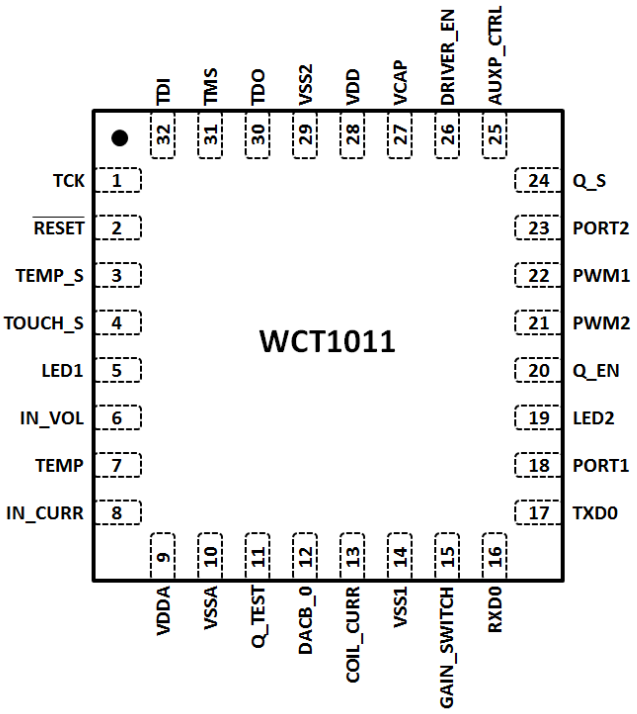


Figure 3 WCT1011 pin configuration (32-pin QFN)

4.3 Pin function description

By default, each pin is configured for its primary function (listed first). Any alternative functionality, shown in parentheses, must be programmed through FreeMASTER GUI tool.

Table 8 Pin signal descriptions

Signal name	Pin No.	Type	Function description
TCK	1	Input	Test clock input, connected internally to a pull-up resistor
$\overline{\text{RESET}}$	2	Input	A direct hardware reset, when RESET is asserted low, device is initialized and placed in the reset state. Connect a pull-up resistor and decoupling capacitor
TEMP_S	3	Output	Analog switch selection to extend analog input number
		Input/Output	General purpose input/output pin
TOUCH_S	4	Input	GPIO touch sensor input
		Input/Output	General purpose input/output pin
LED1	5	Output	LED drive output for system status indicator

		Input/Output	General purpose input/output pin
IN_VOL	6	Input	Input voltage detection, analog input pin
TEMP	7	Input	Temperature detection, analog input pin
IN_CURR	8	Input	Input current detection, analog input pin
VDDA	9	Supply	Analog power to on-chip analog module
VSSA	10	Supply	Analog ground to on-chip analog module
Q_TEST	11	Input	Q factor detection, analog input pin
DACB_0	12	Output	DAC output for Q factor detection
COIL_CURR	13	Input	Primary coil current detection, analog input pin
VSS1	14	Supply	Digital ground to on-chip digital module
GAIN_SWITCH	15	Output	Switch the gain of primary coil current detecting circuit
		Input/Output	General purpose input/output pin
RXD0	16	Input	QSCI receive data pin
		Input/Output	General purpose input/output pin
TXD0	17	Output	QSCI transmit data pin
		Input/Output	General purpose input/output pin
PORT1	18	Input/Output	General purpose input/output pin
LED2	19	Output	LED drive output for system status indicator
		Input/Output	General purpose input/output pin
Q_EN	20	Output	Q factor detection control pin, enable: low level; disable: high level
PWM2	21	Output	PWM output 2, control one half of inverter bridge
PWM1	22	Output	PWM output 1, control another half of inverter bridge
PORT2	23	Input/Output	General purpose input/output pin
Q_S	24	Output	Output pin for Q factor detection
AUXP_CTRL	25	Output	Auxiliary power control pin, enable: high level; disable: low level
		Input/Output	General purpose input/output pin
DRIVER_EN	26	Output	Pre-driver chip output enable pin, enable: high level; disable: low level
		Input/Output	General purpose input/output pin
VCAP	27	Supply	Connect a 2.2μF or greater bypass capacitor between this pin and VSS

VDD	28	Supply	Digital power to on-chip digital module
VSS2	29	Supply	Digital ground to on-chip digital module
TDO	30	Output	Test data output
TMS	31	Input	Test mode select input, connect a pull-up resistor to VDD
TDI	32	Input	Test data input, connected internally to a pull-up resistor

4.4 Ordering information

Table 9 lists the pertinent information needed to place an order. Consult a NXP Semiconductors sales office or authorized distributor to determine availability and to order this device.

Table 9 WCT1011 ordering information

Device	Supply voltage	Package type	Pin count	Ambient temp.	Order number
MWCT1011	2.7 to 3.6V	Quad Flat No-leaded (QFN)	32	-40 to +85℃	MWCT1011CFM

4.5 Package outline drawing

To find a package drawing, go to nxp.com and perform a keyword search for the drawing's document number of 98ASA00473D.

5 Wireless Charging System Operation Principle

5.1 Fundamentals

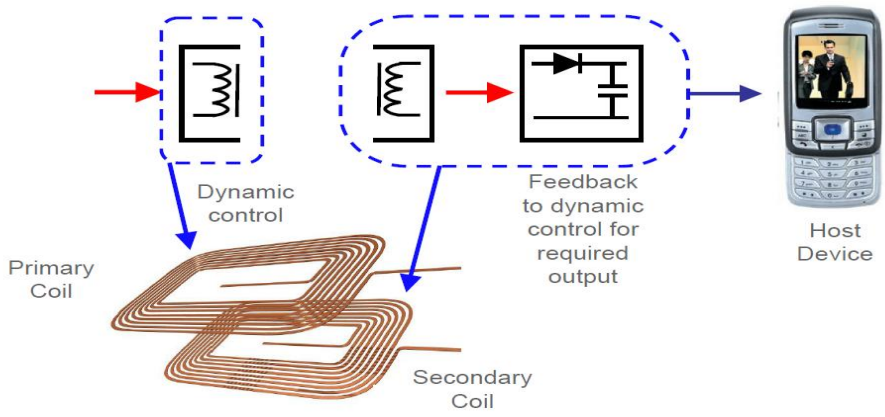


Figure 4 Working principle of the Wireless Charging System

The Wireless Charging system works as the digital switch mode power supply with the transformer, which is separated into two parts: The primary coil of transformer is placed on the transmitter, working as the TX coil, and the secondary coil of transformer is placed on the receiver side as the RX coil. The basic system working principle diagram is shown in Figure 4. As this system works based on magnetic induction, and better coupling between the TX coil and RX coil gains better system efficiency, the RX coil should be closely and center aligned with the TX coil as possible. After the RX coil receives the power from the TX coil by magnetic field, it regulates the received voltage to power the load, and send its operational information to TX according to specific protocol by the communication link. Before entering power transfer, TX also sends its operational information to RX for advanced power transfer contract establishing. Then the system can achieve the closed-loop control, and power the load stably and wirelessly.

5.2 Power transfer

When the wireless charging receiver is centrally placed on the transmitter coil, and, at the same time, the required conditions are met, the power transfer starts.

- The TX coil and RX coil meet proper specifications, such as the inductance, coil dimensions, coil materials, and magnets shielding.
- The distance is in suitable range (less than 6 mm for Z axis) between the TX coil and RX coil.
- The RX coil should be in the active area of the TX charging surface, which means that the TX coil and RX coil should be well coupled. Coil's coupling factor highly impacts the power transfer efficiency, and good coupling can achieve high efficiency.

The coil shielding is also important, because the magnetic field leaking into the air does not transfer power from TX to RX, and the shielding can contain the magnetic field as much as possible to improve the

system efficiency and avoid bad effect of the nearby objects from interference. The shielding should be designed to place at the back of the TX coil and RX coil.

The power transfer must function correctly under the conditions when the RX coil is placed on the TX charging area during the overall system operational phases. To facilitate power transfer control, set the system operation frequency on the right side of resonant frequency of resonant network (because resonant converter works in a soft-switching mode when its operation frequency is over the resonant frequency and its output power changes monotonously with the adjustment of the operation frequency).

For WPC specification, the "Qi" defines the coil inductance and resonant capacitance, the resonant frequency is fixed at 100 kHz, then power transfer can work normally by adjusting the TX operation frequency from 110 kHz to 205 kHz with fixed 50% duty cycle. Besides, the switching topology and phase difference control at breakpoint frequency would be used when charging the extended power profile power receiver. Higher TX operation frequency means lower power transferred to RX, and lower TX operation frequency means higher power transferred to RX. The duty cycle decreases when the operation frequency reaches to 205 kHz and RX requires lower transferred power. When charging the extended power profile power receiver, TX switches the topology to full bridge from half bridge and decreases the phase difference from the initial phase difference when the operation frequency reaches the breakpoint frequency and higher transferred power is required. When the phase difference reaches zero degree, the operation frequency is adjusted again. Figure 5 shows the voltage gain (voltage on resonant inductor vs. the input voltage) change with operation frequency. Voltage gain increases while operation frequency decreases.

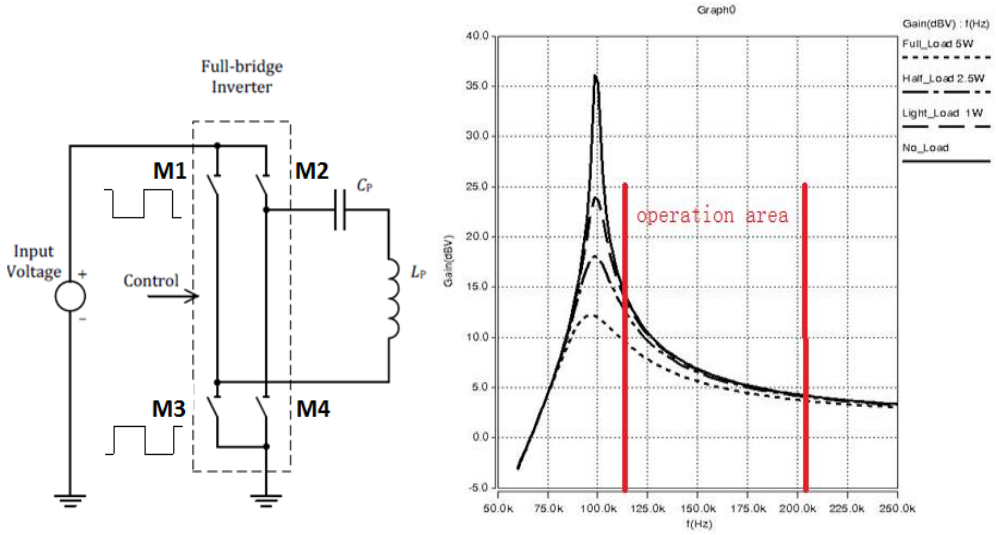


Figure 5 LC parallel resonant converter control principle

5.3 Receiver to transmitter communication

In extended power profile wireless charging application, there is two-way communication link between the receiver and the transmitter. This section is mainly about the communication from RX to TX.

5.3.1 Modulator

The receiver sends the information to the transmitter by communication packages. The information includes the power requirements, received power, receiver ID and version, receiver power ratings, and charging end command.

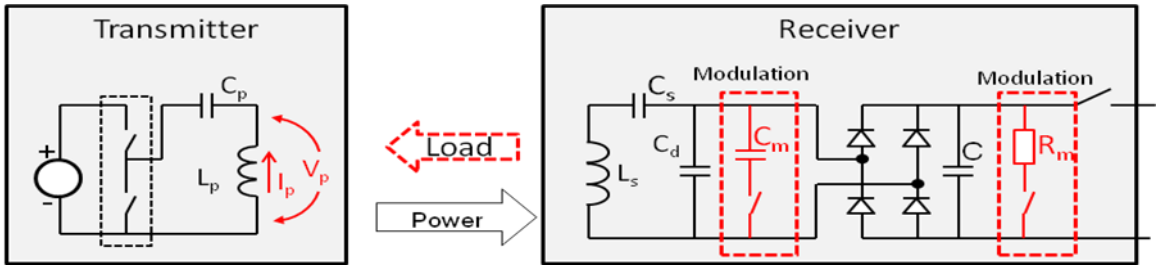


Figure 6 Load modulation scheme

Figure 6 shows the modulation technologies at the RX side. RX modulates load by switching modulation resistor (R_m, AC side or DC side), or modulation capacitor (C_m, AC side). The amplitude of voltage/current on RX coil is modulated by connecting or disconnecting modulation load (resistor or capacitor). The amplitude of voltage/current on TX coil is also modulated to reflect load switching through magnetic induction. Then TX demodulates the sensed amplitude change of current (ΔI_p > 15mA), or voltage (ΔV_p > 200mV) on TX coil. Figure 7 shows how the RX switching modulation capacitor affects the TX resonant characteristics (Gain vs. Frequency characteristics).

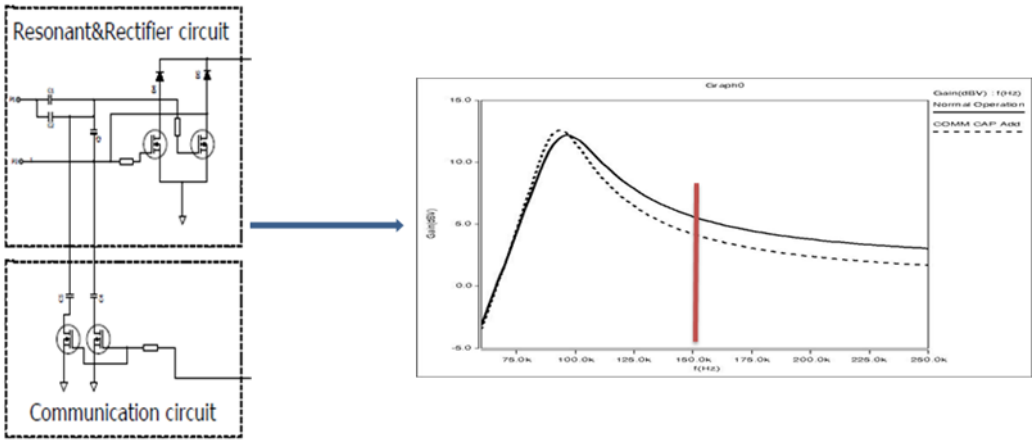


Figure 7 Load modulation principle

The Bode diagram in Figure 7 shows that the voltage amplitude on the TX coil decreases when the modulation capacitor is connected on the RX side and the RX couples the communication signal onto the power signal through modulating power signal directly. WPC defines the modulation baud rate to 2 kbps.

5.3.2 Demodulator

As the RX modulates the communication signal on the power signal, the TX has to demodulate communication signal from power signal to get the correct information sent by RX, and further control the whole system operation. Figure 8 shows the power signal (voltage) waveform coupled with communication signal on TX coil.

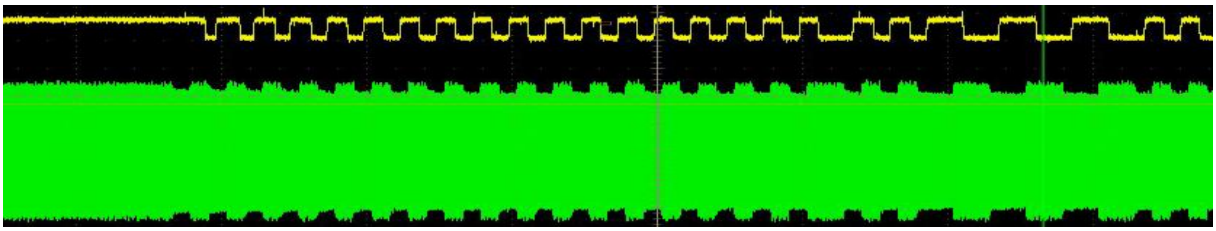


Figure 8 TX coil voltage profile with RX modulation

The WCT1011 employs software solution to implement demodulator, also called digital demodulation technology. WCT1011 directly senses the voltage on resonant capacitor through a very simple, low cost RC circuit (Figure 9), and the high-speed 12-bit cyclic ADC is capable of handling the maximum 205 kHz signal in time to assure accurate signal sampling. After the resonant capacitors voltage value is obtained, the equivalent resonant current in the coil can be calculated, and this coil current is used for the digital demodulation algorithm. After that, the WCT1011 demodulates the signal to get the packet from RX.

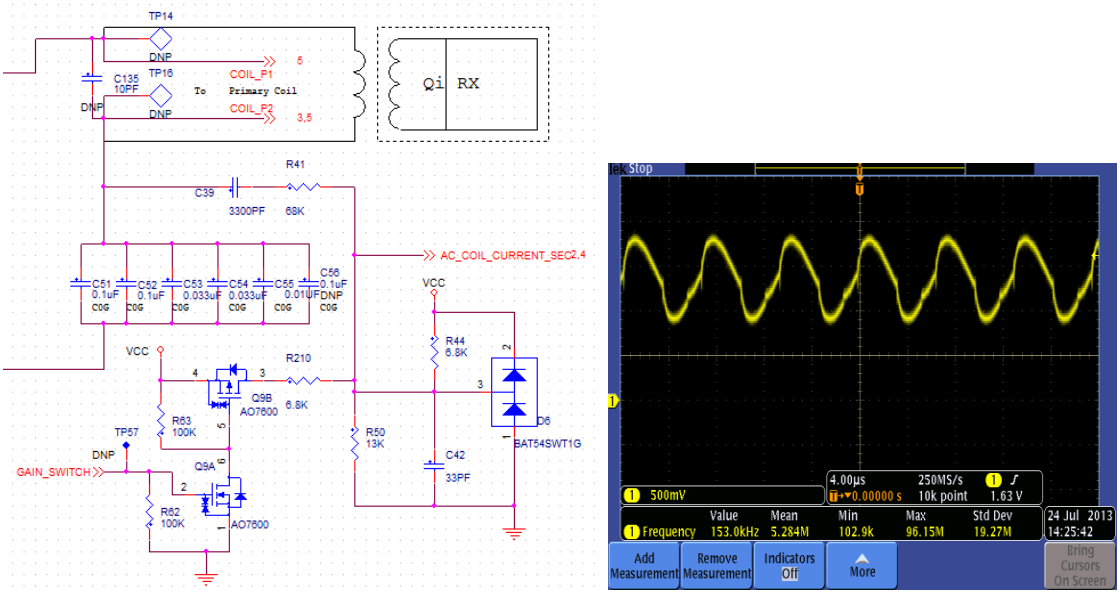


Figure 9 Sensing circuit and waveform of TX resonant capacitor voltage

With NXP digital demodulation algorithm, the WCT1011 can support all modulation types on the RX, such as AC resistor, DC resistor, or AC capacitor.

5.3.3 Message encoding scheme

The WCT1011 demodulates and decodes the message sent from RX, which is encoded by differential bi-phase scheme. A logic ONE bit is encoded using two transitions in the 2 kHz clock period (500 us), and a logic ZERO bit using one transition. One Start bit, 8-bit data, one Parity bit and one Stop bit compose one message byte. A typical packet consists of four parts, namely a preamble (≥ 11 bits), a header (1 byte), a message (1 to 27 bytes), and a checksum (1 byte). Figure 10 shows the detailed message encoding scheme that WPC defines. Digital demodulation module in WCT1011 extracts the digital encoded communication signal from the analog power signal.

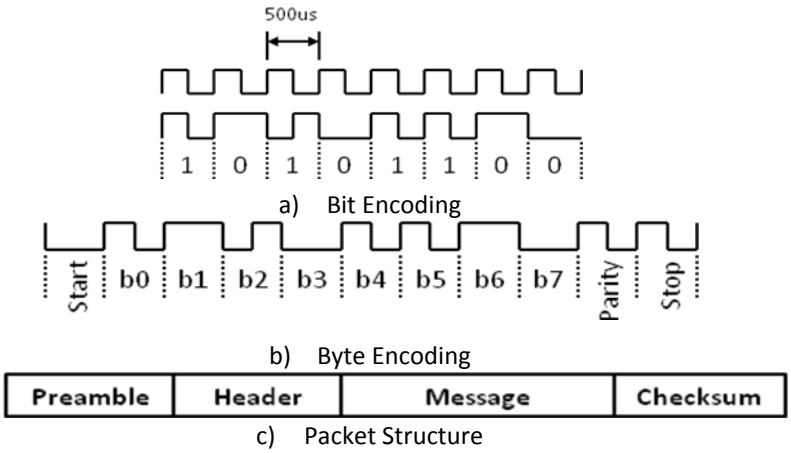


Figure 10 WPC RX to TX communication message encoding scheme

5.4 Transmitter to receiver communication

In extended power profile wireless charging application, there is two-way communication link between the receiver and the transmitter. TX sends messages to RX by FSK.

5.4.1 Modulator

The transmitter sends information to the receiver by communication packages and patterns (ACK, NAK, ND). Packages include transmitter ID and version, guaranteed power, and potential power.

The Power Transmitter modulates the power signal by switching its operation frequency between two states, namely f_{op} and f_{mod}. A modulation level is characterized in that frequency of the Power Signal that is constant at either f_{op} or f_{mod} for 256 +/- 3 cycles. The allowed change in frequency (f_{op} or f_{mod}) must be less than 3% over 400 ms.

The equation shown in below table takes into account two variables from the Power Receivers' configuration packet: FSKDepth and FSKPolarity. FSKDepth defines the amount that the period of the waveform must change and FSKPolarity defines whether the period must increase or decrease (0 for period decrease and 1 for increase).

Table 10 Equation of fmod

FSKPolarity=0	**FSKPolarity**=1

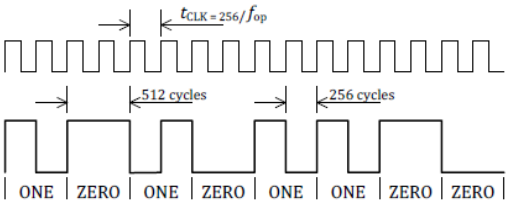
$f_{mod} = \frac{1}{\left(\frac{1}{f_{op}} - (2^{\text{FSKDepth}} \times 31.25\ \text{ns})^{+32\text{ns}}_{-1\text{ns}}\right)}$	$f_{mod} = \frac{1}{\left(\frac{1}{f_{op}} + (2^{\text{FSKDepth}} \times 31.25\ \text{ns})^{+32\text{ns}}_{-1\text{ns}}\right)}$

The Power Transmitter modulates the Power Signal at specific time slot to avoid interrupting communication packets from the Power Receiver. The Power Transmitter may modulate the Power Signal only when responding to Request packets sent by the Power Receiver during the Negotiation phase, Calibration phase and Power Transfer phase.

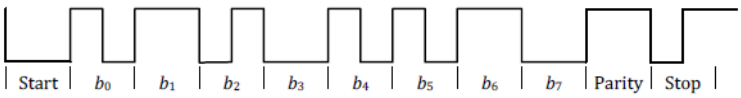
5.4.2 Message encoding scheme

The Power Transmitter uses a differential bi-phase encoding scheme to modulate data bits onto the Power Signal. For this purpose, the Power Transmitter aligns each data bit to 512 periods of the Power Signal frequency. The Transmitter encodes a logic ONE bit by using two transitions in the Power Signal frequency. The first transition occurs at the beginning of the bit period and the second transition occurs after 256 cycles of the Power Signal. The Transmitter encodes a logic ZERO bit by using a single transition in the Power Signal frequency and then remaining at the new frequency for 512 cycles of the Power Signal.

One Start bit, 8-bit data, one Parity bit and one Stop bit compose one packet byte. A typical packet consists of three parts, namely, a header (1 byte), a message, and a checksum (1 byte). Figure 11 shows the detailed message encoding scheme that WPC defines. Besides, patterns (ACK, NAK, ND) just contain one 8-bit data, without header, checksum, Start bit and Stop bit.



(a) Bit Encoding Example



(b) Byte Encoding

(c) Packet Format

Figure 11 WPC TX to RX communication message encoding scheme

5.5 System control state machine

WCT1011 embeds a WPC "Qi" State Machine to process received communication message from RX and control power transfer to RX. The overall system behavior between transmitter and receiver is controlled by the state machine shown in Figure 12.

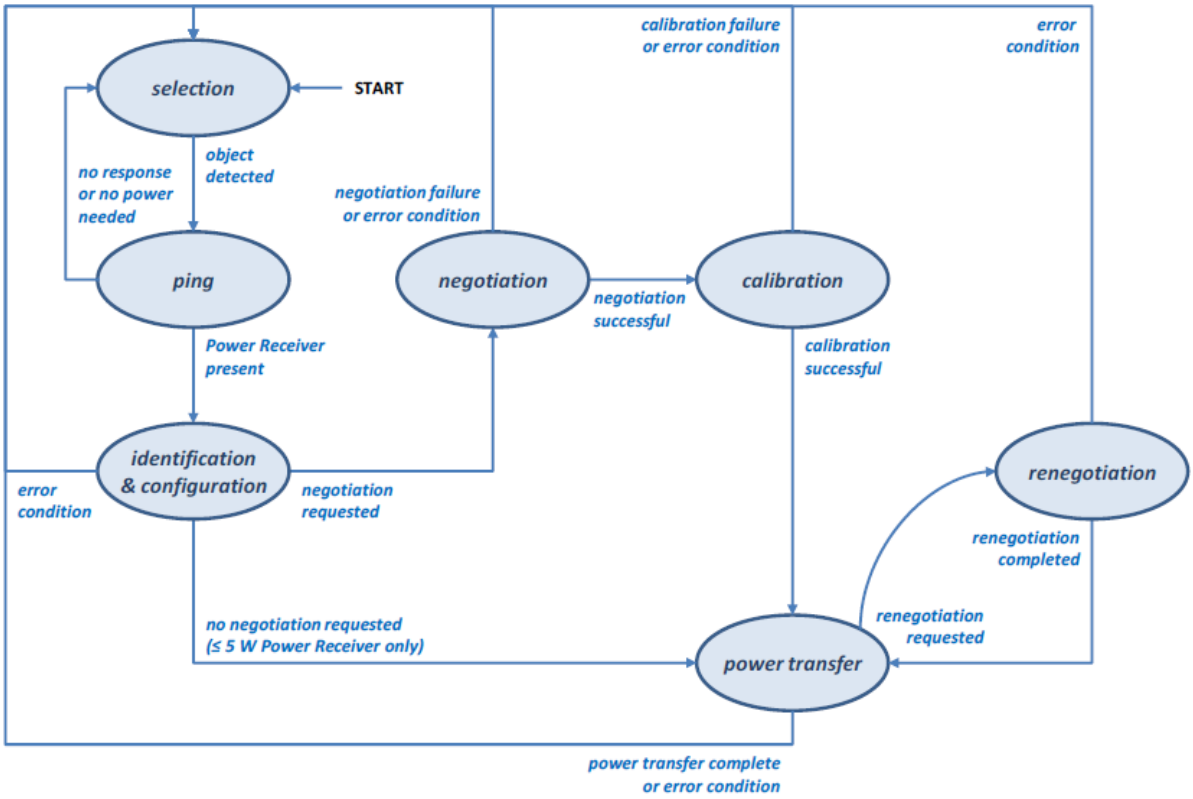


Figure 12 WPC Wireless Charging System state machine

5.5.1 Selection phase

During the Selection phase, the TX system runs in low power mode to judge whether an object is placed on the TX coil surface. The PING operation runs every 400 ms, and during the PING interval, the system is in the Selection phase. If the touch sensor module is enabled, WCT1011 enters deep low power mode as described in the Standby Power section.

5.5.2 Ping phase

During the Ping phase, the TX system works on both analog PING and digital PING to detect a receiver placed on the TX charging area. The analog PING time is far shorter than the digital PING for power-saving purposes. The analog PING enables a very short AC pulse on the TX coil, WCT1011 reads back the coil current and compares it with the predefined current change threshold to judge whether an object is put on. The default coil current change threshold is 5%, which the user can set in FreeMASTER GUI to get good sensitivity.

For digital PING, the TX system applies a power signal at 175 kHz with 50% duty cycle to attempt to set up communication with RX. In response, RX must send out the Signal Strength packet. Signal Strength message indicates the degree of coupling between TX coil and RX coil, and is the percentage of rectifier output signal against the possible maximum PING signal.

$$\text{Signal Strength Value} = \frac{U}{U_{max}} \times 256$$

In this formula, U is the monitored variable, and U_{max} is the maximum value, which the RX expects for during digital PING.

When the Signal Strength packet is received in the Ping phase, the system enters the Identification & Configuration phase.

5.5.3 Identification & Configuration phase

In the Identification & Configuration phase, the TX system continues to identify the receiver device and collects the configuration information to establish a default power transfer contract.

After receiving the configuration packet, the TX performs as follows:

- If the Neg bit in the received configuration packet is set to ZERO, the TX proceeds to the Power Transfer phase without sending a response.
- If the Neg bit in the received configuration packet is set to ONE, the TX sends an ACK response in right timing after the end of the received configuration packet. Subsequently, the TX proceeds to the Negotiation phase.
- If the TX does not proceed to the Power Transfer phase or to the Negotiation phase, the TX removes the power signal in right timing after the end of the configuration packet.

5.5.4 Negotiation phase

During the Negotiation phase, the Power Transmitter receives a series of Packets that contain requests to update the Power Transfer Contract. In response to each Packet, the Power Transmitter sends either of the following:

- A Response to indicate whether it grants the request, denies the request, or does not recognize the request
- A data packet that contains the requested information

Prior to receiving the requests to update the Power Transfer Contract, the Power Transmitter creates a temporary copy of the Power Transfer Contract. The Power Transmitter uses this temporary copy to store updated parameters until successful completion of the Negotiation phase.

5.5.5 Calibration phase

During the Calibration phase, the Power Transmitter receives information from the Power Receiver that the Power Transmitter can use to improve the power loss method for Foreign Object Detection. In

particular, the Power Transmitter receives the Received Power information, with the Power Receiver attached:

- A “light” load
- A “connected” load

If the Power Transmitter does not receive this information, it removes the Power Signal and returns to the Selection phase. In addition, the Power Transmitter attempts to use this information to improve its power loss method only if it ensures that there is no Foreign Object present.

In the Calibration phase, the behavior of the Power Transmitter is the same as in the power transfer phase, with the following additions:

- If the Power Transmitter receives a 24-bit Received Power Packet with Mode = ‘001’ (calibration mode for a light load), and the Received Power Value satisfies the Power Transmitter, it sends an ACK Response. Otherwise, it sends a NAK Response.
- If the Power Transmitter receives a 24-bit Received Power Packet with Mode = ‘010’ (calibration mode for a connected load), and the Received Power Value satisfies the Power Transmitter, it sends an ACK Response and proceed to the Power Transfer phase. Otherwise, it sends a NAK Response.
- If the Power Transmitter receives a 24-bit Received Power Packet with a Mode value other than ‘001’ and ‘010’, it removes the Power Signal and returns to the Selection phase.

5.5.6 Power Transfer phase

The extended power profile TX can discriminate between baseline power profile RX and extended power profile RX.

- During the Power Transfer phase, if the RX is a baseline power profile receiver, the TX configures the inverter to half bridge firstly, and then the TX system receives the Control Error packet from the RX and controls the amount of transferred power by adjusting the operation frequency in the range of 110 kHz – 205 kHz with 50% duty cycle.
    - If the operation frequency reaches 110 kHz and the positive Control Error value is still received (more output power required), the TX system keeps the current power output.
    - If the operation frequency reaches 205 kHz and the negative Control Error value is still received, the TX system decreases PWM duty cycle in the range from 50% to 10%.
- During the Power Transfer phase, if the RX is an extended power profile receiver, the TX configures the inverter to half bridge firstly, and then the TX system receives the Control Error packet from the RX and controls the amount of transferred power by adjusting the operation frequency. When the operation frequency reaches breakpoint frequency and higher power is required, the TX configures the inverter to full bridge from half bridge, and then adjusts the phase difference from the initial phase difference, while the phase difference reaches zero degree, the operation frequency is then adjusted again. When the operation frequency is in the 110 kHz – 205 kHz range, the duty cycle is 50%.

- If the operation frequency reaches 110 kHz and the positive Control Error value is still received (more output power required), the TX system keeps the current power output.
- If the operating frequency reaches 205 kHz and the negative Control Error value is still received, the TX system decreases PWM duty cycle in the range from 50% to 10%.

During the Power Transfer phase, the TX system also executes the FOD algorithm by using the Received Power packet from the RX, and the TX system always checks the timing of the Control Error packet and the Received Power packet, and whether it complies with specification. If any violation occurs, the TX system ends the power transfer. If the mode of the Received Power packet is '000', the TX sends ACK/NAK to the RX. If the mode is '100', the responses are not needed.

5.5.7 Renegotiation phase

During the Renegotiation phase, the TX's behaviors are the same as the ones in the Negotiation phase with the following exceptions:

- If the Power Transmitter receives a Control Error Packet, Received Power Packet, or Charge Status Packet, it discards the temporary Power Transfer Contract, and returns to the Power Transfer phase.
- If the Power Transmitter receives a FOD Status Packet, it sends an ND Response.
- If the Power Transmitter received a Specific Request Packet with Request = 0x00 (End Negotiation), it bases its Response on a verification of the Count Value only.

5.6 Standby power

When there is no charging activity, the TX system enters the standby (Selection phase) mode. In standby mode, all the analog parts on the TX board are powered down by the WCT1011, and the WCT1011 itself runs in low power state during the PING interval. The WCT1011 can enter deep sleep state if NXP GPIO Touch Sensor technology is supported in the TX system. In this use case, WCT1011 is in LPSTOP (low power STOP) state, only one GPIO touch pad, timer and CPU are periodically activated to sense the electrode capacitance change to detect if an object is placed on the TX charging area.

5.7 Foreign object detection

The WCT1011 solution supports the power class 0 FOD framework, which is based on the calibrated power loss method and quality factor (Q factor) method.

6 Application Information

6.1 On-board regulator

The auxiliary power supply provides the voltage source for control, sensing, communication, and MOSFET driver. In power transmitter design, 3.3 V is required for the WCT1011, ADC conditioning circuits, and communication demodulation circuits. 12 V input voltage is supplied for inverter pre-driver circuit. Step-Down Converter MP2314 is selected to generate 3.3 V with 2 A drive capacity. At the same time, other type Step-Down converter can be used to meet the requirements, and the following parameters must be considered for the regulator selection.

- Maximum input voltage: > 14V
- Maximum output current: > 100 mA

6.2 Inverter and driver control

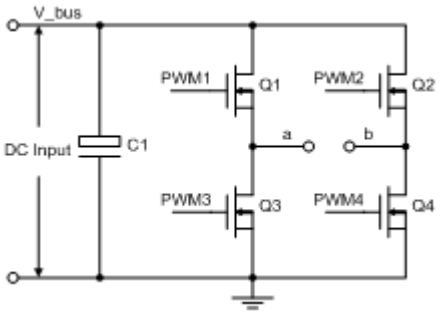


Figure 13 Full-bridge inverter topology

Figure 13 shows the schematic of full-bridge inverter. The input voltage range of this application is from 11 to 13 volts, the input current range is from 0 to 2 amps. LC resonant network is connected between the middle point (a) of bridge leg 1 and the middle point (b) of bridge leg 2. N-channel MOSFETs of Q1–Q4 are controlled by PWMs generated from WCT1011, and the operation frequency range of MOSFETs is 110 kHz to 205 kHz. In addition, the inverter can be configured as half bridge topology by normally turning on the low-side MOSFET (Q4 or Q3) and turn off the high-side MOSFET (Q2 or Q1). To meet the system efficiency and power transfer requirements, these are some suggestions for the MOSFETs and driver IC selection.

- Full-bridge inverter MOSFETs: V_{ds} >= 30 V, $R_{ds(on)}$ < 20 mΩ for power switching application MOSFET is recommended. The MOSFET is the critical component for the system efficiency, AON7400A from AOS is selected as the main power switch, and AON7400A is a 30 V, 40 A, $R_{ds(on)}$ < 10.5 mΩ (V_{gs} = 4.5 V), N-channel power MOSFET.
- Driver: the synchronous BUCK driver IC or bridge driver IC can meet the requirements for the full-bridge inverter. The driver IC handles 14 V voltage input for some de-rating applications. The

synchronous BUCK driver IC is recommended for this application because of good cost advantage, so NCP3420DR2G is selected on this design. This driver IC has the following features:

- Maximum main supply voltage input is 15V.
- Very short propagation delay from input to output (less than 30 ns).
- 2 channels PWM can be controlled by WCT1011 independently.
- Safety Timer and Overlap protection circuit.

6.3 Primary coil and resonant capacitor

The resonant network is shown in Figure 14, which is the basic LC series resonant network circuit. The section of "Power Transfer" in chapter of "Wireless Charging System Operation Principle" describes the basic operation fundamental of LC resonant inverter. For the design principles of resonant components parameters, follow the below two points:

- Set a fixed resonant frequency (WPC defines it as 100 kHz)
- Configure a suitable Q (quality factor) value to output required power in specific operation range like WCT-15W1COILTX type, C_r = 276 nF, L_p = 8.9uH, these resonant network parameters can meet the extended power profile (15 W) wireless charging requirements under defined operation conditions.

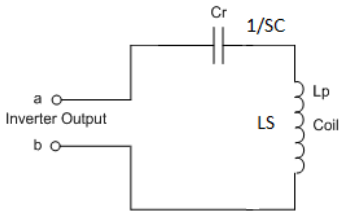
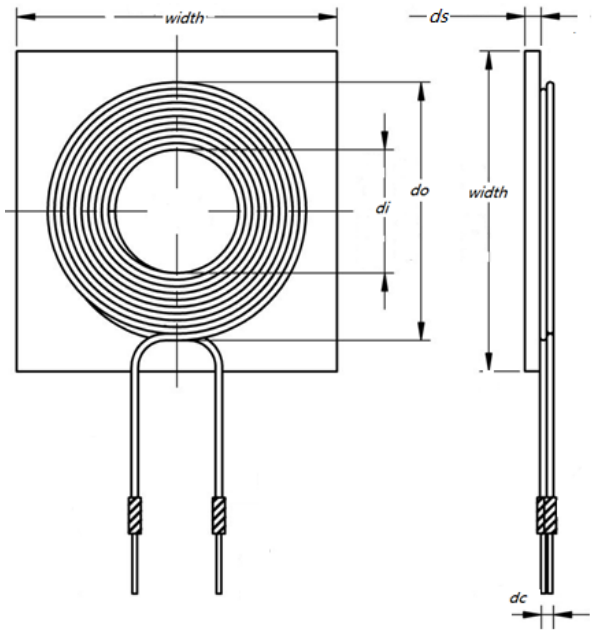


Figure 14 Schematic resonant network circuit

L_p and C_r are connected in series, the resonant frequency of WCT-15W1COILTX resonant network can be obtained:

$$fr = \frac{1}{2\pi\sqrt{LpCr}} = \frac{1}{2\pi\sqrt{8.9 \times 10^{-6} \times 276 \times 10^{-9}}} = 100kHz$$

The electrical and mechanical features of the TX coil are defined in details. Figure 15 shows the mechanical features of WCT-15W1COILTX coil type.



Parameter	Symbol	Value
Shield Inductance	Lp	8.9uH±10%
Outer diameter	do	$48.5^{\pm 1.0mm}$
Inner diameter	di	$23.0^{\pm 1.0mm}$
Thickness	dc	$2.0^{\pm 0.5mm}$
Number of turns per layer	N	11
Number of layers	-	1
Shielding materials	-	Soft-magnetic materials

Figure 15 WCT-15W1COILTX round coil mechanical features

For resonant capacitor, COG ceramic capacitor is selected to meet the critical system requirements, because the capacitance affects the resonant frequency of resonant network, 5% tolerance is allowed for the whole system operation. This capacitance with WCT-15W1COILTX coil can achieve the 100 kHz resonant frequency. Three types of capacitors are recommended to select:

- Murata: GRM3195C2A333JA01D – 1206 –100V – 33nF (2 pcs)
- Murata: GRM31C5C2A104JA01L –1206-100V – 100 nF (2 pcs)
- Murata: GRM3195C2A103JA01 – 1206 –100V – 10nF (1 pcs)

6.4 Low power control

To achieve low power consumption, the driver and analog circuits power are shut down when the system is in standby mode or interval time between the PINGs. AUXP_CTRL signal is designed to achieve this target. Figure 16 shows the typical application circuit to control VDRIVER and AVCC_Q on or off.

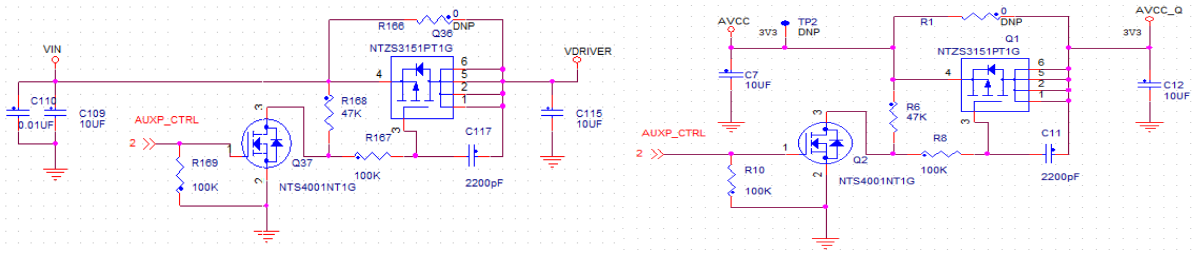


Figure 16 Low power control circuit

The power source of the inverter drivers, current sensor amplifier and Q factor detection circuits can be controlled by the above circuit. This circuit is still benefited from the Touch Sensor technology. When the TX goes to the standby mode, the WCT1011 enters deep sleep mode, and the power of the driver and analog circuits is shut down by the AUXP_CTRL signal.

6.5 GPIO touch sensor

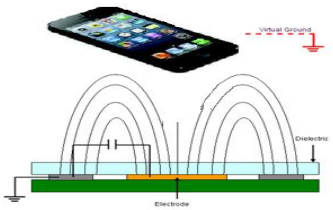


Figure 17 Basic theory of capacitive touch sensor

Capacitive touch sensor is selected in this design, and an additional electrode touch pad is designed to sense the placement of mobile device. When the mobile device is put on the TX coil, GPIO touch sensing detects the capacitance change on the pad, and then enters digital PING phase for device identification. Figure 17 shows the basic theory for this method.

Because of the FOD function, this electrode touch pad should not be placed on the top of the TX coil, and 5 mm XY (horizontal) distance is required between the TX coil and the electrode touch pad.

6.6 ADC input channels

To sense the necessary analog signals in the TX system, 5 ADC input channels are designed for these analog signals, and 1 DAC output channel is used for Q factor detection. This list describes the design details of these analog signals in the default setting. For the specific circuits, see the system example design schematics.

- Input voltage: 154 kΩ and 20 kΩ resistors to divide the input voltage, and when the Q factor detection is enabled, the 20 kΩ resistor is disconnected.
- Temperature: 100 kΩ NTC (NCP15WL104E03RC) and 51 kΩ resistors are recommended to sense the temperature of board or coil (over-temperature protection point: 60°C @ 0.94 ADC input).
- Input current: 15 mΩ current sensing resistor and 1:100 current sensor (CS30CL) are recommended.
- Q_TEST: Operational amplifier and analog switch are used for Q factor detection.
- Coil current: The resistors are used to divide the resonant capacitor voltage. The scale is changed when GAIN_SWITCH is enabled.

6.7 Faults handling/recovery

WCT1011 supports several types of fault protections during the TX system operation, including the FOD fault, TX system fault, and RX device fault. According to the fault severity, the faults are divided into several rates: fatal fault, immediate retry fault, and retry fault after several minutes. The fault thresholds and time limits are described in the *WCT1012 15W V3.0 Single Coil TX Runtime Debugging User's Guide* (WCT1012V30RTDUG).

Table 11 lists all the available fault types and their corresponding fault handlings.

Table 11 System faults handling

Types	Name	Handling	Recovery wait time	Conditions	Description
FOD Fault	FOD fault	TX system shuts off after fault lasts 1 second	Wait 5 minutes or RX removed	1, Power loss base threshold 2, Power loss indication to power cessation 3, Power loss fault retry times	Foreign object is detected and lasts for the defined time. The system shuts off, and waits for recovery time or RX removed to enable power transfer. The time limit can be configured by user.
TX System Fault	Hardware fault (ADC, Chip)	TX system shuts off immediately	No retry any more	-	Once hardware fault happens, the TX system shuts off forever.
	EEPROM corruption fault	TX system shuts off immediately	No retry any more	-	The WCT1011 checks data validity of EEPROM after power on, stop running forever if EEPROM is corrupted.
	Input over-voltage	TX system shuts off immediately	No retry any more	Safety input threshold	When input voltage exceeds the threshold, the TX system shuts off immediately and waits for recovery time to enable power transfer.

	Input over-power	TX system shuts off immediately	Wait for 5 minutes or RX removed	Input power threshold	When input power exceeds the threshold, the TX system shuts off immediately and waits for recovery time to enable power transfer.
	Coil over-current	TX system shuts off immediately	Retry immediately	Coil current threshold	When coil current exceeds the threshold, the TX system shuts off immediately and tries PING again.
	TX over-temperature	TX system shuts off immediately	Wait for 5 minutes or RX removed	Temperature threshold	When the temperature on the board or the coil exceeds the threshold during power transfer, the TX system shuts off immediately and waits for recovery time or RX removed to enable power transfer.
RX Device Fault	RX internal fault (EPT-02)	TX system shuts off immediately	No retry any more	-	The TX system shuts off forever if End Power packet is received and End Power code is internal fault.
	RX over-temperature (EPT-03)	TX system shuts off immediately	Wait for 5 minutes or RX removed	-	The TX system shuts off and waits for recovery time to enable power transfer if End Power packet is received and End Power code is over temperature.
	RXover-voltage (EPT-04)	TX system shuts off immediately	Retry immediately or RX removed	-	The TX system shuts off and tries PING again if End Power packet is received and End Power code is over voltage.
	RX over-current (EPT-05)	TX system shuts off immediately	Retry immediately	-	The TX system shuts off and tries PING again if End Power packet is received and End Power code is over current.
	RX battery failure (EPT-06)	TX system shuts off immediately	No retry any more	-	The TX system shuts off forever if End Power packet is received and End Power code is battery failure.

6.8 LEDs function

Two pins (user can re-configure them to different configuration ports) on WCT1011 are used to drive LEDs for different system status indication in this design, such as charging, standby and fault status, etc. The LEDs can work on different functions using software configuration. WCT1011 controls the LEDs on/off and blink according to the parameters configuration under different system status. For how to

configure LED functions by the FreeMASTER GUI tool, see the WCT1012 15W Single Coil TX Reference Design System User's Guide in the WCT-15W1COILTX reference design platform. The suggested LED functions are listed in the below table for different system status indication.

Table 12 System LED modes

LED configuration option	Description	LED #	LED operation state					
			Standby	Charging	Charge complete	FOD fault	TX fault	RX fault
Default	Default choice	LED 1	Off	Blink slow	Off	On	On	On
		LED 2	Blink slow	On	On	Off	Off	Off
Option 1	Choice 1	LED 1	Off	Blink slow	On	Off	Off	Off
		LED 2	Off	Off	Off	Blink fast	Blink fast	Blink fast
Option 2	Choice 2	LED 1	Off	On	Off	Off	Off	Off
		LED 2	Off	Off	Off	On	Blink slow	Blink slow
Option 3	Choice 3	LED 1	Off	Blink slow	On	Blink fast	Blink fast	Blink fast
		LED 2	-	-	-	-	-	-

6.9 Configurable pins

The WCT1011 supports pin multiplexer, which means that one pin can be configured to different functions. If the default on-chip functions are not used in your applications, such as GPIO touch sensor, and ultra low power control, these pins can be configured for other functions. Table 13 lists the pin multiplexer for WCT1011 configurable pins.

Table 13 Configurable pins multiplexer

Pin No.	Default Function	Alternative Function
3	TEMP_S	GPIO
4	TOUCH_S	GPIO
5	LED1	GPIO
15	GAIN_SWITCH	GPIO
16	RXD0	GPIO
17	TXD0	GPIO
18	GPIO	-
19	LED2	GPIO
23	GPIO	-
25	AUXP_CTRL	GPIO
26	DRIVER_EN	GPIO

6.10 Unused pins

All unused pins can be left open unless otherwise indicated. For better system EMC performance, it is recommended that all unused pins are tied to system digital ground with pull-down resistor and flooded with copper to improve ground shielding.

6.11 Power-on reset

WCT1011 can handle the whole system power on sequence with integrated POR mechanism, so no more action and hardware is needed for the whole system powered on.

6.12 External reset

WCT1011 can be reset when the $\overline{\text{RESET}}$ pin is pull down to logic low (digital ground). A 4.7 kΩ pull-up resistor to 3.3 V digital power and a 0.1 uF filter capacitor to digital ground are recommended for the reliable operation. This pin is used for the JTAG debug and programming purpose in this design.

6.13 Programming & Debug interface

One JTAG and one QSCI communication ports are designed for the communication with the PC. JTAG is used for the system debug, calibration, and programming. And QSCI is used for the communication with the PC to display the system information, such as input voltage, input current, coil current, and operating frequency. For the hardware design, see the system example design schematics.

6.14 Software module

The software in WCT1011 is matured and tested for production ready. NXP provides a Wireless Charging Transmitter (WCT) software library for speeding user designs. In this library, low level drivers of HAL (Hardware Abstract Layer), callback functions for library access are open to user. For the software API and library details, see the WCT1012 15W Single Coil TX Reference Design System User's Guide in the WCT-15W1COILTX reference design platform.

6.14.1 Memory map

WCT1011 has 64 Kbytes on-chip Flash memory and 8 Kbytes program/data RAM. Besides for wireless transmitter library code, the user can develop private functions and link it to library through predefined APIs.

Table 14 WCT1011 memory footprint

Memory	Total size	Example code size	Library size	FreeMASTER size	Free size
Flash	64 Kbytes	40.8 Kbytes	26.8 Kbytes	1.5 Kbytes	23.2 Kbytes
RAM	8 Kbytes	4.67 Kbytes	3.4 Kbytes	0.1 Kbytes	3.33 Kbytes

6.14.2 Software library

The WCT software library provides the complete wireless charging function which is compliant with the latest version WPC “Qi” power class 0 specification. This library includes the “Qi” communication protocol, power transfer control program, FOD algorithm, system status indication module, and fault protection module.

Figure 18 shows the complete software structure of this library. A data structure in the software library can be accessed by user code, which contains runtime data like input current, input voltage, coil current, PWM frequency and duty cycle. For the details of how to use this library, the API definitions, and the data structure, see the WCT1x1x TX Library User’s Guide in the WCT-15W1COILTX reference design platform. In addition, a FreeMASTER calibration module is integrated into this library, which enables the end product customization and FOD calibration through the QSCI port.

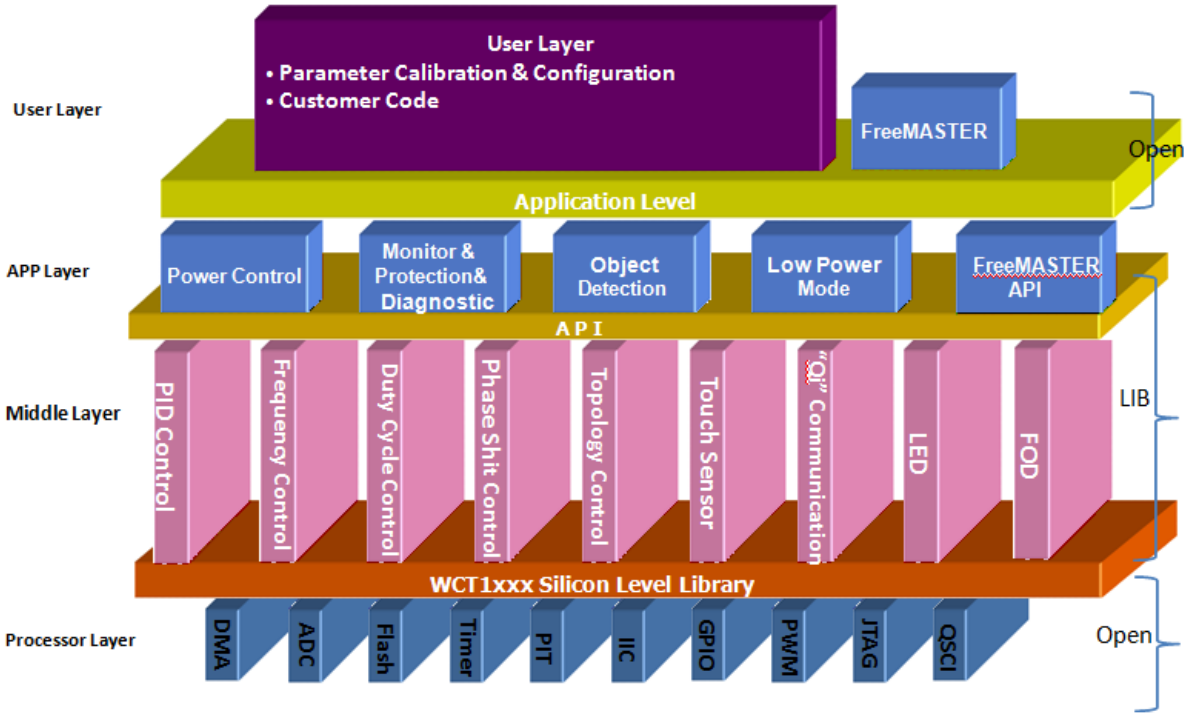


Figure 18 Software structure of WCT library

6.14.3 API description

Through WCT library APIs, the user can easily get the typical signals on TX system, such as the input voltage, input current, coil current, and PWM frequency etc. The user can conveniently know WCT1011 operational status by watching variables through the FreeMASTER GUI tool. For more information about API definitions, see the WCT1x1x TX Library User’s Guide in the WCT-15W1COILTX reference design platform.

6.15 Example design schematics

Go to the NXP website nxp.com and search “WCT1012” to find the schematic details and the WCT-15W1COILTX user guide.

7 Design Considerations

7.1 Electrical design considerations

Use the following list of considerations to assure correct operation of the device and system:

- The minimum bypass requirement is to place 0.01 - 0.1 µF capacitors positioned as near as possible to the package supply pins. The recommended bypass configuration is to place one bypass capacitor on each of the VDD/VSS pairs, including VDDA/VSSA. Ceramic and tantalum capacitors tend to provide better tolerances.
- Bypass the VDD and VSS with approximately 10 µF, plus the number of 0.1 µF ceramic capacitors.
- Consider all device loads as well as parasitic capacitance due to PCB traces when calculating capacitance. This is especially critical in systems with higher capacitive loads that could create higher transient currents in the VDD and VSS circuits.
- Take special care to minimize noise levels on the VDDA, and VSSA pins.
- Using separate power planes for VDD and VDDA and separate ground planes for VSS and VSSA are recommended. Connect the separate analog and digital power and ground planes as near as possible to power supply outputs. If an analog circuit and digital circuit are powered by the same power supply, connect a small inductor or ferrite bead in serial with VDDA traces.
- If desired, connect an external RC circuit to the RESET pin. The resistor value should be in the range of 4.7 kΩ – 10 kΩ; and the capacitor value should be in the range of 0.1 µF – 4.7 µF.
- Add a 2.2 kΩ external pull-up on the TMS pin of the JTAG port to keep device in a restate during normal operation if JTAG converter is not present.
- During reset and after reset but before I/O initialization, all I/O pins are at input mode with internal weak pull-up.
- To eliminate PCB trace impedance effect, each ADC input should have a no less than 33 pF/10 Ω RC filter.
- Need some optional circuits for the power saving function, those circuit can be removed when the design is not sensitive for this requirements, so the GPIO touch sensor and AUXP_CTRL can be removed.

7.2 PCB layout considerations

- Provide a low-impedance path from the board power supply to each VDD pin on the device and from the board ground to each VSS pin.
- Ensure that capacitor leads and associated printed circuit traces that connect to the chip VDD and VSS pins are as short as possible.

- PCB trace lengths should be minimal for high-frequency signals.
- Physically separate analog components from noisy digital components by ground planes. Do not place an analog trace in parallel with digital traces. Place an analog ground trace around an analog signal trace to isolate it from digital traces.
- The decoupling capacitors of 0.1 μF must be placed on the VDD pins as close as possible, and place those ceramic capacitors on the same PCB layer with WCT1011 device. VIA is not recommend between the VDD pins and decoupling capacitors.
- The WCT1011 bottom EP pad should be soldered to the ground plane, which makes the system more stable, and VIA matrix method can be used to connect this pad to the ground plane.
- As the wireless charging system functions as a switching-mode power supply, the power components layout is very important for the whole system power transfer efficiency and EMI performance. The power routing loop should be as small and short as possible, especially for the resonant network. The traces of this circuit should be short and wide, and the current loop should be optimized smaller for the MOSFETs, resonant capacitor and primary coil. Another important thing is that the control circuit and power circuit should be separated.

7.3 Thermal design considerations

WCT1011 power consumption is not so critical, so there is not additional part needed for power dissipation. But the full-bridge inverter needs the additional PCB Cu copper to dissipate the heat, so good thermal package MOSFET is recommended to select, such as DFN package, and for the resonant capacitor, COG material, and 1206 package is recommended to meet the thermal requirement. The transmitter system internal power loss is about 1.5 W with full 15 W loads, and the hottest part is on the inverter, so the user should make some special action to dissipate the heat. Figure 19 shows one thermal strategy for the inverter.

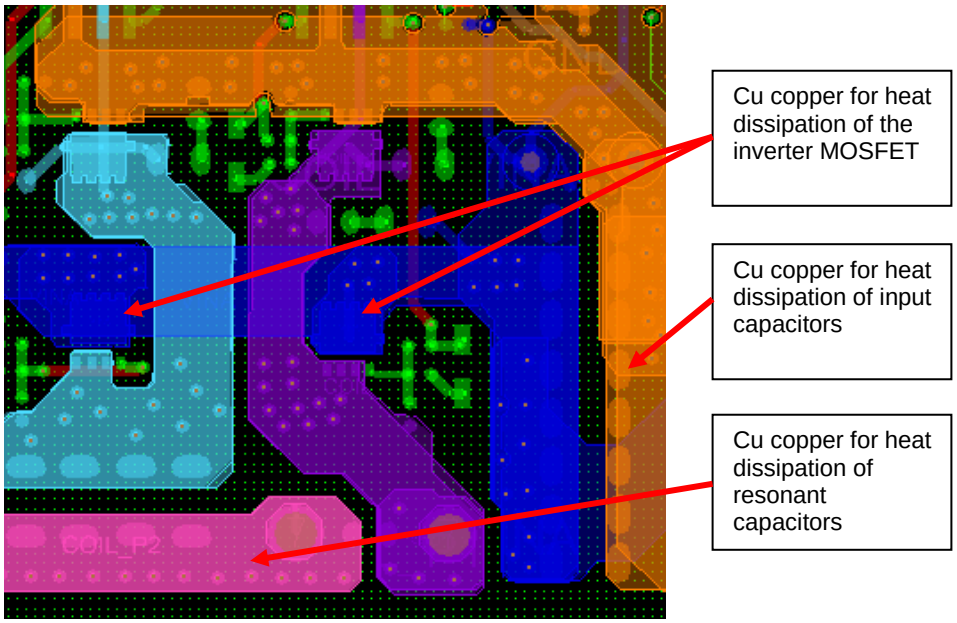


Figure 19 Thermal design strategy for inverter

8 Links

- nxp.com
- nxp.com/products/power-management/wireless-charging-ics
- www.wirelesspowerconsortium.com

9 Revision History

This table summarizes revisions to this document.

Table 15. Revision history

Revision number	Date	Substantial changes
0	09/2016	Initial release.

How to Reach Us:

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Document Number: WCT1011DS
Rev. 0
09/2016

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