

Dual N-Channel 20-V MOSFET

PRODUCT SUMMARY			
V _{DS} (V)	R _{DS(on)} (Ω)	I _D (A) ^{a, g}	Q _g (Typ.)
20	0.216 at V _{GS} = 4.5 V	1.5	1.2 nC
	0.268 at V _{GS} = 2.5 V	1.5	
	0.375 at V _{GS} = 1.8 V	1.0	

FEATURES

- Halogen-free
- TrenchFET[®] Power MOSFET
- New Thermally Enhanced PowerPAK[®] SC-75 Package
 - Small Footprint Area
 - Low On-Resistance

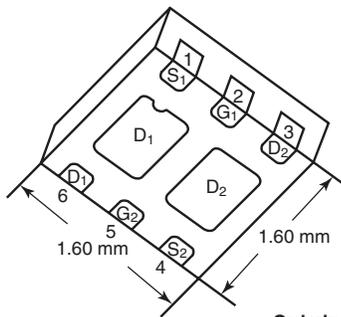


RoHS
COMPLIANT

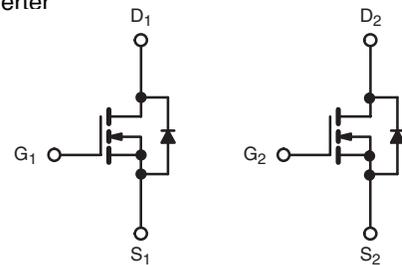
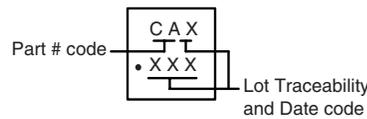
APPLICATIONS

- Load Switch, PA Switch and Battery Switch for Portable Devices
- DC/DC Converter

PowerPAK SC75-6L-Dual



Marking Code



Ordering Information: SiB912DK-T1-GE3 (Lead (Pb)-free and Halogen-free) N-Channel MOSFET N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS T _A = 25 °C, unless otherwise noted				
Parameter	Symbol	Limit	Unit	
Drain-Source Voltage	V _{DS}	20	V	
Gate-Source Voltage	V _{GS}	± 8		
Continuous Drain Current (T _J = 150 °C)	I _D	T _C = 25 °C	1.5 ^a	A
		T _C = 70 °C	1.5 ^a	
		T _A = 25 °C	1.5 ^{a, b, c}	
		T _A = 70 °C	1.4 ^{b, c}	
Pulsed Drain Current	I _{DM}	5		
Continuous Source-Drain Diode Current	I _S	T _C = 25 °C	1.5 ^a	
		T _A = 25 °C	0.9 ^{b, c}	
Maximum Power Dissipation	P _D	T _C = 25 °C	3.1	W
		T _C = 70 °C	2.0	
		T _A = 25 °C	1.1 ^{b, c}	
		T _A = 70 °C	0.7 ^{b, c}	
Operating Junction and Storage Temperature Range	T _J , T _{stg}	- 55 to 150	°C	
Soldering Recommendations (Peak Temperature) ^{d, e}		260		

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^{b, f}	t ≤ 5 s	R _{thJA}	90	115	°C/W
Maximum Junction-to-Case (Drain)	Steady State	R _{thJC}	32	40	

Notes:

- Package limited.
- Surface Mounted on 1" x 1" FR4 board.
- t = 5 s.
- See Solder Profile (<http://www.vishay.com/ppg?73257>). The PowerPAK SC-75 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.
- Maximum under Steady State conditions is 125 °C/W.
- Based on T_C = 25 °C.



SPECIFICATIONS $T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	20			V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	$I_D = 250\text{ }\mu\text{A}$		22		mV/°C
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$			- 2		
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	0.4		1.0	V
Gate-Source Leakage	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 8\text{ V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 20\text{ V}, V_{GS} = 0\text{ V}$			1	μA
		$V_{DS} = 20\text{ V}, V_{GS} = 0\text{ V}, T_J = 55\text{ }^\circ\text{C}$			10	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} \geq 5\text{ V}, V_{GS} = 4.5\text{ V}$	5			A
Drain-Source On-State Resistance ^a	$R_{DS(on)}$	$V_{GS} = 4.5\text{ V}, I_D = 1.8\text{ A}$		0.180	0.216	Ω
		$V_{GS} = 2.5\text{ V}, I_D = 1.6\text{ A}$		0.223	0.268	
		$V_{GS} = 1.8\text{ V}, I_D = 0.3\text{ A}$		0.300	0.375	
Forward Transconductance ^a	g_{fs}	$V_{DS} = 10\text{ V}, I_D = 1.8\text{ A}$		3		S
Dynamic^b						
Input Capacitance	C_{iss}	$V_{DS} = 10\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$		95		pF
Output Capacitance	C_{oss}			24		
Reverse Transfer Capacitance	C_{rss}			11		
Total Gate Charge	Q_g	$V_{DS} = 10\text{ V}, V_{GS} = 8\text{ V}, I_D = 1.8\text{ A}$		2.0	3.0	nC
		$V_{DS} = 10\text{ V}, V_{GS} = 4.5\text{ V}, I_D = 1.8\text{ A}$		1.2	1.8	
Q_{gs}			0.3			
Q_{gd}			0.15			
Gate Resistance	R_g	$f = 1\text{ MHz}$	0.5	2.5	5.0	Ω
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 10\text{ V}, R_L = 7.1\text{ }\Omega$ $I_D \cong 1.4\text{ A}, V_{GEN} = 4.5\text{ V}, R_g = 1\text{ }\Omega$		5	10	ns
Rise Time	t_r			10	20	
Turn-Off Delay Time	$t_{d(off)}$			24	36	
Fall Time	t_f			8	16	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 10\text{ V}, R_L = 7.1\text{ }\Omega$ $I_D \cong 1.4\text{ A}, V_{GEN} = 8\text{ V}, R_g = 1\text{ }\Omega$		2	4	
Rise Time	t_r			9	18	
Turn-Off Delay Time	$t_{d(off)}$			8	16	
Fall Time	t_f			7	14	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	$T_C = 25\text{ }^\circ\text{C}$			1.5 ^c	A
Pulse Diode Forward Current	I_{SM}				5	
Body Diode Voltage	V_{SD}	$I_S = 1.4\text{ A}, V_{GS} = 0\text{ V}$		0.7	1.2	V
Body Diode Reverse Recovery Time	t_{rr}	$I_F = 1.4\text{ A}, di/dt = 100\text{ A}/\mu\text{s}, T_J = 25\text{ }^\circ\text{C}$		9	18	ns
Body Diode Reverse Recovery Charge	Q_{rr}			3	6	nC
Reverse Recovery Fall Time	t_a			6		ns
Reverse Recovery Rise Time	t_b			3		

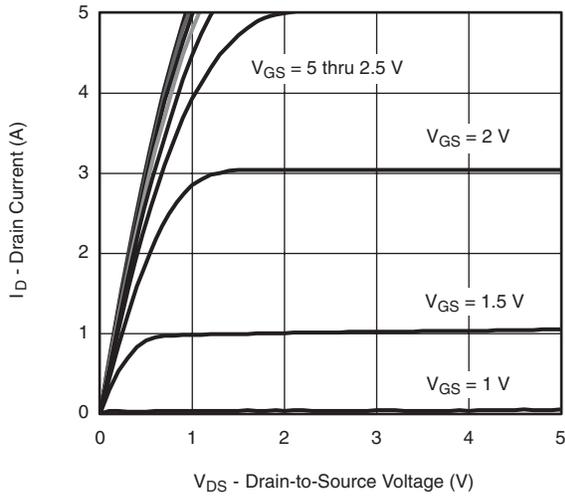
Notes:

- Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.
- Guaranteed by design, not subject to production testing.
- Package limited.

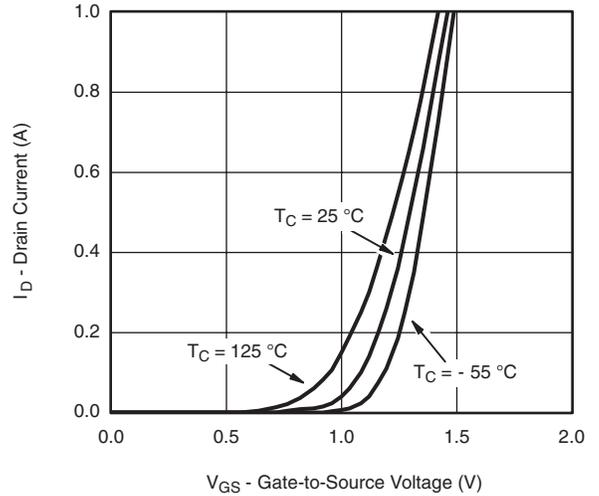
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



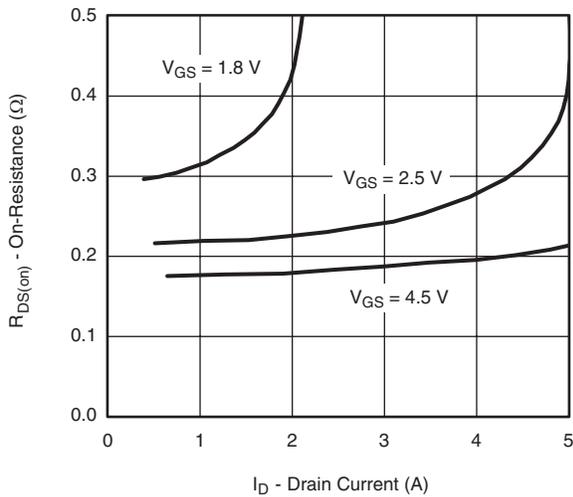
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



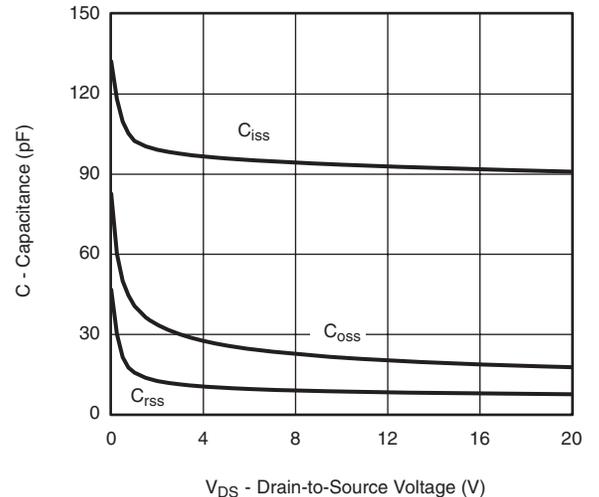
Output Characteristics



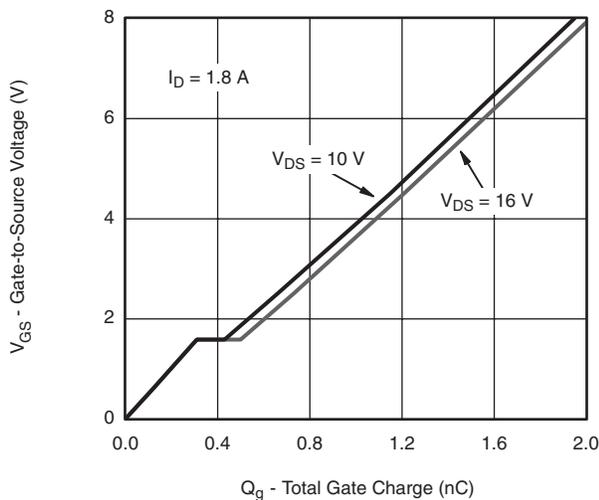
Transfer Characteristics



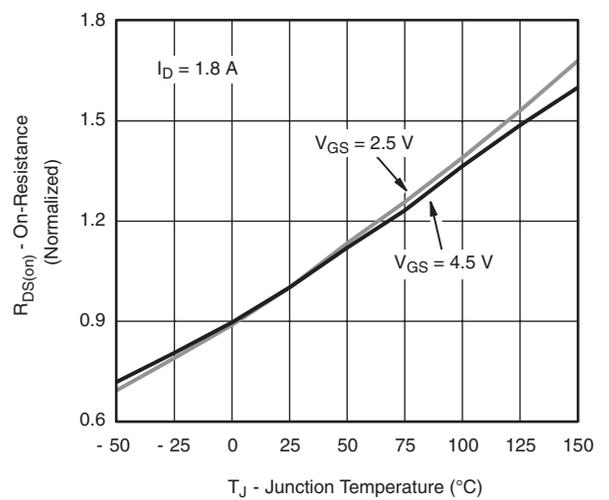
On-Resistance vs. Drain Current and Gate Voltage



Capacitance



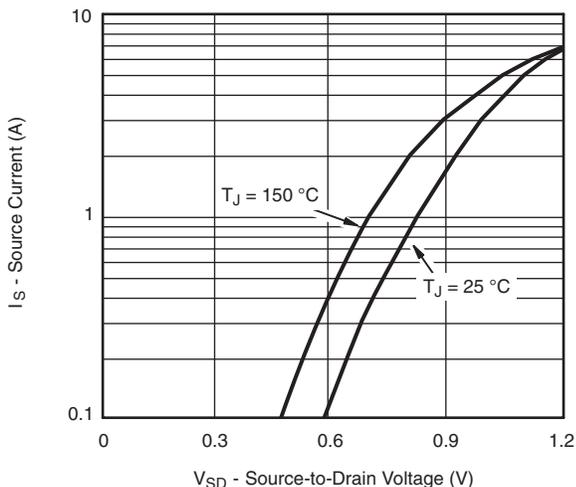
Gate Charge



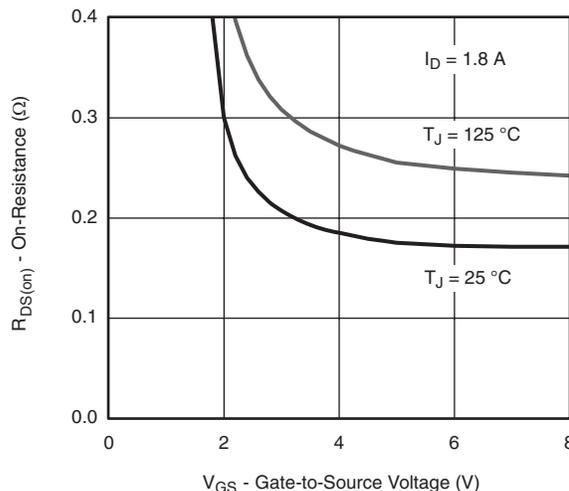
On-Resistance vs. Junction Temperature



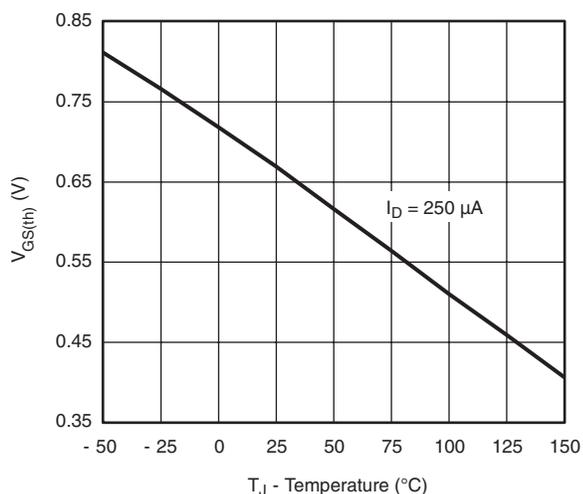
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



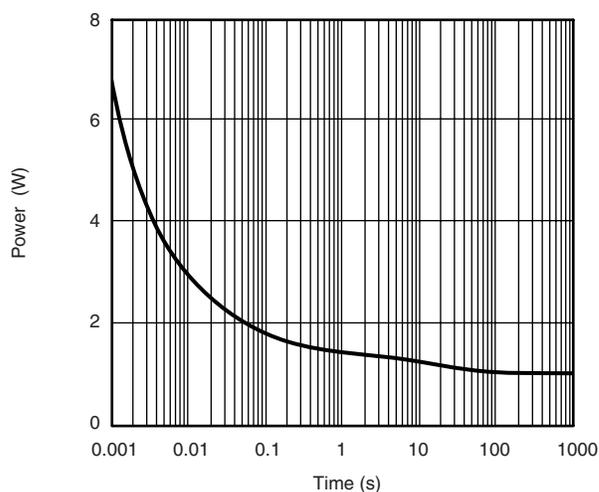
Source-Drain Diode Forward Voltage



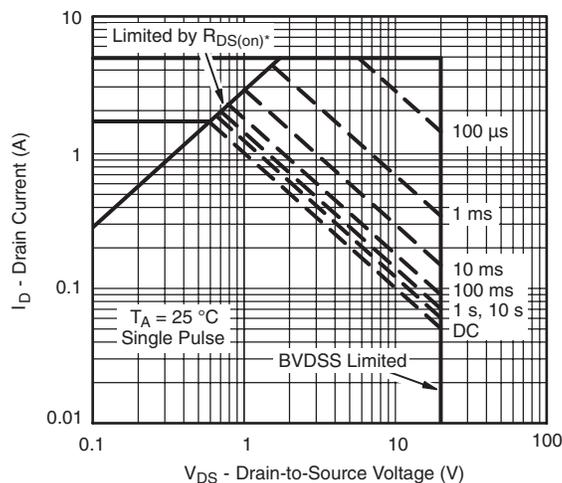
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



Single Pulse Power, Junction-to-Ambient

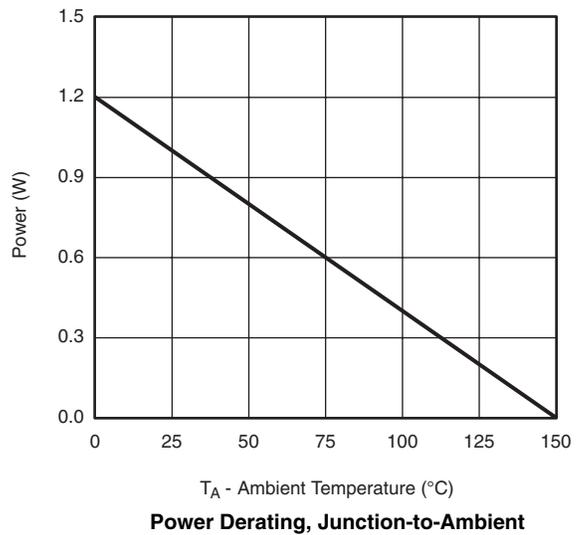
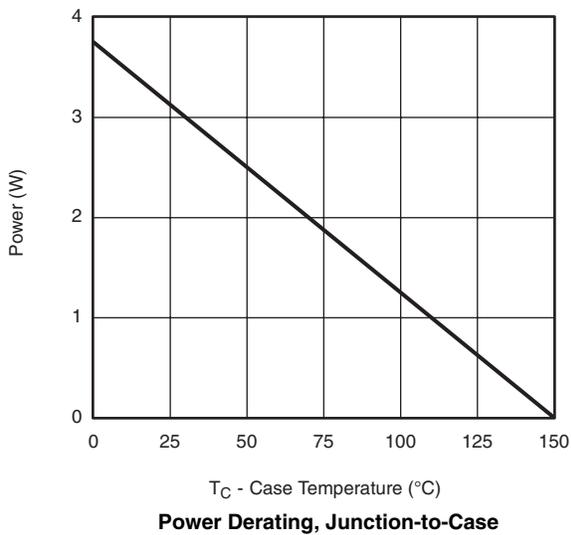
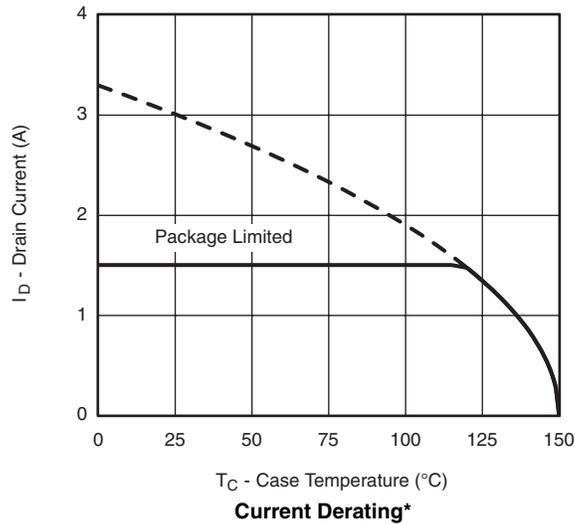


* $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified

Safe Operating Area, Junction-to-Case



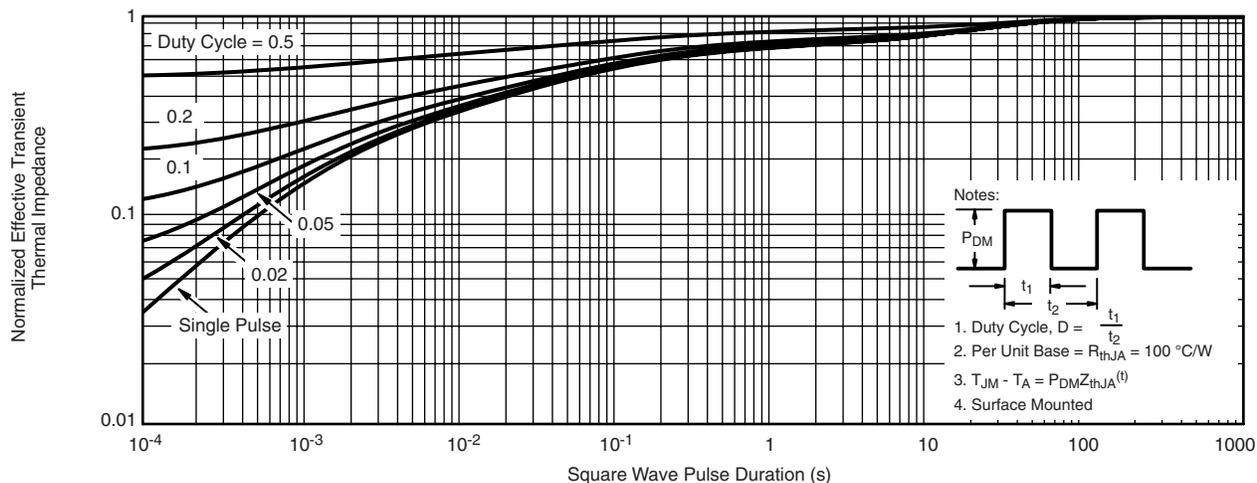
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



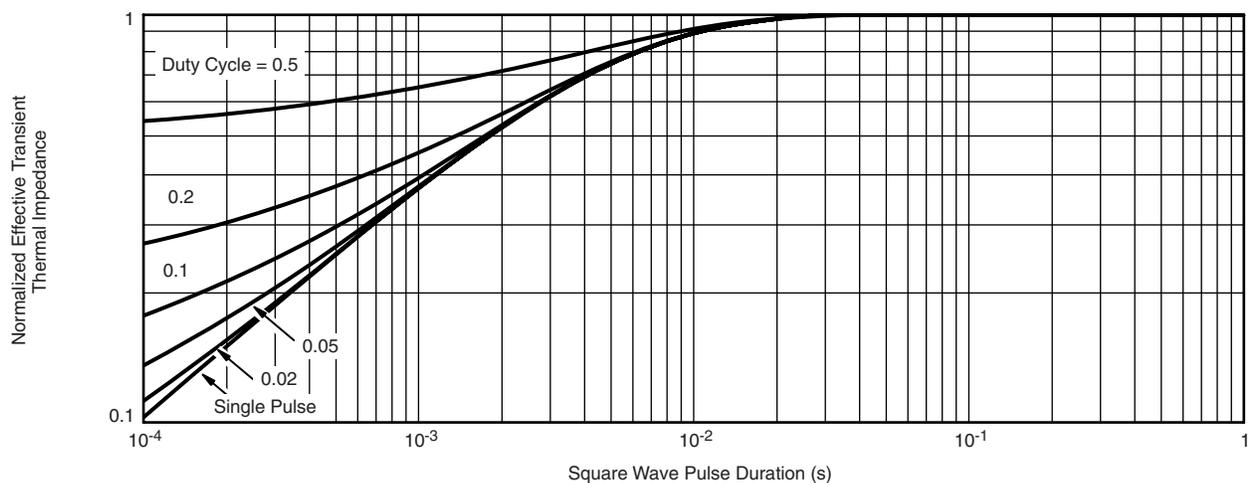
* The power dissipation P_D is based on $T_{J(max)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.



TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Normalized Thermal Transient Impedance, Junction-to-Ambient

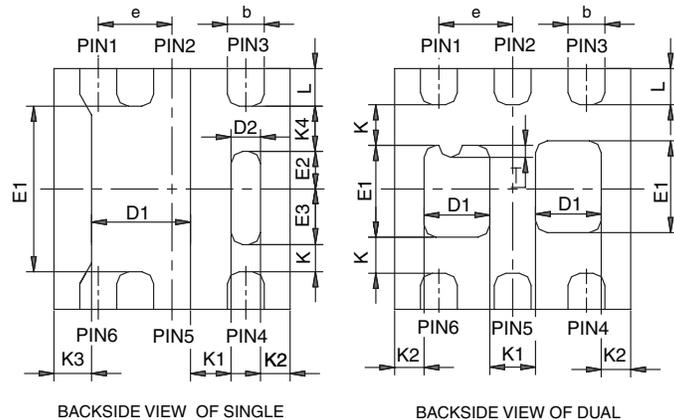


Normalized Thermal Transient Impedance, Junction-to-Case

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see <http://www.vishay.com/ppg?68883>.

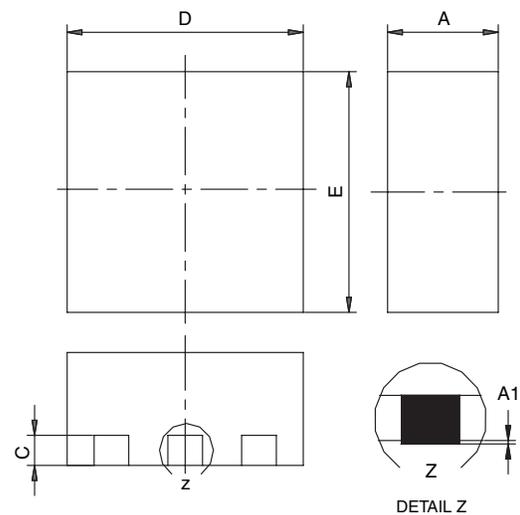


PowerPAK® SC75-6L



BACKSIDE VIEW OF SINGLE

BACKSIDE VIEW OF DUAL

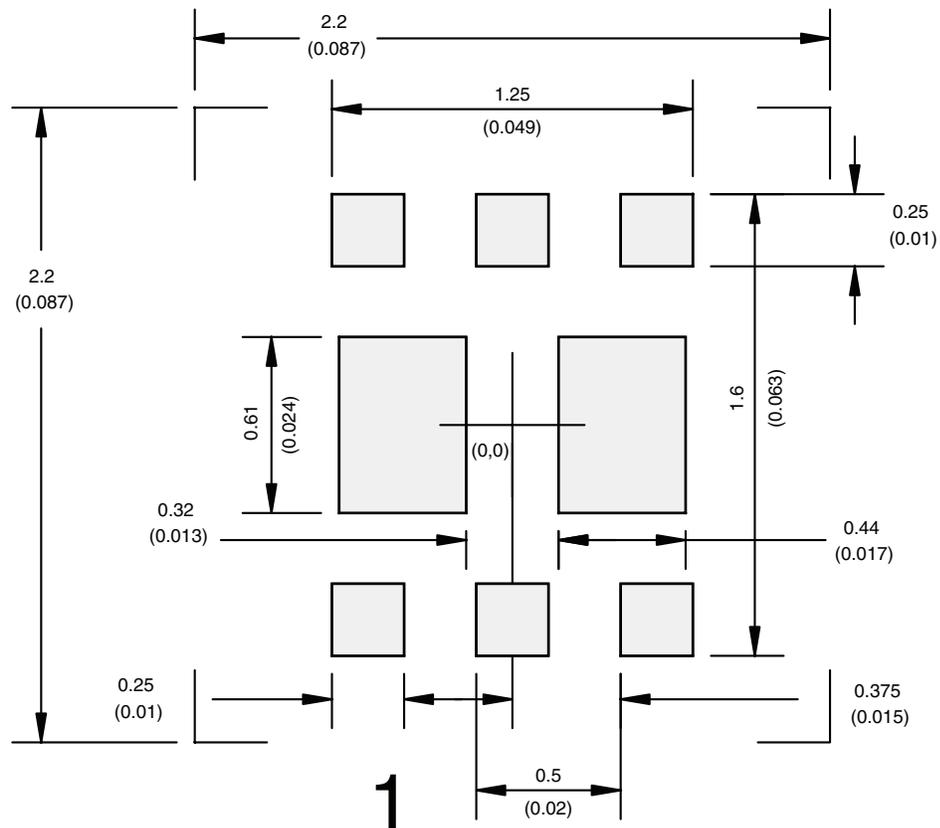


- Notes:
 1. All dimensions are in millimeters
 2. Package outline exclusive of mold flash and metal burr
 3. Package outline inclusive of plating

DIM	SINGLE PAD						DUAL PAD					
	MILLIMETERS			INCHES			MILLIMETERS			INCHES		
	Min	Nom	Max	Min	Nom	Max	Min	Nom	Max	Min	Nom	Max
A	0.675	0.75	0.80	0.027	0.030	0.032	0.675	0.75	0.80	0.027	0.030	0.032
A1	0	-	0.05	0	-	0.002	0	-	0.05	0	-	0.002
b	0.18	0.25	0.33	0.007	0.010	0.013	0.18	0.25	0.33	0.007	0.010	0.013
C	0.15	0.20	0.25	0.006	0.008	0.010	0.15	0.20	0.25	0.006	0.008	0.010
D	1.53	1.60	1.70	0.060	0.063	0.067	1.53	1.60	1.70	0.060	0.063	0.067
D1	0.57	0.67	0.77	0.022	0.026	0.030	0.34	0.44	0.54	0.013	0.017	0.021
D2	0.10	0.20	0.30	0.004	0.008	0.012						
E	1.53	1.60	1.70	0.060	0.063	0.067	1.53	1.60	1.70	0.060	0.063	0.067
E1	1.00	1.10	1.20	0.039	0.043	0.047	0.51	0.61	0.71	0.020	0.024	0.028
E2	0.20	0.25	0.30	0.008	0.010	0.012						
E3	0.32	0.37	0.42	0.013	0.015	0.017						
e	0.50 BSC			0.020 BSC			0.50 BSC			0.020 BSC		
K	0.180 TYP			0.007 TYP			0.245 TYP			0.010 TYP		
K1	0.275 TYP			0.011 TYP			0.320 TYP			0.013 TYP		
K2	0.200 TYP			0.008 TYP			0.200 BSC			0.008 TYP		
K3	0.255 TYP			0.010 TYP								
K4	0.300 TYP			0.012 TYP								
L	0.15	0.25	0.35	0.006	0.010	0.014	0.15	0.25	0.35	0.006	0.010	0.014
T							0.03	0.08	0.13	0.001	0.003	0.005

ECN: C-07431 – Rev. C, 06-Aug-07
 DWG: 5935

RECOMMENDED PAD LAYOUT FOR PowerPAK® SC75-6L Dual



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<http://moschip.ru/get-element>

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Сотрудничество с глобальными дистрибьюторами электронных компонентов, предоставляет возможность заказывать и получать с международных складов практически любой перечень компонентов в оптимальные для Вас сроки.

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