Description

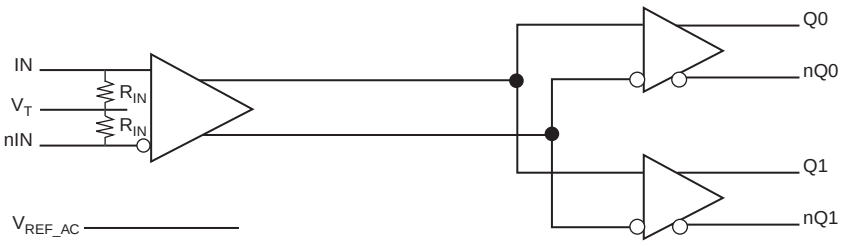
The ICS858S011I is a high-speed 1-to-2 Differential-to-CML Fanout Buffer. The device is optimized for high-speed and very low output skew, making it suitable for use in demanding applications such as SONET, 1 Gigabit and 10 Gigabit Ethernet, and Fibre Channel. The internally terminated differential input and V_{REF_AC} pin allow other differential signal families such as LVDS, LVPECL, SSTL, and CML to be easily interfaced to the input with minimal use of external components.

The ICS858S011I is packaged in a small 3mm x 3mm 16-pin VFQFN package which makes it ideal for use in space-constrained applications.

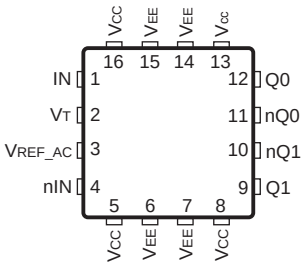
Features

- Two differential CML outputs
- IN/nIN pair can accept the following differential input levels: LVPECL, LVDS, CML, SSTL
- Maximum output frequency: 2GHz
- Output skew: 25ps (maximum)
- Part-to-part skew: 250ps (maximum)
- Additive phase jitter, RMS: 0.042ps (typical)
- Propagation delay: 525ps (maximum)
- Operating voltage supply range: V_{CC} = 2.375V to 3.63V, V_{EE} = 0V
- -40°C to 85°C ambient operating temperature
- Available in lead-free (RoHS 6) package

Block Diagram



Pin Assignment



ICS858S011I

16-Lead VFQFN
3mm x 3mm x 0.925mm package body
K Package
Top View

Table 1. Pin Descriptions

Number	Name	Type	Description
1	IN	Input	Non-inverting differential LVPECL clock input.
2	V_T	Input	Termination input.
3	V_{REF_AC}	Output	Reference voltage for AC-coupled applications.
4	nIN	Input	Inverting differential LVPECL clock input.
5, 8, 13, 16	V_{CC}	Power	Power supply pins.
6, 7, 14, 15	V_{EE}	Power	Negative supply pins.
9, 10	Q1, nQ1	Output	Differential output pair. CML interface levels.
11, 12	nQ0, Q0	Output	Differential output pair. CML interface levels.

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{CC}	4.6V (CML mode, V_{EE} = 0V)
Inputs, V_I	-0.5V to V_{CC} + 0.5V
Outputs, I_O Continuous Current Surge Current	 20mA 40mA
Input Current, IN/nIN	+50mA
V_T Current, I_{VT}	+100mA
Input Sink/Source, I_{REF_AC}	±2mA
Operating Temperature Range, T_A	-40°C to 85°C
Storage Temperature, T_{STG}	-65°C to 150°C
Package Thermal Impedance, θ_{JA} (Junction-to-Ambient)	74.7°C/W (0 mps)

DC Electrical Characteristics

Table 2A. Power Supply DC Characteristics, V_{CC} = 2.375V to 3.63V, V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Positive Supply Voltage		2.375	3.3	3.63	V
I_{EE}	Power Supply Current				57	mA

Table 2B. DC Characteristics, V_{CC} = 2.375V to 3.63V, V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
R_{IN}	Differential Input Resistance	IN/nIN	IN to V_T, nIN to V_T	40	50	60	Ω
V_{IH}	Input High Voltage	IN/nIN		1.2		V_{CC}	V
V_{IL}	Input Low Voltage	IN/nIN		0		V_{IH} – 0.15	V
V_{IN}	Input Voltage Swing; NOTE 1			0.15		1.2	V
V_{DIFF_IN}	Differential Input Voltage Swing			0.3			V
IN to V_T	Voltage between IN and V_T	IN/nIN				1.28	V
V_{REF_AC}	Reference Voltage			V_{CC} – 1.4	V_{CC} – 1.3	V_{CC} – 1.2	V

NOTE 1: Refer to Parameter Measurement Information, *Input Voltage Swing Diagram.*

Table 2C. CML DC Characteristics, V_{CC} = 2.375V to 3.63V, V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage; NOTE 1		V_{CC} – 0.020	V_{CC} – 0.010	V_{CC}	V
V_{OUT}	Output Voltage Swing		325	400		mV
V_{DIFF_OUT}	Differential Output Voltage Swing		650	800		mV
R_{OUT}	Output Source Impedance		40	50	60	Ω

NOTE 1: Outputs terminated with 50Ω to V_{CC}.

AC Electrical Characteristics

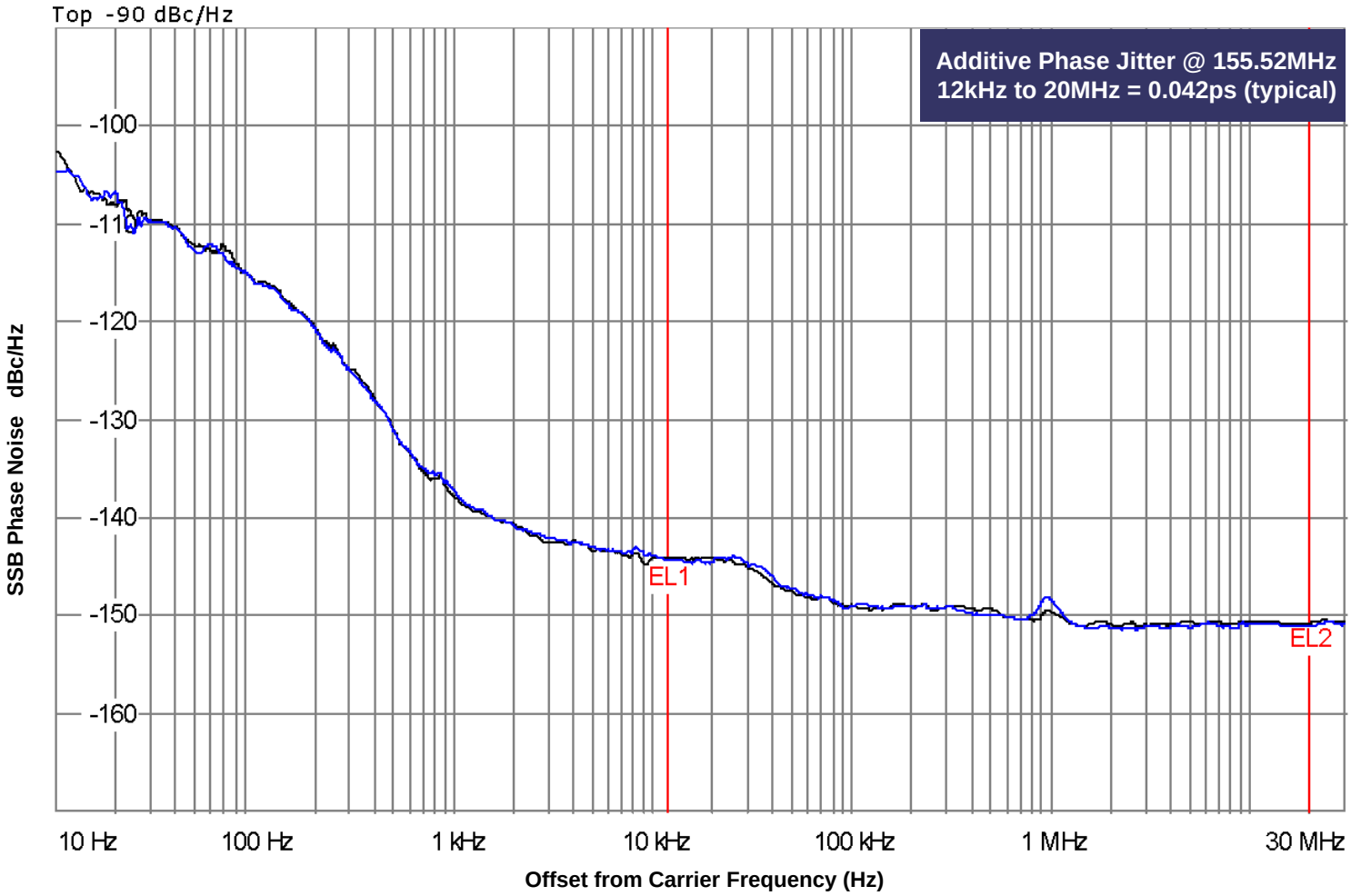
Table 3. AC Characteristics, V_{CC} = 2.375V to 3.63V, V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency				2	GHz
t_{PD}	Propagation Delay, Differential; NOTE 1		275		525	ps
*t*sk(o)	Output Skew; NOTE 2, 4				25	ps
*t*sk(pp)	Part-to-Part Skew; NOTE 3, 4				250	ps
*t*jit	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter Section	155.52MHz @ 3.3V, Integration Range: 12kHz – 20MHz		0.042		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	60		200	ps

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. Device will meet specifications after thermal equilibrium has been reached under these conditions.
All parameters characterized at ≤ 1.2GHz unless otherwise noted.
NOTE 1: Measured from the differential input crossing point to the differential output crossing point.
NOTE 2: Defined as skew between outputs at the same supply voltage, same temperature, same frequency and with equal load conditions. Measured at the output differential cross points.
NOTE 3: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.
NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.

Additive Phase Jitter

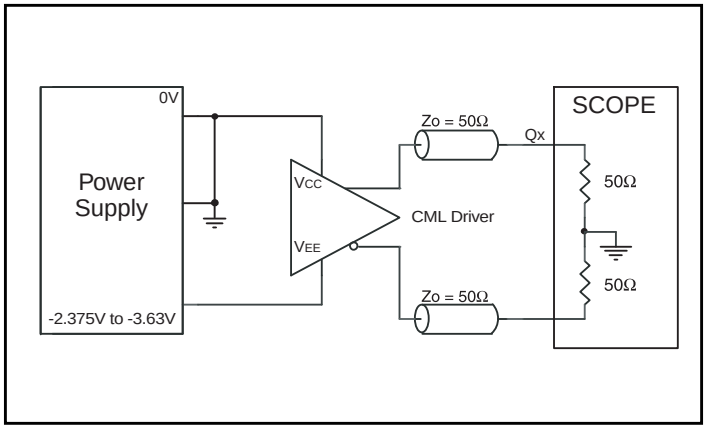
The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the ***dBc Phase Noise.*** This value is normally expressed using a Phase noise plot and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels (dBm) or a ratio of the power in the 1Hz band to the power in the fundamental. When the required offset is specified, the phase noise is called a ***dBc*** value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.



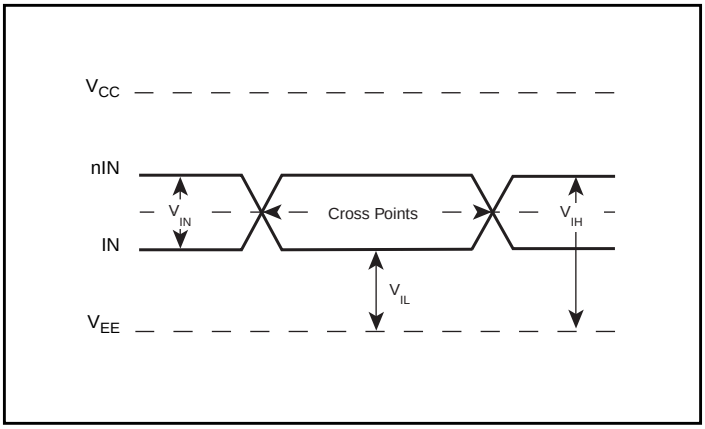
As with most timing specifications, phase noise measurements has issues relating to the limitations of the equipment. Often the noise floor of the equipment is higher than the noise floor of the device. This is illustrated above. The device meets the noise floor of what is shown, but can actually be lower. The phase noise is dependent on the input source and measurement equipment.

The source generator “Rohde & Schwarz SMA100A Low Noise Signal Generator as external input to an Agilent 8133A 3GHz Pulse Generator”.

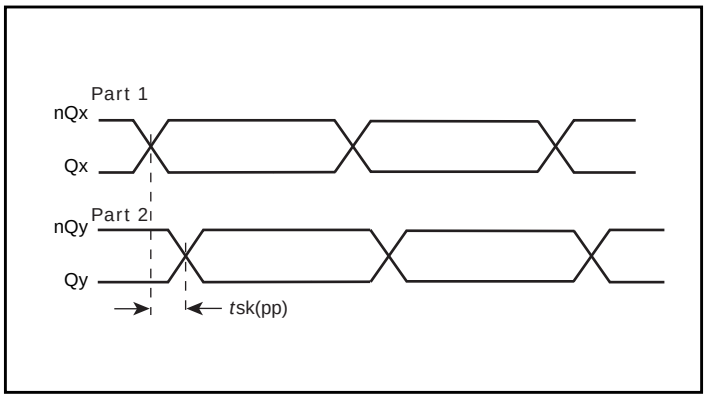
Parameter Measurement Information



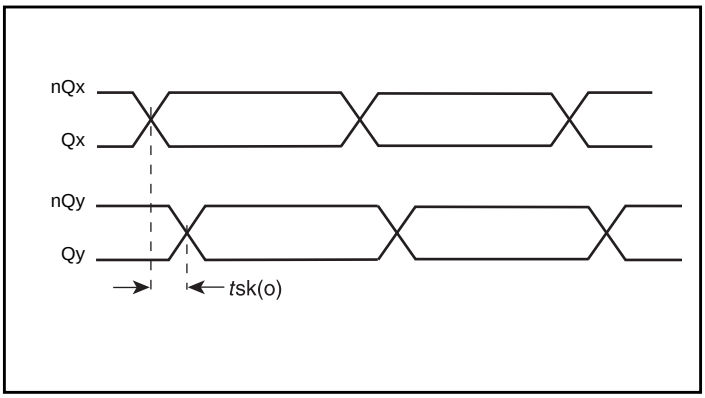
CML Output Load AC Test Circuit



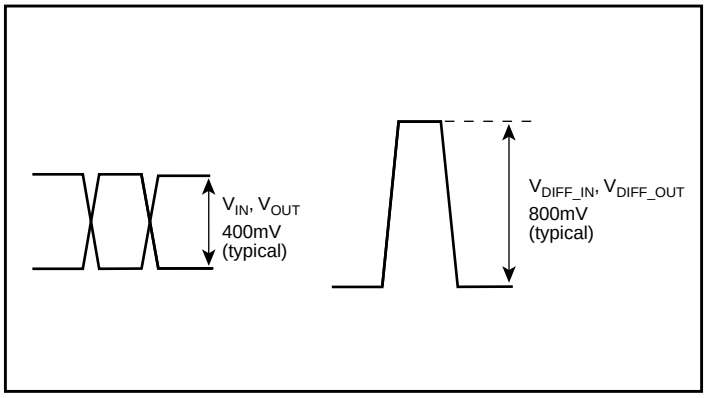
Differential Input Level



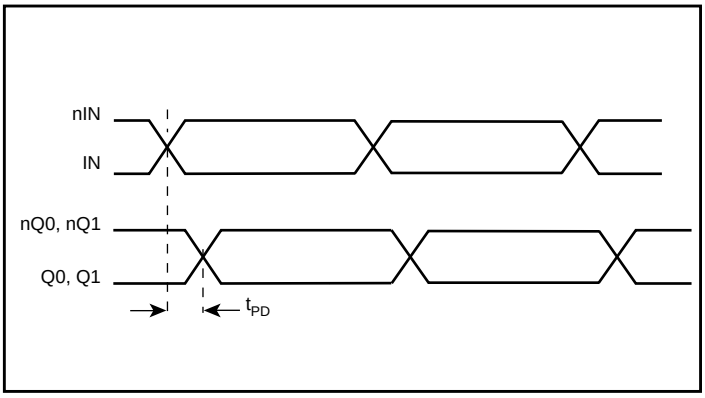
Part-to-Part Skew



Output Skew

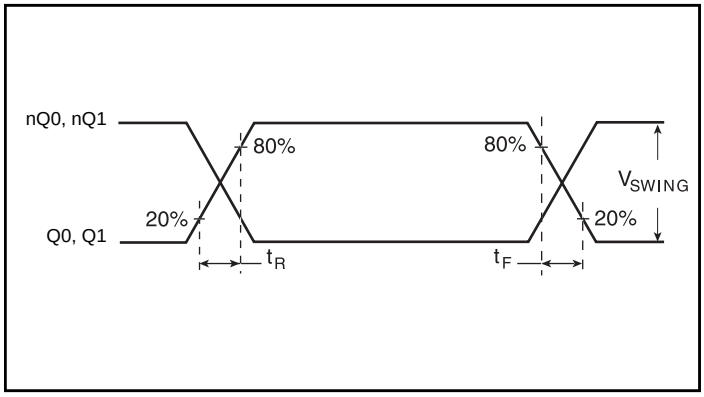


Single-ended & Differential Input Voltage Swing



Propagation Delay

Parameter Measurement Information, continued



Output Rise/Fall Time

Applications Information

Recommendations for Unused Output Pins

Outputs:

CML Outputs

All unused CML outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

3.3V LVPECL Input with Built-In 50Ω Termination Interface

The IN /nIN with built-in 50Ω terminations accept LVDS, LVPECL, CML, SSTL and other differential signals. Both differential inputs must meet the V_{PP} and V_{CMR} input requirements. *Figures 1A to 1E* show interface examples for the IN /nIN input with built-in 50Ω terminations driven by the most common driver types. The input interfaces suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.

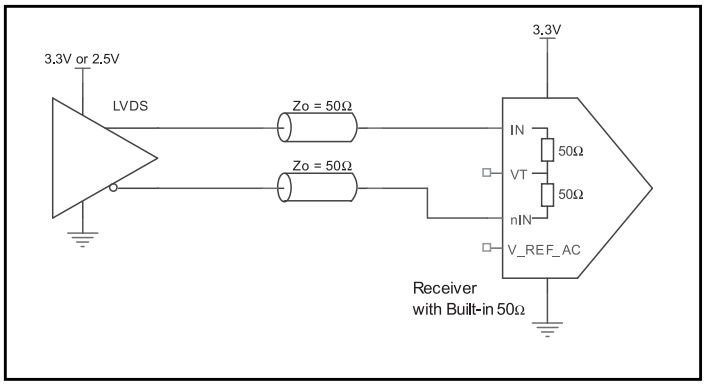


Figure 1A. IN/nIN Input with Built-In 50Ω Driven by an LVDS Driver

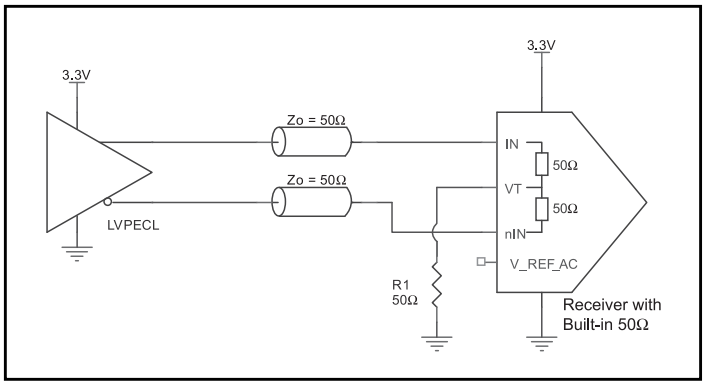


Figure 1B. IN/nIN Input with Built-In 50Ω Driven by an LVPECL Driver

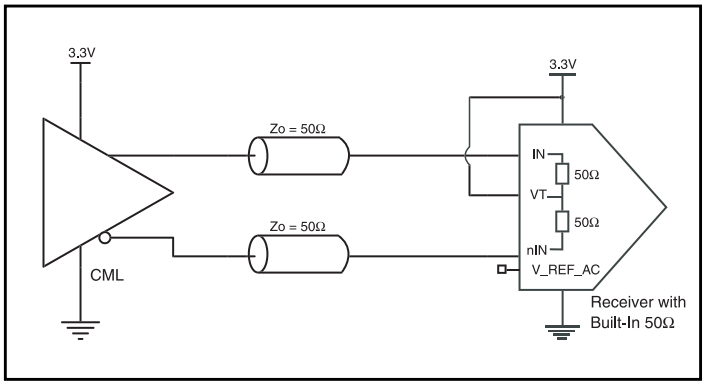


Figure 1C. IN/nIN Input with Built-In 50Ω Driven by a CML Driver with Open Collector

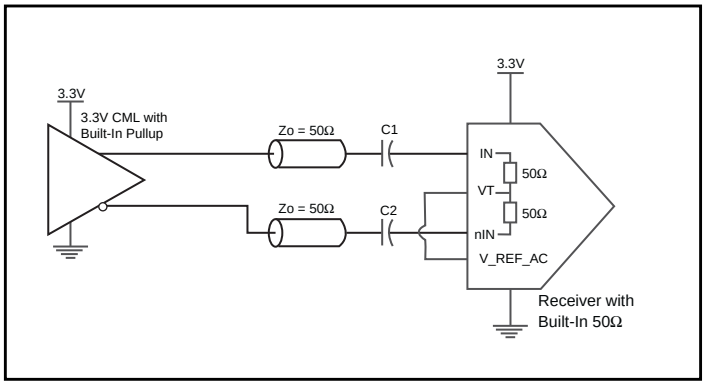


Figure 1D. IN/nIN Input with Built-In 50Ω Driven by a CML Driver with Built-In 50Ω Pullup

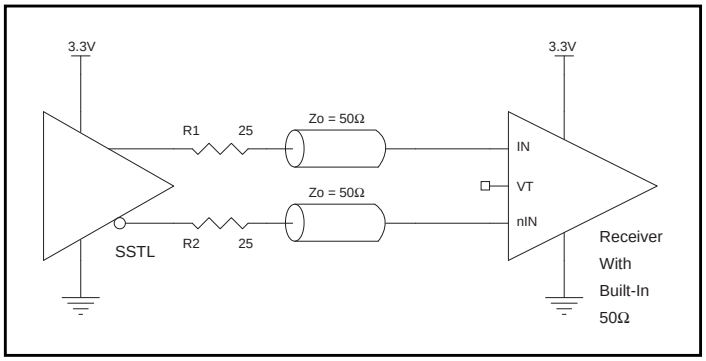


Figure 1E. IN/nIN Input with Built-In 50Ω Driven by an SSTL Driver

2.5V LVPECL Input with Built-In 50Ω Termination Interface

The IN /nIN with built-in 50Ω terminations accept LVDS, LVPECL, CML, SSTL and other differential signals. Both differential inputs must meet the V_{PP} and V_{CMR} input requirements. *Figures 2A to 2E* show interface examples for the IN /nIN with built-in 50Ω termination input driven by the most common driver types. The input interfaces suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.

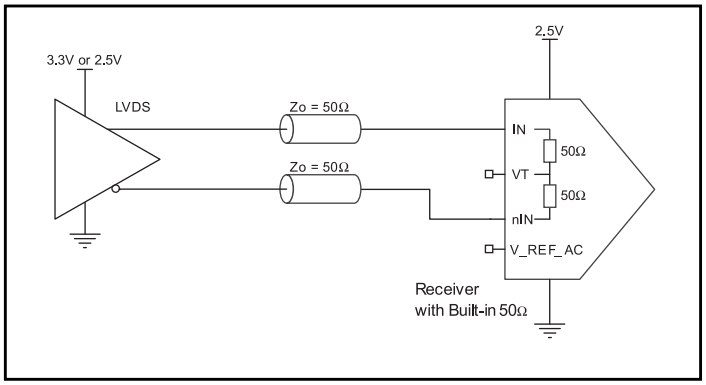


Figure 2A. IN/nIN Input with Built-In 50Ω Driven by an LVDS Driver

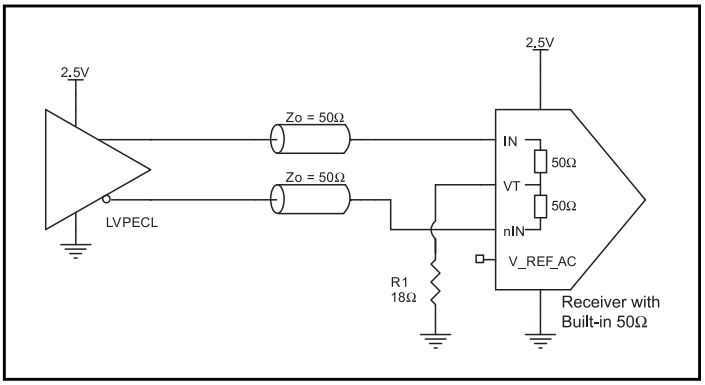


Figure 2B. IN/nIN Input with Built-In 50Ω Driven by an LVPECL Driver

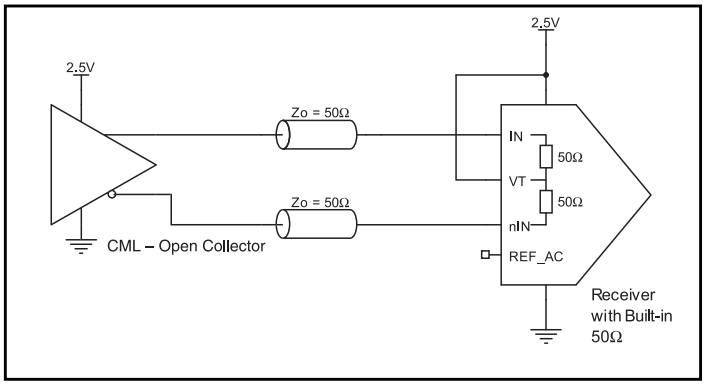


Figure 2C. IN/nIN Input with Built-In 50Ω Driven by a CML Driver

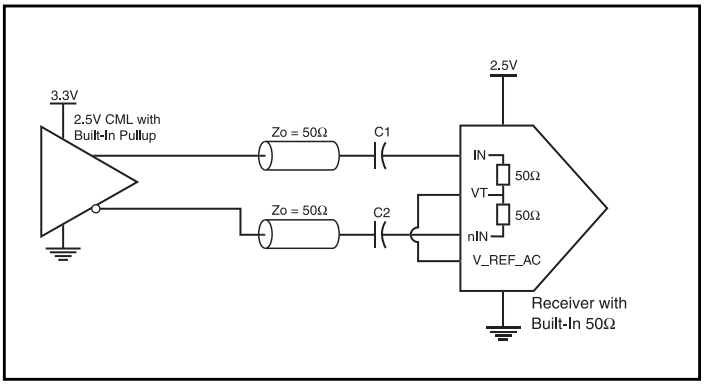


Figure 2D. IN/nIN Input with Built-In 50Ω Driven by a CML Driver with Built-In 50Ω Pullup

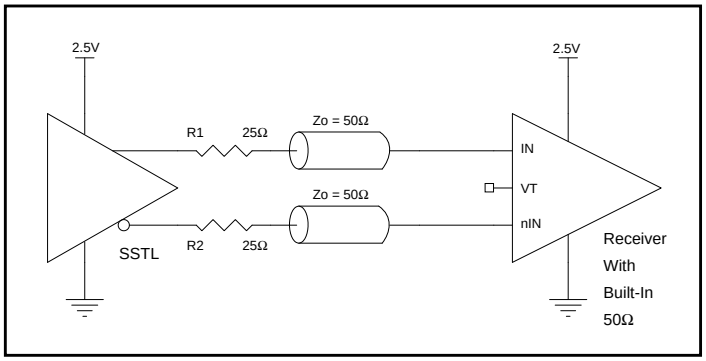


Figure 2E. IN/nIN Input with Built-In 50Ω Driven by an SSTL Driver

Schematic Example

Figure 3 shows a schematic example of the ICS858S011I. This schematic provides examples of input and output handling. The ICS858S011I input has built-in 50Ω termination resistors. The input can directly accept various types of differential signal without AC couple. If AC couple termination is used, the ICS858S011I also provides VREF_AC pin for proper offset level after AC couple. This example shows the ICS858S011I input driven by a 3.3V LVPECL driver. The ICS858S011I outputs are CML driver with built-in 50Ω pullup resistors. In this example, we assume the traces are long transmission line and the receiver is high input impedance without built-in matched load. An external 100Ω resistor across the receiver input is required.

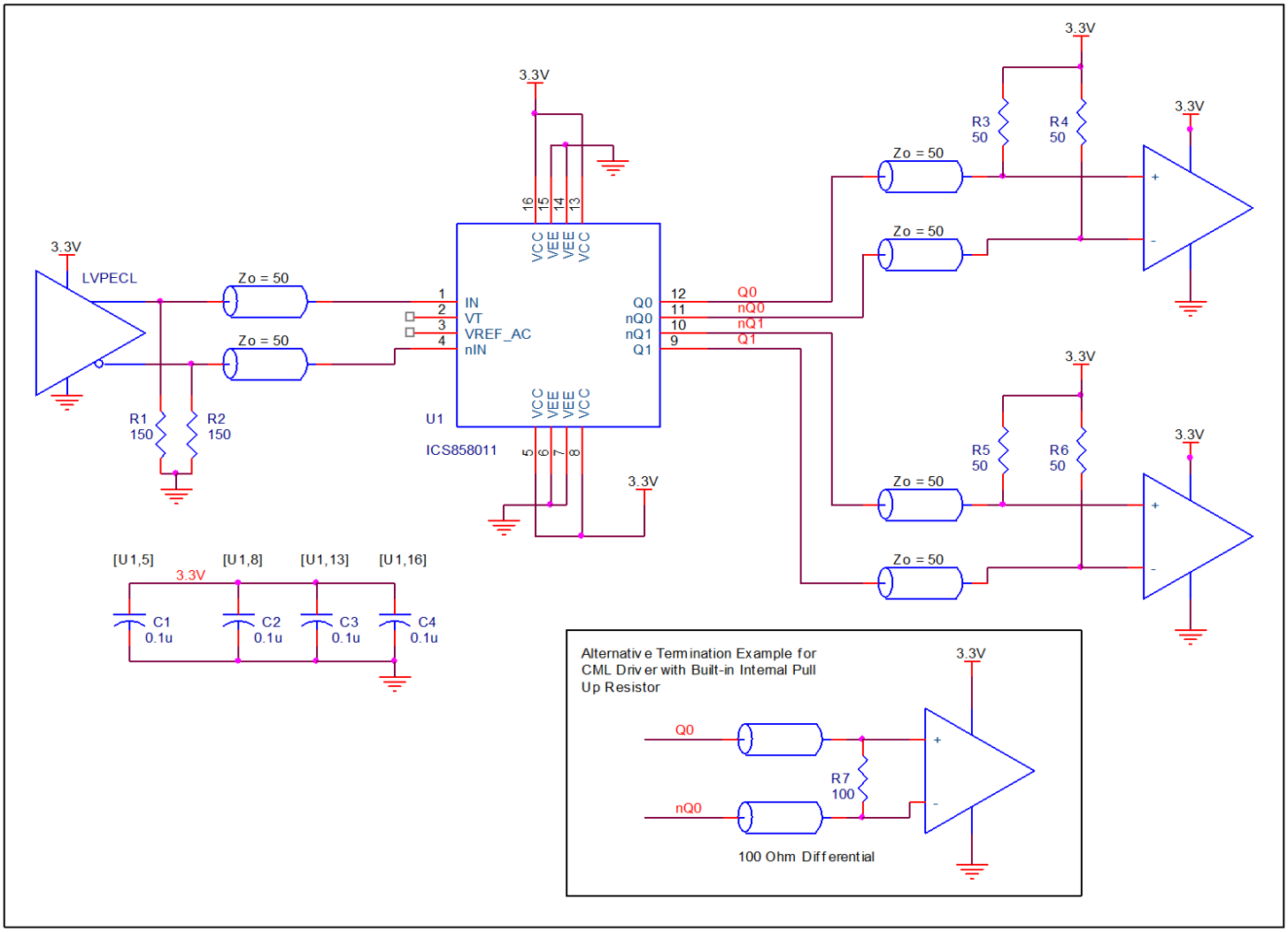


Figure 3. ICS858S011I Application Schematic Example

VFQFN EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in *Figure 4.* The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as “heat pipes”. The number of vias (i.e. “heat pipes”) are application specific and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, please refer to the Application Note on the Surface Mount Assembly of Amkor’s Thermally/ Electrically Enhance Leadframe Base Package, Amkor Technology.

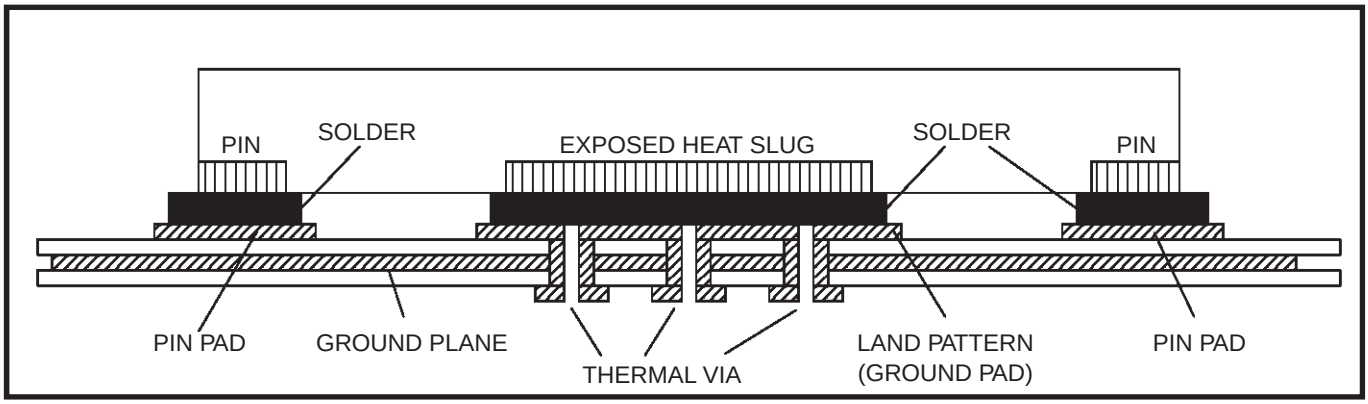


Figure 4. P.C. Assembly for Exposed Pad Thermal Release Path – Side View (drawing not to scale)

Power Considerations

This section provides information on power dissipation and junction temperature for the ICS858S011I.
Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the ICS858S011I is the sum of the core power plus the power dissipation in the load(s).
The following is the power dissipation for V_{DD} = 3.3V + 10% = 3.63V, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipation in the load.

- Power $(core)_{MAX} = V_{DD\_MAX} * I_{DD}$ = 3.63V * 57mA = **206.9mW**
- Power Dissipation for internal termination R_T
  Power $(R_T)_{MAX} = 4 * (V_{IN\_MAX})^2 / R_{T\_MIN} = (1.2V)^2 / 80\Omega$ = **72mW**

Total Power$_{\_MAX}$ = 206.9mW + 72mW = **278.9mW**

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad, and directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 74.7°C/W per Table 4 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 0.279W * 74.7°C/W = 105.8°C. This is well below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 4. Thermal Resistance θ_{JA} for 16 Lead VFQFN, Forced Convection

θ_{JA} by Velocity			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	74.7°C/W	65.3°C/W	58.5°C/W

Reliability Information

Table 5. θ_{JA} vs. Air Flow Table for a 16 Lead VFQFN

θ_{JA} vs. Air Flow			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	74.7°C/W	65.3°C/W	58.5°C/W

Transistor Count

The transistor count for ICS858S011I is: 216

Pin Compatible with 858011

Package Outline Drawings

The package outline drawings are located in the last section of this document. The package information is the most current data available and is subject to change without notice or revision of this document.

Ordering Information

Table 7. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
858S011AKILF	011A	“Lead-Free” 16 Lead VFQFN	Tube	-40°C to 85°C
858S011AKILFT	011A	“Lead-Free” 16 Lead VFQFN	2500 Tape & Reel	-40°C to 85°C

NOTE: Parts that are ordered with an “LF” suffix to the part number are the Pb-Free configuration and are RoHS compliant.

Revision History

Revision Date	Description of Change
September 19, 2017	Updated the package outline drawings; however, no mechanical changes Completed other minor improvements
October 12, 2010	Initial release.

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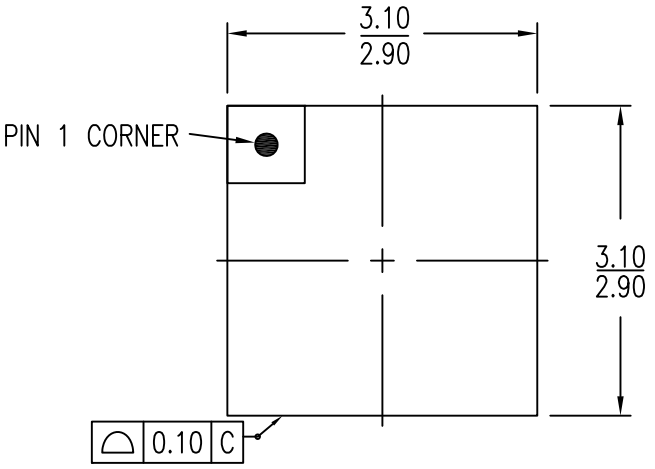
Tech Support
www.IDT.com/go/support

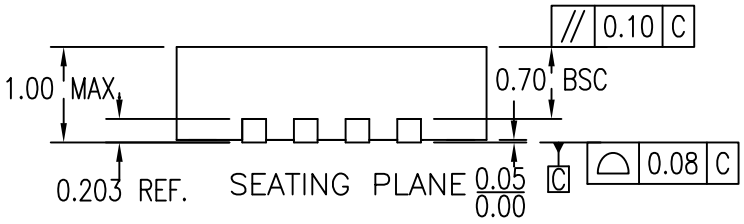
16L-QFN Package Outline Drawing

3.0 x 3.0 x 1.0 mm, 0.5 mm Pitch, 1.70 x 1.70 mm Epad

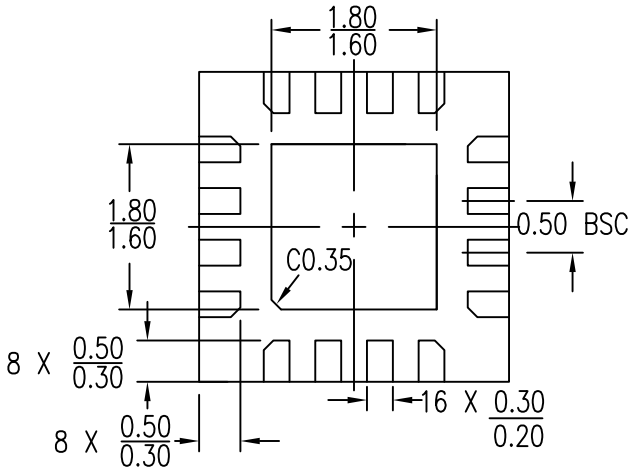
NL/NLG16P2, PSC-4169-02, Rev 03, Page 1



TOP VIEW



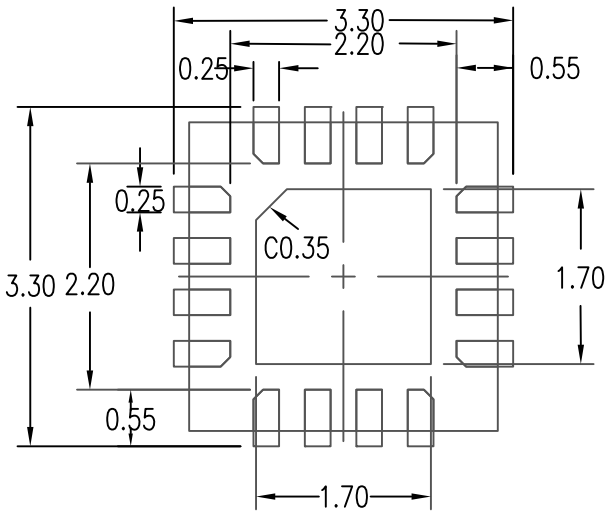
SIDE VIEW



BOTTOM VIEW

NOTES:

1. ALL DIMENSIONS ARE IN mm.ANGLES IN DEGREES



RECOMMENDED LAND PATTERN

NOTES:
1. ALL DIMENSIONS ARE IN mm.ANGLES IN DEGREES
2. TOP DOWN VIEW–AS VIEWED ON PCB
3. LAND PATTERN RECOMMENDATION IS PER IPC–7351B GENERIC REQUIREMENT FOR SURFACE MOUNT DESIGN AND LAND PATTERN

Package Revision History		
Date Created	Rev No.	Description
Aug 15, 2017	Rev 03	Update Epad Range
Jul 28, 2017	Rev 02	New format

Общество с ограниченной ответственностью «МосЧип» ИНН 7719860671 / КПП 771901001
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Данный компонент на территории Российской Федерации

Вы можете приобрести в компании MosChip.

Для оперативного оформления запроса Вам необходимо перейти по данной ссылке:

http://moschip.ru/get-element

Вы можете разместить у нас заказ для любого Вашего проекта, будь то серийное производство или разработка единичного прибора.

В нашем ассортименте представлены ведущие мировые производители активных и пассивных электронных компонентов.

Нашей специализацией является поставка электронной компонентной базы двойного назначения, продукции таких производителей как XILINX, Intel (ex.ALTERA), Vicor, Microchip, Texas Instruments, Analog Devices, Mini-Circuits, Amphenol, Glenair.

Сотрудничество с глобальными дистрибьюторами электронных компонентов, предоставляет возможность заказывать и получать с международных складов практически любой перечень компонентов в оптимальные для Вас сроки.

На всех этапах разработки и производства наши партнеры могут получить квалифицированную поддержку опытных инженеров.

Система менеджмента качества компании отвечает требованиям в соответствии с ГОСТ Р ИСО 9001, ГОСТ РВ 0015-002 и ЭС РД 009

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