2.5V/3.3V HIGH-PERFORMANCE, DUAL 1:10 OR LVPECL CLOCK DRIVER w/ INTERNAL TERMINATION AND REDUNDANT SWITCHOVER

Precision Edge® SY89829U

FEATURES

- **Dual 1:10 fanout buffer/translator**
- **Accepts LVPECL or LVDS inputs**
- **Multiplexed inputs ideal for redundant clock switchover**
- **Guaranteed AC parameters:**
  - **> 2GHz f_{MAX} (toggle)**
  - **< 50ps ch-ch skew**
- **LVDS input includes 100Ω internal termination**
- **Low supply voltage: 2.5V, 3.3V**
- **–40°C to +85°C temperature range**
- **Output enable (OE) pin**
- **Available in 64 EPAD-TQFP**

APPLICATIONS

- **High-performance PCs**
- **Workstations**
- **Parallel processor-based systems**
- **Other high-performance computing**
- **Communications**
- **Redundant LVPECL or LVDS bus clock switchover**

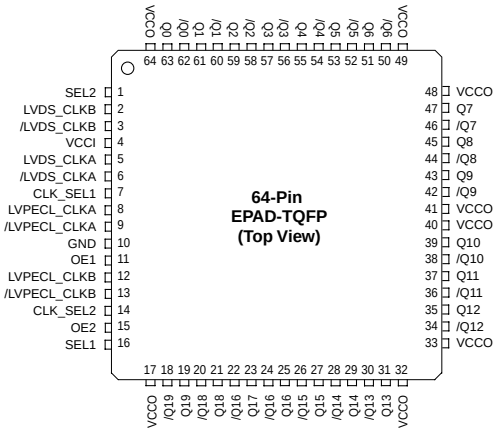
Precision Edge®

DESCRIPTION

The SY89829U is a High Performance dual 1:10 or single 1:20 LVPECL Clock Driver. The part is designed for use in low voltage (2.5V/3.3V) applications which require a large number of outputs to drive precisely aligned, ultra low skew signals to their destination. The input is multiplexed from either LVDS or LVPECL by the CLK_SEL pin. The LVDS inputs include a 100Ω internal termination across the input pair, thus eliminating any need for external termination. The 2:1 input mux makes this device an ideal choice for redundant clock applications that need to switch between two reference clocks. The output enable (OE) is synchronous so that the outputs will only be enabled/disabled when they are already in the LOW state. This eliminates any chance of generating a runt clock pulse when the device is enabled/disabled as can happen with an asynchronous control.

The SY89829U features low pin-to-pin skew (50ps max.) and low part-to-part skew (200ps max.)—performance previously unachievable in a standard product having such a high number of outputs. The SY89829U is available in a single space saving package which provides a lower overall cost solution. In addition, a single chip solution improves timing budgets by eliminating the multiple device solution with their corresponding large part-to-part skew.

PACKAGE/ORDERING INFORMATION



64-Pin TQFP (H64-1)

Ordering Information(1)

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY89829UHI	H64-1	Industrial	SY89829UHI	Sn-Pb
SY89829UHITR(2)	H64-1	Industrial	SY89829UHI	Sn-Pb
SY89829UHY(3)	H64-1	Industrial	SY89829UHY with Pb-Free bar-line indicator	Pb-Free Matte-Sn
SY89829UHYTR(2, 3)	H64-1	Industrial	SY89829UHY with Pb-Free bar-line indicator	Pb-Free Matte-Sn

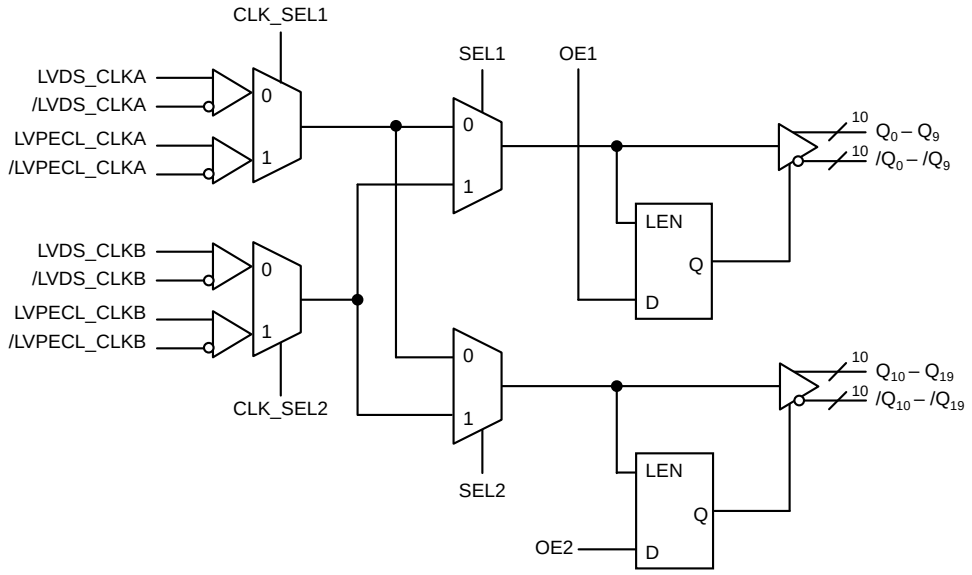
Notes:

1. Contact factory for die availability. Dice are guaranteed at T_A = 25°C, DC electricals only.
2. Tape and Reel.
3. Pb-Free package recommended for new designs.

PIN NAMES

Pin	Function
LVDS_CLKA, /LVDS_CLKA, LVDS_CLKB, /LVDS_CLKB	Differential LVDS Inputs with Internal 100Ω Termination.
LVPECL_CLKA, /LVPECL_CLKA LVPECL_CLKB, /LVPECL_CLKB	Differential LVPECL Inputs. For DC-coupled input signals, terminate the input signal with 50Ω to V_{CC} –2V. For AC-coupled to V_{CC} –2V. For AC-coupled terminate the input signal with 50Ω to V_{CC} –3V.
CLK_SEL1, CLK_SEL2	Input CLK Select (LVTTL).
SEL1, SEL2	Input Select (LVTTL).
OE1, OE2	Output Enable (LVTTL).
$Q_0 – Q_{19}$, $/Q_0 – /Q_{19}$	Differential LVPECL Outputs. Normally terminated with 50Ω to V_{CC} –2V. Unused output pairs can be left floating.
GND	Ground.
V_{CCI}	Power Supply for Output Drivers.

LOGIC SYMBOL



TRUTH TABLE

OE	CLK_SEL1	CLK_SEL2	SEL1	SEL2	$Q_0 - Q_9$	$/Q_0 - /Q_9$	$Q_{10} - Q_{19}$	$/Q_{10} - /Q_{19}$
1	0	0	0	0	LVDS_CLKA	/LVDS_CLKA	LVDS_CLKA	/LVDS_CLKA
1	0	0	0	1	LVDS_CLKA	/LVDS_CLKA	LVDS_CLKB	/LVDS_CLKB
1	0	0	1	0	LVDS_CLKB	/LVDS_CLKB	LVDS_CLKA	/LVDS_CLKA
1	0	0	1	1	LVDS_CLKB	/LVDS_CLKB	LVDS_CLKB	/LVDS_CLKB
1	0	1	0	0	LVDS_CLKA	/LVDS_CLKA	LVDS_CLKA	/LVDS_CLKA
1	0	1	0	1	LVDS_CLKA	/LVDS_CLKA	LVPECL_CLKB	/LVPECL_CLKB
1	0	1	1	0	LVPECL_CLKB	/LVPECL_CLKB	LVDS_CLKA	/LVDS_CLKA
1	0	1	1	1	LVPECL_CLKB	/LVPECL_CLKB	LVPECL_CLKB	/LVPECL_CLKB
1	1	0	0	0	LVPECL_CLKA	/LVPECL_CLKA	LVPECL_CLKA	/LVPECL_CLKA
1	1	0	0	1	LVPECL_CLKA	/LVPECL_CLKA	LVDS_CLKB	/LVDS_CLKB
1	1	0	1	0	LVDS_CLKB	/LVDS_CLKB	LVPECL_CLKA	/LVPECL_CLKA
1	1	0	1	1	LVDS_CLKB	/LVDS_CLKB	LVDS_CLKB	/LVDS_CLKB
1	1	1	0	0	LVPECL_CLKA	/LVPECL_CLKA	LVPECL_CLKA	/LVPECL_CLKA
1	1	1	0	1	LVPECL_CLKA	/LVPECL_CLKA	LVPECL_CLKB	/LVPECL_CLKB
1	1	1	1	0	LVPECL_CLKB	/LVPECL_CLKB	LVPECL_CLKA	/LVPECL_CLKA
1	1	1	1	1	LVPECL_CLKB	/LVPECL_CLKB	LVPECL_CLKB	/LVPECL_CLKB
0	X	X	X	X	LOW	HIGH	LOW	HIGH

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating		Value	Unit
V_{CCI} / V_{CCO}	V_{CC} Pin Potential to Ground Pin		–0.5 to +4.0	V
V_{IN}	Input Voltage		–0.5 to V_{CCI}	V
I_{OUT}	DC Output Current (Output HIGH)		–50	mA
T_{LEAD}	Lead Temperature (soldering, 20sec.)		260	°C
T_{store}	Storage Temperature		–65 to +150	°C
θ_{JA}	Package Thermal Resistance (Junction-to-Ambient)			
	With exposed pad soldered to GND	– Still-Air (multi-layer PCB)	23	°C/W
		– 200lfpm (multi-layer PCB)	18	°C/W
		– 500lfpm (multi-layer PCB)	15	°C/W
	Exposed pad *not* soldered to GND	– Still-Air (multi-layer PCB)	44	°C/W
		– 200lfpm (multi-layer PCB)	36	°C/W
		– 500lfpm (multi-layer PCB)	30	°C/W
θ_{JC}	Package Thermal Resistance (Junction-to-Case)		4.3	°C/W

NOTE:

1. Permanent device damage may occur if absolute maximum ratings are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data book. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

Power Supply

Symbol	Parameter	T_A = –40°C			T_A = +25°C			T_A = +85°C			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{CCI}, V_{CCO}	Power Supply(1)	2.37	—	3.6	2.37	—	3.8	2.37	—	3.6	V
I_{CC}	I_{CC} Total Supply Current(2)	—	100	150	—	100	150	—	100	150	mA

NOTES:

1. V_{CCI} and V_{CCO} must be connected together on the PCB such that they remain at the same potential. V_{CCI} and V_{CCO} are not internally connected on the die.
2. No load. Outputs floating.

LVDS Input (V_{CC} = 2.37V to 3.6V, GND = 0V)

Symbol	Parameter	T_A = –40°C			T_A = +25°C			T_A = +85°C			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{IN}	Input Voltage Range	0	—	2.4	0	—	2.4	0	—	2.4	V
V_{ID}	Differential Input Swing	100	—	—	100	—	—	100	—	—	mV
I_{IL}	Input Low Current(1)	–1.0	—	—	–1.0	—	—	–1.0	—	—	mA
R_{IN}	LVDS Differential Input Resistance (LVDS_CLK to /LVDS_CLK)	80	100	120	80	100	120	80	100	120	Ω

NOTE:

1. For I_{IL}, both LVDS inputs are grounded.

LVPECL Input / Output (V_{CC} = 2.37V to 3.6V, GND = 0V)

Symbol	Parameter	T_A = –40°C		T_A = +25°C		T_A = +85°C		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	Input HIGH Voltage	V_{CC} – 1.165	V_{CC} – 0.88	V_{CC} – 1.165	V_{CC} – 0.88	V_{CC} – 1.165	V_{CC} – 0.88	V
V_{IL}	Input LOW Voltage	V_{CC} – 1.945	V_{CC} – 1.625	V_{CC} – 1.945	V_{CC} – 1.625	V_{CC} – 1.945	V_{CC} – 1.625	V
V_{PP}	Minimum Input Swing(1) LVPECL_CLK	600	—	600	—	600	—	mV
V_{CMR}	Common Mode Range(2) LVPECL_CLK	–1.5	–0.4	–1.5	–0.4	–1.5	–0.4	V
V_{OH}	Output HIGH Voltage	V_{CCO} – 1.085	V_{CCO} – 0.880	V_{CCO} – 1.025	V_{CCO} – 0.880	V_{CCO} – 1.025	V_{CCO} – 0.880	V
V_{OL}	Output LOW Voltage	V_{CCO} – 1.830	V_{CCO} – 1.555	V_{CCO} – 1.810	V_{CCO} – 1.620	V_{CCO} – 1.810	V_{CCO} – 1.620	V
I_{IH}	Input HIGH Current	—	150	—	150	—	150	µA
I_{IL}	Input LOW Current	0.5	—	0.5	—	0.5	—	µA

NOTES:

1. The V_{PP} (min.) is defined as the minimum input differential voltage which will cause no increase in the propagation delay.
2. V_{CMR} is defined as the range within which the V_{IH} level may vary, with the device still meeting the propagation delay specification. The numbers in the table are referenced to V_{CCI}. The V_{IL} level must be such that the peak-to-peak voltage is less than 1.0V and greater than or equal to V_{PP} (min.). The lower end of the CMR range varies 1:1 with V_{CCI}. The V_{CMR} (min) will be fixed at 3.3V – $|V_{CMR}$ (min)|.

LVCMOS/LVTTL Control Input (OE1, OE2, CLK_SEL1, CLK_SEL2)

Symbol	Parameter	T_A = –40°C			T_A = +25°C			T_A = +85°C			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{IH}	Input HIGH Voltage	2.0	—	—	2.0	—	—	2.0	—	—	V
V_{IL}	Input LOW Voltage	—	—	0.8	—	—	0.8	—	—	0.8	V
I_{IH}	Input HIGH Current	+20	—	–250	+20	—	–250	+20	—	–250	µA
I_{IL}	Input LOW Current	—	—	–600	—	—	–600	—	—	–600	µA

AC ELECTRICAL CHARACTERISTICS[1]

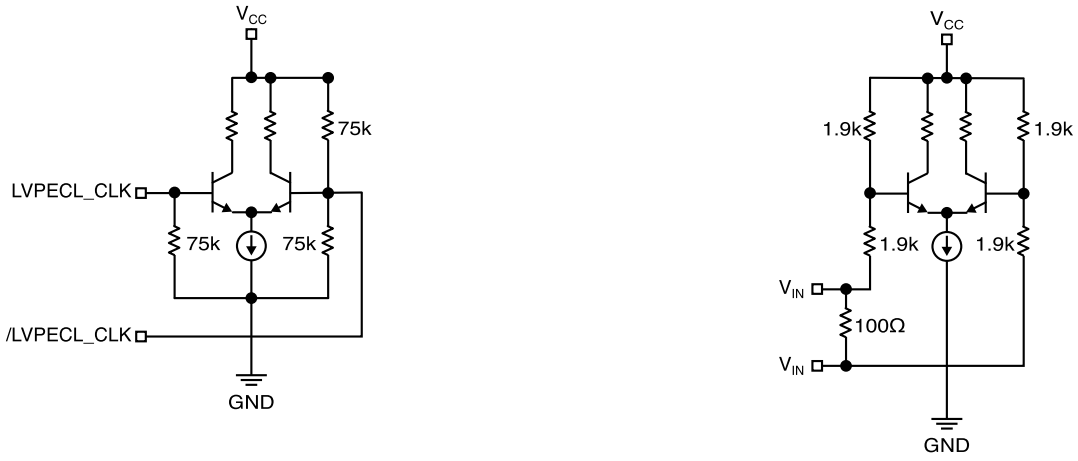
V_{CC} = 2.37V to 3.6V, GND = 0V

Symbol	Parameter	T_A = –40°C			T_A = +25°C			T_A = +85°C			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
f_{MAX}	Max Toggle Frequency[2]	2	—	—	2	—	—	2	—	—	GHz
t_{PD}	Propagation Delay (Differential)[3] LVPECL IN	0.900	—	1.5	0.900	1.2	1.5	0.900	—	1.5	ns
	LVDS IN	1.1	—	1.7	1.1	—	1.7	1.1	—	1.7	
t_{SKEW}	Within-Device Skew[4]	—	—	35	—	20	35	—	—	35	ps
	Part-to-Part Skew[5]	—	100	200	—	100	200	—	100	200	ps
$t_{S(OE)}$	OE Set-Up Time[6]	1.0	—	—	1.0	—	—	1.0	—	—	ns
$t_{H(OE)}$	OE Hold Time[6]	0.5	—	—	0.5	—	—	0.5	—	—	ns
t_r t_f	Output Rise/Fall Time (20% – 80%)	300	—	600	300	450	600	300	—	600	ps
$t_{(switchover)}$	Input Switchover CLK_SEL-to-valid output	—	—	1.2	—	—	1.2	—	—	1.2	ns

NOTES:

1. Outputs loaded with 50Ω to V_{CC} – 2V. Airflow ≥ 300lfpm.
2. f_{MAX} is defined as the maximum toggle frequency measured. Measured with a 750mV input signal, all loading with 50Ω to V_{CC} –2V.
3. Differential propagation delay is defined as the delay from the crossing point of the differential input signals to the crossing point of the differential output signals.
4. The within-device skew is defined as the worst case difference between any two similar delay paths within a single device operating at the same voltage and temperature.
5. The part-to-part skew is defined as the absolute worst case difference between any two delay paths on any two devices operating at the same voltage and temperature. Part-to-part skew is the total skew difference; pin-to-pin skew + part-to-part skew.
6. Set-up and hold time applies to synchronous applications that intend to enable/disable before the next clock cycle. For asynchronous applications, set-up and hold time does not apply. OE set-up time is defined with respect to the rising edge of the clock. OE HIGH to LOW transition ensures outputs remain disabled during the next clock cycle. OE LOW to HIGH transition enables normal operation of the next input clock.

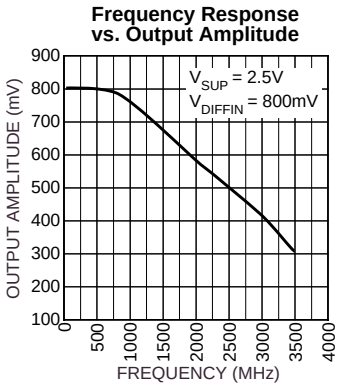
LVDS/LVPECL INPUTS



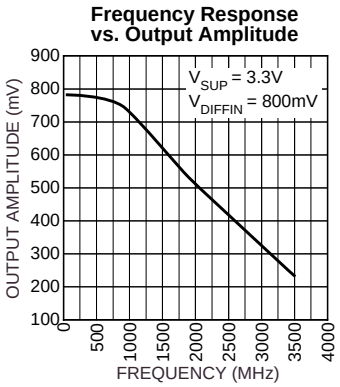
LVPECL Input Stage **LVDS Input Stage**

Figure 1. Simplified LVPECL & LVDS Input Stage

TYPICAL CHARACTERISTICS



Frequency Response vs. Output Amplitude @2.5V



Frequency Response vs. Output Amplitude @3.3V

LVPECL TERMINATION RECOMMENDATIONS

Output Considerations

Be sure to properly terminate all outputs as shown below, or equivalent. For AC coupled applications, be sure to include a pull down resistor at the output of each driver. The emmiter follower outputs requires a DC current path to GND. Unused outputs can be left floating with minimal impact on skew and jitter.

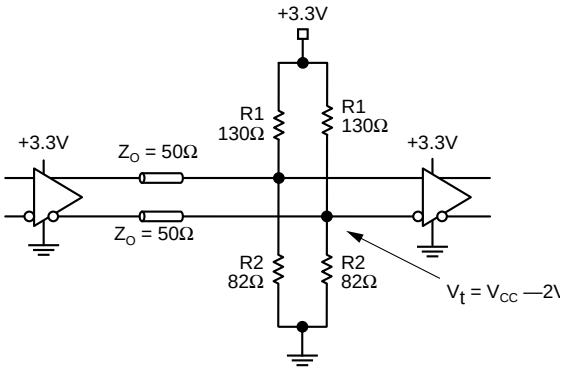


Figure 1. Parallel Termination–Thevenin Equivalent

Notes:

1. For +2.5V systems:
   R1 = 250Ω
   R2 = 62.5Ω

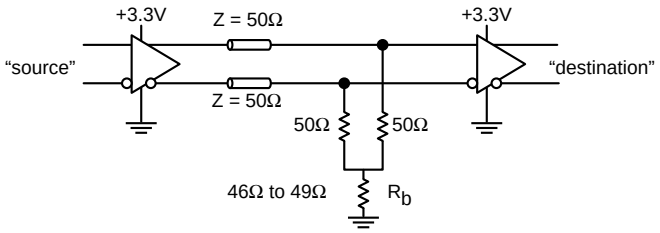
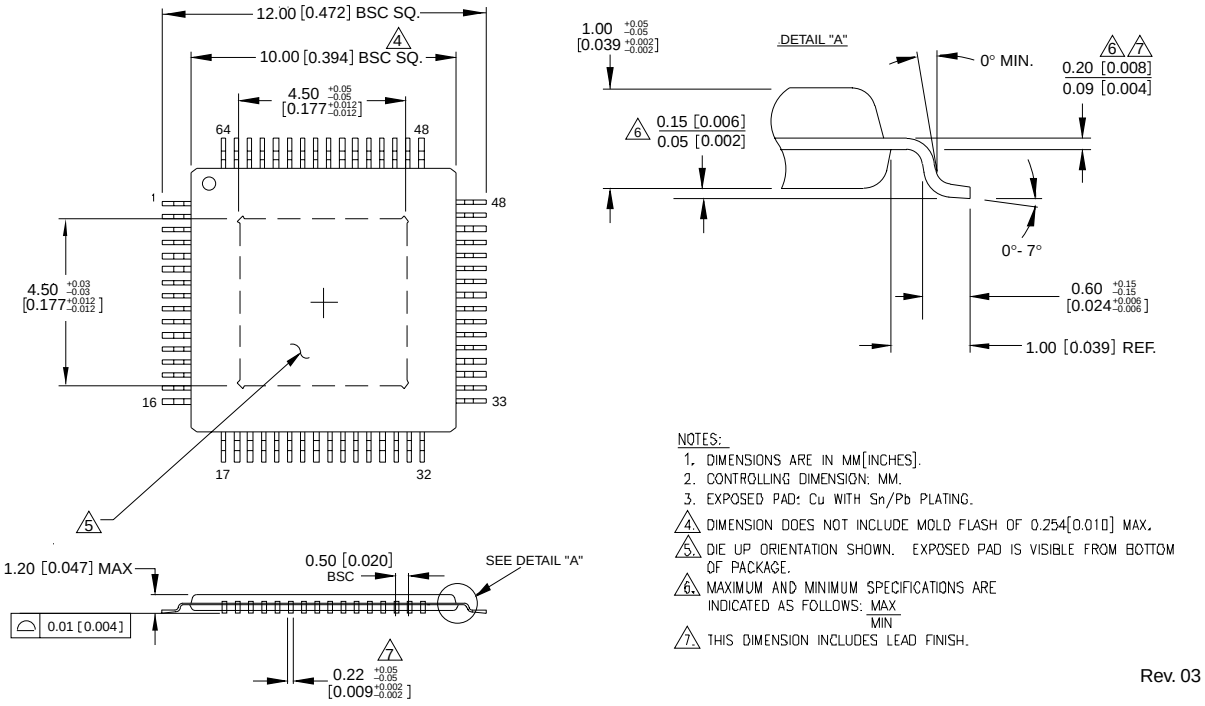


Figure 2. Three-Resistor "Y–Termination"

Notes:

1. Power-saving alternative to Thevenin termination.
2. Place termination resistors as close to destination inputs as possible.
3. R_b resistor sets the DC bias voltage equal to V_t. For +3.3V systems R_b = 46Ω to 50Ω.
4. Precision, low-cost 3-Resistor networks are available from resistor manufacturers such as Thin Film Technology (www.thinfilm.com).

64-PIN EPAD-TQFP (DIE UP) (H64-1)



NOTES:
1. DIMENSIONS ARE IN MM[INCHES].
2. CONTROLLING DIMENSION: MM.
3. EXPOSED PAD: Cu WITH Sn/Pb PLATING.
4. DIMENSION DOES NOT INCLUDE MOLD FLASH OF 0.254[0.010] MAX.
5. DIE UP ORIENTATION SHOWN. EXPOSED PAD IS VISIBLE FROM BOTTOM OF PACKAGE.
6. MAXIMUM AND MINIMUM SPECIFICATIONS ARE INDICATED AS FOLLOWS: MAX / MIN
7. THIS DIMENSION INCLUDES LEAD FINISH.

Rev. 03

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