# L6561

## POWER FACTOR CORRECTOR

## 1 FEATURES

- VERY PRECISE ADJUSTABLE OUTPUT OVERVOLTAGE PROTECTION
- MICRO POWER START-UP CURRENT (50µA TYP.)
- VERY LOW OPERATING SUPPLY CURRENT(4mA TYP.)
- INTERNAL START-UP TIMER
- CURRENT SENSE FILTER ON CHIP
- DISABLE FUNCTION
- 1% PRECISION (@ $T_j$ = 25°C) INTERNAL REFERENCE VOLTAGE
- TRANSITION MODE OPERATION
- TOTEM POLE OUTPUT CURRENT: ±400mA
- DIP-8/SO-8 PACKAGES

## 2 DESCRIPTION

L6561 is the improved version of the L6560 standard Power Factor Corrector. Fully compatible with the standard version, it has a superior performant multiplier making the device capable of working in wide input voltage range applications (from 85V to 265V) with an excellent THD. Furthermore the start up current has been reduced at few tens of mA and a disable function has been implemented on the ZCD pin, guaranteeing lower current consumption in stand by mode.

**Figure 1. Packages**

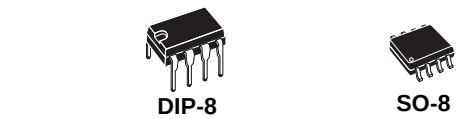



**Table 1. Order Codes**

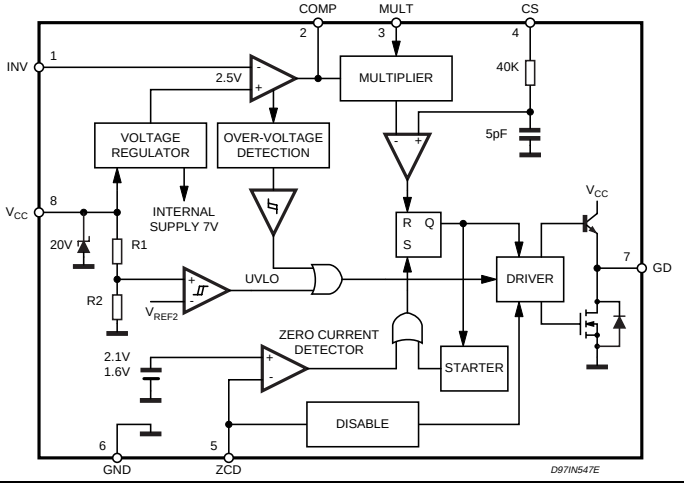
| Part Number | Package |
|---|---|
| L6561 | DIP-8 |
| L6561D | SO-8 |
| L6561D013TR | Tape & Reel |

Realised in mixed BCD technology, the chip gives the following benefits:

- micro power start up current
- 1% precision internal reference voltage
- (Tj = 25°C)
- Soft Output Over Voltage Protection
- no need for external low pass filter on the current sense
- very low operating quiescent current minimises power dissipation

The totem pole output stage is capable of driving a Power MOS or IGBT with source and sink currents of ±400mA. The device is operating in transition mode and it is optimised for Electronic Lamp Ballast application, AC-DC adaptors and SMPS.

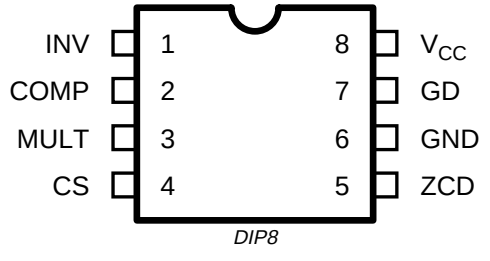
**Figure 2. Block Diagram**



### Table 2. Absolute Maximum Ratings

| Symbol | Pin | Parameter | Value | Unit |
|---|---|---|---|---|
| $I_{Vcc}$ | 8 | $I_q + I_Z$; ($I_{GD}$ = 0) | 30 | mA |
| $I_{GD}$ | 7 | Output Totem Pole Peak Current (2µs) | ±700 | mA |
| INV, COMP MULT | 1, 2, 3 | Analog Inputs & Outputs | -0.3 to 7 | V |
| CS | 4 | Current Sense Input | -0.3 to 7 | V |
| ZCD | 5 | Zero Current Detector | 50 (source)<br>-10 (sink) | mA<br>mA |
| $P_{tot}$ | | Power Dissipation @$T_{amb}$ = 50 °C (DIP-8)<br>(SO-8) | 1<br>0.65 | W<br>W |
| $T_j$ | | Junction Temperature Operating Range | -40 to 150 | °C |
| $T_{stg}$ | | Storage Temperature | -55 to 150 | °C |

### Figure 3. Pin Connection (Top view)




*DIP8*

### Table 3. Thermal Data

| Symbol | Parameter | SO 8 | MINIDIP | Unit |
|---|---|---|---|---|
| $R_{th\ j\text{-}amb}$ | Thermal Resistance Junction to ambient | 150 | 100 | °C/W |

### Table 4. Pin Description

| N. | Name | Function |
|---|---|---|
| 1 | INV | Inverting input of the error amplifier. A resistive divider is connected between the output regulated voltage and this point, to provide voltage feedback. |
| 2 | COMP | Output of error amplifier. A feedback compensation network is placed between this pin and the INV pin. |
| 3 | MULT | Input of the multiplier stage. A resistive divider connects to this pin the rectified mains. A voltage signal, proportional to the rectified mains, appears on this pin. |
| 4 | CS | Input to the comparator of the control loop. The current is sensed by a resistor and the resulting voltage is applied to this pin. |
| 5 | ZCD | Zero current detection input. If it is connected to GND, the device is disabled. |
| 6 | GND | Current return for driver and control circuits. |
| 7 | GD | Gate driver output. A push pull output stage is able to drive the Power MOS with peak current of 400mA (source and sink). |
| 8 | $V_{CC}$ | Supply voltage of driver and control circuits. |

(1) Parameter guaranteed by design, not tested in production.

**Table 5. Electrical Characteristics**

($V_{CC}$ = 14.5V; $T_{amb}$ = -25°C to 125°C;unless otherwise specified)

| Symbol | Pin | Parameter | Test Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| **SUPPLY VOLTAGE SECTION** | | | | | | | |
| $V_{CC}$ | 8 | Operating Range | after turn-on | 11 | | 18 | V |
| $V_{CC\ ON}$ | 8 | Turn-on Threshold | | 11 | 12 | 13 | V |
| $V_{CC\ OFF}$ | 8 | Turn-off Threshold | | 8.7 | 9.5 | 10.3 | V |
| Hys | 8 | Hysteresis | | 2.2 | 2.5 | 2.8 | V |
| **SUPPLY CURRENT SECTION** | | | | | | | |
| $I_{START-U}$ | 8 | Start-up Current | before turn-on ($V_{CC}$ =11V) | 20 | 50 | 90 | µA |
| $I_q$ | 8 | Quiescent Current | | | 2.6 | 4 | mA |
| $I_{CC}$ | 8 | Operating Supply Current | $C_L$ = 1nF @ 70KHz | | 4 | 5.5 | mA |
| | | | in OVP condition $V_{pin1}$ = 2.7V | | 1.4 | 2.1 | mA |
| Iq | 8 | Quiescent Current | $V_{PIN5}$ ≤150mV, $V_{CC} > V_{CC\ off}$ | | 1.4 | 2.1 | mA |
| | 8 | | $V_{PIN5} \leq 150mV$, $V_{CC} < V_{CC\ off}$ | 20 | 50 | 90 | µA |
| $V_Z$ | 8 | Zener Voltage | $I_{CC}$ = 25mA | 18 | 20 | 22 | V |
| **ERROR AMPLIFIER SECTION** | | | | | | | |
| $V_{INV}$ | 1 | Voltage Feedback Input Threshold | $T_{amb}$ = 25°C | 2.465 | 2.5 | 2.535 | V |
| | | | 12V < $V_{CC}$ < 18V | 2.44 | | 2.56 | V |
| | | Line Regulation | $V_{CC}$ = 12 to 18V | | 2 | 5 | mV |
| $I_{INV}$ | 1 | Input Bias Current | | | -0.1 | -1 | µA |
| $G_V$ | | Voltage Gain | Open loop | 60 | 80 | | dB |
| GB | | Gain Bandwidth | | | 1 | | MHz |
| $I_{COMP}$ | 2 | Source Current | $V_{COMP}$ = 4V, $V_{INV}$ = 2.4V | -2 | -4 | -8 | mA |
| | | Sink Current | $V_{COMP}$ = 4V, $V_{INV}$ = 2.6V | 2.5 | 4.5 | | mA |
| $V_{COMP}$ | 2 | Upper Clamp Voltage | $I_{SOURCE}$ = 0.5mA | | 5.8 | | V |
| | | Lower Clamp Voltage | $I_{Sink}$ = 0.5mA | | 2.25 | | V |
| **MULTIPLIER SECTION** | | | | | | | |
| $V_{MULT}$ | 3 | Linear Operating Voltage | | 0 to 3 | 0 to 3.5 | | V |
| $\frac{\Delta V_{CS}}{\Delta V_{mult}}$ | | Output Max. Slope | $V_{MULT}$ = from 0V to 0.5V<br>$V_{COMP}$ = Upper Clamp Voltage | 1.65 | 1.9 | | |
| K | | Gain | $V_{MULT}$ = 1V $V_{COMP}$ = 4V | 0.45 | 0.6 | 0.75 | 1/V |
| **CURRENT SENSE COMPARATOR** | | | | | | | |
| $V_{CS}$ | 4 | Current Sense Reference Clamp | $V_{MULT}$ = 2.5V<br>$V_{COMP}$ = Upper Clamp Voltage | 1.6 | 1.7 | 1.8 | V |
| $I_{CS}$ | 4 | Input Bias Current | $V_{OS}$ = 0 | | -0.05 | -1 | µA |
| $t_{d\ (H-L)}$ | 4 | Delay to Output | | | 200 | 450 | ns |
| | 4 | Current Sense Offset | | | 0 | 15 | mV |
| **ZERO CURRENT DETECTOR** | | | | | | | |
| $V_{ZCD}$ | 5 | Input Threshold Voltage Rising Edge | (1) | | 2.1 | | V |
| | | Hysteresis | (1) | 0.3 | 0.5 | 0.7 | V |
| $V_{ZCD}$ | 5 | Upper Clamp Voltage | $I_{ZCD}$ = 20µA | 4.5 | 5.1 | 5.9 | V |
| $V_{ZCD}$ | 5 | Upper Clamp Voltage | $I_{ZCD}$ = 3mA | 4.7 | 5.2 | 6.1 | V |

**Table 5. Electrical Characteristics** (continued)
($V_{CC}$ = 14.5V; $T_{amb}$ = -25°C to 125°C;unless otherwise specified)

| Symbol | Pin | Parameter | Test Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| $V_{ZCD}$ | 5 | Lower Clamp Voltage | $I_{ZCD}$ = -3mA | 0.3 | 0.65 | 1 | V |
| $I_{ZCD}$ | 5 | Sink Bias Current | 1V ≤ $V_{ZCD}$ ≤ 4.5V | | 2 | | µA |
| $I_{ZCD}$ | 5 | Source Current Capability | | -3 | | -10 | mA |
| $I_{ZCD}$ | 5 | Sink Current Capability | | 3 | | 10 | mA |
| $V_{DIS}$ | 5 | Disable threshold | | 150 | 200 | 250 | mV |
| $I_{ZCD}$ | 5 | Restart Current After Disable | $V_{ZCD}$ < $V_{dis}$; $V_{CC}$ > $V_{CCOFF}$ | -100 | -200 | -300 | µA |
| **OUTPUT SECTION** | | | | | | | |
| $V_{GD}$ | 7 | Dropout Voltage | $I_{GDsource}$ = 200mA | | 1.2 | 2 | V |
| | | | $I_{GDsource}$ = 20mA | | 0.7 | 1 | V |
| | | | $I_{GDsink}$ = 200mA | | | 1.5 | V |
| | | | $I_{GDsink}$ = 20mA | | | 0.3 | V |
| $t_r$ | 7 | Output Voltage Rise Time | $C_L$ = 1nF | | 40 | 100 | ns |
| $t_f$ | 7 | Output Voltage Fall Time | $C_L$ = 1nF | | 40 | 100 | ns |
| $I_{GD\ off}$ | 7 | IGD Sink Current | $V_{CC}$ =3.5V $V_{GD}$ = 1V | 5 | 10 | - | mA |
| **OUTPUT OVERVOLTAGE SECTION** | | | | | | | |
| $I_{OVP}$ | 2 | OVP Triggering Current | | 35 | 40 | 45 | µA |
| | | Static OVP Threshold | | 2.1 | 2.25 | 2.4 | V |
| **RESTART TIMER** | | | | | | | |
| $t_{START}$ | | Start Timer | | 70 | 150 | 400 | µs |

# 3 OVER VOLTAGE PROTECTION OVP

The output voltage is expected to be kept by the operation of the PFC circuit close to its nominal value. This is set by the ratio of the two external resistors R1 and R2 (see fig. 5), taking into consideration that the non inverting input of the error amplifier is biased inside the L6561 at 2.5V.

In steady state conditions, the current through R1 and R2 is:

$$I_{R1sc} = \frac{V_{out} - 2.5}{R1} = I_{R2} = \frac{2.5V}{R2}$$

and, if the external compensation network is made only with a capacitor $C_{comp}$, the current through $C_{comp}$ equals zero.When the output voltage increases abruptly the current through R1 becomes:

$$I_{R1} = \frac{V_{outsc} + \Delta V_{out} - 2.5}{R1} = I_{R1sc} + \Delta I_{R1}$$

Since the current through R2 does not change, $\Delta I_{R1}$ must flow through the capacitor $C_{comp}$ and enter the error amplifier.

This current is monitored inside the L6561 and when reaches about 37µA the output voltage of the multiplier is forced to decrease, thus reducing the energy drawn from the mains. If the current exceeds 40µA, the OVP protection is triggered (Dynamic OVP), and the external power transistor is switched off until the current falls approximately below 10µA.

However, if the overvoltage persists, an internal comparator (Static OVP) confirms the OVP condition keeping the external power switch turned off (see fig. 4).Finally, the overvoltage that triggers the OVP function is:

$$\Delta V_{out} = R_1 \cdot 40\mu A.$$

Typical values for $R_1$, $R_2$ and C are shown in the application circuits. The overvoltage can be set indepen-

dently from the average output voltage. The precision in setting the overvoltage threshold is 7% of the overvoltage value (for instance $\Delta V$ = 60V ± 4.2V).

### 3.1 Disable function

The zero current detector (ZCD) pin can be used for device disabling as well. By grounding the ZCD voltage the device is disabled reducing the supply current consumption at 1.4mA typical (@ 14.5V supply voltage).

Releasing the ZCD pin the internal start-up timer will restart the device.

**Figure 4.**

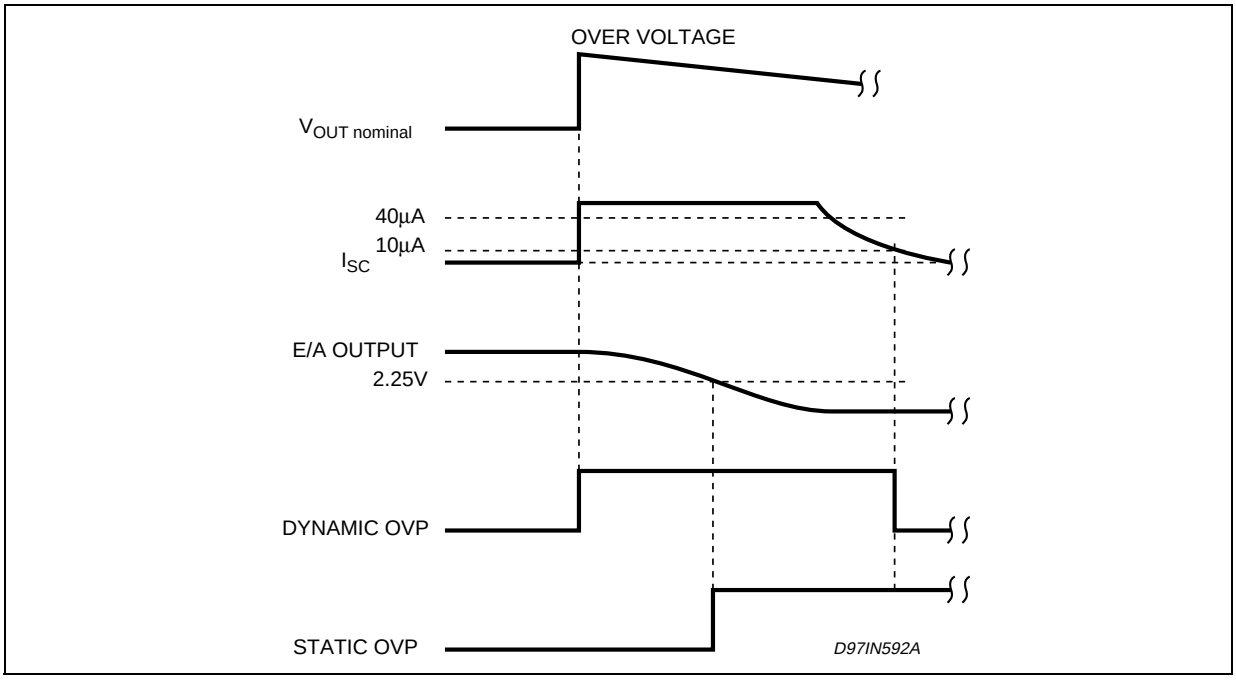
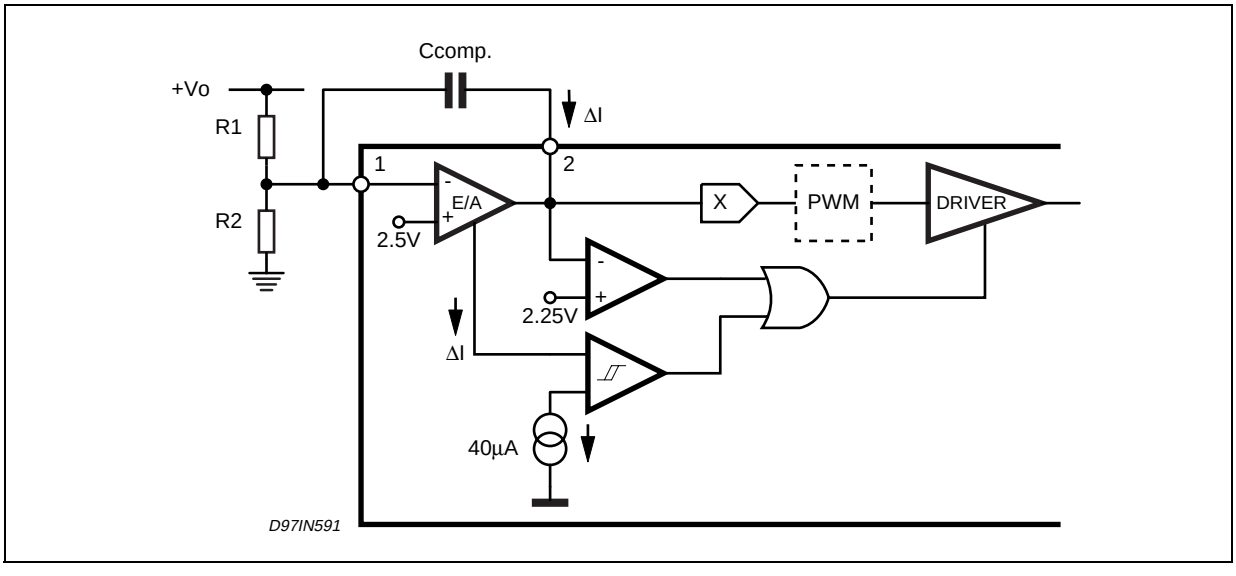
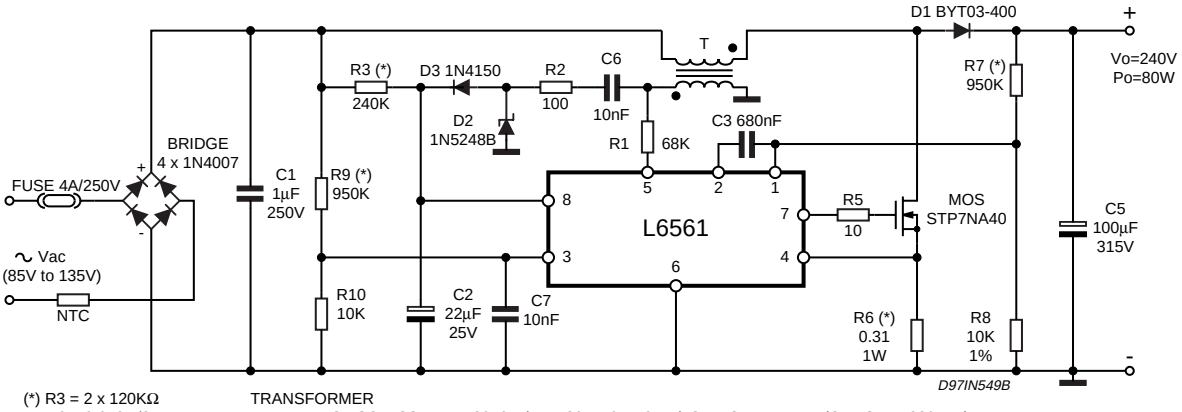



**Figure 5. Overvoltage Protection Circuit**



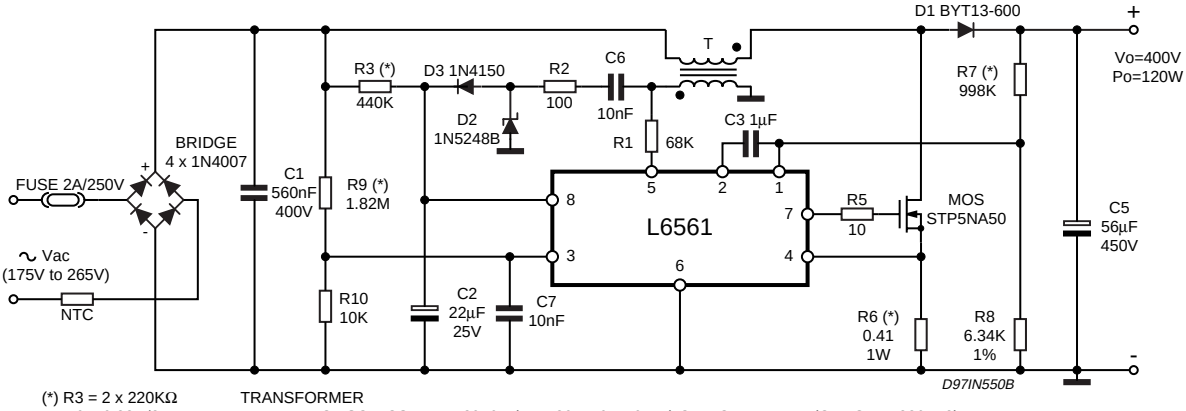
## Figure 6. Typical Application Circuit (80W, 110VAC)




(*) R3 = 2 x 120KΩ
R6 = 0.619Ω/2
R7 = 2 x 475KΩ, 1%
R9 = 2 x 475KΩ

TRANSFORMER
T: core THOMSON-CSF B1ET2910A (ETD 29 x 16 x 10mm) OR EQUIVALENT (OREGA 473201A7)
primary 90T of Litz wire 10 x 0.2mm
secondary 11T of #27 AWG (0.15mm)
gap 1.8mm for a total primary inductance of 0.7mH

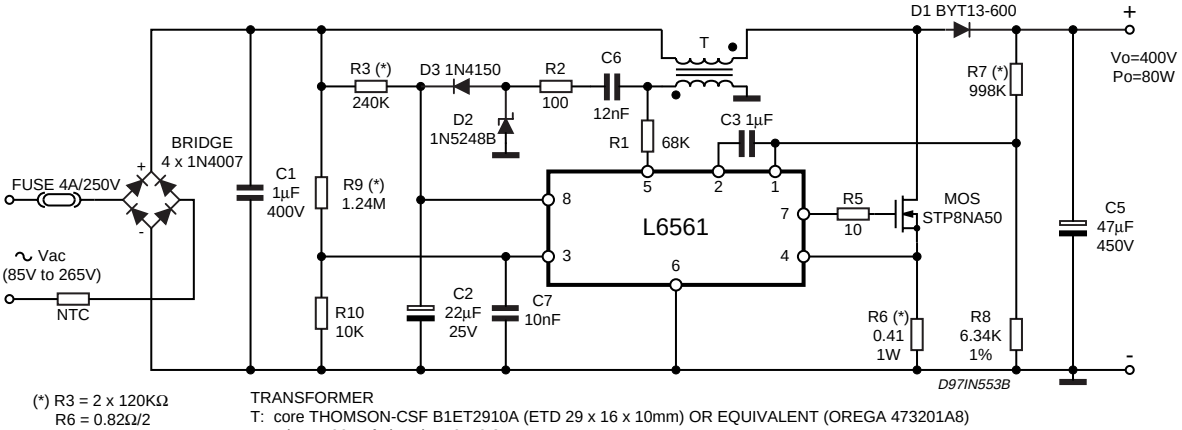
## Figure 7. Typical Application Circuit (120W, 220VAC)




(*) R3 = 2 x 220KΩ
R6 = 0.82Ω/2
R7 = 2 x 499KΩ, 1%
R9 = 2 x 909KΩ

TRANSFORMER
T: core THOMSON-CSF B1ET2910A (ETD 29 x 16 x 10mm) OR EQUIVALENT (OREGA 473201A8)
primary 90T of Litz wire 10 x 0.2mm
secondary 7T of #27 AWG (0.15mm)
gap 1.25mm for a total primary inductance of 0.8mH

## Figure 8. Typical Application Circuit (80W, Wide-range Mains)




(*) R3 = 2 x 120KΩ
R6 = 0.82Ω/2
R7 = 2 x 499KΩ, 1%
R9 = 2 x 620KΩ

TRANSFORMER
T: core THOMSON-CSF B1ET2910A (ETD 29 x 16 x 10mm) OR EQUIVALENT (OREGA 473201A8)
primary 90T of Litz wire 10 x 0.2mm
secondary 7T of #27 AWG (0.15mm)
gap 1.25mm for a total primary inductance of 0.8mH

**Figure 9. Demo Board (EVAL6561-80) Electrical Schematic**

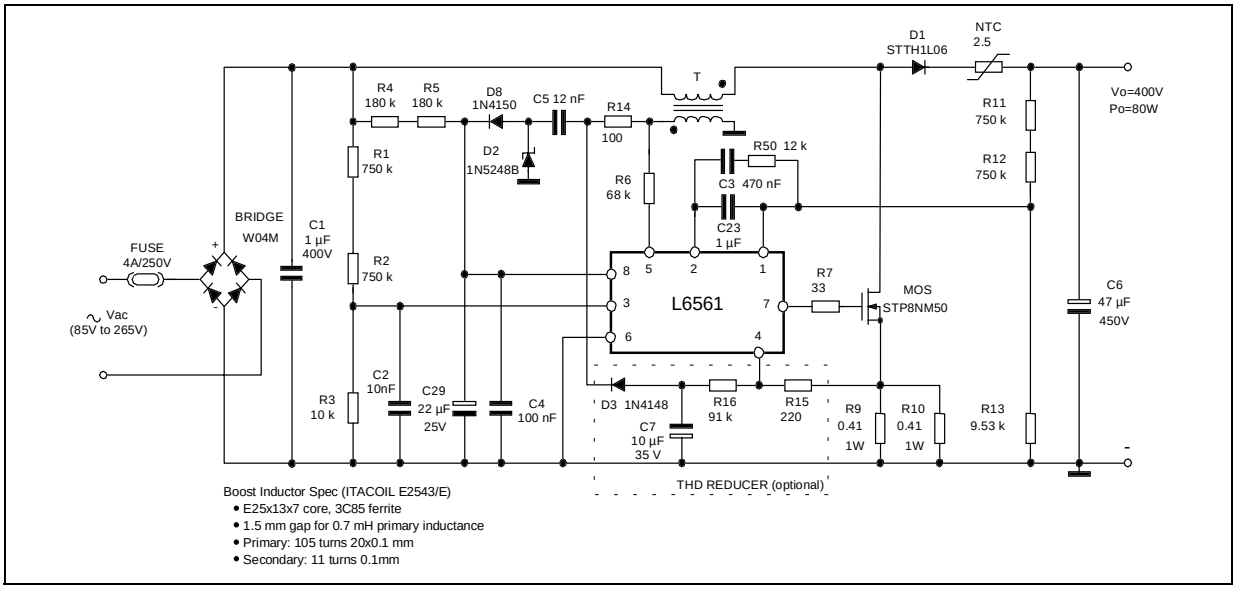



**Figure 10. EVAL6561-80: PCB and Component Layout (Top view, real size 57x108mm)**

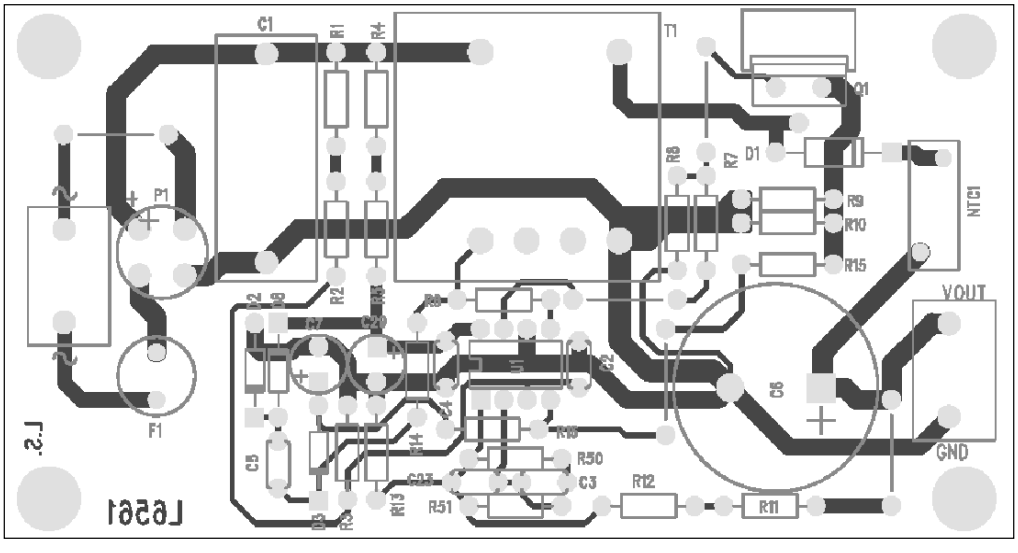



**Table 6. EVAL6561-80: Evaluation Results.**

| $V_{in}$ (Vac) | Pin (W) | $V_o$ (Vdc) | ΔVo (Vdc) | Po (W) | η (%) | w/o THD reducer | | with THD reducer | |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | | PF | THD (%) | PF | THD (%) |
| 85 | 87.2 | 400.1 | 14 | 80.7 | 92.8 | 0.999 | 3.7 | 0.999 | 2.9 |
| 110 | 85.2 | 400.1 | 14 | 80.7 | 94.7 | 0.996 | 5.0 | 0.996 | 3.2 |
| 135 | 84.2 | 400.1 | 14 | 80.7 | 95.8 | 0.989 | 6.2 | 0.989 | 3.7 |
| 175 | 83.5 | 400.1 | 14 | 80.7 | 96.6 | 0.976 | 8.3 | 0.976 | 4.3 |
| 220 | 83.1 | 400.1 | 14 | 80.7 | 97.1 | 0.940 | 10.7 | 0.941 | 5.6 |
| 265 | 82.9 | 400.1 | 14 | 80.7 | 97.3 | 0.890 | 13.7 | 0.893 | 8.1 |

**Figure 11. OVP Current Threshold vs. Temperature**

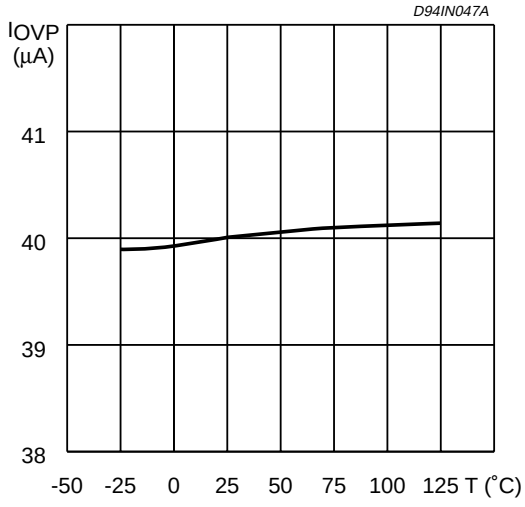



**Figure 12. Undervoltage Lockout Threshold vs. Temperature**

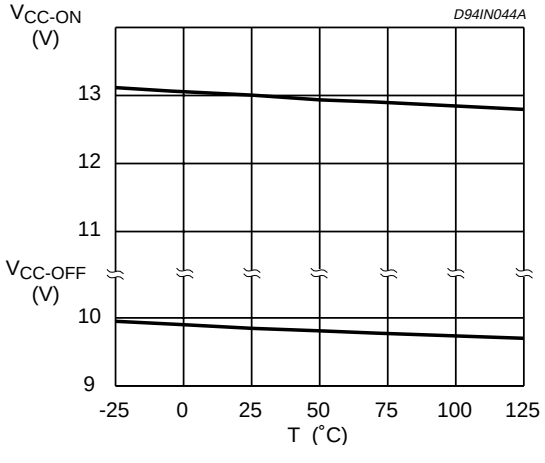



**Figure 13. Supply Current vs. Supply Voltage**

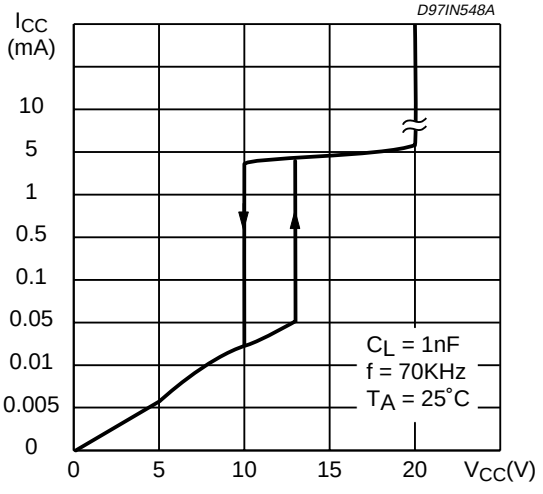



**Figure 14. Voltage Feedback Input Threshold vs. Temperature**

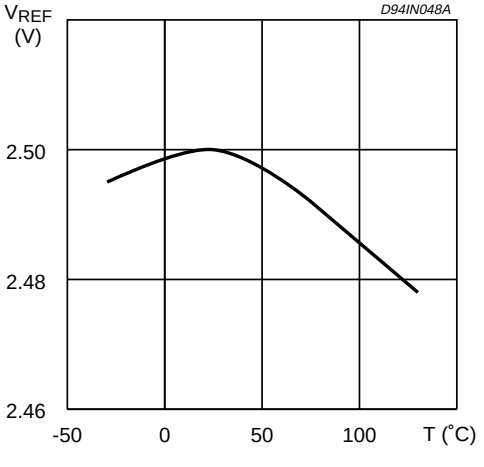


**Figure 15. Output Saturation Voltage vs. Sink Current**

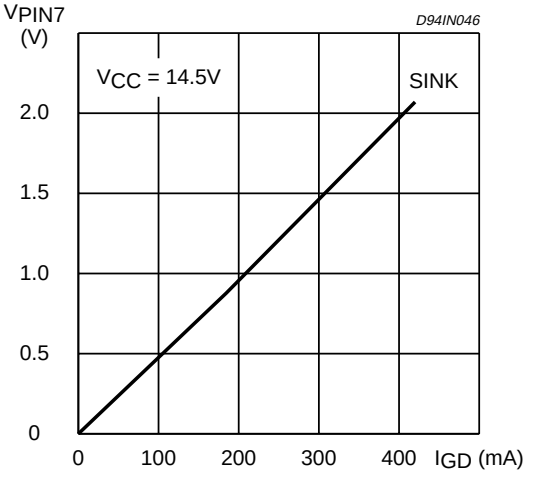



**Figure 16. Output Saturation Voltage vs. Source Current**

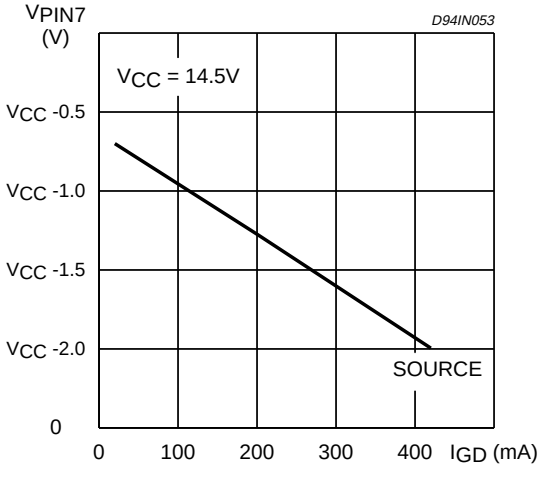



**Figure 17. Multiplier Characteristics Family**

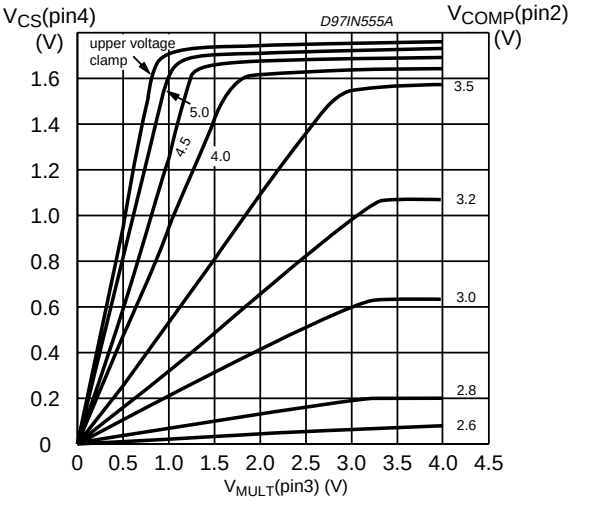
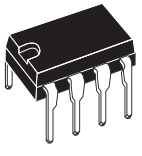


**Figure 18. DIP-8 Mechanical Data & Package Dimensions**

| DIM. | mm | | | inch | | |
|---|---|---|---|---|---|---|
| | MIN. | TYP. | MAX. | MIN. | TYP. | MAX. |
| A | | 3.32 | | | 0.131 | |
| a1 | 0.51 | | | 0.020 | | |
| B | 1.15 | | 1.65 | 0.045 | | 0.065 |
| b | 0.356 | | 0.55 | 0.014 | | 0.022 |
| b1 | 0.204 | | 0.304 | 0.008 | | 0.012 |
| D | | | 10.92 | | | 0.430 |
| E | 7.95 | | 9.75 | 0.313 | | 0.384 |
| e | | 2.54 | | | 0.100 | |
| e3 | | 7.62 | | | 0.300 | |
| e4 | | 7.62 | | | 0.300 | |
| F | | | 6.6 | | | 0.260 |
| I | | | 5.08 | | | 0.200 |
| L | 3.18 | | 3.81 | 0.125 | | 0.150 |
| Z | | | 1.52 | | | 0.060 |

**OUTLINE AND MECHANICAL DATA**



**DIP-8**

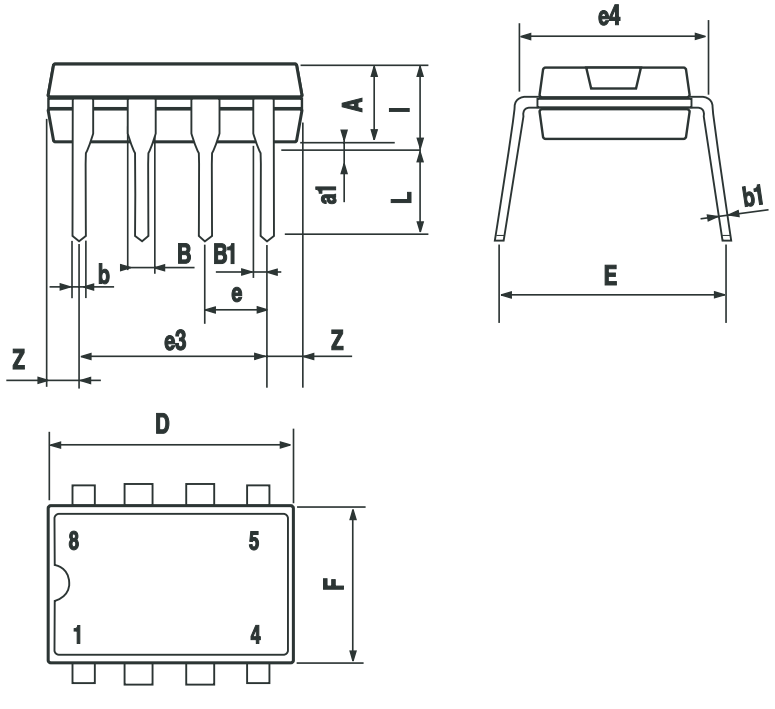
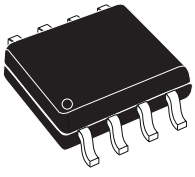


**Figure 19. SO-8 Mechanical Data & Package Dimensions**

| DIM. | mm | | | inch | | |
|---|---|---|---|---|---|---|
| | MIN. | TYP. | MAX. | MIN. | TYP. | MAX. |
| A | 1.35 | | 1.75 | 0.053 | | 0.069 |
| A1 | 0.10 | | 0.25 | 0.004 | | 0.010 |
| A2 | 1.10 | | 1.65 | 0.043 | | 0.065 |
| B | 0.33 | | 0.51 | 0.013 | | 0.020 |
| C | 0.19 | | 0.25 | 0.007 | | 0.010 |
| D (1) | 4.80 | | 5.00 | 0.189 | | 0.197 |
| E | 3.80 | | 4.00 | 0.15 | | 0.157 |
| e | | 1.27 | | | 0.050 | |
| H | 5.80 | | 6.20 | 0.228 | | 0.244 |
| h | 0.25 | | 0.50 | 0.010 | | 0.020 |
| L | 0.40 | | 1.27 | 0.016 | | 0.050 |
| k | 0° (min.), 8° (max.) | | | | | |
| ddd | | | 0.10 | | | 0.004 |

Note: (1) Dimensions D does not include mold flash, protrusions or gate burrs.
Mold flash, potrusions or gate burrs shall not exceed 0.15mm (.006inch) in total (both side).

**OUTLINE AND MECHANICAL DATA**



**SO-8**

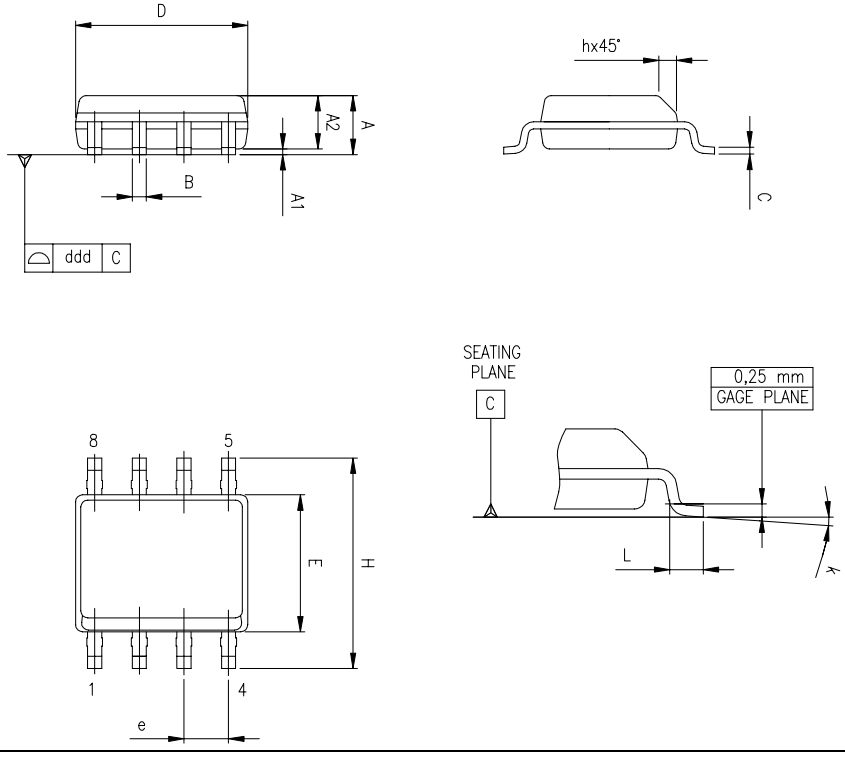


**Table 7. Revision History**

| Date | Revision | Description of Changes |
|---|---|---|
| January 2004 | 15 | First Issue |
| June 2004 | 16 | Modified the Style-look in compliance with the “Corporate Technical Publications Design Guide”.<br>Changed input of the power amplifier connected to Multiplier (Fig. 2). |

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