



DUAL N-CHANNEL ENHANCEMENT MODE MOSFET

Product Summary

| V _{(BR)DSS} | R _{DS(ON)} max | I _D max T _A = +25°C |
|----------------------|------------------------------|--|
| 60V | 5.0Ω @ $V_{GS} = 10V$ | 230mA |
| | 7.5Ω @ V _{GS} = 5V | 190mA |

Description

This MOSFET is designed to minimize the on-state resistance ($R_{DS(ON)}$) and yet maintain superior switching performance, making it ideal for high efficiency power management applications.

Applications

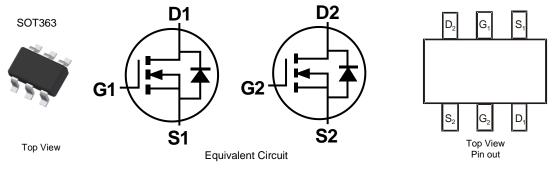
- Motor Control
- Power Management Functions

Features

- Dual N-Channel MOSFET
- Low On-Resistance
- Low Gate Threshold Voltage
- Low Input Capacitance
- Fast Switching Speed
- Low Input/Output Leakage
- Ultra-Small Surface Mount Package
- Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)
- Halogen and Antimony Free. "Green" Device (Note 3)
- Qualified to AEC-Q101 Standards for High Reliability

Mechanical Data

- Case: SOT363
- Case Material: Molded Plastic. "Green" Molding Compound.
 UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Matte Tin Finish Annealed over Alloy 42 Leadframe (Lead Free Plating). Solderable per MIL-STD-202, Method 208 (3)
- Terminal Connections: See Diagram
- Weight: 0.006 grams (Approximate)



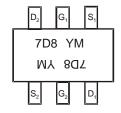
Ordering Information (Note 4)

| Part Number | Case | Packaging |
|---------------|--------|-------------------|
| DMN67D8LDW-7 | SOT363 | 3000/Tape & Reel |
| DMN67D8LDW-13 | SOT363 | 10000/Tape & Reel |

Notes:

- 1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant.
- 2. See http://www.diodes.com/quality/lead_free.html for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
- 3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
- 4. For packaging details, go to our website at http://www.diodes.com/products/packages.html.

Marking Information



7D8 = Product Type Marking Code YM = Date Code Marking Y or Y = Year (ex: C = 2015) M = Month (ex: 9 = September)

Date Code Key

| Year | 2014 | 2015 | 2016 | 2017 | 2018 | 2019 | 2020 | 2021 | 2022 | 2023 | 2024 | 2025 |
|-------|------|------|------|------|------|------|------|------|------|------|------|------|
| Code | В | С | D | Е | F | G | Н | | J | K | L | М |
| Month | Jan | Feb | Mar | Apr | May | Jun | Jul | Aug | Sep | Oct | Nov | Dec |
| Code | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 0 | N | D |



Maximum Ratings ($@T_A = +25^{\circ}C$, unless otherwise specified.)

| Characteristic | | Symbol | Value | Unit |
|---|----------------|-----------------|-------|------|
| Drain-Source Voltage | | V_{DSS} | 60 | V |
| Gate-Source Voltage | | V_{GSS} | ±30 | V |
| Continuous Drain Current (Note 6) V _{GS} = 10V | I _D | 230 180 | mA | |
| Maximum Continuous Body Diode Forward Curren | t (Note 6) | I _S | 0.5 | Α |
| Pulsed Drain Current (10µs Pulse, Duty Cycle = 1% | 6) (Note 6) | I _{DM} | 0.8 | Α |

Thermal Characteristics (@TA = +25°C, unless otherwise specified.)

| Characteristic | | Symbol | Value | Unit |
|--|--------------|----------------------------------|-------------|------|
| Total Power Dissipation (Note 5) | | P_D | 320 | mW |
| Thermal Resistance, Junction to Ambient (Note 5) | Steady State | R _{0JA} | 400 | °C/W |
| Total Power Dissipation (Note 6) | | P_{D} | 410 | mW |
| Thermal Resistance, Junction to Ambient (Note 6) | Steady State | R _{θJA} | 312 | °C/W |
| Operating and Storage Temperature Range | | T _{J,} T _{STG} | -55 to +150 | °C |

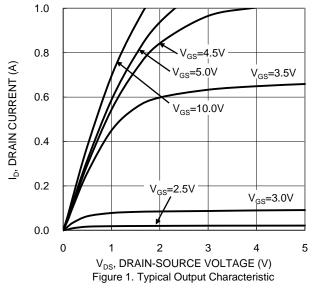
Electrical Characteristics (@T_A = +25°C, unless otherwise specified.)

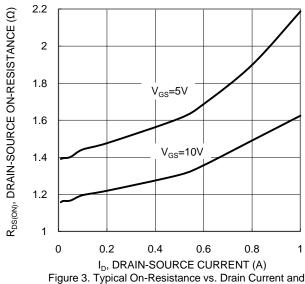
| Characteristic | Symbol | Min | Тур | Max | Unit | Test Condition |
|--|---------------------|-----|------|------|------|---|
| OFF CHARACTERISTICS (Note 7) | | | | | | |
| Drain-Source Breakdown Voltage | BV _{DSS} | 60 | _ | _ | V | $V_{GS} = 0V, I_{D} = 10\mu A$ |
| Zero Gate Voltage Drain Current | I _{DSS} | | - | 1.0 | μΑ | $V_{DS} = 60V$, $V_{GS} = 0V$ |
| Gate-Source Leakage | IGSS | - | _ | ±100 | nΑ | $V_{GS} = \pm 20V, V_{DS} = 0V$ |
| ON CHARACTERISTICS (Note 7) | | | | | | |
| Gate Threshold Voltage | V _{GS(TH)} | 1.0 | _ | 2.5 | V | $V_{DS} = 10V, I_D = 250\mu A$ |
| Static Drain-Source On-Resistance | D-s/s/s | | 1.5 | 5.0 | Ω | $V_{GS} = 10V, I_D = 0.5A$ |
| Static Dialif-Source Off-Resistance | R _{DS(ON)} | _ | 3.2 | 7.5 | 12 | $V_{GS} = 5V, I_D = 0.05A$ |
| Forward Transfer Admittance | Y _{fs} | 80 | _ | _ | mS | $V_{DS} = 10V, I_D = 0.2A$ |
| Diode Forward Voltage | V_{SD} | | 0.78 | 1.5 | V | $V_{GS} = 0V, I_{S} = 115mA$ |
| DYNAMIC CHARACTERISTICS (Note 8) | | | | | | |
| Input Capacitance | Ciss | | 22 | _ | рF | V 0514 14 014 |
| Output Capacitance | Coss | - | 4.1 | _ | рF | $V_{DS} = 25V, V_{GS} = 0V$ f = 1.0MHz |
| Reverse Transfer Capacitance | Crss | l | 2.5 | | pF | 1 - 1.01VII 12 |
| Gate Resistance | R_g | 1 | 120 | _ | Ω | $f = 1.0MHz$, $V_{GS} = 0V$, $V_{DS} = 0V$ |
| Total Gate Charge (V _{GS} = 4.5V) | Q_{g} | l | 361 | _ | рС | |
| Total Gate Charge (V _{GS} = 10V) | Qg | - | 821 | _ | рС | $V_{GS} = 4.5V, V_{DS} = 10V,$ |
| Gate-Source Charge | Q_{gs} | 1 | 162 | _ | рС | $I_D = 250 \text{mA}$ |
| Gate-Drain Charge | Q_{gd} | - | 116 | _ | рС | |
| Turn-On Delay Time | t _{D(ON)} | | 2.8 | _ | ns | |
| Turn-On Rise Time | t _R | | 3.0 | _ | ns | $V_{DD} = 30V, I_D = 0.2A,$ |
| Turn-Off Delay Time | t _{D(OFF)} | | 7.6 | _ | ns | $R_L = 150\Omega$, $V_{GS} = 10V$, $R_G = 25\Omega$ |
| Turn-Off Fall Time | t _F | _ | 5.6 | _ | ns | |

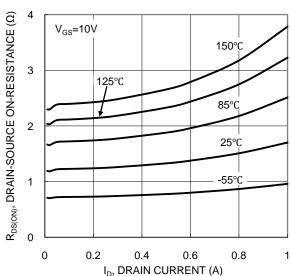
Notes:

- 5. Device mounted on FR-4 PCB, with minimum recommended pad layout.
- 6. Device mounted on 1" x 1" FR-4 PCB with high coverage 2oz. Copper, single sided.
- 7. Short duration pulse test used to minimize self-heating effect.
- 8. Guaranteed by design. Not subject to product testing.



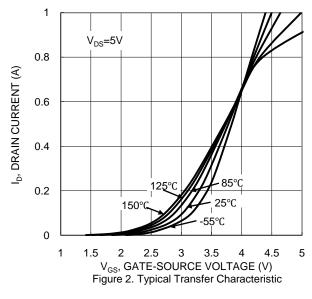


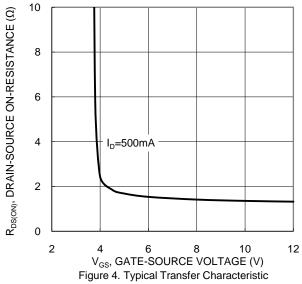




Gate Voltage

Figure 5. Typical On-Resistance vs. Drain Current and Junction Temperature





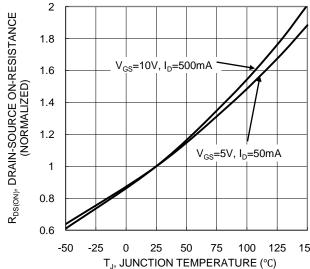


Figure 6. On-Resistance Variation with Junction Temperature



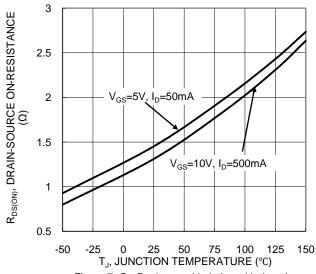
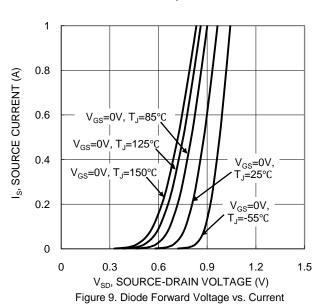
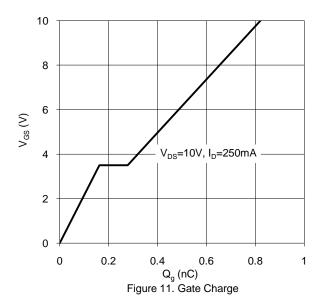


Figure 7. On-Resistance Variation with Junction Temperature





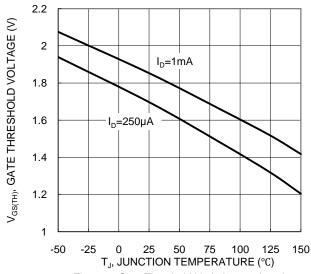
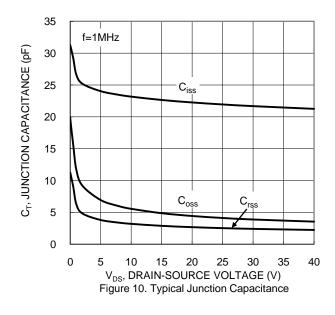


Figure 8. Gate Threshold Variation vs. Junction Temperature



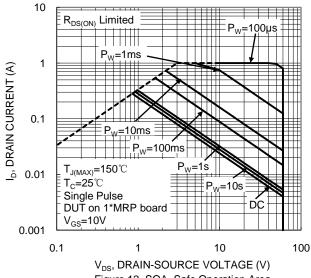
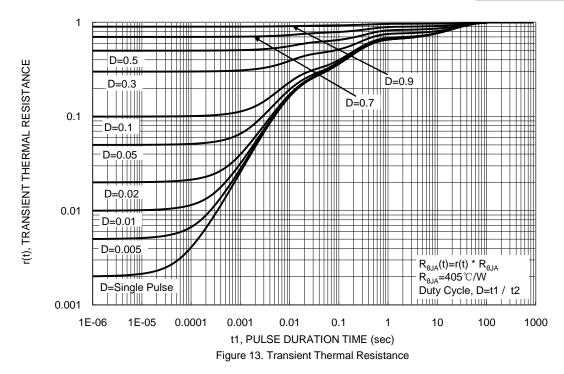


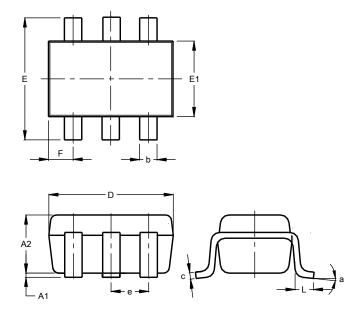
Figure 12. SOA, Safe Operation Area





Package Outline Dimensions

Please see AP02002 at http://www.diodes.com/datasheets/ap02002.pdf for the latest version.

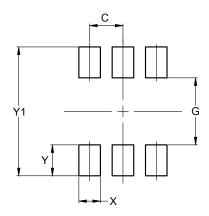


| SOT363 | | | | | | | | |
|--------|----------------------|-----------|-------|--|--|--|--|--|
| Dim | Min | Max | Тур | | | | | |
| A1 | 0.00 | 0.10 | 0.05 | | | | | |
| A2 | 0.90 | 1.00 | 1.00 | | | | | |
| b | 0.10 | 0.30 | 0.25 | | | | | |
| С | 0.10 | 0.22 | 0.11 | | | | | |
| D | 1.80 | 2.20 | 2.15 | | | | | |
| E | 2.00 | 2.20 | 2.10 | | | | | |
| E1 | 1.15 | 1.35 | 1.30 | | | | | |
| е | (| 0.650 BSC | | | | | | |
| F | 0.40 | 0.45 | 0.425 | | | | | |
| L | 0.25 | 0.40 | 0.30 | | | | | |
| а | a 8° | | | | | | | |
| All | All Dimensions in mm | | | | | | | |



Suggested Pad Layout

Please see AP02001 at http://www.diodes.com/datasheets/ap02001.pdf for the latest version.



| Dimensions | Value (in mm) | | | | |
|------------|------------------|--|--|--|--|
| С | 0.650 | | | | |
| G | 1.300 | | | | |
| Х | 0.420 | | | | |
| Υ | 0.600 | | | | |
| Y1 | 2.500 | | | | |

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