Non-Volatile/Low Power/2-Wire/64 Taps

The X9241A integrates four digitally controlled potentiometers (XDCP) on a monolithic CMOS integrated microcircuit.

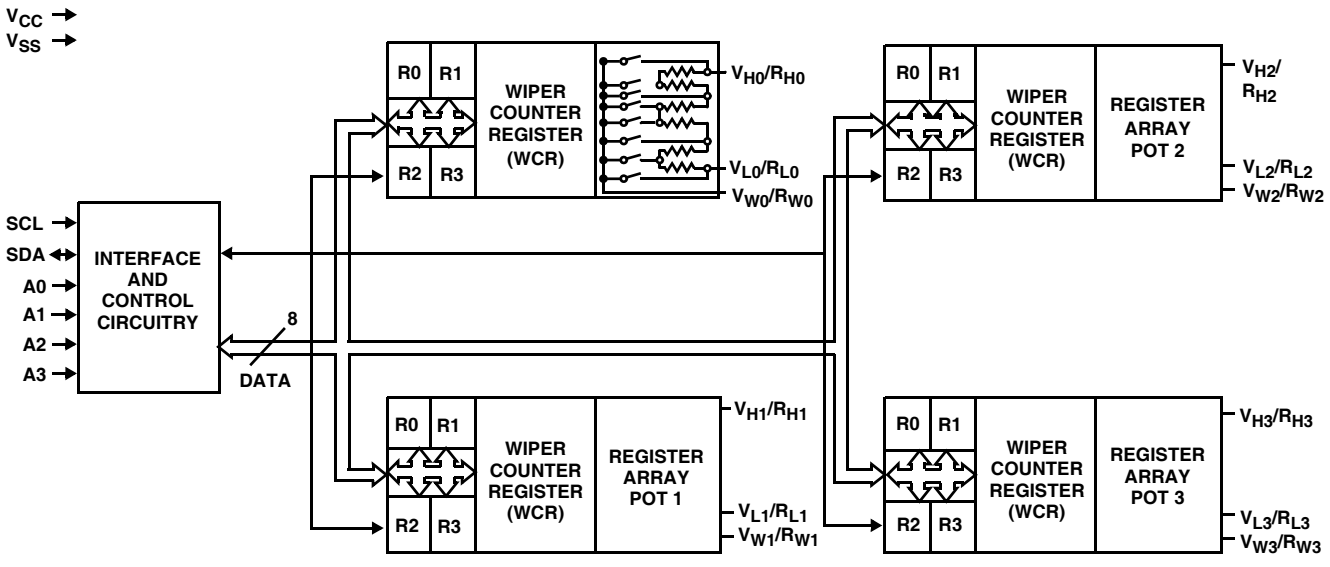
The digitally controlled potentiometer is implemented using 63 resistive elements in a series array. Between each element are tap points connected to the wiper terminal through switches. The position of the wiper on the array is controlled by the user through the 2-wire bus interface. Each potentiometer has associated with it a volatile Wiper Counter Register (WCR) and 4 nonvolatile Data Registers (DR0:DR3) that can be directly written to and read by the user. The contents of the WCR controls the position of the wiper on the resistor array through the switches. Power up recalls the contents of DR0 to the WCR.

The XDCP can be used as a three-terminal potentiometer or as a two-terminal variable resistor in a wide variety of applications including control, parameter adjustments, and signal processing.

Features

- Four potentiometers in one package
- 2-wire serial interface
- Register oriented format
  - Direct read/write/transfer of wiper positions
  - Store as many as four positions per potentiometer
- Terminal Voltages: +5V, -3.0V
- Cascade resistor arrays
- Low power CMOS
- High Reliability
  - Endurance–100,000 data changes per bit per register
  - Register data retention–100 years
- 16-bytes of nonvolatile memory
- 3 resistor array values
  - 2kΩ, 10kΩ, 50kΩ or combination
  - Cascadable for values of 4kΩ to 200kΩ
- Resolution: 64 taps each pot
- 20 Ld plastic DIP, 20 Ld TSSOP and 20 Ld SOIC packages
- Pb-free available (RoHS compliant)

Block Diagram



CAUTION: These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.
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Ordering Information

PART NUMBER	PART MARKING	V_{CC} LIMITS (V)	POTENTIOMETER ORGANIZATION (k)	TEMP RANGE (°C)	PACKAGE
X9241AMP	X9241AMP	5 ±10%	2/10/50	0 to +70	20 Ld PDIP
X9241AMPZ (Note)	X9241AMPZ		Pot 0 = 2k	0 to +70	20 Ld PDIP*** (Pb-free)
X9241AMPI	X9241AMPI		Pot 1 = 10k	-40 to +85	20 Ld PDIP
X9241AMPIZ (Note)	X9241AMPIZ		Pot 2 = 10k	-40 to +85	20 Ld PDIP*** (Pb-free)
X9241AMS*	X9241AMS		Pot 3 = 50k	0 to +70	20 Ld SOIC
X9241AMSZ* (Note)	X9241AMS Z			0 to +70	20 Ld SOIC (Pb-free)
X9241AMSI*, **	X9241AMSI			-40 to +85	20 Ld SOIC
X9241AMSIZ* (Note)	X9241AMSI Z			-40 to +85	20 Ld SOIC (Pb-free)
X9241AMV	X9241AM V			0 to +70	20 Ld TSSOP
X9241AMVZ (Note)	X9241AM VZ			0 to +70	20 Ld TSSOP (Pb-free)
X9241AMVI*, **	X9241AM VI			-40 to +85	20 Ld TSSOP
X9241AMVIZ* (Note)	X9241AM VIZ			-40 to +85	20 Ld TSSOP (Pb-free)
X9241AWP	X9241AWP		10	0 to +70	20 Ld PDIP
X9241AWPI	X9241AWPI		Pot 0 = 10k	-40 to +85	20 Ld PDIP
X9241AWPIZ (Note)	X9241AWPIZ		Pot 1 = 10k	-40 to +85	20 Ld PDIP*** (Pb-free)
X9241AWS*, **	X9241AWS		Pot 2 = 10k	0 to +70	20 Ld SOIC
X9241AWSZ* (Note)	X9241AWS Z		Pot 3 = 10k	0 to +70	20 Ld SOIC (Pb-free)
X9241AWSI*, **	X9241AWSI			-40 to +85	20 Ld SOIC
X9241AWSIZ* (Note)	X9241AWSI Z			-40 to +85	20 Ld SOIC (Pb-free)
X9241AWV*, **	X9241AW V			0 to +70	20 Ld TSSOP
X9241AWVZ* (Note)	X9241AW VZ			0 to +70	20 Ld TSSOP (Pb-free)
X9241AWVI*, **	X9241AW VI			-40 to +85	20 Ld TSSOP
X9241AWVIZ* (Note)	X9241AW VIZ			-40 to +85	20 Ld TSSOP (Pb-free)
X9241AYP	X9241AYP		2	0 to +70	20 Ld PDIP
X9241AYPZ (Note)	X9241AYPZ		Pot 0 = 2k	0 to +70	20 Ld PDIP*** (Pb-free)
X9241AYS*	X9241AYS		Pot 1 = 2k	0 to +70	20 Ld SOIC
X9241AYSZ* (Note)	X9241AYS Z		Pot 2 = 2k	0 to +70	20 Ld SOIC (Pb-free)
X9241AYSI*	X9241AYSI		Pot 3 = 2k	-40 to +85	20 Ld SOIC
X9241AYSIZ* (Note)	X9241AYSI Z			-40 to +85	20 Ld SOIC (Pb-free)
X9241AYV	X9241AY V			0 to +70	20 Ld TSSOP
X9241AYVZ (Note)	X9241AY VZ			0 to +70	20 Ld TSSOP (Pb-free)
X9241AYVI*, **	X9241AY VI			-40 to +85	20 Ld TSSOP
X9241AYVIZ* (Note)	X9241AY VIZ			-40 to +85	20 Ld TSSOP (Pb-free)

Ordering Information (Continued)

PART NUMBER	PART MARKING	V_{CC} LIMITS (V)	POTENTIOMETER ORGANIZATION (k)	TEMP RANGE (°C)	PACKAGE
X9241AUP	X9241AUP	5 ±10%	50	0 to +70	20 Ld PDIP
X9241AUPZ (Note)	X9241AUPZ		Pot 0 = 50k	0 to +70	20 Ld PDIP*** (Pb-free)
X9241AUPI	X9241AUPI		Pot 1 = 50k	-40 to +85	20 Ld PDIP
X9241AUPIZ (Note)	X9241AUPIZ		Pot 2 = 50k	-40 to +85	20 Ld PDIP*** (Pb-free)
X9241AUS	X9241AUS		Pot 3 = 50k	0 to +70	20 Ld SOIC
X9241AUSZ* (Note)	X9241AUS Z			0 to +70	20 Ld SOIC (Pb-free)
X9241AUSI*, **	X9241AUSI			-40 to +85	20 Ld SOIC
X9241AUSIZ* (Note)	X9241AUSI Z			-40 to +85	20 Ld SOIC (Pb-free)
X9241AUV*	X9241AU V			0 to +70	20 Ld TSSOP
X9241AUVZ* (Note)	X9241AU VZ			0 to +70	20 Ld TSSOP (Pb-free)
X9241AUVI*, **	X9241AU VI			-40 to +85	20 Ld TSSOP
X9241AUVIZ* (Note)	X9241AU VIZ			-40 to +85	20 Ld TSSOP (Pb-free)

*Add "T1" suffix for tape and reel.

**Add “T2” suffix for tape and reel.

***Pb-free PDIPs can be used for through hole wave solder processing only. They are not intended for use in Reflow solder processing applications.

NOTE: These Intersil Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate PLUS ANNEAL - e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Pin Descriptions

Host Interface Pins

Serial Clock (SCL)

The SCL input is used to clock data into and out of the X9241A.

Serial Data (SDA)

SDA is a bidirectional pin used to transfer data into and out of the device. It is an open drain output and may be wire-ORed with any number of open drain or open collector outputs. An open drain output requires the use of a pull-up resistor. For selecting typical values, refer to the guidelines for calculating typical values on the bus pull-up resistors graph.

Address

The Address inputs are used to set the least significant 4-bits of the 8-bit slave address. A match in the slave address serial data stream must be made with the Address input in order to initiate communication with the X9241A.

Potentiometer Pins

V_H/R_H(V_{H0}/R_{H0} TO V_{H3}/R_{H3}), V_L/R_L (V_{L0}/R_{L0} TO V_{L3}/R_{L3})

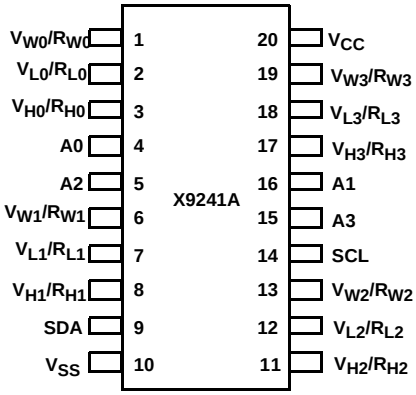
The R_H and R_L inputs are equivalent to the terminal connections on either end of a mechanical potentiometer.

V_W/R_W (V_{W0}/R_{W0} TO V_{W3}/R_{W3})

The wiper outputs are equivalent to the wiper output of a mechanical potentiometer.

Pinout

X9241A
(20 LD DIP, SOIC, TSSOP)
TOP VIEW



Pin Names

SYMBOL	DESCRIPTION
SCL	Serial Clock
SDA	Serial Data
A0 to A3	Address
V_{H0}/R_{H0} to V_{H3}/R_{H3}, V_{L0}/R_{L0} to V_{L3}/R_{L3}	Potentiometer Pins (terminal equivalent)
V_{W0}/R_{W0} to V_{W3}/R_{W3}	Potentiometer Pins (wiper equivalent)

Principles of Operation

The X9241A is a highly integrated microcircuit incorporating four resistor arrays, their associated registers and counters and the serial interface logic providing direct communication between the host and the XDCP potentiometers.

Serial Interface

The X9241A supports a bidirectional bus oriented protocol. The protocol defines any device that sends data onto the bus as a transmitter and the receiving device as the receiver. The device controlling the transfer is a master and the device being controlled is the slave. The master will always initiate data transfers and provide the clock for both transmit and receive operations. Therefore, the X9241A will be considered a slave device in all applications.

Clock and Data Conventions

Data states on the SDA line can change only during SCL LOW periods (t_{LOW}). SDA state changes during SCL HIGH are reserved for indicating start and stop conditions.

Start Condition

All commands to the X9241A are preceded by the start condition, which is a HIGH to LOW transition of SDA while SCL is HIGH (t_{HIGH}). The X9241A continuously monitors the SDA and SCL lines for the start condition and will not respond to any command until this condition is met.

Stop Condition

All communications must be terminated by a stop condition, which is a LOW to HIGH transition of SDA while SCL is HIGH.

Acknowledge

Acknowledge is a software convention used to provide a positive handshake between the master and slave devices on the bus to indicate the successful receipt of data. The transmitting device, either the master or the slave, will release the SDA bus after transmitting 8-bits. The master generates a ninth clock cycle and during this period the receiver pulls the SDA line LOW to acknowledge that it successfully received the 8-bits of data. See Figure 7.

The X9241A will respond with an acknowledge after recognition of a start condition and its slave address and once again after successful receipt of the command byte. If the command is followed by a data byte the X9241A will respond with a final acknowledge.

Array Description

The X9241A is comprised of four resistor arrays. Each array contains 63 discrete resistive segments that are connected in series. The physical ends of each array are equivalent to the fixed terminals of a mechanical potentiometer (V_H/R_H and V_L/R_L inputs).

At both ends of each array and between each resistor segment is a FET switch connected to the wiper (V_W/R_W) output. Within each individual array only one switch may be turned on at a time. These switches are controlled by the Wiper Counter Register (WCR). The 6 least significant bits of the WCR are decoded to select, and enable, 1 of 64 switches.

The WCR may be written directly, or it can be changed by transferring the contents of one of four associated Data Registers into the WCR. These Data Registers and the WCR can be read and written by the host system.

Device Addressing

Following a start condition the master must output the address of the slave it is accessing. The most significant 4-bits of the slave address are the device type identifier (refer to Figure 1). For the X9241A, this is fixed as 0101[B].

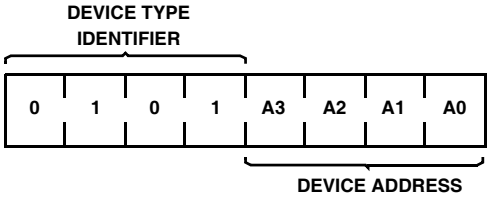


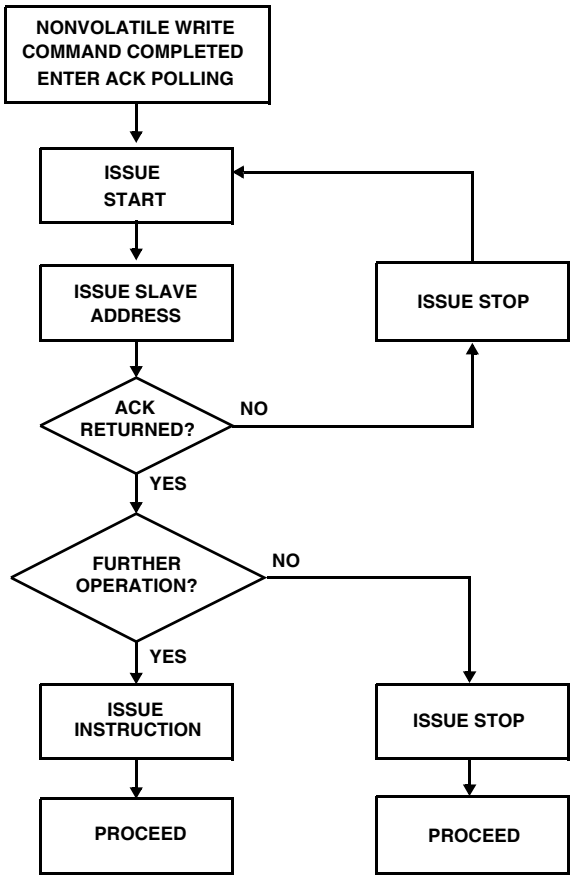
FIGURE 1. SLAVE ADDRESS

The next 4-bits of the slave address are the device address. The physical device address is defined by the state of the A0 to A3 inputs. The X9241A compares the serial data stream with the address input state; a successful compare of all 4 address bits is required for the X9241A to respond with an acknowledge.

Acknowledge Polling

The disabling of the inputs, during the internal nonvolatile write operation, can be used to take advantage of the typical 5ms EEPROM write cycle time. Once the stop condition is issued to indicate the end of the nonvolatile write command, the X9241A initiates the internal write cycle. ACK polling can be initiated immediately. This involves issuing the start condition followed by the device slave address. If the X9241A is still busy with the write operation, no ACK will be returned. If the X9241A has completed the write operation, an ACK will be returned and the master can then proceed with the next operation.

Flow 1. ACK Polling Sequence



Instruction Structure

The next byte sent to the X9241A contains the instruction and register pointer information. The 4 most significant bits are the instruction. The next 4-bits point to one of four pots and when applicable they point to one of four associated registers. The format is in Figure 2.

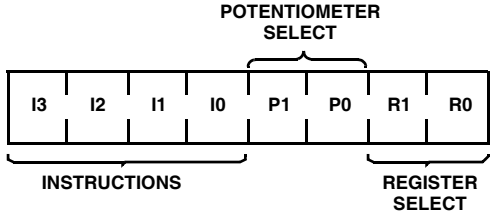


FIGURE 2. INSTRUCTION BYTE FORMAT

The 4 high order bits define the instruction. The next 2-bits (P1 and P0) select which one of the four potentiometers is to be affected by the instruction. The last 2-bits (R1 and R0) select one of the four registers that are to be acted upon when a register oriented instruction is issued.

Four of the nine instructions end with the transmission of the instruction byte. The basic sequence is illustrated in Figure 3. These two-byte instructions exchange data between the WCR and one of the data registers. A transfer from a Data Register to a WCR is essentially a write to a static RAM. The response of the wiper to this action will be delayed t_{STPWV}. A transfer from WCR current wiper position to a Data Register is a write to nonvolatile memory and takes a minimum of t_{WR} to complete. The transfer can occur between one of the four potentiometers and one of its associated registers; or it may occur globally, wherein the transfer occurs between all four of the potentiometers and one of their associated registers.

Four instructions require a three-byte sequence to complete. These instructions transfer data between the host and the X9241A; either between the host and one of the Data Registers or directly between the host and the WCR. These instructions are: Read WCR, read the current wiper position of the selected pot; Write WCR, change current wiper position of the selected pot; Read Data Register, read the contents of the selected nonvolatile register; Write Data Register, write a new value to the selected Data Register. The sequence of operations is shown in Figure 4.

The Increment/Decrement command is different from the other commands. Once the command is issued and the X9241A has responded with an acknowledge, the master can clock the selected wiper up and/or down in one segment steps; thereby, providing a fine tuning capability to the host. For each SCL clock pulse (t_{HIGH}) while SDA is HIGH, the selected wiper will move one resistor segment towards the V_H/R_H terminal. Similarly, for each SCL clock pulse while SDA is LOW, the selected wiper will move one resistor segment towards the V_L/R_L terminal. A detailed illustration of the sequence and timing for this operation is shown in Figures 5 and 6 respectively.

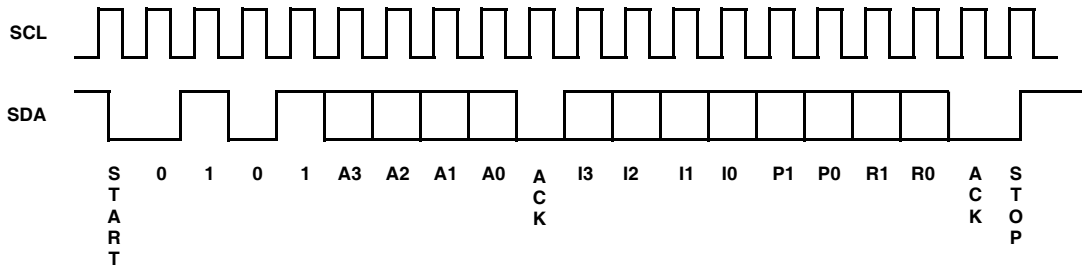


FIGURE 3. TWO-BYTE INSTRUCTION SEQUENCE

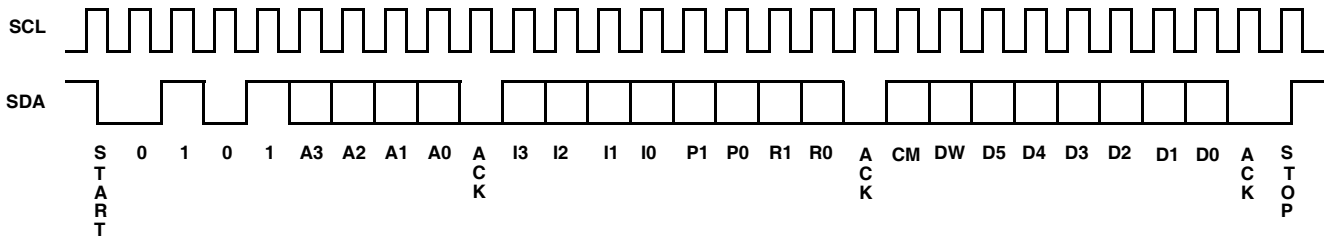


FIGURE 4. THREE-BYTE INSTRUCTION SEQUENCE

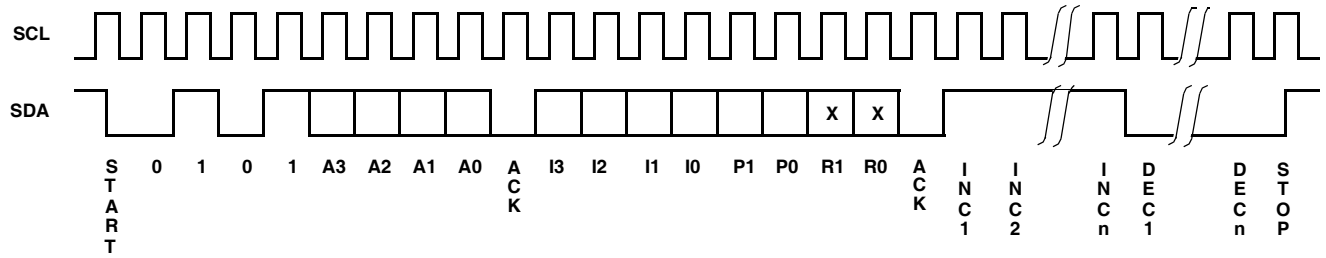


FIGURE 5. INCREMENT/DECREMENT INSTRUCTION SEQUENCE

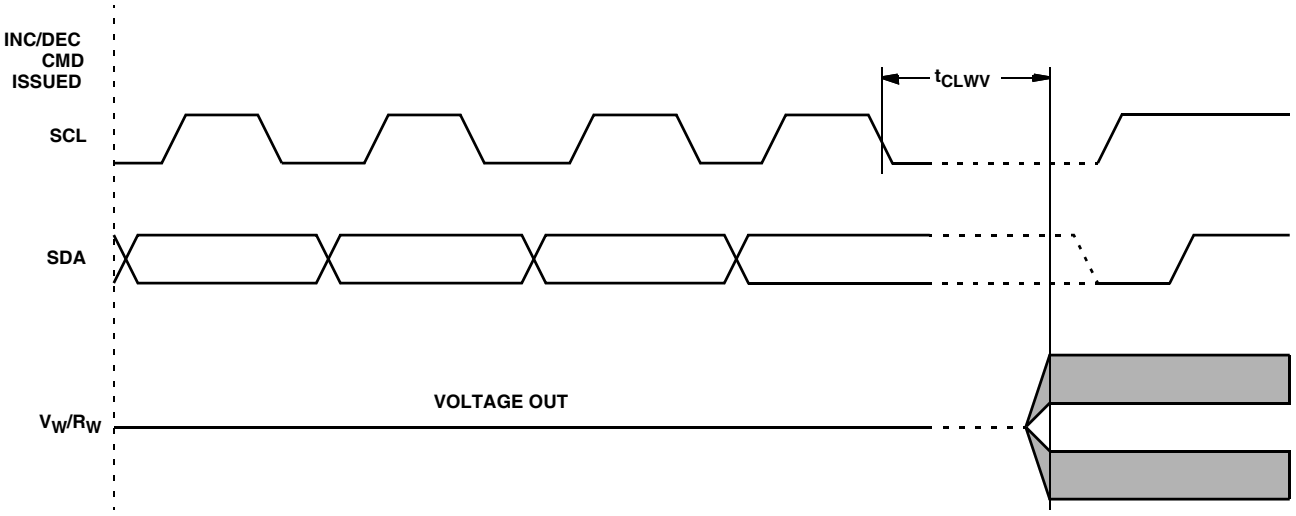


FIGURE 6. INCREMENT/DECREMENT TIMING LIMITS

TABLE 1. INSTRUCTION SET

INSTRUCTION	INSTRUCTION FORMAT								OPERATION
	I_3	I_2	I_1	I_0	P_1	P_0	R_1	R_0	
Read WCR	1	0	0	1	1/0 (Note 1)	1/0	X (Note 2)	X	Read the contents of the Wiper Counter Register pointed to by P_1 to P_0
Write WCR	1	0	1	0	1/0	1/0	X	X	Write new value to the Wiper Counter Register pointed to by P_1 to P_0
Read Data Register	1	0	1	1	1/0	1/0	1/0	1/0	Read the contents of the Register pointed to by P_1 to P_0 and R_1 to R_0
Write Data Register	1	1	0	0	1/0	1/0	1/0	1/0	Write new value to the Register pointed to by P_1 to P_0 and R_1 to R_0

TABLE 1. INSTRUCTION SET (Continued)

INSTRUCTION	INSTRUCTION FORMAT								OPERATION
	I_3	I_2	I_1	I_0	P_1	P_0	R_1	R_0	
XFR Data Register to WCR	1	1	0	1	1/0	1/0	1/0	1/0	Transfer the contents of the Register pointed to by P_1 to P_0 and R_1 to R_0 to its associated WCR
XFR WCR to Data Register	1	1	1	0	1/0	1/0	1/0	1/0	Transfer the contents of the WCR pointed to by P_1 to P_0 to the Register pointed to by R_1 to R_0
Global XFR Data Register to WCR	0	0	0	1	X	X	1/0	1/0	Transfer the contents of the Data Registers pointed to by R_1 to R_0 of all four pots to their respective WCR
Global XFR WCR to Data Register	1	0	0	0	X	X	1/0	1/0	Transfer the contents of all WCRs to their respective data Registers pointed to by R_1 to R_0 of all four pots
Increment/ Decrement Wiper	0	0	1	0	1/0	1/0	X	X	Enable Increment/decrement of the WCR pointed to by P_1 to P_0

NOTES:

1. 1/0 = data is one or zero
2. X = Not applicable or don't care; that is, a data register is not involved in the operation and need not be addressed (typical).

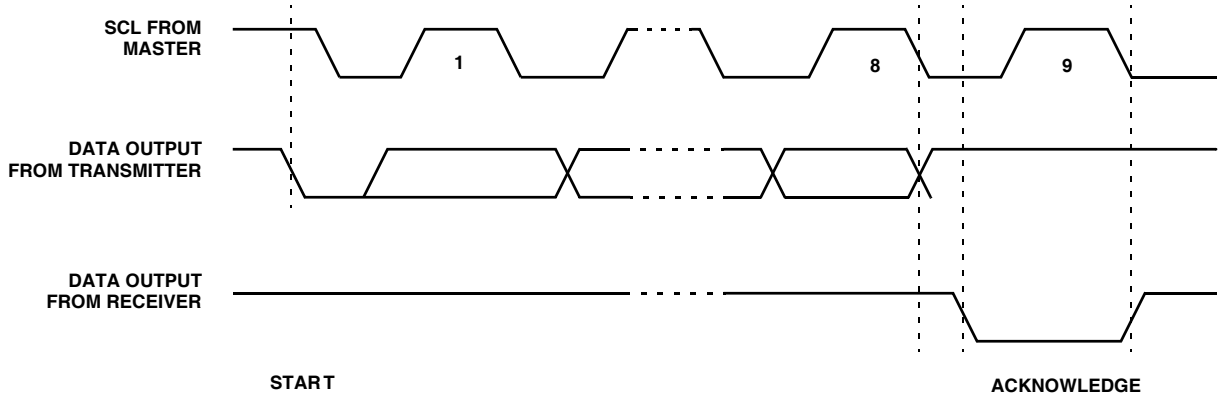


FIGURE 7. ACKNOWLEDGE RESPONSE FROM RECEIVER

Detailed Operation

All four XDCP potentiometers share the serial interface and share a common architecture. Each potentiometer is comprised of a resistor array, a Wiper Counter Register and four Data Registers. A detailed discussion of the register organization and array operation follows.

Wiper Counter Register

The X9241A contains four volatile Wiper Counter Registers (WCR), one for each XDCP potentiometer. The WCR can be envisioned as a 6-bit parallel and serial load counter with its outputs decoded to select one of sixty-four switches along its resistor array. The contents of the WCR can be altered in four ways: it may be written directly by the host via the Write WCR instruction (serial load); it may be written indirectly by transferring the contents of one of four associated Data Registers via the XFR Data Register instruction (parallel load); it can be modified one step at a time by the increment/decrement instruction; finally, it is loaded with the contents of its Data Register zero (DR0) upon power-up.

The WCR is a volatile register; that is, its contents are lost when the X9241A is powered-down. Although the register is automatically loaded with the value in DR0 upon power-up, it should be noted this may be different from the value present at power-down.

Data Registers

Each potentiometer has four nonvolatile Data Registers. These can be read or written directly by the host and data can be transferred between any of the four Data Registers and the WCR. It should be noted all operations changing data in one of these registers is a nonvolatile operation and will take a maximum of 10ms.

If the application does not require storage of multiple settings for the potentiometer, these registers can be used as regular memory locations that could possibly store system parameters or user preference data.

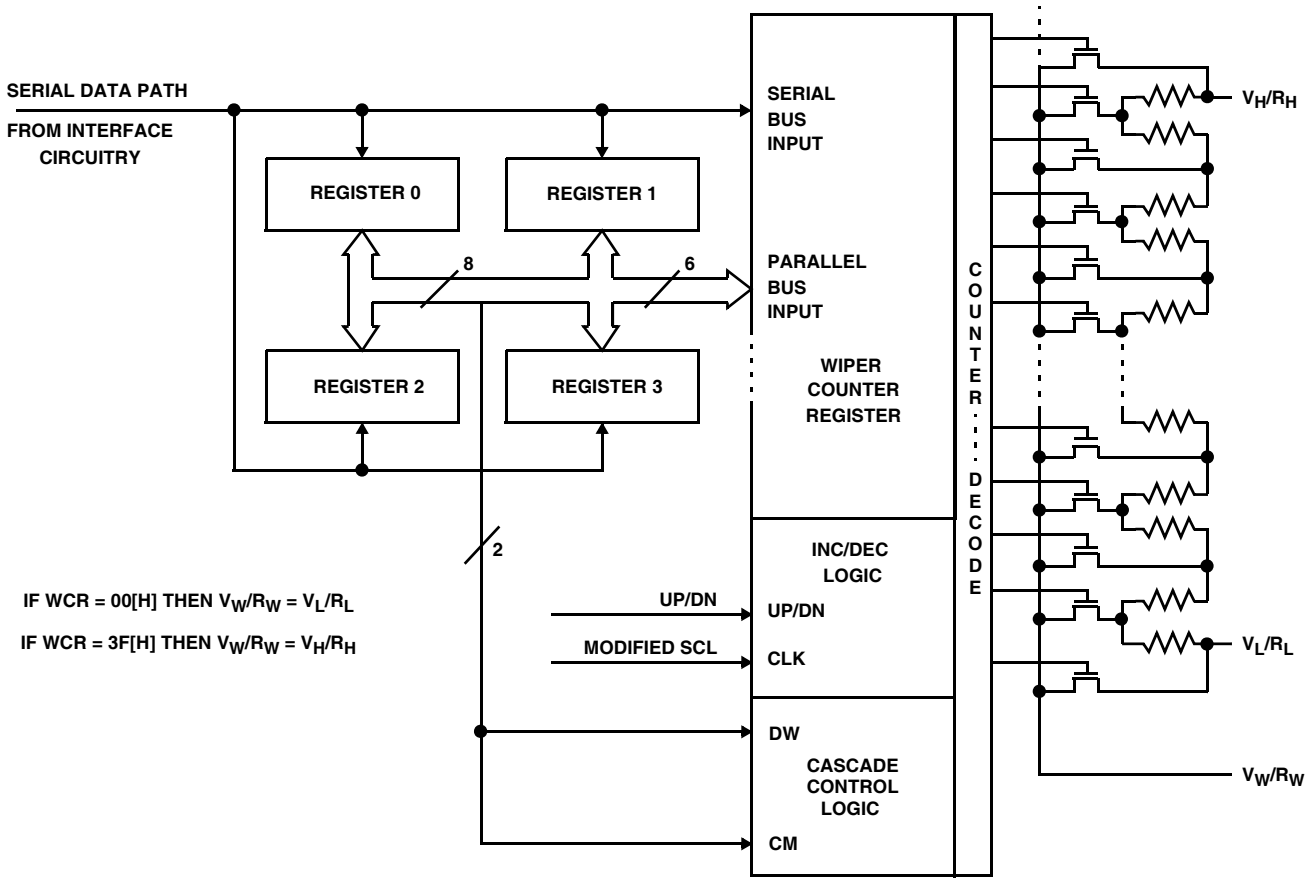


FIGURE 8. DETAILED POTENTIOMETER BLOCK DIAGRAM

Cascade Mode

The X9241A provides a mechanism for cascading the arrays. That is, the sixty-three resistor elements of one array may be cascaded (linked) with the resistor elements of an adjacent array. The V_L/R_L of the higher order array must be connected to the V_H/R_H of the lower order array (See Figure 9).

Cascade Control Bits

The data byte, for the three-byte commands, contains 6-bits (LSBs) for defining the wiper position plus 2 high order bits, CM (Cascade Mode) and DW (Disable Wiper, normal operation).

The state of the CM bit (bit 7 of WCR) enables or disables cascade mode. When the CM bit of the WCR is set to “0” the potentiometer is in the normal operation mode. When the CM bit of the WCR is set to “1” the potentiometer is cascaded with its adjacent higher order potentiometer. For example; if bit 7 of WCR2 is set to “1”, pot 2 will be cascaded to pot 3.

The state of DW enables or disables the wiper. When the DW bit (bit 6 of the WCR) is set to “0” the wiper is enabled; when set to “1” the wiper is disabled. If the wiper is disabled, the wiper terminal will be electrically isolated and float.

When operating in cascade mode V_H/R_H, V_L/R_L and the wiper terminals of the cascaded arrays must be electrically connected externally. All but one of the wipers must be disabled. The user can alter the wiper position by writing directly to the WCR or indirectly by transferring the contents of the Data Registers to the WCR or by using the Increment/Decrement command.

When using the Increment/Decrement command the wiper position will automatically transition between arrays. The current position of the wiper can be determined by reading the WCR registers; if the DW bit is “0”, the wiper in that array is active. If the current wiper position is to be maintained on power-down a global XFR WCR to Data Register command must be issued to store the position in NV memory before power-down.

It is possible to connect three or all four potentiometers in cascade mode. It is also possible to connect POT 3 to POT 0 as a cascade. The requirements for external connections of V_L/R_L, V_H/R_H and the wipers are the same in these cases.

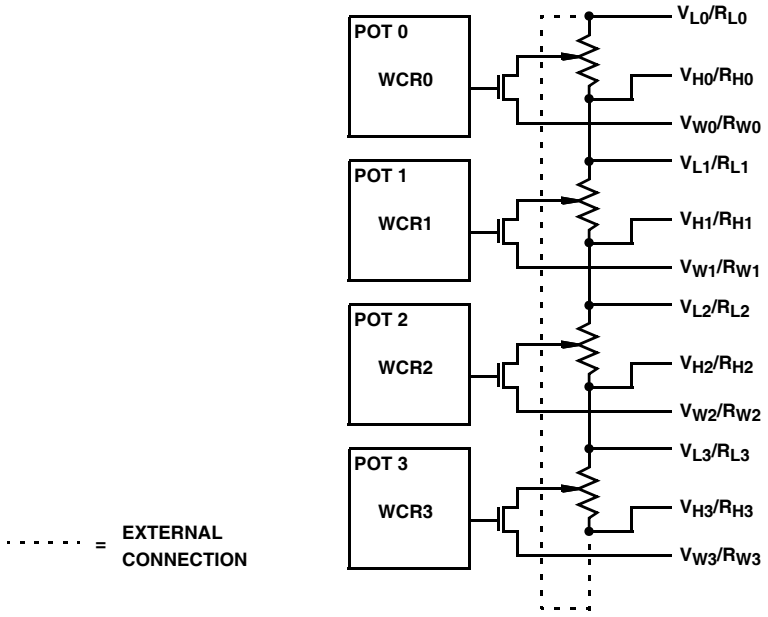


FIGURE 9. CASCADING ARRAYS

Absolute Maximum Ratings

Supply Voltage (V_{CC}) Limits
X9241A. . . . . 5V ±10%
Max Wiper Current for 2k R_{TOTAL} . . . . . ±4mA
Max Wiper Current for 10k and 50k R_{TOTAL} . . . . . ±3mA
Voltage on SCK, SCL or any address input with respect to V_{SS} . . . . . -1V to +7V
Voltage on any V_H/R_H, V_W/R_W or V_L/R_L referenced to V_{SS} . . . . . +6V/-4V
$\Delta V = |V_H/R_H - V_L/R_L|$. 10V
I_W (10s) . . . . . ±6mA
Power rating (each pot) 50mW

Thermal Information

Temperature under bias. . . . . .-65 to +135°C
Storage temperature . . . . . .-65 to +150°C
Pb-free reflow profile . . . . . .see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

Recommended Operating Conditions

Temperature (Commercial) . . . . . 0°C to +70°C
Temperature (Industrial). . . . . .-40°C to +85°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

Analog Specifications (Over recommended operating conditions unless otherwise stated).

SYMBOL	PARAMETER	TEST CONDITION	LIMITS			UNIT
			MIN (Note 11)	TYP	MAX (Note 11)	
R_{TOTAL}	End to end resistance		-20		+20	%
R_W	Wiper resistance	Wiper Current = $(V_H - V_L)/R_{TOTAL}$		40	130	Ω
V_{TERM}	Voltage on any V_H/R_H, V_W/R_W or V_L/R_L Pin		-3.0		+5	V
	Noise	Ref: 1kHz (Note 7)		≤120		dBV
	Resolution	(Note 7)		1.6		%
	Absolute linearity (Note 3)	$R_{w(n)(actual)} - R_{w(n)(expected)}$			±1	MI (Note 5)
	Relative linearity (Note 4)	$R_{w(n+1)} - [R_{w(n)} + MI]$			±0.2	MI (Note 5)
	Temperature coefficient of R_{TOTAL}	(Note 7)		±300		ppm/°C
	Ratiometric temperature coefficient	(Note 7)		±20		ppm/C
$C_H/C_L/C_W$	Potentiometer capacitances	See Circuit #3 and (Note 7)		15/15/25		pF
I_{AL}	R_H, R_I, R_W leakage current	$V_{IN} = V_{TERM}$. Device is in stand-by mode.		0.1	1	µA

DC Electrical Specifications (Over recommended operating conditions unless otherwise stated.)

SYMBOL	PARAMETER	TEST CONDITION	LIMITS			UNIT
			MIN (Note 11)	TYP	MAX (Note 11)	
I_{CC}	Supply current (active)	f_{SCL} = 100kHz, Write/Read to WCR, Other Inputs = V_{SS}			3	mA
I_{SB}	V_{CC} current (standby)	SCL = SDA = V_{CC}, Addr. = V_{SS}		200	500	µA
I_{LI}	Input leakage current	$V_{IN} = V_{SS}$ to V_{CC}			10	µA
I_{LO}	Output leakage current	$V_{OUT} = V_{SS}$ to V_{CC}			10	µA
V_{IH}	Input HIGH voltage		2			V
V_{IL}	Input LOW voltage				0.8	V
V_{OL}	Output LOW voltage	I_{OL} = 3mA			0.4	V

NOTES:

3. Absolute Linearity is utilized to determine actual wiper voltage versus expected voltage as determined by wiper position when used as a potentiometer.
4. Relative Linearity is utilized to determine the actual change in voltage between two successive tap positions when used as a potentiometer. It is a measure of the error in step size.
5. MI = RTOT/63 or $(R_H - R_L)/63$, single pot
6. Max = all four arrays cascaded together, Typical = individual array resolutions.

Endurance and Data Retention

PARAMETER	MIN	UNIT
Minimum endurance	100,000	Data changes per bit per register
Data retention	100	Years

Capacitance

SYMBOL	PARAMETER	TEST CONDITION	TYP	UNIT
$C_{I/O}$ (Note 7)	Input/output capacitance (SDA)	$V_{I/O}$ = 0V	19	pF
C_{IN} (Note 7)	Input capacitance (A0, A1, A2, A3 and SCL)	V_{IN} = 0V	12	pF

Power-up Timing

SYMBOL	PARAMETER	MIN (Note 11)	TYP	MAX (Note 11)	UNIT
t_{PUR} (Note 8)	Power-up to initiation of read operation			1	ms
t_{PUW} (Note 8)	Power-up to initiation of write operation			5	ms
$t_R V_{CC}$	V_{CC} Power up ramp rate	0.2		50	V/ms

Power-up Requirements (Power Up sequencing can affect correct recall of the wiper registers)

The preferred power-on sequence is as follows: First V_{CC}, then the potentiometer pins. It is suggested that Vcc reach 90% of its final value before power is applied to the potentiometer pins. The V_{CC} ramp rate specification should be met, and any glitches or slope changes in the V_{CC} line should be held to <100mV if possible. Also, V_{CC} should not reverse polarity by more than 0.5V.

NOTES:

7. Limits should be considered typical and are not production tested.
8. Limits established by characterization and are not production tested.
9. Maximum Wiper Current is derated over temperature. See the Wiper Current Derating Curve.
10. T_i value denotes the maximum noise glitch pulse width that the device will ignore on either SCL or SDA pins. Any noise glitch pulse width that is greater than this maximum value will be considered as a valid clock or data pulse and may cause communication failure to the device.
11. Parts are 100% tested at either +70°C or +85°C. Over temperature limits established by characterization and are not production tested.

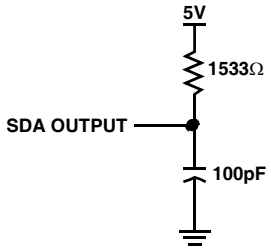
AC Conditions of Test

Input pulse levels	V_{CC} x 0.1 to V_{CC} x 0.9
Input rise and fall times	10ns
Input and output timing levels	V_{CC} x 0.5
Input pulse levels	V_{CC} x 0.1 to V_{CC} x 0.9

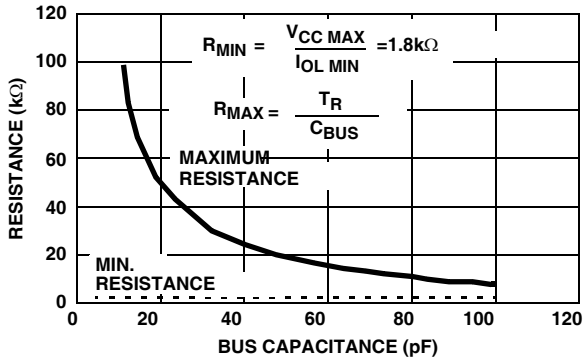
Symbol Table

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from LOW to HIGH	Will change from LOW to HIGH
	May change from HIGH to LOW	Will change from HIGH to LOW
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

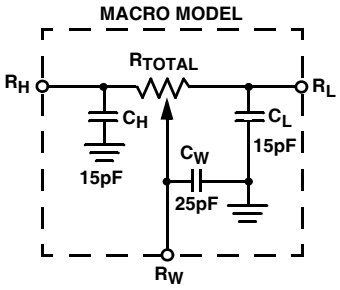
Equivalent AC Test Circuit



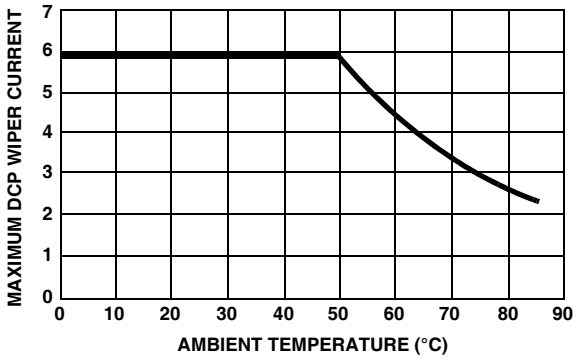
Guidelines for Calculating Typical Values of Bus Pull-Up Resistors



Circuit #3 SPICE Macro Model



DCP Wiper Current De-rating Curve



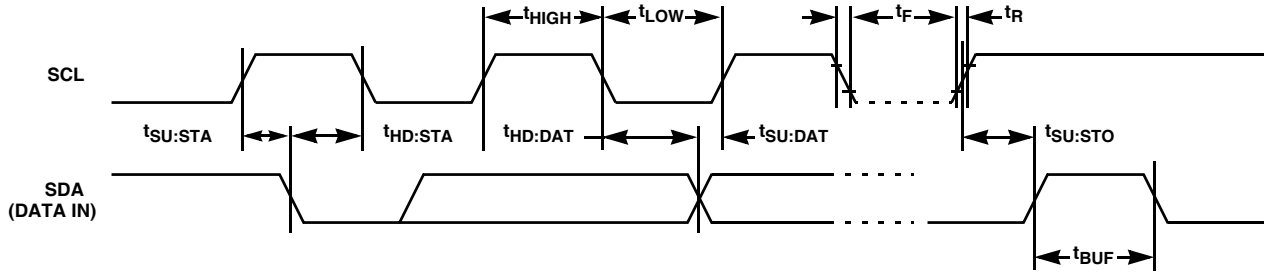


FIGURE 10. INPUT BUS TIMING

AC Electrical Specifications (Over recommended operating conditions unless otherwise stated).

SYMBOL	PARAMETER	LIMITS		UNIT	REFERENCE FIGURE NUMBER(S)
		MIN (Note 11)	MAX (Note 11)		
f_{SCL}	SCL clock frequency	0	100	kHz	10
t_{LOW}	Clock LOW period	4700		ns	10
t_{HIGH}	Clock HIGH period	4000		ns	10
t_R	SCL and SDA rise time		1000	ns	10
t_F	SCL and SDA fall time		300	ns	10
T_i, (Note 11)	Noise suppression time constant (glitch filter)		20	ns	10
$t_{SU:STA}$	Start condition setup time (for a repeated start condition)	4000		ns	10 and 12
$t_{HD:STA}$	Start condition hold time	4000		ns	10 and 12

AC Electrical Specifications (Over recommended operating conditions unless otherwise stated). **(Continued)**

SYMBOL	PARAMETER	LIMITS		UNIT	REFERENCE FIGURE NUMBER(S)
		MIN (Note 11)	MAX (Note 11)		
$t_{SU:DAT}$	Data in setup time	250		ns	10
$t_{HD:DAT}$	Data in hold time	0		ns	10
t_{AA}	SCL LOW to SDA data out valid		3500	ns	11
t_{DH}	Data out hold time	30		ns	11
$t_{SU:STO}$	Stop condition setup time	4000		ns	10 and 12
t_{BUF}	Bus free time prior to new transmission	4700		ns	10
t_{WR}	Write cycle time (nonvolatile write operation)		10	ms	13
t_{STPWV}	Wiper response time from stop generation		500	µs	13
t_{CLWV}	Wiper response from SCL LOW		1000	µs	6

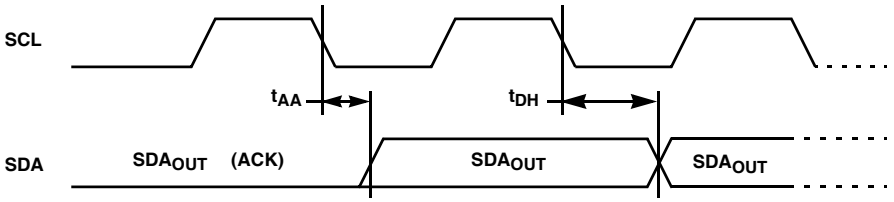


FIGURE 11. OUTPUT BUS TIMING

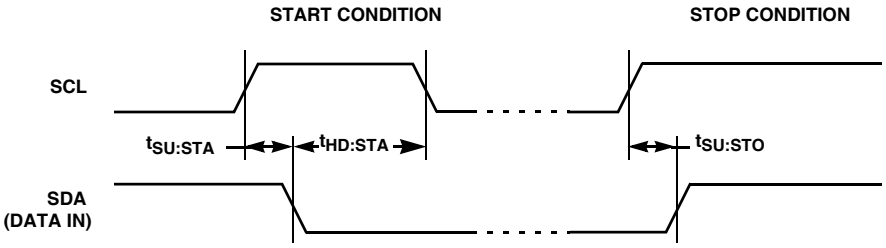


FIGURE 12. START STOP TIMING

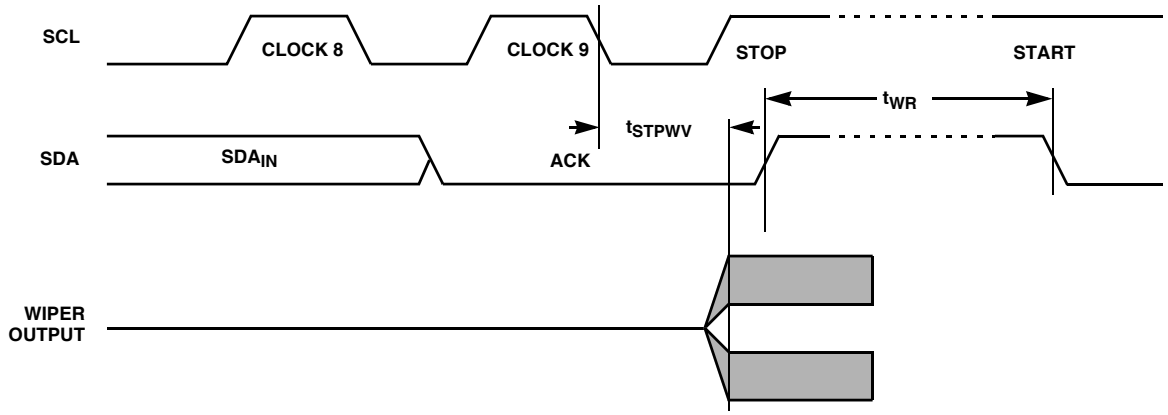
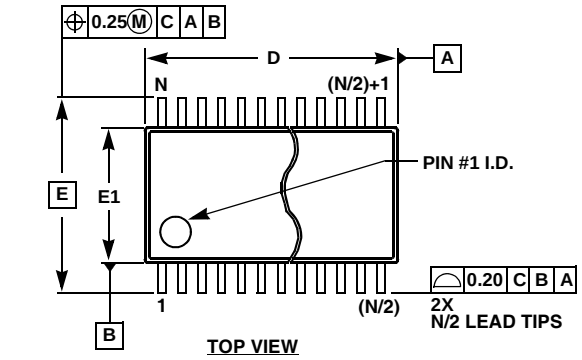
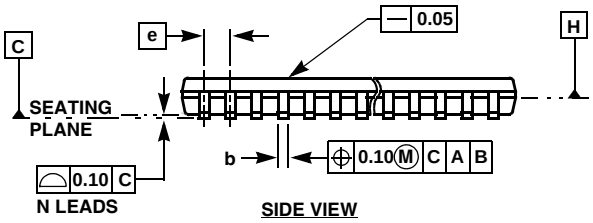
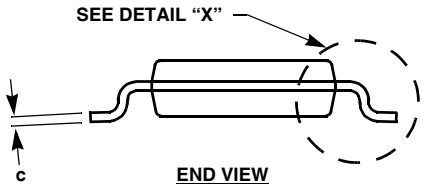


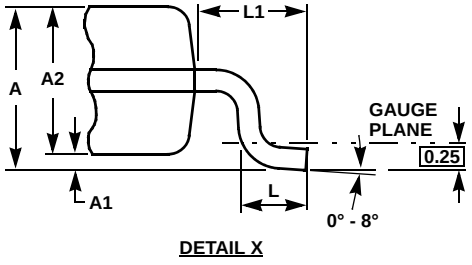
FIGURE 13. WRITE CYCLE AND WIPER RESPONSE TIMING

Thin Shrink Small Outline Package Family (TSSOP)









MDP0044

THIN SHRINK SMALL OUTLINE PACKAGE FAMILY

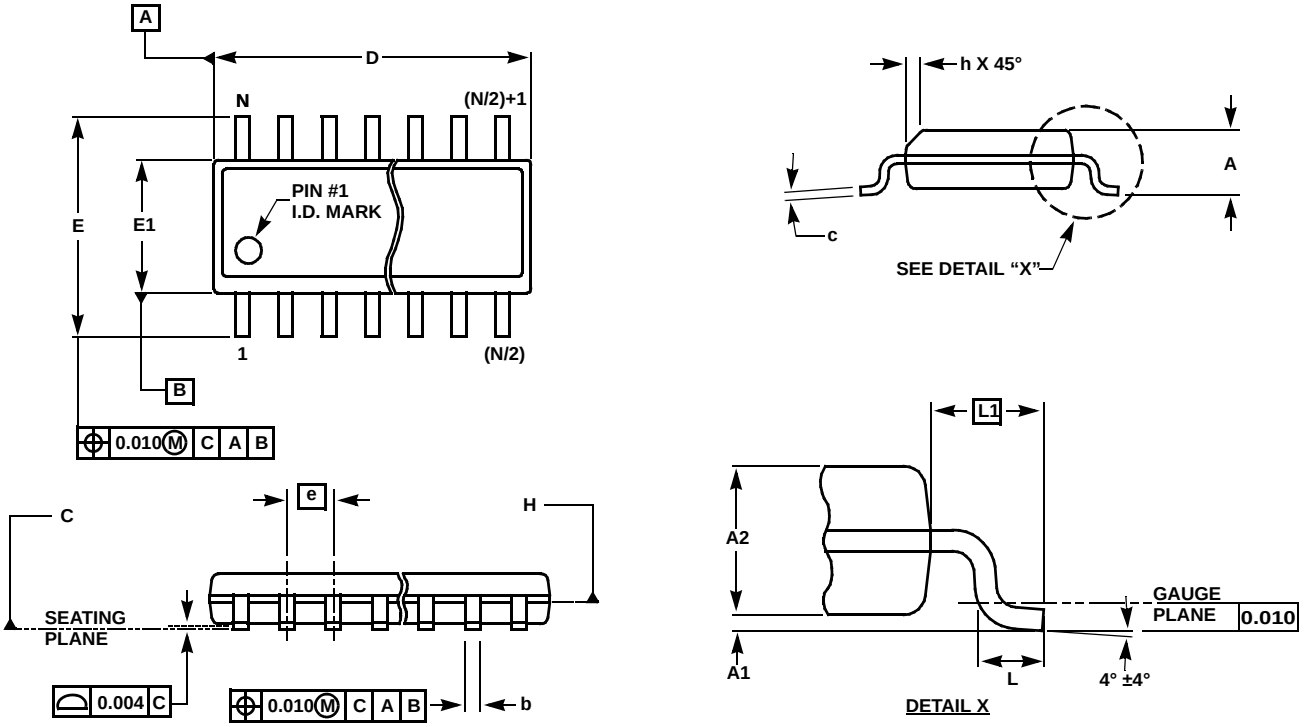
SYMBOL	MILLIMETERS					TOLERANCE
	14 LD	16 LD	20 LD	24 LD	28 LD	
A	1.20	1.20	1.20	1.20	1.20	Max
A1	0.10	0.10	0.10	0.10	0.10	±0.05
A2	0.90	0.90	0.90	0.90	0.90	±0.05
b	0.25	0.25	0.25	0.25	0.25	+0.05/-0.06
c	0.15	0.15	0.15	0.15	0.15	+0.05/-0.06
D	5.00	5.00	6.50	7.80	9.70	±0.10
E	6.40	6.40	6.40	6.40	6.40	Basic
E1	4.40	4.40	4.40	4.40	4.40	±0.10
e	0.65	0.65	0.65	0.65	0.65	Basic
L	0.60	0.60	0.60	0.60	0.60	±0.15
L1	1.00	1.00	1.00	1.00	1.00	Reference

Rev. F 2/07

NOTES:

1. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15mm per side.
2. Dimension “E1” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm per side.
3. Dimensions “D” and “E1” are measured at dAtum Plane H.
4. Dimensioning and tolerancing per ASME Y14.5M-1994.

Small Outline Package Family (SO)



MDP0027

SMALL OUTLINE PACKAGE FAMILY (SO)

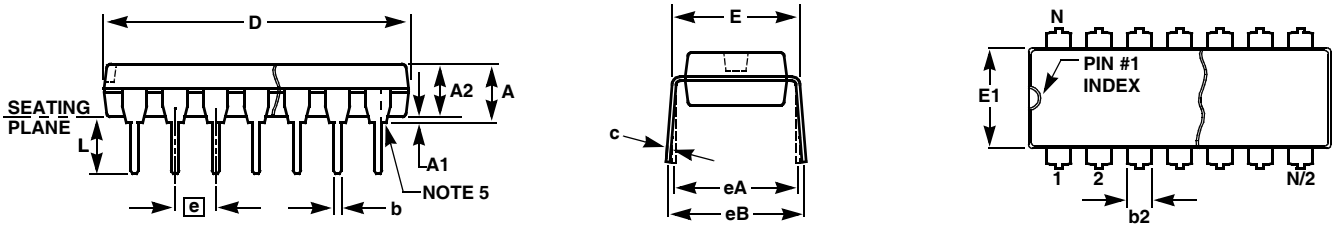
SYMBOL	INCHES							TOLERANCE	NOTES
	SO-8	SO-14	SO16 (0.150")	SO16 (0.300") (SOL-16)	SO20 (SOL-20)	SO24 (SOL-24)	SO28 (SOL-28)		
A	0.068	0.068	0.068	0.104	0.104	0.104	0.104	MAX	-
A1	0.006	0.006	0.006	0.007	0.007	0.007	0.007	±0.003	-
A2	0.057	0.057	0.057	0.092	0.092	0.092	0.092	±0.002	-
b	0.017	0.017	0.017	0.017	0.017	0.017	0.017	±0.003	-
c	0.009	0.009	0.009	0.011	0.011	0.011	0.011	±0.001	-
D	0.193	0.341	0.390	0.406	0.504	0.606	0.704	±0.004	1, 3
E	0.236	0.236	0.236	0.406	0.406	0.406	0.406	±0.008	-
E1	0.154	0.154	0.154	0.295	0.295	0.295	0.295	±0.004	2, 3
e	0.050	0.050	0.050	0.050	0.050	0.050	0.050	Basic	-
L	0.025	0.025	0.025	0.030	0.030	0.030	0.030	±0.009	-
L1	0.041	0.041	0.041	0.056	0.056	0.056	0.056	Basic	-
h	0.013	0.013	0.013	0.020	0.020	0.020	0.020	Reference	-
N	8	14	16	16	20	24	28	Reference	-

Rev. M 2/07

NOTES:

1. Plastic or metal protrusions of 0.006" maximum per side are not included.
2. Plastic interlead protrusions of 0.010" maximum per side are not included.
3. Dimensions "D" and "E1" are measured at Datum Plane "H".
4. Dimensioning and tolerancing per ASME Y14.5M-1994

Plastic Dual-In-Line Packages (PDIP)



MDP0031

PLASTIC DUAL-IN-LINE PACKAGE

SYMBOL	INCHES					TOLERANCE	NOTES
	PDIP8	PDIP14	PDIP16	PDIP18	PDIP20		
A	0.210	0.210	0.210	0.210	0.210	MAX	
A1	0.015	0.015	0.015	0.015	0.015	MIN	
A2	0.130	0.130	0.130	0.130	0.130	±0.005	
b	0.018	0.018	0.018	0.018	0.018	±0.002	
b2	0.060	0.060	0.060	0.060	0.060	+0.010/-0.015	
c	0.010	0.010	0.010	0.010	0.010	+0.004/-0.002	
D	0.375	0.750	0.750	0.890	1.020	±0.010	1
E	0.310	0.310	0.310	0.310	0.310	+0.015/-0.010	
E1	0.250	0.250	0.250	0.250	0.250	±0.005	2
e	0.100	0.100	0.100	0.100	0.100	Basic	
eA	0.300	0.300	0.300	0.300	0.300	Basic	
eB	0.345	0.345	0.345	0.345	0.345	±0.025	
L	0.125	0.125	0.125	0.125	0.125	±0.010	
N	8	14	16	18	20	Reference	

Rev. C 2/07

NOTES:

1. Plastic or metal protrusions of 0.010” maximum per side are not included.
2. Plastic interlead protrusions of 0.010” maximum per side are not included.
3. Dimensions E and eA are measured with the leads constrained perpendicular to the seating plane.
4. Dimension eB is measured with the lead tips unconstrained.
5. 8 and 16 lead packages have half end-leads as shown.

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