TS5N118
1-OF-8 FET MULTIPLEXER/DEMULTIPLEXER HIGH-BANDWIDTH BUS SWITCH

SCDS205–AUGUST 2005

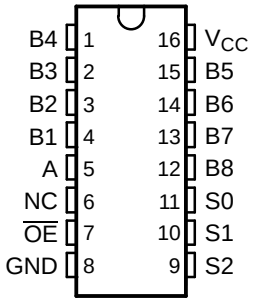
FEATURES

- **Low and Flat ON-State Resistance (r_{on}) Characteristics Over Operating Range (r_{on} = 3 Ω Typ)**
- **0- to 10-V Switching on Data I/O Ports**
- **Bidirectional Data Flow With Near-Zero Propagation Delay**
- **Low Input/Output Capacitance Minimizes Loading and Signal Distortion ($C_{io(OFF)}$ = 20 pF Max, B Port)**
- **V_{CC} Operating Range From 4.75 V to 5.25 V**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Performance Tested Per JESD 22**
  - **2000-V Human-Body Model (A114-B, Class II)**
  - **1000-V Charged-Device Model (C101)**
- **Supports Both Digital and Analog Applications**

APPLICATIONS

- **PCI Interface**
- **Differential Signal Interface**
- **Memory Interleaving**
- **Bus Isolation**
- **Low-Distortion Signal Gating**

DBQ OR PW PACKAGE
(TOP VIEW)



NC − No internal connection

DESCRIPTION/ORDERING INFORMATION

The TS5N118 is a high-bandwidth FET bus switch utilizing a charge pump to elevate the gate voltage of the pass transistor, providing a low and flat ON-state resistance (r_{on}). The low and flat ON-state resistance allows for minimal propagation delay and supports rail-to-rail switching on the data input/output (I/O) ports. The device also features low data I/O capacitance to minimize capacitive loading and signal distortion on the data bus. Specifically designed to support high-bandwidth applications, the TS5N118 provides an optimized interface solution ideally suited for broadband communications, networking, and data-intensive computing systems.

The TS5N118 is a 1-of-8 multiplexer/demultiplexer with a single output-enable ($\overline{OE}$) input. The select (S0, S1, S2) inputs control the data path of the multiplexer/demultiplexer. When $\overline{OE}$ is low, the multiplexer/demultiplexer is enabled and the A port is connected to the B port, allowing bidirectional data flow between ports. When $\overline{OE}$ is high, the multiplexer/demultiplexer is disabled and a high-impedance state exists between the A and B ports.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry prevents damaging current backflow through the device when it is powered down. The device has isolation during power off.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

ORDERING INFORMATION

T_A	PACKAGE(1)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	SSOP (QSOP) – DBQ	Tape and reel	TS5N118DBQR	YB118
	TSSOP – PW	Tape and reel	TS5N118PWR	

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

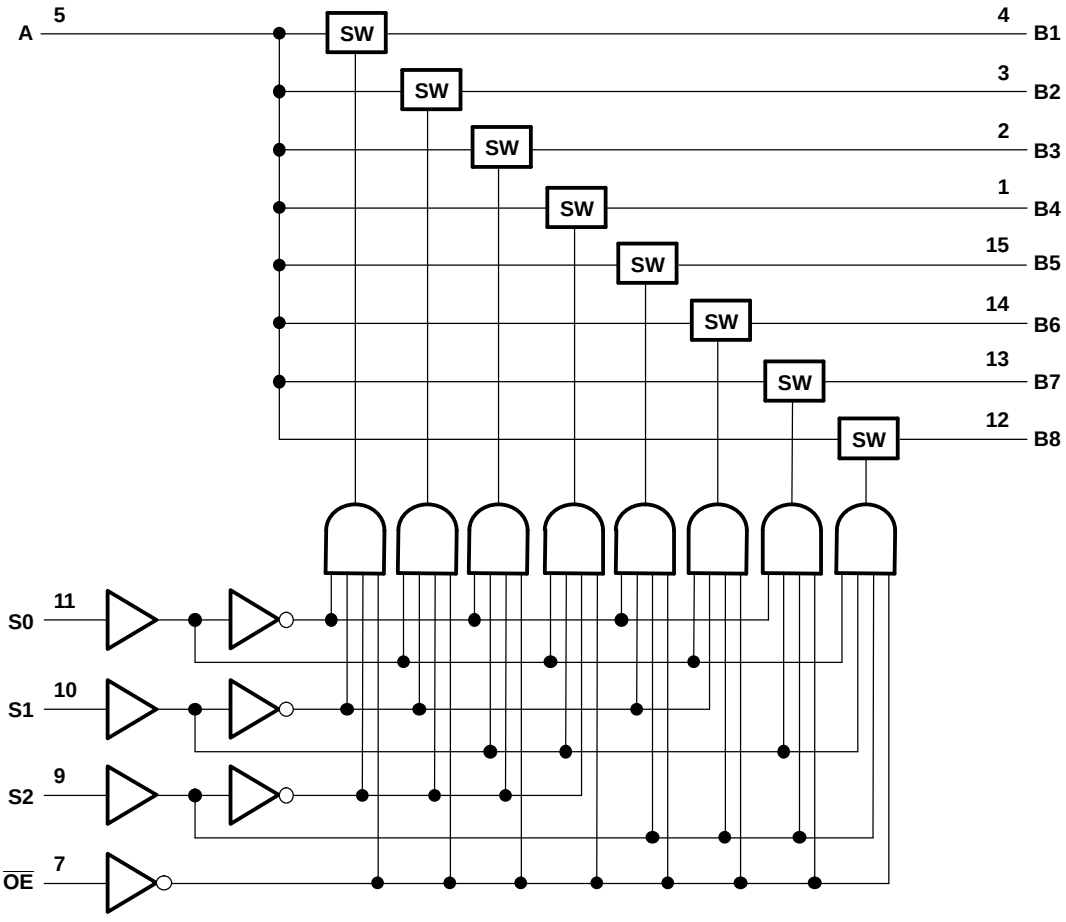
PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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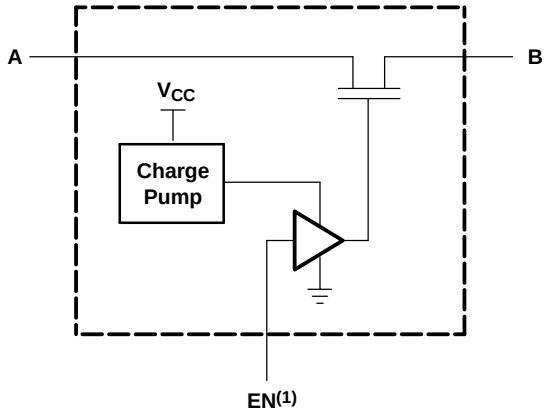
FUNCTION TABLE

INPUTS				INPUT/OUTPUT A	FUNCTION
$\overline{OE}$	S2	S1	S0		
L	L	L	L	B1	A port = B1 port
L	L	L	H	B2	A port = B2 port
L	L	H	L	B3	A port = B3 port
L	L	H	H	B4	A port = B4 port
L	H	L	L	B5	A port = B5 port
L	H	L	H	B6	A port = B6 port
L	H	H	L	B7	A port = B7 port
L	H	H	H	B8	A port = B8 port
H	X	X	X	Z	Disconnect

LOGIC DIAGRAM (POSITIVE LOGIC)



SIMPLIFIED SCHEMATIC, EACH FET SWITCH (SW)



(1) EN is the internal enable signal applied to the switch.

Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		–0.5	7	V
V_{IN}	Control input voltage range(2)(3)		–0.5	7	V
$V_{I/O}$	Switch I/O voltage range(2)(3)(4)		–0.5	11	V
$I_{I/O}$	ON-state switch current(5)			±100	mA
	Continuous current through V_{CC} or GND			±100	mA
θ_{JA}	Package thermal impedance(6)	DBQ package		90	°C/W
		PW package		108	
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to ground, unless otherwise specified.
(3) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(4) V_I and V_O are used to denote specific conditions for $V_{I/O}$.
(5) I_I and I_O are used to denote specific conditions for $I_{I/O}$.
(6) The package thermal impedance is calculated in accordance with JESD 51-7.

Recommended Operating Conditions(1)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4.75	5.25	V
V_{IH}	High-level control input voltage	2	5.25	V
V_{IL}	Low-level control input voltage	0	0.8	V
$V_{I/O}$	Data input/output voltage	0	10	V
T_A	Operating free-air temperature	–40	85	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

Electrical Characteristics(1)

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP(2)	MAX	UNIT
I_{IN}	Control inputs	V_{CC} = 5.25 V,	V_{IN} = 0 to V_{CC}				10	μA
I_{OZ}(3)		V_{CC} = 5.25 V,	V_O = 0 to 10 V, V_I = 0,	Switch OFF, V_{IN} = V_{CC} or GND			10	μA
		V_{CC} = 0 V,	V_O = Open,	V_I = 0 to 10 V			10	
I_{CC}		V_{CC} = 5.25 V,	$I_{I/O}$ = 0, Switch ON or OFF,	V_{IN} = V_{CC} or GND			10	mA
C_{in}	Control inputs	V_{CC} = 5 V,	V_{IN} = 10 V or 0				10	pF
$C_{io(OFF)}$	A port	V_{CC} = 5 V,	Switch OFF, V_{IN} = V_{CC} or GND,	$V_{I/O}$ = 10 V or 0			120	pF
	B port	V_{CC} = 5 V,	Switch OFF, V_{IN} = V_{CC} or GND,	$V_{I/O}$ = 10 V or 0			20	
$C_{io(ON)}$		V_{CC} = 5 V,	Switch ON, V_{IN} = V_{CC} or GND,	$V_{I/O}$ = 10 V or 0			160	pF
r_{on}(4)		V_{CC} = 4.75 V, TYP at V_{CC} = 5 V	V_I = 0,	I_O = 50 mA		3	7.5	Ω
			V_I = 8 V,	I_O = –50 mA			7.5	
			V_I = 10 V,	I_O = –50 mA			12.5	

(1) V_{IN} and I_{IN} refer to control inputs. V_I, V_O, I_I, and I_O refer to data pins
(2) All typical values are at V_{CC} = 5 V (unless otherwise noted), T_A = 25°C.
(3) For I/O ports, the parameter I_{OZ} includes the I/O leakage current.
(4) Measured by the voltage drop between the A and B terminals at the indicated current through the switch. ON-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V ± 0.25 V		UNIT
			MIN	MAX	
t_{pd}(1)	A or B	B or A		0.1	ns
$t_{pd(s)}$	S	A		200	ns
t_{en}	S	B		200	ns
	$\overline{OE}$	A or B		200	
t_{dis}	S	B		200	ns
	OE	A or B		200	

(1) The propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

Dynamic Characteristics

over recommended operating free-air temperature range, V_{CC} = 5 V ± 5% (unless otherwise noted)

PARAMETER	TEST CONDITIONS				MIN	TYP(1)	MAX	UNIT
Bandwidth (BW)(2)	R_L = 50 Ω,	V_I = 0.632 V (P-P),	See Figure 4		25			MHz
OFF isolation (O_{ISO})	R_L = 50 Ω,	V_I = 0.632 V (P-P),	f = 25 MHz,	See Figure 5		–50		dB
Crosstalk (X_{TALK})	R_L = 50 Ω,	V_I = 0.632 V (P-P),	f = 25 MHz,	See Figure 6		–50		dB

(1) All typical values are at V_{CC} = 5 V (unless otherwise noted), T_A = 25°C.
(2) Bandwidth is the frequency at which the gain is –3 dB below the DC gain.

TYPICAL PERFORMANCE

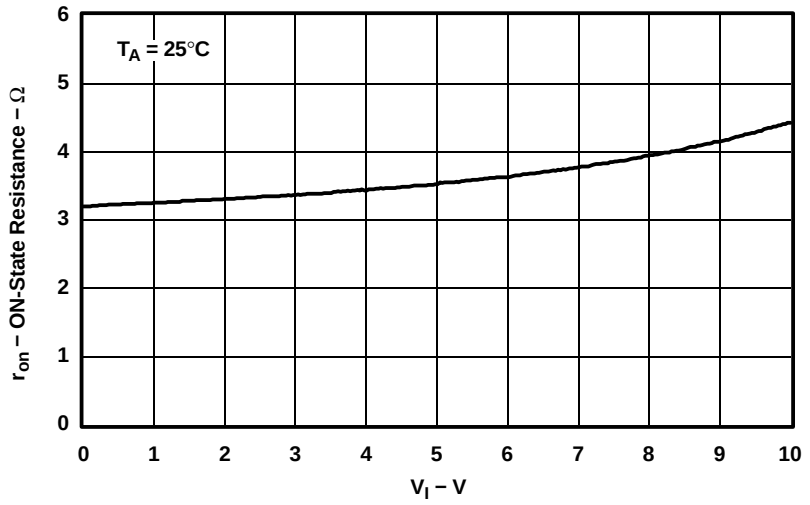


Figure 1. Typical r_{on} vs V_I, V_{CC} = 5 V and I_O = –50 mA

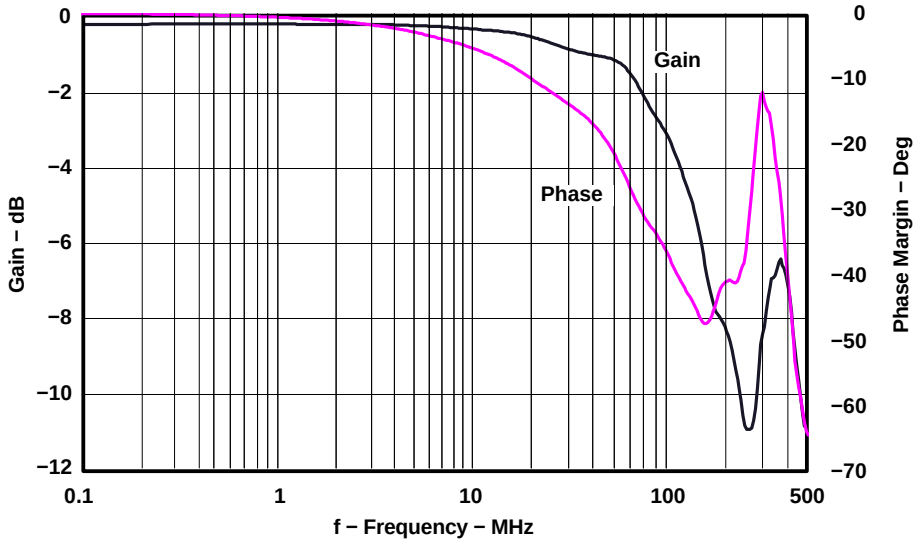


Figure 2. Frequency Response vs Bandwidth

TYPICAL PERFORMANCE

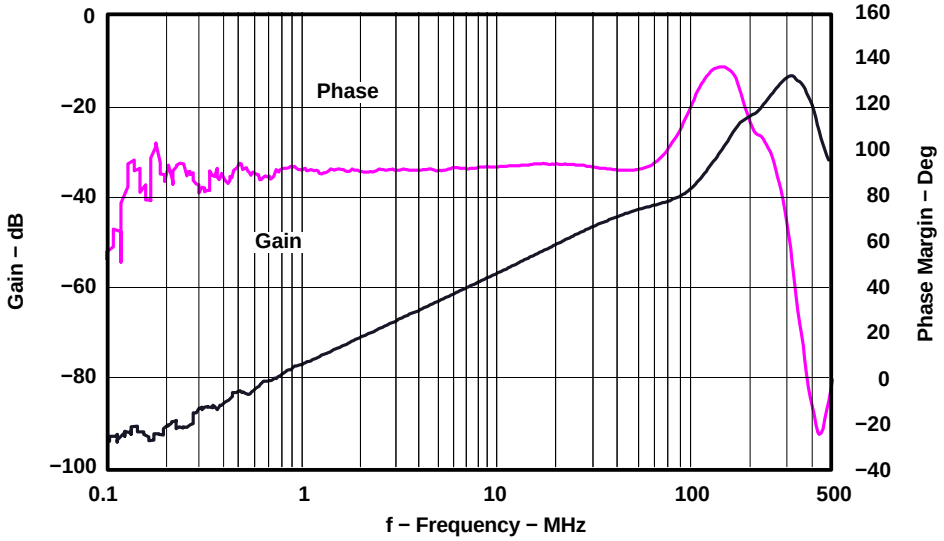


Figure 3. Frequency Response vs OFF Isolation

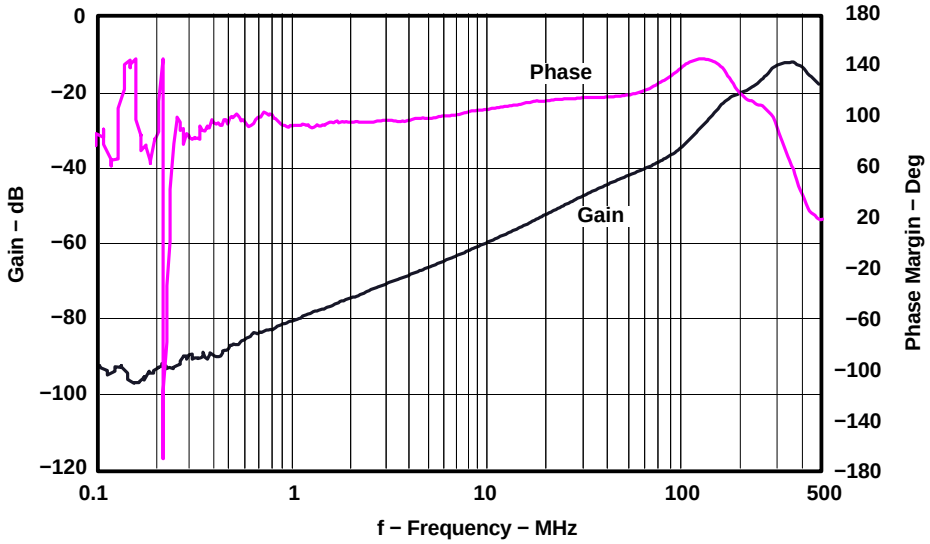
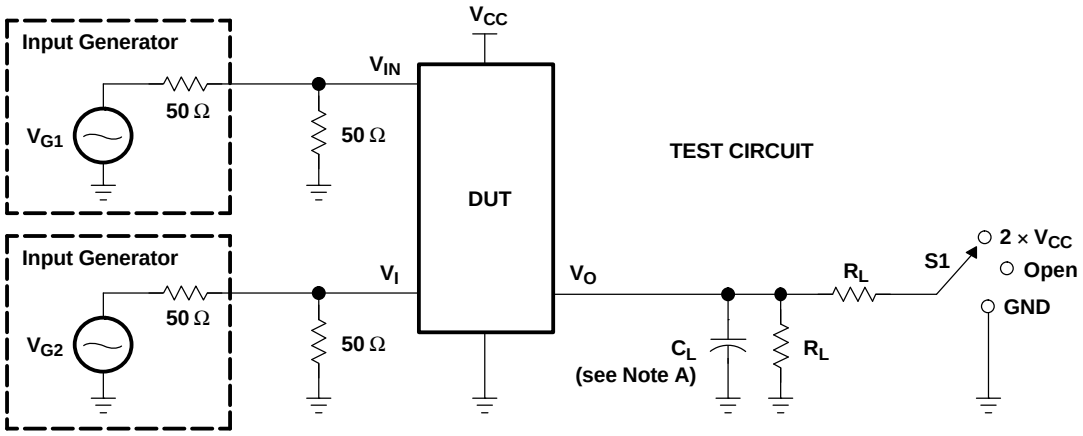


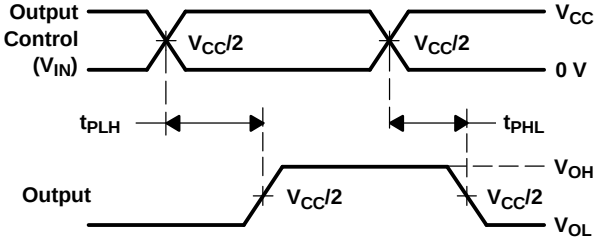
Figure 4. Frequency Response vs Crosstalk

PARAMETER MEASUREMENT INFORMATION

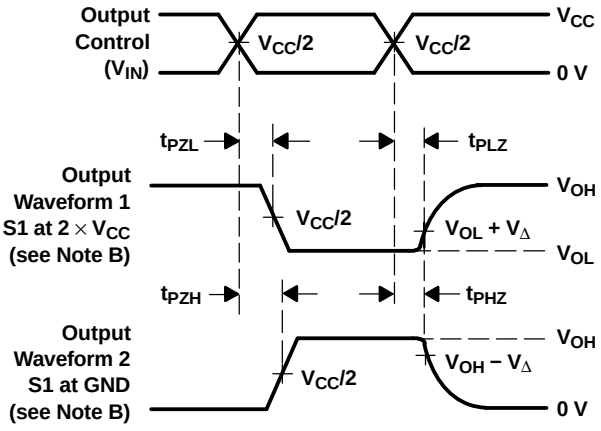


TEST	V_{CC}	S1	R_L	V_I	C_L	V_Δ
$t_{pd(s)}$†	5 V ± 0.25 V	Open	100 Ω	V_{CC}	35 pF	
t_{PLZ}/t_{PZL}	5 V ± 0.25 V	2 × V_{CC}	100 Ω	GND	35 pF	0.3 V
t_{PHZ}/t_{PZH}	5 V ± 0.25 V	GND	100 Ω	V_{CC}	35 pF	0.3 V

† t_{pds} is measured with Demux inputs at opposite voltage levels, i.e. V_{B1} = 5 V, V_{B2} = GND.



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES ($t_{pd(s)}$)



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r < 25 ns, t_f < 25 ns.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as $t_{pd(s)}$. The tpd propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).
H. All parameters and waveforms are not applicable to all devices.

Figure 5. Test Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION

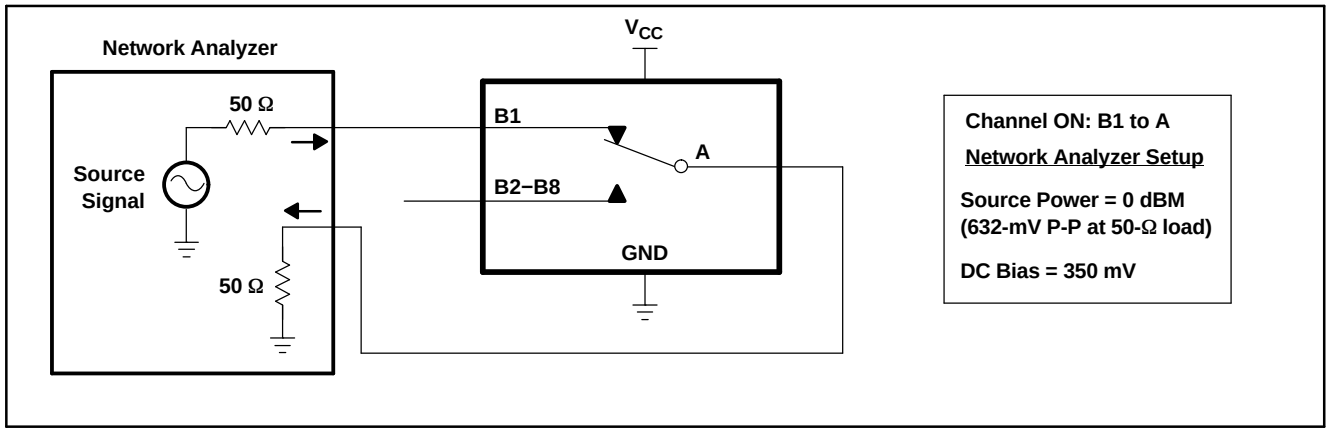


Figure 6. Bandwidth (BW)

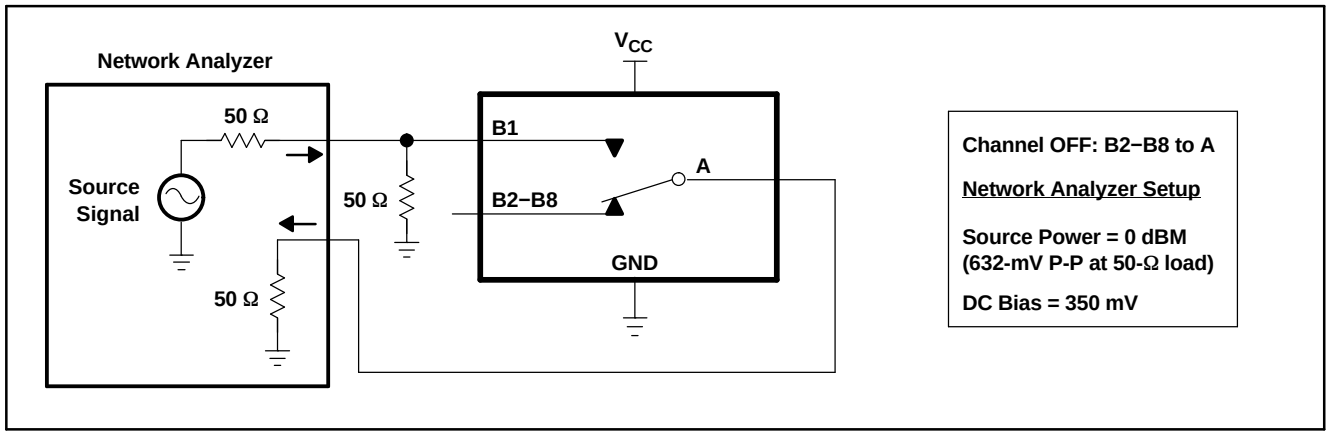


Figure 7. OFF Isolation (O_{ISO})

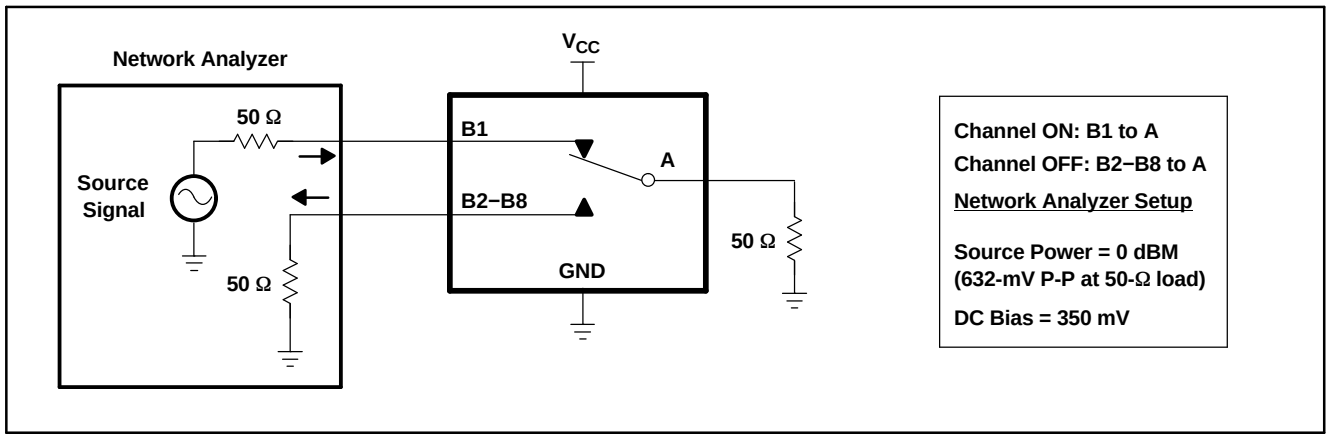
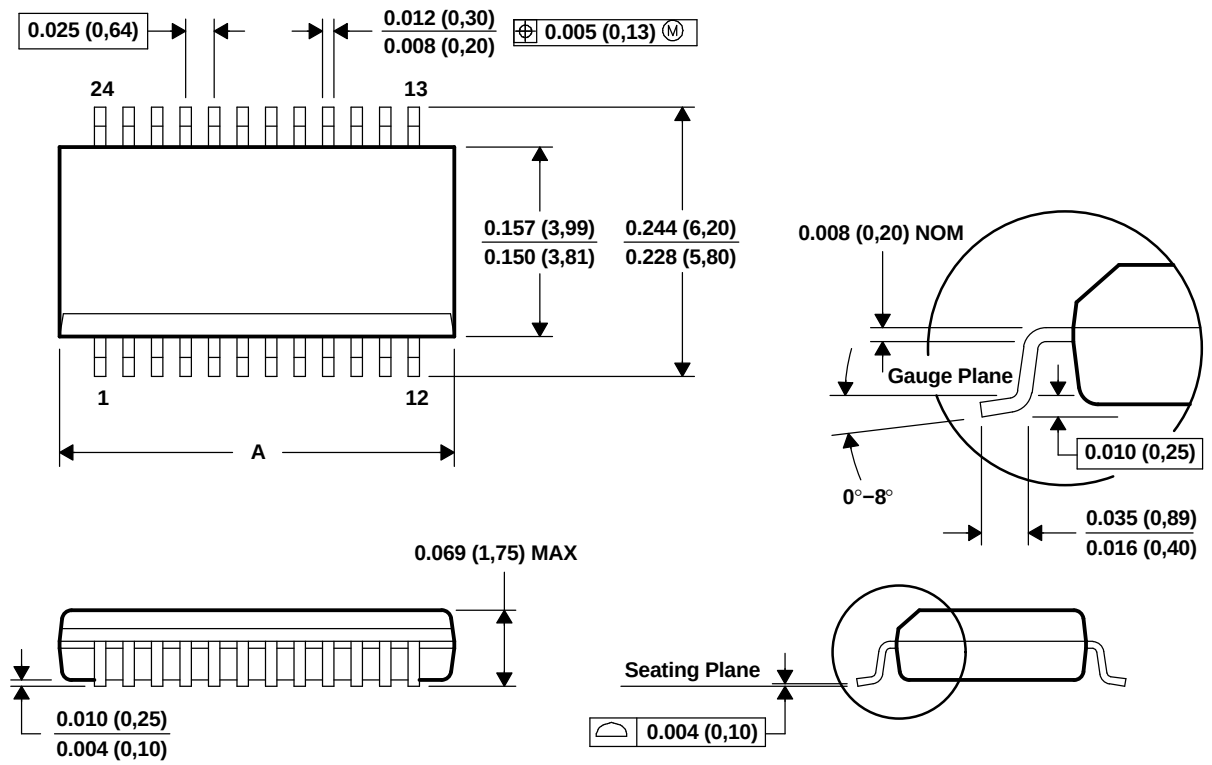


Figure 8. Crosstalk (X_{TALK})

MECHNICAL DATA

DBQ (R-PDSO-G**)



DIM \ PINS **	16	20	24	28
A MAX	0.197 (5,00)	0.344 (8,74)	0.344 (8,74)	0.394 (10,01)
A MIN	0.189 (4,80)	0.337 (8,56)	0.337 (8,56)	0.386 (9,80)
D M0−137 VARIATION	AB	AD	AE	AF

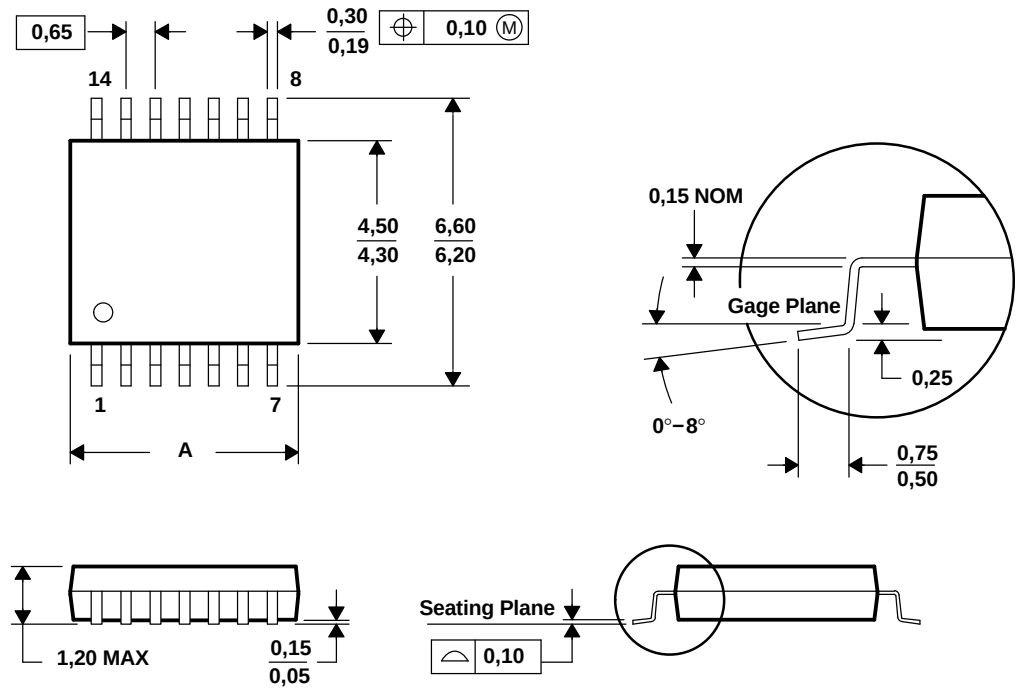
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NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MO−137.

MECHNICAL DATA

PW (R-PDSO-G**)

14 PINS SHOWN



DIM \ PINS **	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/F 01/97

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
TS5N118DBQR	ACTIVE	SSOP	DBQ	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
TS5N118DBQRE4	ACTIVE	SSOP	DBQ	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
TS5N118DBQRG4	ACTIVE	SSOP	DBQ	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
TS5N118PW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TS5N118PWE4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TS5N118PWG4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TS5N118PWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TS5N118PWRE4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TS5N118PWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

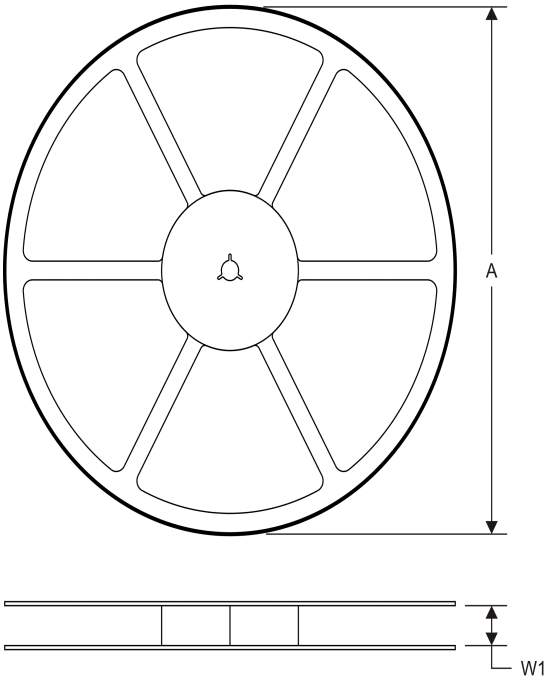
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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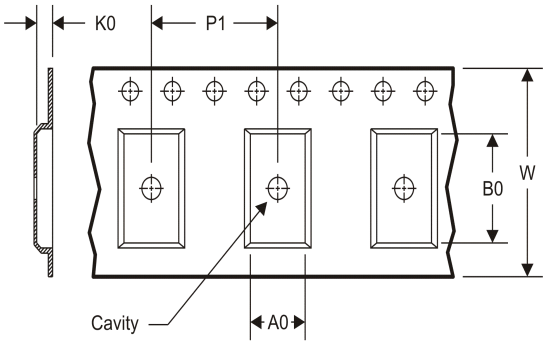
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TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



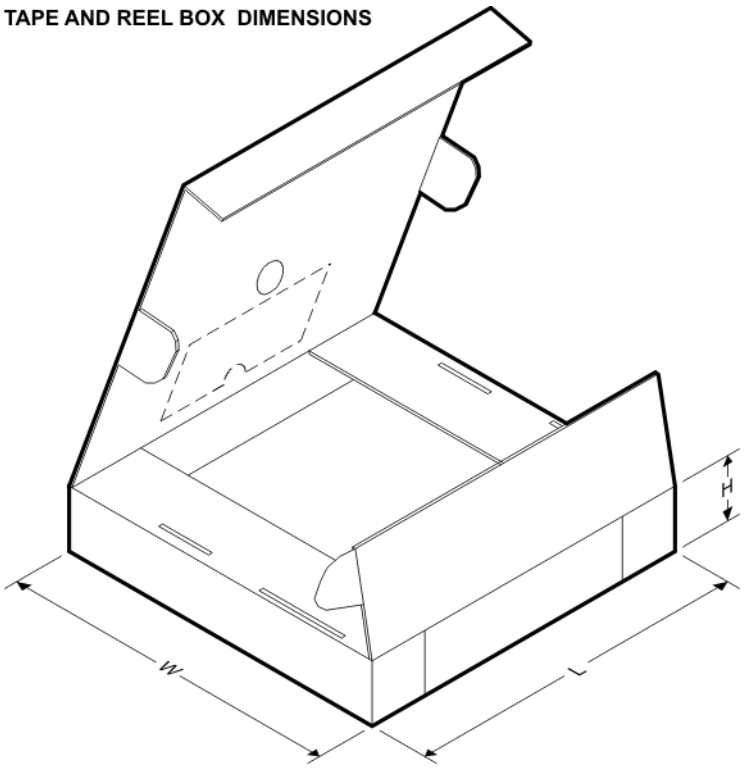
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TS5N118PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

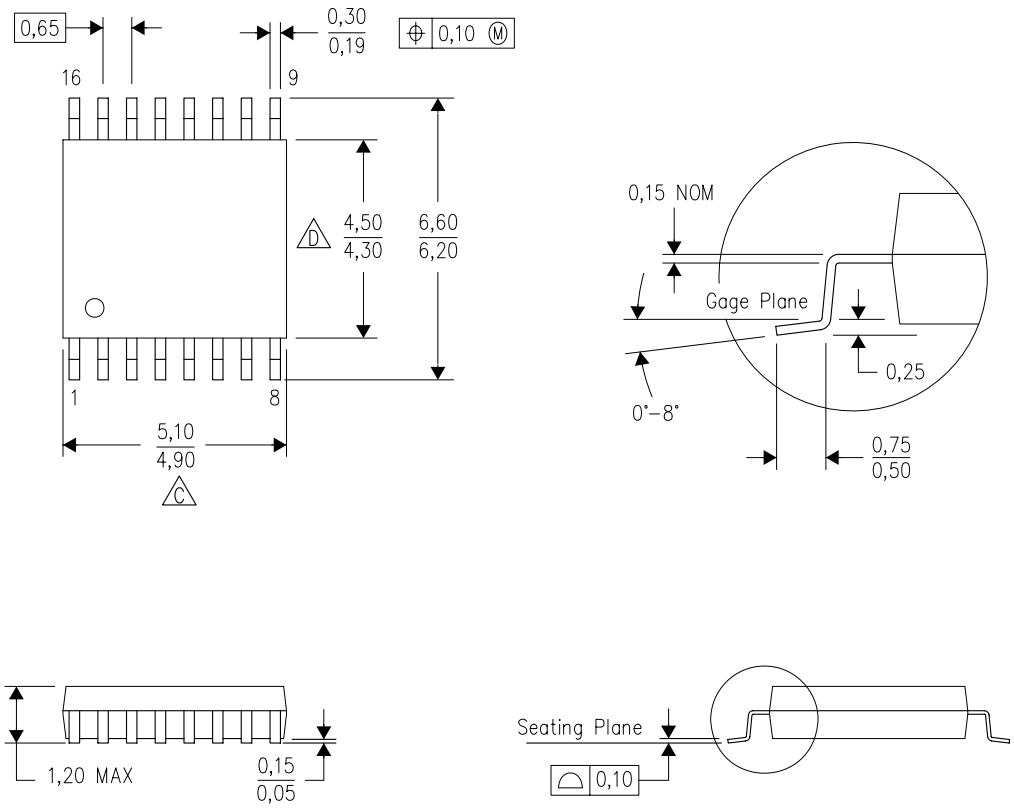
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TS5N118PWR	TSSOP	PW	16	2000	367.0	367.0	35.0

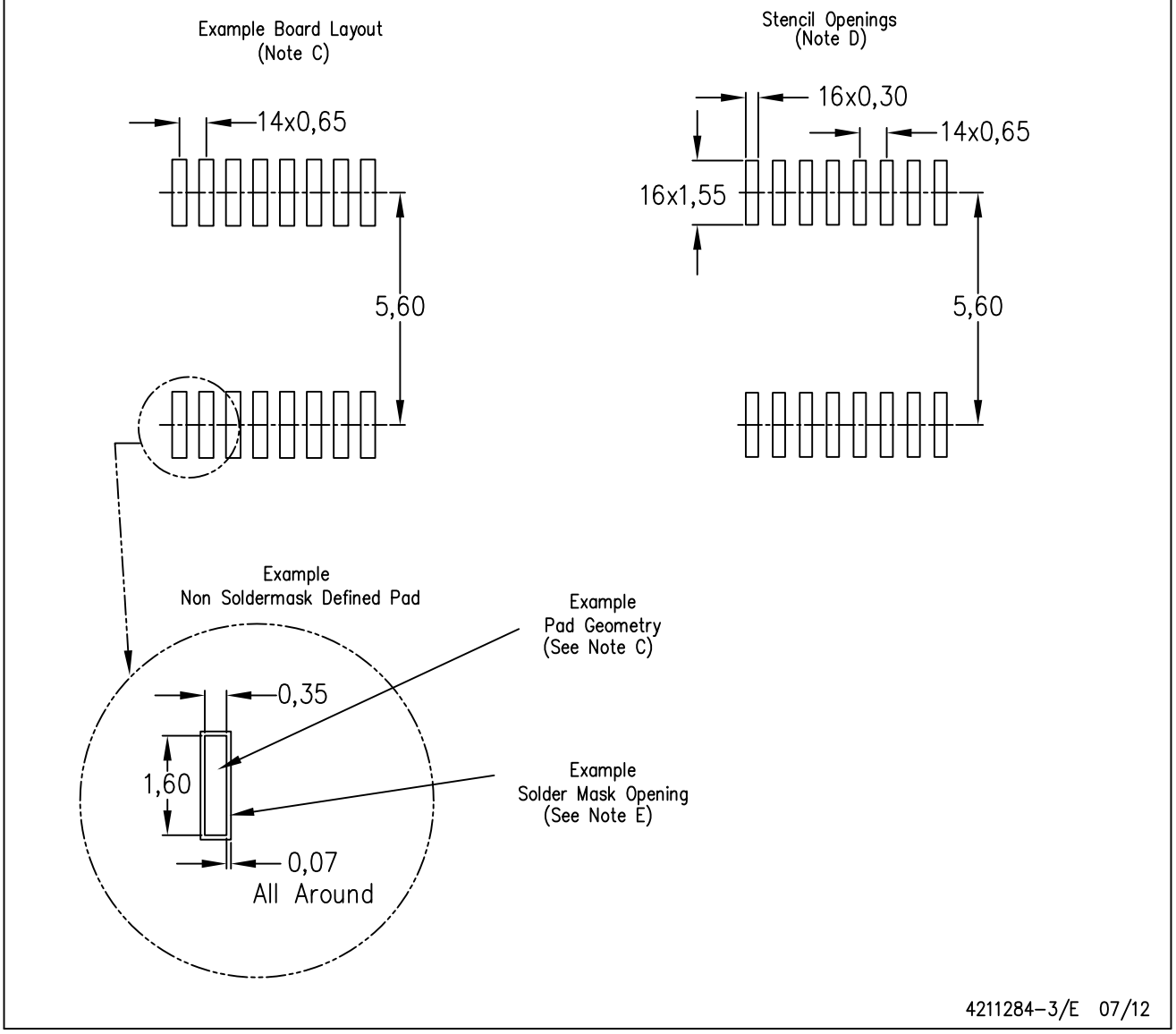
PW (R–PDSO–G16) PLASTIC SMALL OUTLINE



4040064–4/G 02/11

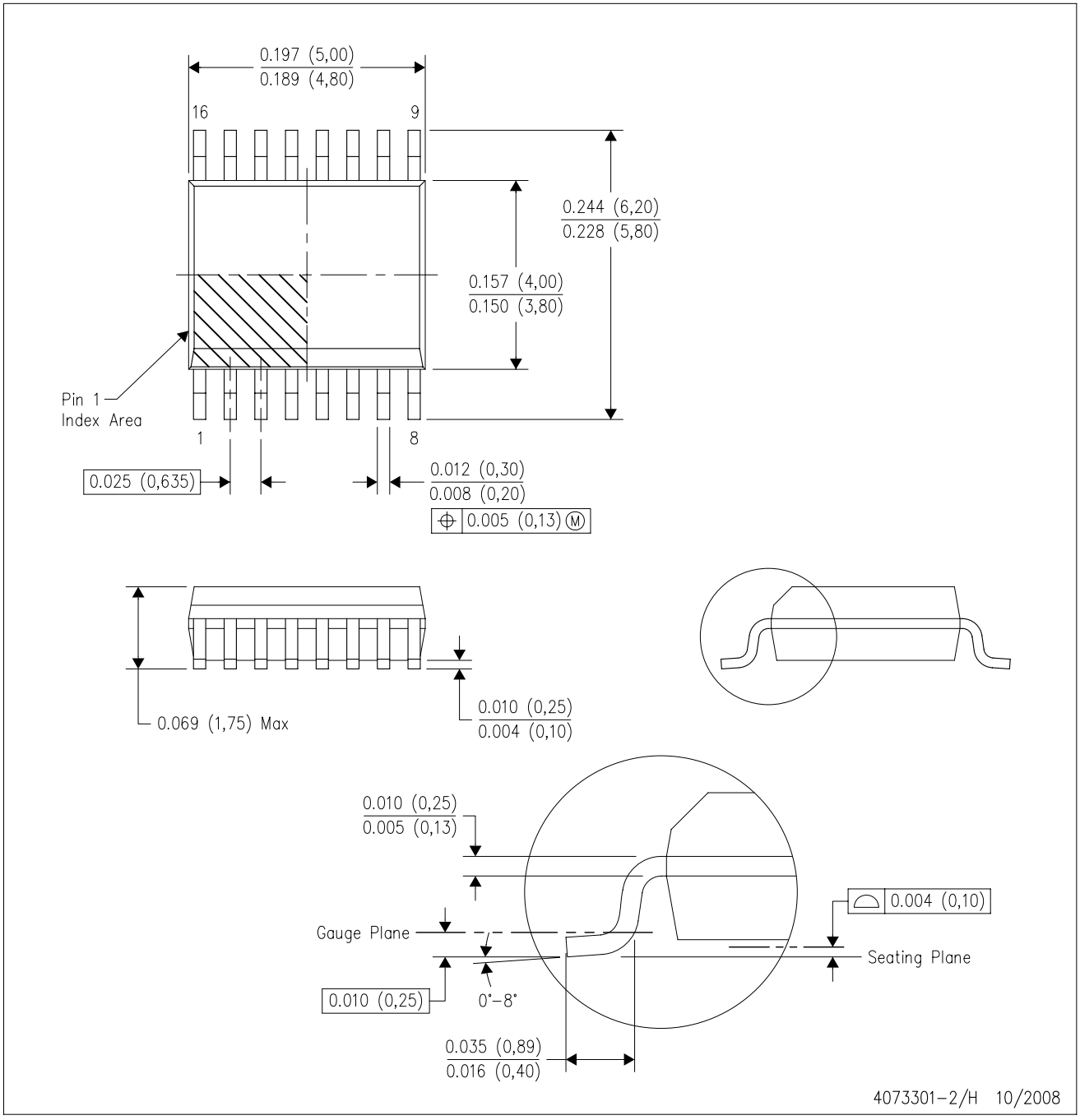
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G16) PLASTIC SMALL OUTLINE



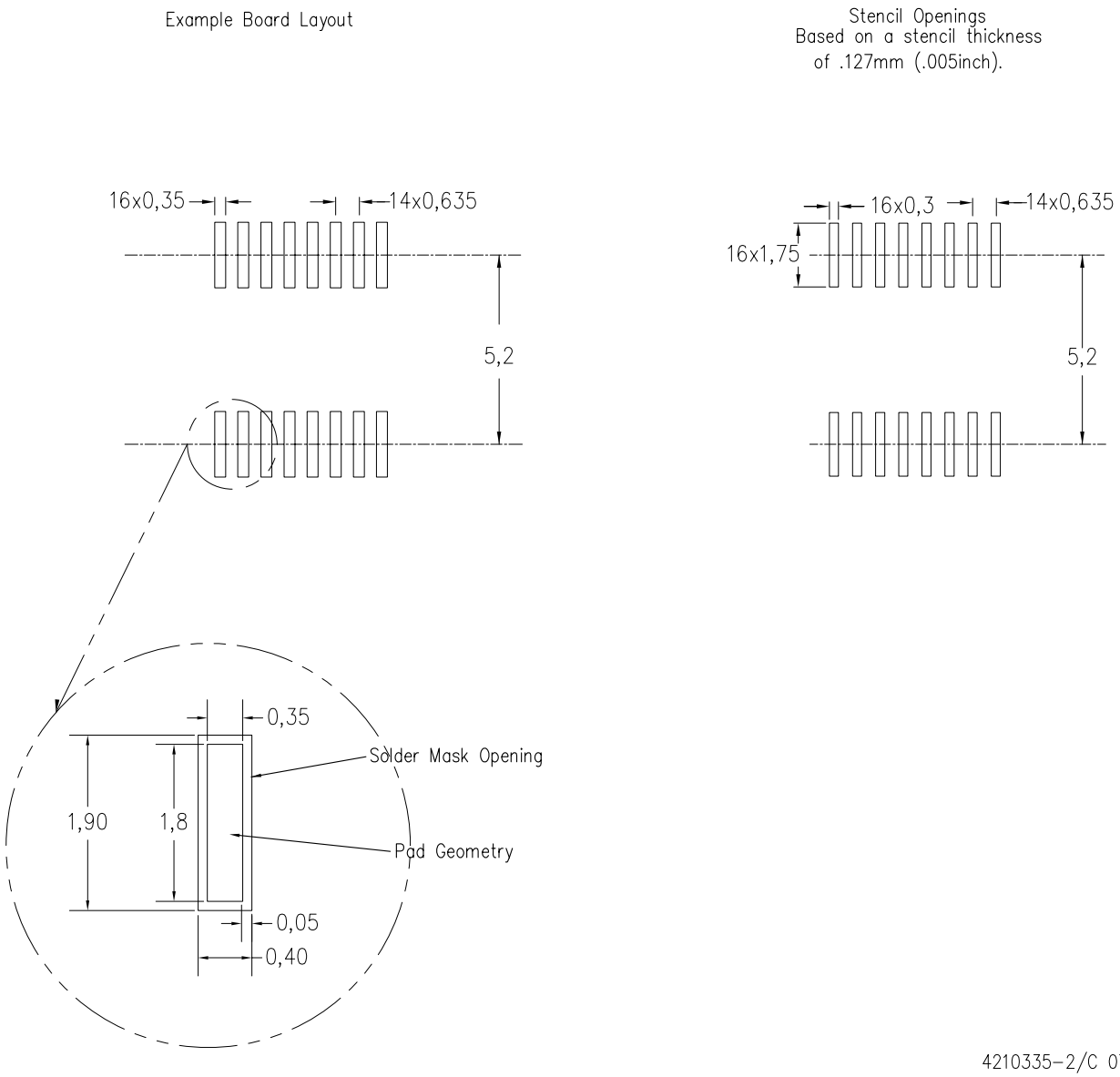
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

DBQ (R–PDSO–G16) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15) per side.
D. Falls within JEDEC MO–137 variation AB.

DBQ (R–PDSO–G16) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

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