December 2004

# FDS6690AS

## 30V N-Channel PowerTrench® SyncFET™

### General Description

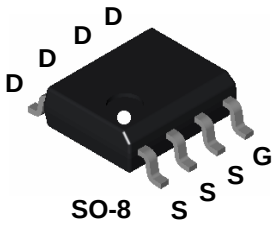
The FDS6690AS is designed to replace a single SO-8 MOSFET and Schottky diode in synchronous DC:DC power supplies. This 30V MOSFET is designed to maximize power conversion efficiency, providing a low $R_{DS(ON)}$ and low gate charge. The FDS6690AS includes an integrated Schottky diode using Fairchild's monolithic SyncFET technology. The performance of the FDS6690AS as the low-side switch in a synchronous rectifier is close to the performance of the FDS6690A in parallel with a Schottky diode.

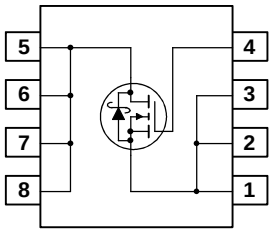
### Applications

- DC/DC converter
- Low side notebooks

### Features

- 10 A, 30 V. $R_{DS(ON)}$ max= 12 mΩ @ $V_{GS}$ = 10 V
  $R_{DS(ON)}$ max= 15 mΩ @ $V_{GS}$ = 4.5 V
- Includes SyncFET Schottky diode
- Low gate charge (16nC typical)
- High performance trench technology for extremely low $R_{DS(ON)}$
- High power and current handling capability




## Absolute Maximum Ratings

$T_A$=25°C unless otherwise noted

| Symbol | Parameter | | Ratings | Units |
|---|---|---|---|---|
| $V_{DSS}$ | Drain-Source Voltage | | 30 | V |
| $V_{GSS}$ | Gate-Source Voltage | | ±20 | V |
| $I_D$ | Drain Current – Continuous | (Note 1a) | 10 | A |
| | – Pulsed | | 50 | |
| $P_D$ | Power Dissipation for Single Operation | (Note 1a) | 2.5 | W |
| | | (Note 1b) | 1.2 | |
| | | (Note 1c) | 1 | |
| $T_J$, $T_{STG}$ | Operating and Storage Junction Temperature Range | | –55 to +150 | °C |

## Thermal Characteristics

| | | | | |
|---|---|---|---|---|
| $R_{\theta JA}$ | Thermal Resistance, Junction-to-Ambient | (Note 1a) | 50 | °C/W |
| $R_{\theta JC}$ | Thermal Resistance, Junction-to-Case | (Note 1) | 25 | °C/W |

## Package Marking and Ordering Information

| Device Marking | Device | Reel Size | Tape width | Quantity |
|---|---|---|---|---|
| FDS6690AS | FDS6690AS | 13'' | 12mm | 2500 units |
| FDS6690AS | FDS6690AS_NL (Note 4) | 13'' | 12mm | 2500 units |

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## Electrical Characteristics

$T_A$ = 25°C unless otherwise noted

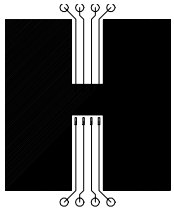
| Symbol | Parameter | Test Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **Off Characteristics** | | | | | | |
| $BV_{DSS}$ | Drain–Source Breakdown Voltage | $V_{GS}$ = 0 V, $I_D$ = 1 mA | 30 | | | V |
| $\frac{\Delta BV_{DSS}}{\Delta T_J}$ | Breakdown Voltage Temperature Coefficient | $I_D$ = 1 mA, Referenced to 25°C | | 28 | | mV/°C |
| $I_{DSS}$ | Zero Gate Voltage Drain Current | $V_{DS}$ = 24 V, $V_{GS}$ = 0 V | | | 500 | μA |
| $I_{GSS}$ | Gate–Body Leakage | $V_{GS}$ = ±20 V, $V_{DS}$ = 0 V | | | ±100 | nA |
| **On Characteristics** (Note 2) | | | | | | |
| $V_{GS(th)}$ | Gate Threshold Voltage | $V_{DS}$ = $V_{GS}$, $I_D$ = 1 mA | 1 | 1.6 | 3 | V |
| $\frac{\Delta V_{GS(th)}}{\Delta T_J}$ | Gate Threshold Voltage Temperature Coefficient | $I_D$ = 1 mA, Referenced to 25°C | | –3 | | mV/°C |
| $R_{DS(on)}$ | Static Drain–Source On–Resistance | $V_{GS}$ = 10 V, $I_D$ = 10 A<br>$V_{GS}$ = 4.5 V, $I_D$ = 8.5 A<br>$V_{GS}$=10 V, $I_D$ =10A, $T_J$=125°C | | 10<br>12<br>15 | 12<br>15<br>19 | mΩ |
| $I_{D(on)}$ | On–State Drain Current | $V_{GS}$ = 10 V, $V_{DS}$ = 5 V | 50 | | | A |
| $g_{FS}$ | Forward Transconductance | $V_{DS}$ = 15 V, $I_D$ = 10 A | | 45 | | S |
| **Dynamic Characteristics** | | | | | | |
| $C_{iss}$ | Input Capacitance | $V_{DS}$ = 15 V, $V_{GS}$ = 0 V, f = 1.0 MHz | | 910 | | pF |
| $C_{oss}$ | Output Capacitance | | | 270 | | pF |
| $C_{rss}$ | Reverse Transfer Capacitance | | | 100 | | pF |
| $R_G$ | Gate Resistance | $V_{GS}$ = 15 mV, f = 1.0 MHz | | 2.0 | | Ω |
| **Switching Characteristics** (Note 2) | | | | | | |
| $t_{d(on)}$ | Turn–On Delay Time | $V_{DS}$ = 15 V, $I_D$ = 1 A, $V_{GS}$ = 10 V, $R_{GEN}$ = 6 Ω | | 8 | 16 | ns |
| $t_r$ | Turn–On Rise Time | | | 5 | 10 | ns |
| $t_{d(off)}$ | Turn–Off Delay Time | | | 25 | 40 | ns |
| $t_f$ | Turn–Off Fall Time | | | 6 | 12 | ns |
| $t_{d(on)}$ | Turn–On Delay Time | $V_{DS}$ = 15 V, $I_D$ = 1 A, $V_{GS}$ = 4.5 V, $R_{GEN}$ = 6 Ω | | 11 | 20 | ns |
| $t_r$ | Turn–On Rise Time | | | 11 | 20 | ns |
| $t_{d(off)}$ | Turn–Off Delay Time | | | 15 | 27 | ns |
| $t_f$ | Turn–Off Fall Time | | | 8 | 16 | ns |
| $Q_{g(TOT)}$ | Total Gate Charge at Vgs=10V | $V_{DD}$ = 15 V, $I_D$ = 10 A | | 16 | 23 | nC |
| $Q_g$ | Total Gate Charge at Vgs=5V | | | 9 | 13 | nC |
| $Q_{gs}$ | Gate–Source Charge | | | 2.3 | | nC |
| $Q_{gd}$ | Gate–Drain Charge | | | 3.0 | | nC |

## Electrical Characteristics TA = 25°C unless otherwise noted

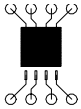
| Symbol | Parameter | Test Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **Drain–Source Diode Characteristics and Maximum Ratings** | | | | | | |
| $I_S$ | Maximum Continuous Drain–Source Diode Forward Current | | | | 3.5 | A |
| $V_{SD}$ | Drain–Source Diode Forward Voltage | $V_{GS}$ = 0 V, $I_S$ = 3.5 A (Note 2) | | 0.6 | 0.7 | V |
| $T_{rr}$ | Diode Reverse Recovery Time | $I_F$ = 10A, | | 16 | | nS |
| $Q_{rr}$ | Diode Reverse Recovery Charge | $d_{iF}/d_t$ = 300 A/µs (Note 3) | | 9 | | nC |

**Notes:**

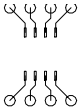
**1.** $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a) 50°/W when mounted on a 1 $in^2$ pad of 2 oz copper



b) 105°/W when mounted on a .04 $in^2$ pad of 2 oz copper



c) 125°/W when mounted on a minimum pad.

Scale 1 : 1 on letter size paper

**2.** Pulse Test: Pulse Width < 300µs, Duty Cycle < 2.0%

**3.** See "SyncFET Schottky body diode characteristics" below.

**4.** FDS6690AS_NL is a lead free product. The FDS6690AS_NL marking will appear on the reel label.

## Typical Characteristics

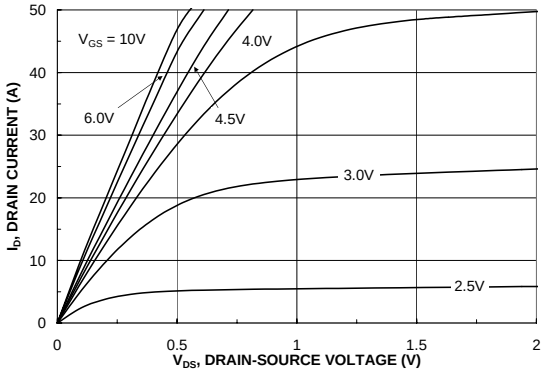



**Figure 1. On-Region Characteristics.**

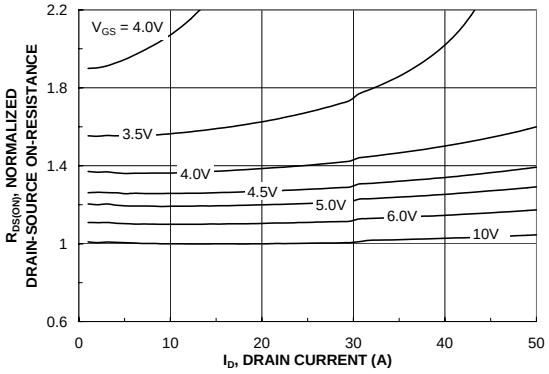



**Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.**

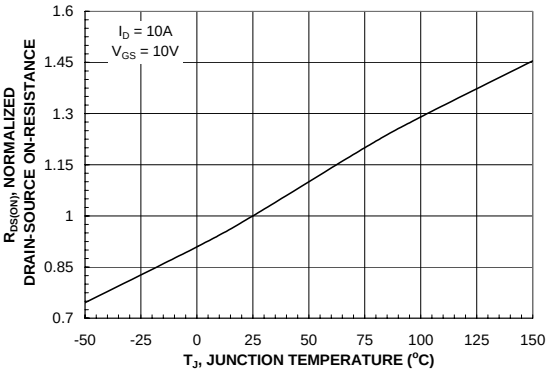



**Figure 3. On-Resistance Variation with Temperature.**

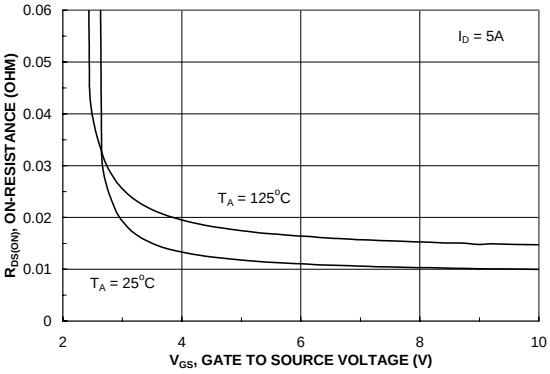



**Figure 4. On-Resistance Variation with Gate-to-Source Voltage.**

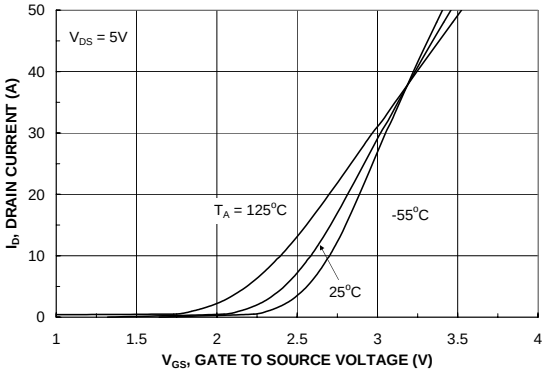



**Figure 5. Transfer Characteristics.**

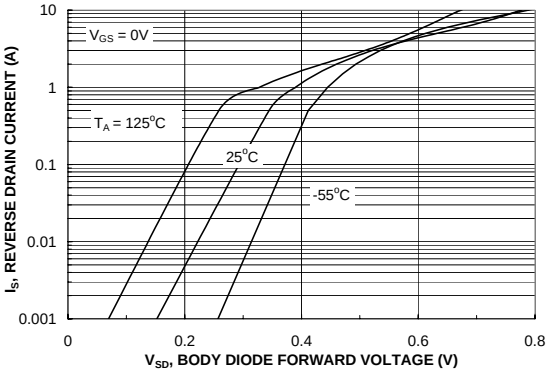



**Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.**

## Typical Characteristics

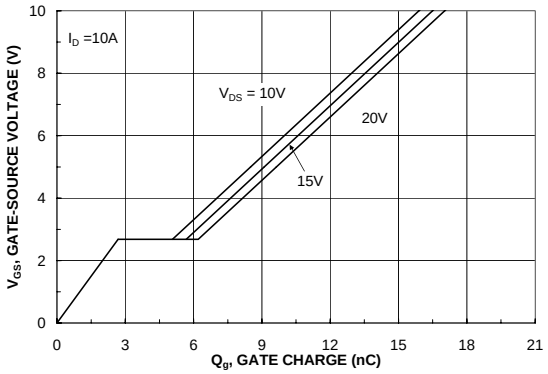



**Figure 7. Gate Charge Characteristics.**

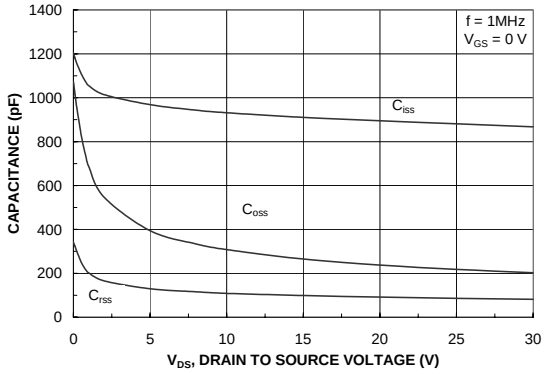



**Figure 8. Capacitance Characteristics.**

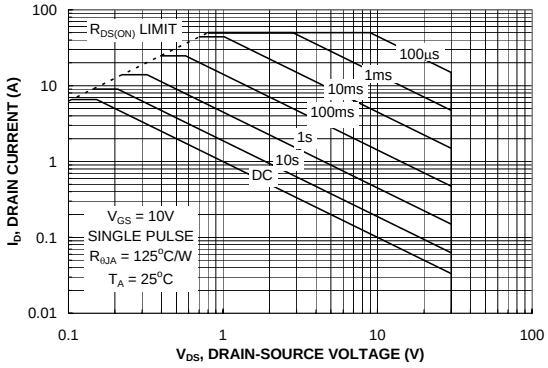



**Figure 9. Maximum Safe Operating Area.**

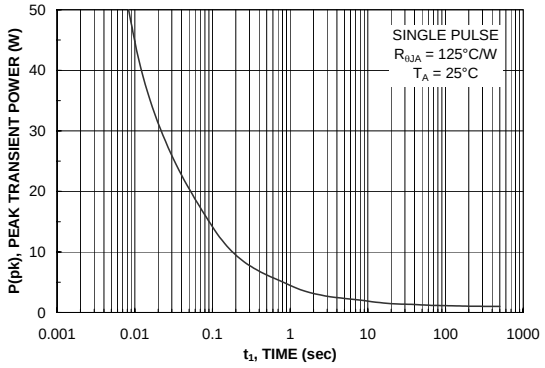



**Figure 10. Single Pulse Maximum Power Dissipation.**

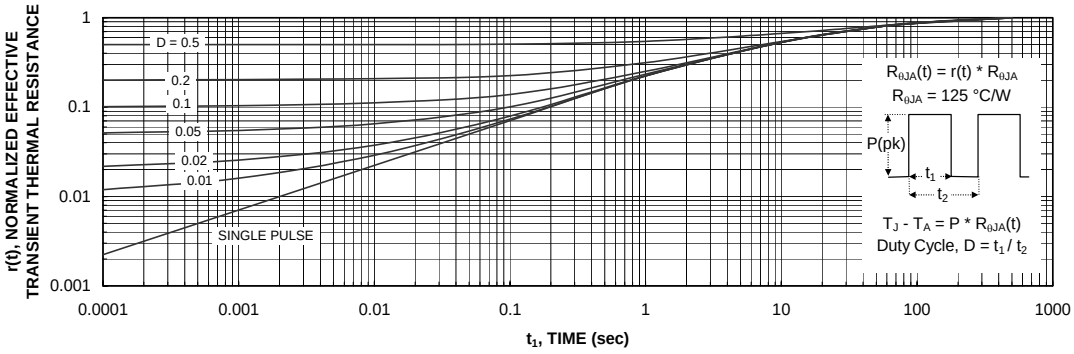



**Figure 11. Transient Thermal Response Curve.**

**Thermal characterization performed using the conditions described in Note 1c.**
**Transient thermal response will change depending on the circuit board design.**

## Typical Characteristics (continued)

### SyncFET Schottky Body Diode Characteristics

Fairchild's SyncFET process embeds a Schottky diode in parallel with PowerTrench MOSFET. This diode exhibits similar characteristics to a discrete external Schottky diode in parallel with a MOSFET. Figure 12 shows the reverse recovery characteristic of the FDS6690AS.

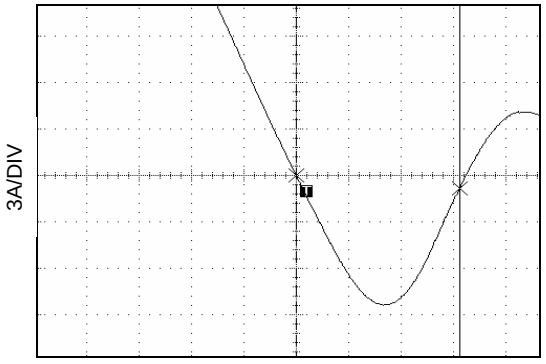



**Figure 12. FDS6690AS SyncFET body diode reverse recovery characteristic.**

For comparison purposes, Figure 13 shows the reverse recovery characteristics of the body diode of an equivalent size MOSFET produced without SyncFET (FDS6690A).

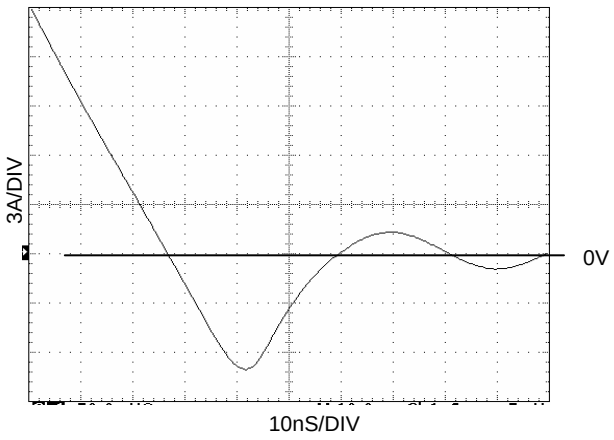



**Figure 13. Non-SyncFET (FDS6690A) body diode reverse recovery characteristic.**

Schottky barrier diodes exhibit significant leakage at high temperature and high reverse voltage. This will increase the power in the device.

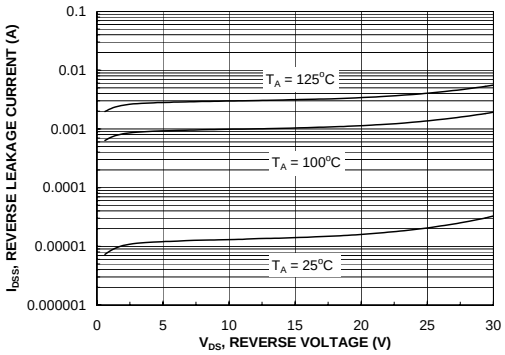



**Figure 14. SyncFET body diode reverse leakage versus drain-source voltage and temperature.**

## Typical Characteristics

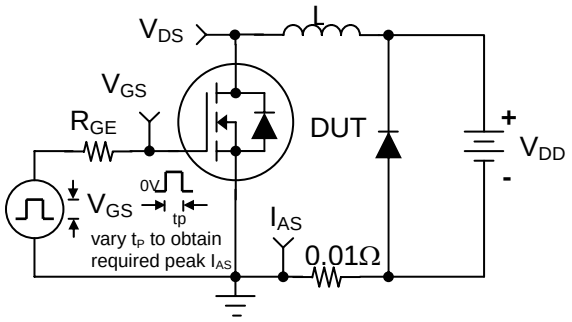



Figure 15. Unclamped Inductive Load Test Circuit

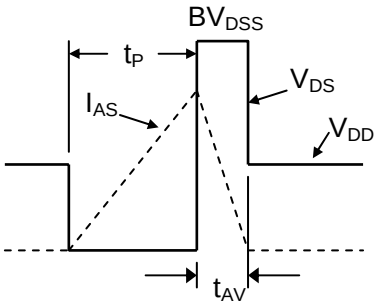



Figure 16. Unclamped Inductive Waveforms

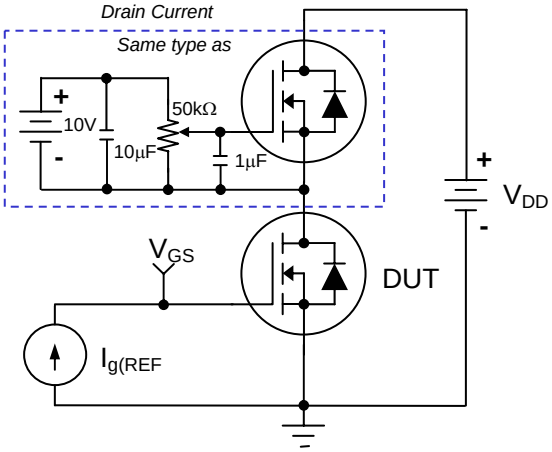



Figure 17. Gate Charge Test Circuit

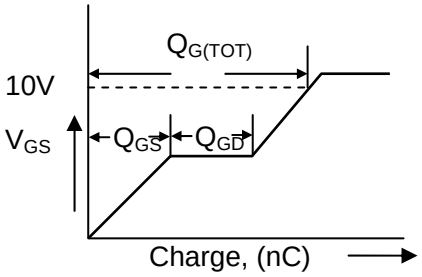



Figure 18. Gate Charge Waveform

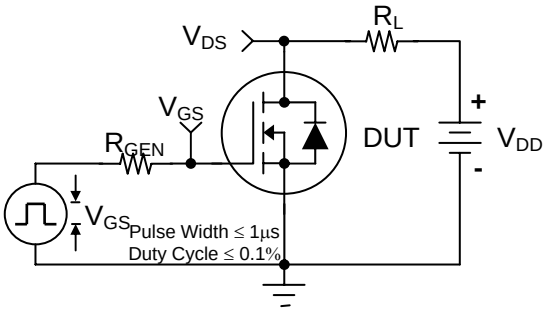



Figure 19. Switching Time Test Circuit

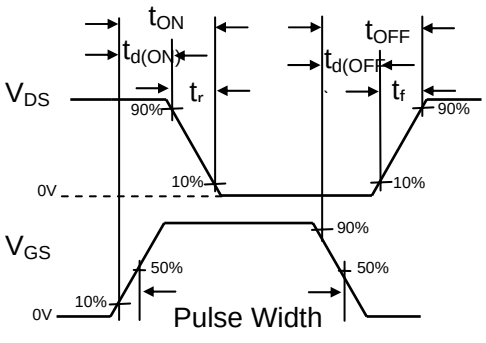



Figure 20. Switching Time Waveforms

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