



### FEATURES

- Qualified for automotive applications
- 2 device-enabling outputs with 6 factory programmed monitoring inputs (see Table 1)
- Two 30 V monitoring inputs with shutdown control of external devices
  - Factory programmed overvoltage, undervoltage, turn-on and turn-off thresholds, and shutdown timings
  - Shutdown warning with fault detection
  - Reset control of external devices
- 5 V and 7.96 V monitoring inputs with reset control of external devices
  - Factory programmed reset thresholds and hold time
- eMOST-compatible inputs
  - Diagnostic application using  $V_{2MON}$  and  $V_{4MON}$
- Two supervisory functions
  - Watchdog reset controller with timeout and selectable floating input
  - Manual reset control for external devices
- Digital interface and programmability
  - I<sup>2</sup>C-compatible interface
  - OTP can be overwritten for dynamic adjustments
  - Power-up by edge triggered signal
  - Power-down over I<sup>2</sup>C bus
- Operating range
  - Supply voltage: 6.0 V to 30 V
  - Temperature range: -40°C to +125°C
- Shutdown current: 5  $\mu$ A max
- Operating current: 2 mA max
- High voltage input antimigration shielding pinouts

### APPLICATIONS

- Automotive systems
- Network equipment
- Computers, controllers, and embedded systems

### GENERAL DESCRIPTION

The AD5100 is a factory programmed system management IC that combines four channels of voltage monitoring and watchdog supervision. The AD5100 can be used to shut down external supplies, reset processors, or disable any other system electronics when the system malfunctions. The AD5100 can also be used to protect systems from improper device power-up sequencing. The AD5100 is a robust watchdog reset controller, and can monitor two 30 V inputs with shutdown and reset controls, one 2.3 V to 5.0 V input, and one 1.6 V to 7.96 V input. Most monitoring input thresholds and timing settings have a range of settings which are factory programmed by Analog Devices, Inc. in the one-time programmable EPROM (OTP) memory, or can be programmed on-the-fly over the serial interface.

The AD5100 is versatile for system monitoring applications where critical microprocessor, DSP, and embedded systems operate under harsh conditions, such as automotive, industrial, or communications network environments.

The AD5100 is available in a compact 16-lead QSOP package and can operate in an extended automotive temperature range from -40°C to +125°C.

Analog Devices provides non-OTP programmed AD5100 parts for use in evaluating the desired threshold and delay settings. Only factory programmed AD5100 parts are shipped in production quantities. Contact Analog Devices directly to inquire about factory programmed models.

Table 1. AD5100 General Input and Output Information

Input	Monitoring Range <sup>1</sup>	Shutdown Control	Reset Control	Fault Detection
$V_{1MON}$	6 V to 28.29 V	Yes	Yes	Yes
$V_{2MON}$	3 V to 24.75 V	Yes	Yes	Yes
$V_{3MON}$	2.32 V to 4.97 V	No	Yes	Yes
$V_{4MON}$	1.67 V to 7.96 V	No	Yes	Yes
WDI	0 V to 5 V	Yes	Yes	No
$\overline{MR}$	0 V to 5 V	No	Yes	No

<sup>1</sup> With programmable threshold and programmable delay.

#### Rev. A

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## REVISION HISTORY

### 6/10—Rev. 0 to Rev. A

Changed Programmable to Factory Programmed Throughout .....	1	Changes to Overcurrent Protection Section .....	22
Changes to Features Section and General Description Section .....	1	Changes to ADI Register Map Section .....	23
Changes to $R_{\text{IN}_V2\text{MON}}$ , $R_{\text{IN}_V3\text{MON}}$ , $R_{\text{IN}_V4\text{MON}}$ , and MR Resistance Specifications Throughout .....	4	Changes to Table 11 .....	23
Changes to Table 2 .....	4	Changes to I <sup>2</sup> C Serial Interface Section and Table 12 .....	26
Changes to Table 5 .....	9	Changes to Table 14 and Reading Data from AD5100 Section .....	27
Deleted Figure 18; Renumbered Sequentially .....	21	Deleted Figure 25 .....	28
Changes to Rising Edge Triggered Wake-Up Mode Section .....	21	Deleted Permanent Setting of AD5100 Registers Section .....	30
		Changes to Ordering Guide and added Automotive Products Section .....	35

### 9/08—Revision 0: Initial Version

FUNCTIONAL BLOCK DIAGRAM

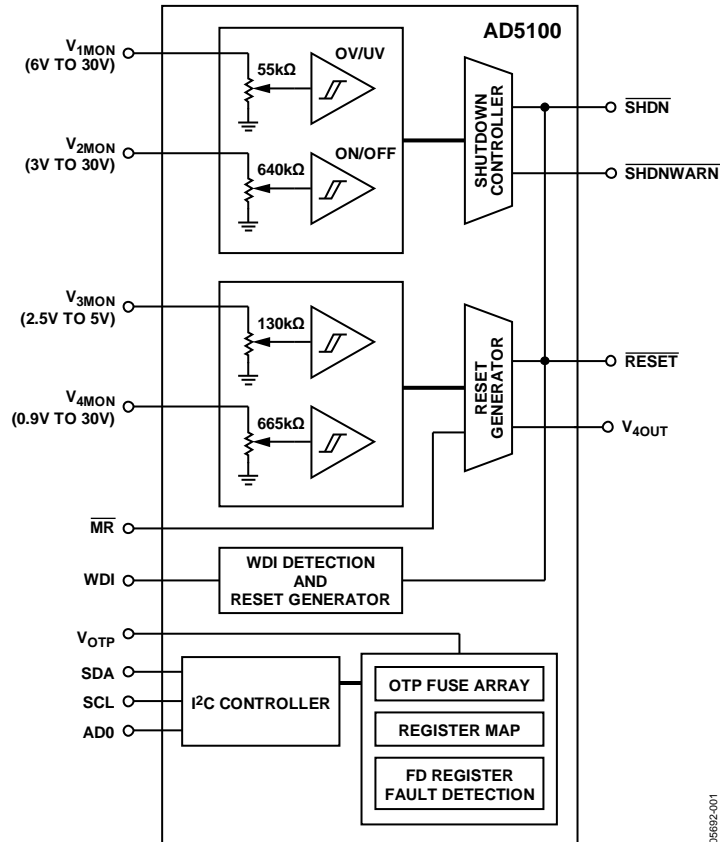


Figure 1.

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## SPECIFICATIONS

### ELECTRICAL SPECIFICATIONS

$6\text{ V} \leq V_{1\text{MON}} \leq 30\text{ V}$  and  $3\text{ V} \leq V_{2\text{MON}} \leq 30\text{ V}$ ,  $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ , unless otherwise noted.

Table 2.

Parameter	Symbol	Conditions	Min	Typ <sup>1</sup>	Max	Unit
<b>HIGH VOLTAGE MONITORING INPUTS</b>						
$V_{1\text{MON}}$						
Voltage Range	$V_{1\text{MON}}$		6		30	V
Input Resistance	$R_{\text{IN}_V1\text{MON}}$		36	55	70	k $\Omega$
OV, UV Threshold Tolerance (See Figure 7 and Table 6)	$\Delta\text{OV}, \Delta\text{UV}$	$T_A = 25^\circ\text{C}$	-1.6		+1.6	%
		$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$	-1.8		+1.8	%
		$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$	-2		+2	%
Hysteresis				1.5		%
Programmable Shutdown Hold Time Tolerance (See Figure 7 and Table 8)	$\Delta t_{1\text{SD\_HOLD}}$	$T_A = 25^\circ\text{C}$ ; does not apply to Code 0x7	-10		+10	%
Programmable Shutdown Delay Tolerance (See Figure 7 and Table 8)	$\Delta t_{1\text{SD\_DELAY}}$	$T_A = 25^\circ\text{C}$ ; does not apply to Code 0x7	-10		+10	%
		$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$ ; does not apply to Code 0x7	-17		+17	%
Fault Detection Delay	$t_{\text{FD\_DELAY}}$			60		$\mu\text{s}$
Glitch Immune Time	$t_{\text{GLITCH}}$	Guaranteed by evaluation		45		$\mu\text{s}$
$V_{2\text{MON}}$						
Input Voltage	$V_{2\text{MON}}$	Minimum voltage on $V_{2\text{MON}}$ to ensure AD5100 $V_{\text{REG}}$ power-up	2.2			V
Voltage Range <sup>2</sup>	$V_{2\text{MON}}$		3		30	V
Input Resistance	$R_{\text{IN}_V2\text{MON}}$		500	675	860	k $\Omega$
On, Off Threshold Tolerance <sup>3</sup> (See Figure 7 and Table 6)	$\Delta\text{On}, \Delta\text{Off}$	$T_A = 25^\circ\text{C}$	-2		+2	%
		$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$	-2.4		+2.4	%
		$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$	-2.5		+2.5	%
Hysteresis				1.5		%
Turn-On Programmable $\overline{\text{SHDN}}$ Hold Time Tolerance (See Figure 7 and Table 8)	$\Delta t_{2\text{SD\_HOLD}}$	$T_A = 25^\circ\text{C}$ ; does not apply to Code 0x7	-10		+10	%
Turn-Off Programmable $\overline{\text{SHDN}}$ Delay Time Tolerance (See Figure 7 and Table 8)	$\Delta t_{2\text{SD\_DELAY}}$	$T_A = 25^\circ\text{C}$ ; does not apply to Code 0x7	-10		+10	%
		$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$ ; does not apply to Code 0x7	-17		+17	%
Fault Detection Delay	$t_{\text{FD\_DELAY}}$	$V_{2\text{MON\_OFF}}$ only		60		$\mu\text{s}$
Glitch Immune Time	$t_{\text{GLITCH}}$			45		$\mu\text{s}$
$\overline{\text{SHDN}}$						
$\overline{\text{SHDN}}$ Output High	$V_{\text{OH}}$	$V_{\text{RAIL}} = V_{\text{REG}}, I_{\text{SOURCE}} = 40\ \mu\text{A}$	2.4			V
		$V_{\text{RAIL}} = V_{1\text{MON}}, I_{\text{SOURCE}} = 600\ \mu\text{A}$	$V_{1\text{MON}} - 0.5$			V
$\overline{\text{SHDN}}$ Output Low	$V_{\text{OL}}$	$I_{\text{SINK}} = 1.6\ \text{mA}$			0.4	V
		$V_{1\text{MON}} = 12\ \text{V}, I_{\text{SINK}} = 40\ \text{mA}$		1.5	3	V
$\overline{\text{SHDN}}$ Sink Current	$I_{\text{SINK}}$	$V_{1\text{MON}} = 12\ \text{V}, \overline{\text{SHDN}}$ forced to 12 V		10	13.5	mA
$\overline{\text{SHDNWARN}}$ (Open-Drain Output)						
$\overline{\text{SHDNWARN}}$ Inactive Leakage Current	$I_{\text{OH\_SHDNWARN}}$			0.9		$\mu\text{A}$
$\overline{\text{SHDNWARN}}$ Active	$V_{\text{OL\_SHDNWARN}}$	$I_{\text{SINK}} = 3\ \text{mA}$			0.4	V

Parameter	Symbol	Conditions	Min	Typ <sup>1</sup>	Max	Unit
<b>LOW VOLTAGE MONITORING INPUTS</b>						
$V_{3MON}, V_{4MON}$						
$V_{3MON}$ Voltage Range	$V_{3MON}$		2.0		5.5	V
Input Resistance	$R_{IN\_V3MON}$		85	130	180	k $\Omega$
$V_{3MON}$ Threshold Tolerance (See Figure 10 and Table 6)	$\Delta V_{3MON}$	$T_A = 25^\circ\text{C}$	-2.5		+2.5	%
		$T_A = -40^\circ\text{C to } +85^\circ\text{C}$	-2.75		+2.75	%
		$T_A = -40^\circ\text{C to } +125^\circ\text{C}$	-3		+3	%
$V_{3MON}$ Hysteresis	$V_{3\_HYSTERESIS}$			1.2		%
$V_{4MON}$ Voltage Range <sup>4</sup>	$V_{4MON}$		0.9		30	V
Input Resistance	$R_{IN\_V4MON}$		500	675	860	k $\Omega$
$V_{4MON}$ Threshold Tolerance (See Figure 12 and Table 6)	$\Delta V_{4MON}$	$T_A = 25^\circ\text{C}$	-2.5		+2.5	%
		$T_A = -40^\circ\text{C to } +85^\circ\text{C}$	-2.75		+2.75	%
		$T_A = -40^\circ\text{C to } +125^\circ\text{C}$	-3		+3	%
$V_{4MON}$ Hysteresis	$V_{4\_HYSTERESIS}$			5		%
<b>RESET</b>						
RESET Hold Time Tolerance (See Figure 10, Figure 12, and Table 8)	$\Delta t_{RS\_HOLD}$	$T_A = 25^\circ\text{C}$ ; does not apply to Code 0x6 and Code 0x7	-10		+10	%
		$T_A = -40^\circ\text{C to } +125^\circ\text{C}$ ; does not apply to Code 0x6 and Code 0x7	-17		+17	%
$V_{3MON}/V_{4MON}$ -to-RESET Delay	$t_{RS\_DELAY}$			60		$\mu\text{s}$
RESET Output Voltage High	$V_{OH}$	$V_{3MON} \geq 4.38\text{ V}, I_{SOURCE} = 120\ \mu\text{A}$	$V_{3MON} - 1.5$			V
		$2.7\text{ V} < V_{3MON} \leq 4.38\text{ V}, I_{SOURCE} = 30\ \mu\text{A}$	$0.8 \times V_{3MON}$			V
		$2.3\text{ V} < V_{3MON} \leq 2.7\text{ V}, I_{SOURCE} = 20\ \mu\text{A}$	$0.8 \times V_{3MON}$			V
		$1.8\text{ V} \leq V_{3MON} \leq 2.3\text{ V}, I_{SOURCE} = 8\ \mu\text{A}$	$0.8 \times V_{3MON}$			V
RESET Output Voltage Low	$V_{OL}$	$V_{3MON} > 4.38\text{ V}, I_{SINK} = 3.2\text{ mA}$			0.4	V
		$V_{3MON} < 4.38\text{ V}, I_{SINK} = 1.2\text{ mA}$			0.3	V
RESET Output Short-Circuit Current <sup>5</sup>	$I_{SOURCE}$	RESET = 0, $V_{3MON} = 5.5\text{ V}$			825	$\mu\text{A}$
		RESET = 0, $V_{3MON} = 3.6\text{ V}$			400	$\mu\text{A}$
Glitch Immune Time	$t_{GLITCH}$			50		$\mu\text{s}$
$V_{4OUT}$ Maximum Output	$V_{4OUT\_MAX}$	Open drain			5.5	V
$V_{4OUT}$ Propagation Delay	$t_{V4OUT\_DELAY}$			70		$\mu\text{s}$
$V_{4OUT}$ Maximum Frequency	$f_{V4OUT}$	Applies to RESET disabled only		10		kHz
<b>WDI (WATCHDOG INPUT)</b>						
WDI Programmable Timeout Tolerance (see Figure 13 and Table 8)	$\Delta t_{WD}$	$T_A = 25^\circ\text{C}$	-10		+10	%
		$T_A = -40^\circ\text{C to } +125^\circ\text{C}$	-17		+17	%
WDI Pulse Width	$t_{WDI}$		50			ns
Watchdog Initiated RESET Pulse Width	$t_{WDR}$	When no WDI		$t_{WD}/50$		ms
Watchdog Initiated SHDN	$t_{WD\_SHDN}$	When no WDI activity > 4 $t_{WD}$		1		sec
WDI Input Voltage Low	$V_{IL\_WD}$				$0.3 \times V_{3MON}$	V
WDI Input Voltage High	$V_{IH\_WD}$		$0.7 \times V_{3MON}$			V
WDI Input Current		WDI = $V_{3MON}$			160	$\mu\text{A}$
		WDI = 0	-20			$\mu\text{A}$
<b>MR (MANUAL RESET) INPUT</b>						
MR Input Voltage Low	$V_{IL\_MR}$				$0.3 \times V_{3MON}$	V
MR Input Voltage High	$V_{IH\_MR}$		$0.7 \times V_{3MON}$			V
Input Current					1	$\mu\text{A}$
MR Pulse Width	$t_{MR}$		1			$\mu\text{s}$
MR Deglitching	$t_{MR\_GLITCH}$			100		ns
MR-to-RESET Delay	$t_{MR\_DELAY}$			1		$\mu\text{s}$

# AD5100

Parameter	Symbol	Conditions	Min	Typ <sup>1</sup>	Max	Unit
MR Pull-Up Resistance (Internal to V <sub>3MON</sub> )			37	60	82	kΩ
RESET Hold Time Tolerance (see Figure 12 and Table 8)	Δ <sub>TRRS_HOLD</sub>	T <sub>A</sub> = 25°C; does not apply to Code 0x6 and Code 0x7 T <sub>A</sub> = -40°C to +125°C; does not apply to Code 0x06 and Code 0x7	-10		+10	%
			-17		+17	%
<b>SERIAL INTERFACES</b>						
Input Logic High (SCL, SDA) <sup>5</sup>	V <sub>IH</sub>	External R <sub>PULL-UP</sub> = 2.2 kΩ	2.0		5.5	V
Input Logic Low (SCL, SDA)	V <sub>IL</sub>	External R <sub>PULL-UP</sub> = 2.2 kΩ	0		0.8	V
Output Logic High (SDA)	V <sub>OH</sub>	V <sub>RAIL</sub> = 2 V to 5.5 V	0.7 × V <sub>RAIL</sub>			V
Output Logic Low (SDA)	V <sub>OL</sub>	I <sub>OL</sub> = 3 mA	0		0.4	V
Input Current		V <sub>IN</sub> = 0 V to 5.5 V			1	μA
Input Capacitance	C <sub>I</sub>			5		pF
<b>POWER SUPPLY</b>						
Supply Voltage Range	V <sub>1MON</sub>		6.0		30	V
Sleep Mode Supply Current	I <sub>SLEEP_V1MON</sub>	V <sub>2MON</sub> = 0 V			5	μA
Active Mode Supply Current	I <sub>POWER_V1MON</sub>	V <sub>2MON</sub> = 12 V V <sub>2MON</sub> edge triggered mode selected			2	mA
					2	mA
Device Power-On Threshold	V <sub>2MON,IH</sub> V <sub>2MON,IL</sub>		2.2		0.4	V
Device Power-Up V <sub>2MON</sub> , Minimum Pulse Width	t <sub>V2MON,PW</sub>		4			ms
Device Power-Down Delay	T <sub>VREG_OFF_DELAY</sub>	V <sub>2MON</sub> < 0.4 V (normal mode) I <sup>2</sup> C-initiated power-down		2		sec
				10		μs

<sup>1</sup> Represent typical values at 25°C, V<sub>1MON</sub> = 12 V, and V<sub>2MON</sub> = 12 V.

<sup>2</sup> Initial V<sub>2MON</sub> turn-on minimum remains as 2.2 V but the 3 V to 30 V specifications apply afterward.

<sup>3</sup> Does not apply if V<sub>2MON</sub> is a digital signal.

<sup>4</sup> V<sub>4MON</sub> threshold limits (see Table 6) are designed to primarily allow V<sub>4MON</sub> to monitor low voltage inputs. The V<sub>4MON</sub> input pin is capable of withstanding voltages up to 30 V. One application where this 30 V capability is useful is electronic media-oriented systems transport (eMOST) diagnostic circuits.

<sup>5</sup> The RESET short-circuit current is the maximum pull-up current when RESET is driven low by a microprocessor bidirectional reset pin.

<sup>6</sup> It is typical for the SCL and SDA to have resistors pulled up to V<sub>3MON</sub>. However, care must be taken to ensure that the minimum V<sub>IH</sub> is met when the SCL and SDA are driven directly from a low voltage logic controller without pull-up resistors.

**TIMING SPECIFICATIONS**

Table 3.

Parameter	Description	Min	Typ	Max	Unit
<b>I<sup>2</sup>C INTERFACE TIMING CHARACTERISTICS<sup>1, 2</sup></b>					
f <sub>SCL</sub>	SCL clock frequency			400	kHz
t <sub>1</sub>	t <sub>BUF</sub> , bus free time between start and stop	1.3			μs
t <sub>2</sub>	t <sub>HD,STA</sub> , hold time after (repeated) start condition; after this period, the first clock is generated	0.6			μs
t <sub>3</sub>	t <sub>LOW</sub> , low period of SCL clock	1.3			μs
t <sub>4</sub>	t <sub>HIGH</sub> , high period of SCL clock	0.6	50		μs
t <sub>5</sub>	t <sub>SU,STA</sub> , setup time for start condition	0.6			μs
t <sub>6</sub>	t <sub>HD,DAT</sub> , data hold time			0.9	μs
t <sub>7</sub>	t <sub>SU,DAT</sub> , data setup time	0.1			μs
t <sub>8</sub>	t <sub>F</sub> , fall time of both SDA and SCL signals			0.3	μs
t <sub>9</sub>	t <sub>R</sub> , rise time of both SDA and SCL signals			0.3	μs
t <sub>10</sub>	t <sub>SU,STO</sub> , setup time for stop condition	0.6			μs

<sup>1</sup> Guaranteed by design and not subject to production test.

<sup>2</sup> See Figure 2.

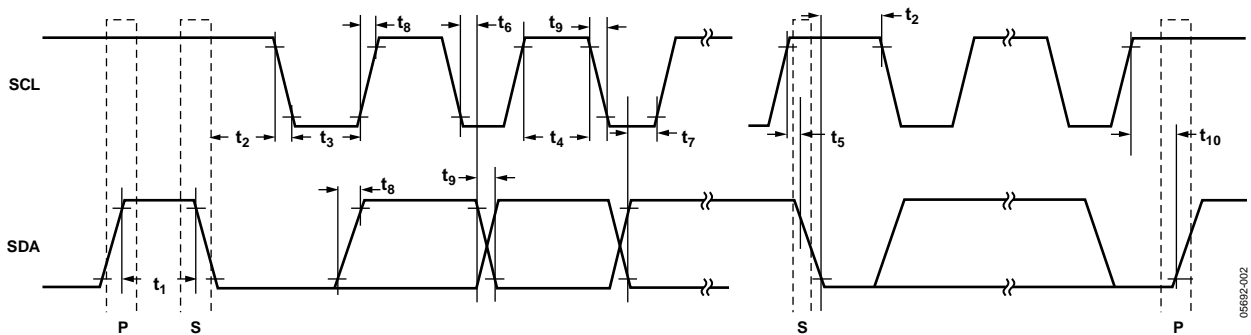


Figure 2. Digital Interface Timing Diagram

## ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
V <sub>1MON</sub> to GND	-0.3 V, +33 V
V <sub>2MON</sub> to GND	-0.3 V, +33 V
V <sub>3MON</sub> to GND	-0.3 V, +7 V
V <sub>4MON</sub> to GND	-0.3 V, +33 V
V <sub>OTP</sub> to GND	-0.3 V, +7 V
Digital Input Voltage to GND (MR, WDI, SCL, SDA, AD0)	0 V, +7 V
Digital Output Voltage to GND (RESET, V <sub>4OUT</sub> , SHDNWARN)	0 V, +7 V
Digital Output Voltage to GND (SHDN)	0 V, +33 V
Operating Temperature Range	-40°C to +125°C
Storage Temperature Range	-65°C to +150°C
ESD Rating (HBM)	3.5 kV
Maximum Junction Temperature (T <sub>Jmax</sub> )	150°C
Power Dissipation <sup>1</sup>	(T <sub>Jmax</sub> - T <sub>A</sub> <sup>2</sup> )/θ <sub>JA</sub>
Thermal Impedance <sup>3</sup>	
θ <sub>JA</sub> Junction-to-Ambient	105.44°C/W
θ <sub>JC</sub> Junction-to-Case	38.8°C/W
IR Reflow Soldering (RoHS-Compliant Package)	
Peak Temperature	260°C (+0°C)
Time at Peak Temperature	20 sec to 40 sec
Ramp-Up Rate	3°C/sec max
Ramp-Down Rate	-6°C/sec max
Time from 25°C to Peak Temperature	8 minutes max

<sup>1</sup> Values relate to the package being used on a 4-layer board.

<sup>2</sup> T<sub>A</sub> = ambient temperature.

<sup>3</sup> Junction-to-case resistance is applicable to components featuring a preferential flow direction, for example, components mounted on a heat sink. Junction-to-ambient resistance is more useful for air-cooled PCB-mounted components.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### ESD CAUTION



#### ESD (electrostatic discharge) sensitive device.

Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.



## PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

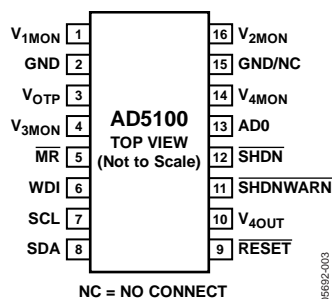


Figure 3. Pin Configuration

Table 5. AD5100 Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V <sub>1MON</sub>	High Voltage Monitoring Input. AD5100 internal supply is derived from V <sub>1MON</sub> . There must be a 10 $\mu$ F electrolytic capacitor between this pin and GND, placed as close as possible to the V <sub>1MON</sub> pin.
2	GND	Ground.
3	V <sub>OTP</sub>	One-Time Programmable Supply Voltage for EPROM. A 10 $\mu$ F decoupling capacitor (low ESR) to GND is required.
4	V <sub>3MON</sub>	Low Voltage Monitoring Input.
5	MR	Manual Reset Input. Active low.
6	WDI	Watchdog Input.
7	SCL	I <sup>2</sup> C Serial Input Register Clock. Open-drain input. If it is driven directly from a logic driver without the pull-up resistor, ensure that the V <sub>IH</sub> minimum is 3.3 V.
8	SDA	I <sup>2</sup> C Serial Data Input/Output. Open-drain input/output. If it is driven directly from a logic driver without the pull-up resistor, ensure that the V <sub>IH</sub> minimum is 3.3 V.
9	RESET	Reset. Push-pull output with rail voltage of V <sub>3MON</sub> .
10	V <sub>4OUT</sub>	Open-Drain Output. Triggered by V <sub>4MON</sub> .
11	SHDNWARN	Shutdown Warning. Active low, open-drain output.
12	SHDN	Shutdown Output. Push-pull output with selectable rail voltage of V <sub>1MON</sub> or V <sub>REG</sub> , the AD5100 internal power (30 V maximum).
13	ADO	I <sup>2</sup> C Slave Address Configuration. If tied high, this pin can only be tied to 3.3 V maximum.
14	V <sub>4MON</sub>	Low Voltage Monitoring Input. Capable of withstanding 30 V.
15	GND/NC	Ground/No Connect. Can be grounded or left floating but do not connect to any other potentials.
16	V <sub>2MON</sub>	High Voltage Monitoring Input. It is also the internal supply voltage enabling input.

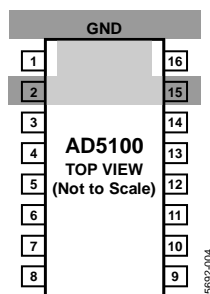


Figure 4. Recommended PCB Layout for Shielded High Voltage Inputs

# AD5100

## ONE-TIME PROGRAMMABLE (OTP) OPTIONS

All values are typical ratings; see Table 2 for tolerances.

**Table 6. Available Programmable Thresholds at T<sub>A</sub> = 25°C**

V <sub>1MON OV</sub> Threshold <sup>1</sup>	V <sub>1MON UV</sub> Threshold	V <sub>2MON On</sub> Threshold	V <sub>2MON Off</sub> Threshold <sup>2</sup>	V <sub>3MON</sub> Threshold	V <sub>4MON</sub> Threshold
7.92 V	6.00 V	3.00 V	3.00 V	2.32 V	1.67 V
9.00 V	6.49 V	3.5 V	3.5 V	2.64 V	2.31 V
9.90 V	6.95 V	4.00 V	4.00 V	2.93 V <sup>3</sup>	3.05 V
11.00 V	7.47 V	4.77 V	4.77 V	3.10 V	4.62 V
12.00 V	7.92 V	6.00 V	6.00 V	4.36 V	6.51 V
13.20 V	8.43 V <sup>3</sup>	6.49 V	6.49 V	4.65 V	7.16 V
14.14 V	9.00 V	6.95 V	6.95 V <sup>3</sup>	4.75 V	7.54 V <sup>3</sup>
15.23 V	9.43 V	7.47 V <sup>3</sup>	7.47 V	4.97 V	7.96 V
15.84 V	9.90 V	7.92 V	7.92 V	Reserved	Reserved
17.22 V	10.42 V	8.43 V	8.43 V	Reserved	Reserved
18.00 V <sup>3</sup>	11.00 V	9.00 V	9.00 V	Reserved	Reserved
18.86 V	11.65 V	9.43 V	9.43 V	Reserved	Reserved
19.80 V	12.00 V	9.90 V	9.90 V	Reserved	Reserved
22.00 V	12.38 V	15.23 V	15.23 V	Reserved	Reserved
24.75 V	13.20 V	19.80 V	19.80 V	Reserved	Reserved
28.29 V	13.66 V	24.75 V	Rising edge triggered wake-up mode	Reserved	Reserved

<sup>1</sup> V<sub>1MON OV</sub> must be > V<sub>1MON UV</sub>.

<sup>2</sup> V<sub>2MON OFF</sub> is ignored if > V<sub>2MON ON</sub>, but V<sub>2MON OFF</sub> cannot be = V<sub>2MON ON</sub>.

<sup>3</sup> AD5100-0 default settings. Contact Analog Devices if other default settings are required.

**Table 7. Look-Up Table of Programming Code vs. Typical Thresholds Shown in Table 6**

Code	V <sub>1MON OV</sub> Threshold	V <sub>1MON UV</sub> Threshold	V <sub>2MON On</sub> Threshold	V <sub>2MON Off</sub> Threshold	V <sub>3MON</sub> Threshold	V <sub>4MON</sub> Threshold
0000	18.00 V <sup>1</sup>	8.43 V <sup>1</sup>	7.47 V <sup>1</sup>	6.95 V <sup>1</sup>	2.93 V <sup>1</sup>	7.54 V <sup>1</sup>
0001	18.86 V	7.92 V	6.95 V	7.47 V	4.65 V	1.67 V
0010	15.84 V	9.43 V	6.49 V	6.00 V	4.75 V	2.31 V
0011	17.22 V	9.00 V	6.00 V	6.49 V	4.97 V	3.05 V
0100	24.75 V	6.49 V	4.77 V	4.00 V	2.32 V	4.62 V
0101	28.29 V	6.00 V	4.00 V	4.77 V	2.64 V	6.51 V
0110	19.80 V	7.47 V	3.50 V	3.00 V	4.36 V	7.16 V
0111	22.00 V	6.95 V	3.00 V	3.50 V	3.10 V	7.96 V
1000	9.90 V	12.38 V	24.75 V	19.80 V	Reserved	Reserved
1001	11.00 V	12.00 V	19.80 V	Rising edge triggered wake-up mode	Reserved	Reserved
1010	7.92 V	13.66 V	15.23 V	9.90 V	Reserved	Reserved
1011	9.00 V	13.20 V	9.90 V	15.23 V	Reserved	Reserved
1100	14.14 V	10.42 V	9.43 V	9.00 V	Reserved	Reserved
1101	15.23 V	9.90 V	9.00 V	9.43 V	Reserved	Reserved
1110	12.00 V	11.65 V	8.43 V	7.92 V	Reserved	Reserved
1111	13.20 V	11.00 V	7.92 V	8.43 V	Reserved	Reserved

<sup>1</sup>AD5100-0 default settings. Contact Analog Devices if other default settings are required.

**Table 8. Available Programmable Hold Time and Delay**

<b>t<sub>1SD_HOLD</sub></b>	<b>t<sub>1SD_DELAY</sub></b>	<b>t<sub>2SD_HOLD</sub></b>	<b>t<sub>2SD_DELAY</sub></b>	<b>t<sub>RS_HOLD</sub></b>	<b>t<sub>WD</sub></b>
0.07 ms	0.07 ms	0.07 ms	0.07 ms	0.1 ms	100 ms
20 ms	50 ms	10 ms <sup>1</sup>	50 ms	1 ms	250 ms
40 ms	100 ms	20 ms	100 ms <sup>1</sup>	15 ms	500 ms
60 ms	200 ms	30 ms	200 ms	30 ms	750 ms
80 ms	400 ms	40 ms	400 ms	50 ms	1000 ms
100 ms	800 ms	50 ms	800 ms	100 ms	1250 ms
150 ms	1000 ms	100 ms	1000 ms	150 ms	1500 ms <sup>1</sup>
200 ms <sup>1</sup>	1200 ms <sup>1</sup>	200 ms	1200 ms	200 ms <sup>1</sup>	2000 ms

<sup>1</sup> AD5100-0 default settings. Contact Analog Devices if other default settings are required.

**Table 9. Look-Up Table of Programming Code vs. Typical Timings Shown in Table 8**

<b>Code</b>	<b>t<sub>1SD_HOLD</sub></b>	<b>t<sub>1SD_DELAY</sub></b>	<b>t<sub>2SD_HOLD</sub></b>	<b>t<sub>2SD_DELAY</sub></b>	<b>t<sub>RS_HOLD</sub></b>	<b>t<sub>WD</sub></b>
000	200 ms <sup>1</sup>	1200 ms <sup>1</sup>	10 ms <sup>1</sup>	100 ms <sup>1</sup>	200 ms <sup>1</sup>	1500 ms <sup>1</sup>
001	150 ms	1000 ms	20 ms	50 ms	150 ms	2000 ms
010	100 ms	800 ms	30 ms	200 ms	100 ms	1250 ms
011	80 ms	400 ms	40 ms	400 ms	50 ms	1000 ms
100	60 ms	200 ms	50 ms	800 ms	30 ms	750 ms
101	40 ms	100 ms	100 ms	1000 ms	15 ms	500 ms
110	20 ms	50 ms	200 ms	1200 ms	1 ms	250 ms
111	0.07 ms	0.07 ms	0.07 ms	0.07 ms	0.1 ms	100 ms

<sup>1</sup> AD5100-0 default settings. Contact Analog Devices if other default settings are required.

## THEORY OF OPERATION

The AD5100 is a programmable system management IC that has four channels of monitoring inputs. Three inputs have high voltage (30 V) capability. For example, if the AD5100 is used in an automotive application,  $V_{1MON}$  (Monitoring Input 1) can be connected to the battery and the  $V_{2MON}$  can be connected to the ignition switch, a rising edge trigger wake-up signal, or the media-oriented systems transport (MOST) wake-up signal ( $V_{4MON}$  is connected to  $V_{2MON}$  for MOST applications). Two other inputs,  $V_{3MON}$  and  $V_{4MON}$ , are designed for low voltage monitoring, with programmable thresholds from 2.93 V to 7.96 V. The two high voltage monitoring inputs control the

shutdown signal,  $\overline{SHDN}$  and reset signal,  $\overline{RESET}$ , while the two low voltage monitoring inputs control the reset signal,  $\overline{RESET}$ .  $\overline{SHDN}$  and  $\overline{RESET}$  are both disabling signals for external devices. The differences between these two outputs are in output level and driving capabilities, as described in the Outputs section. The WDI (watchdog) and  $\overline{MR}$  (manual reset) inputs also control the  $\overline{RESET}$  output, for use with an external digital processor. Figure 5 shows the general flow chart and Table 10 summarizes the AD5100 functions and features.

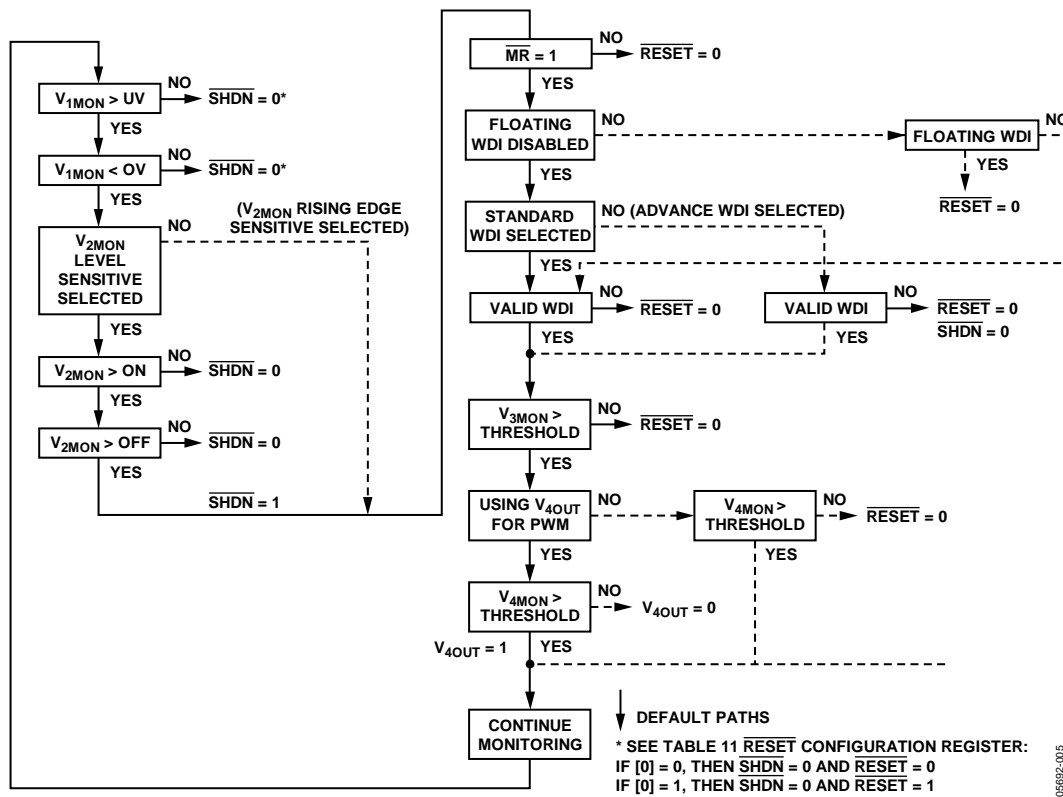


Figure 5. General Flow Chart

Table 10. AD5100 Functions and Features

Input	Monitoring Range	Shutdown Control	Reset Control	Fault Detection	Functions and Features	If Not Used
$V_{1MON}$	6 V to 28.29 V	Yes	Yes	Yes	Overvoltage/undervoltage thresholds	Does not apply
$V_{2MON}$	3 V to 24.75 V	Yes	Yes	Yes	On/off voltage thresholds; pseudo rising edge triggered, wake-up selectable; MOST wake-up signal ( $V_{2MON}$ connected to $V_{4MON}$ )	Connect to $V_{1MON}$ , minimum input 6 V
$V_{3MON}$	2.32 V to 4.97 V	No	Yes	Yes		Connect to $V_{OTP}$ and set threshold to minimum
$V_{4MON}$	1.67 V to 7.96 V	No	Yes	Yes	Additional output	Connect to GND
WDI	0 V to 5 V	Yes	Yes	No	Standard, advance, or floating; watchdog selectable	Leave floating
$\overline{MR}$	0 V to 5 V	Yes	Yes	No	Highest priority on $\overline{RESET}$ over other inputs	Leave floating

## MONITORING INPUTS

### $V_{1MON}$

$V_{1MON}$  is a high voltage monitoring input that controls the  $\overline{\text{SHDN}}$  and  $\overline{\text{RESET}}$  functions of the external devices. In addition, it provides a shutdown warning to the system.  $V_{1MON}$  monitors inputs from 6 V to 30 V.

The  $V_{1MON}$  pin is monitored by two comparators, one for overvoltage and one for undervoltage detection. Both are designed with 1.5% hysteresis.

When the  $V_{1MON}$  input goes above the programmed overvoltage (OV) threshold, the comparator becomes active immediately, indicating that an OV condition has occurred. Due to hysteresis, the  $V_{1MON}$  input must be brought below the programmed OV threshold by 1.5% before the comparator becomes inactive, indicating that the OV condition has gone away (see Figure 6).

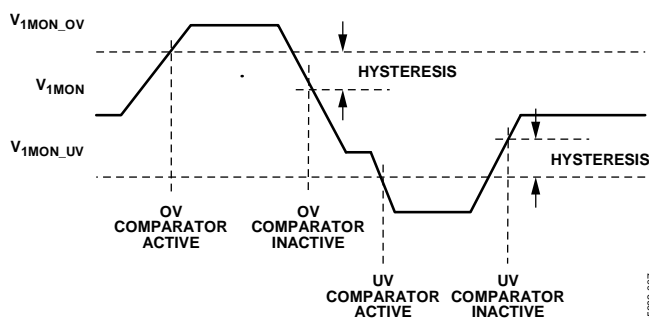


Figure 6.  $V_{1MON}$  Hysteresis

When the  $V_{1MON}$  input drops below the programmed undervoltage (UV) threshold, the comparator becomes active immediately, indicating that a UV condition has occurred. Similarly, due to hysteresis, the  $V_{1MON}$  input must be brought above the programmed UV threshold by 1.5% before the comparator becomes inactive, indicating that the UV condition has gone away.

Both  $V_{1MON}$  comparators are used (in conjunction with hold and delay timers) to control the  $\overline{\text{SHDN}}$  and  $\overline{\text{RESET}}$  pins.

$V_{1MON}$  has a 16-level programmable OV threshold (Register 0x01) and UV threshold (Register 0x02) with an 8-step 0.07 ms to 200 ms shutdown hold time ( $t_{\text{ISD\_HOLD}}$ ) and 0.07 ms to 1200 ms

shutdown delay ( $t_{\text{ISD\_DELAY}}$ ). The shutdown hold time means that the  $\overline{\text{SHDN}}$  signal is held low for  $t_{\text{ISD\_HOLD}}$  after  $V_{1MON}$  returns within its UV and OV thresholds. The shutdown delay means that the  $\overline{\text{SHDN}}$  signal activation is delayed until the programmed  $t_{\text{ISD\_DELAY}}$  has elapsed.  $\overline{\text{SHDN}}$  activates once the voltage on  $V_{1MON}$  is outside the OV or UV threshold for a time longer than  $t_{\text{GLITCH}}$ .  $\overline{\text{RESET}}$  follows  $\overline{\text{SHDN}}$  delay and hold timings when triggered by  $V_{1MON}$ .

The OV threshold chosen must be greater than the UV threshold. When the shutdown is triggered, either because the input has reached the OV or UV threshold, such fault conditions are temporarily recorded in the fault detection register.

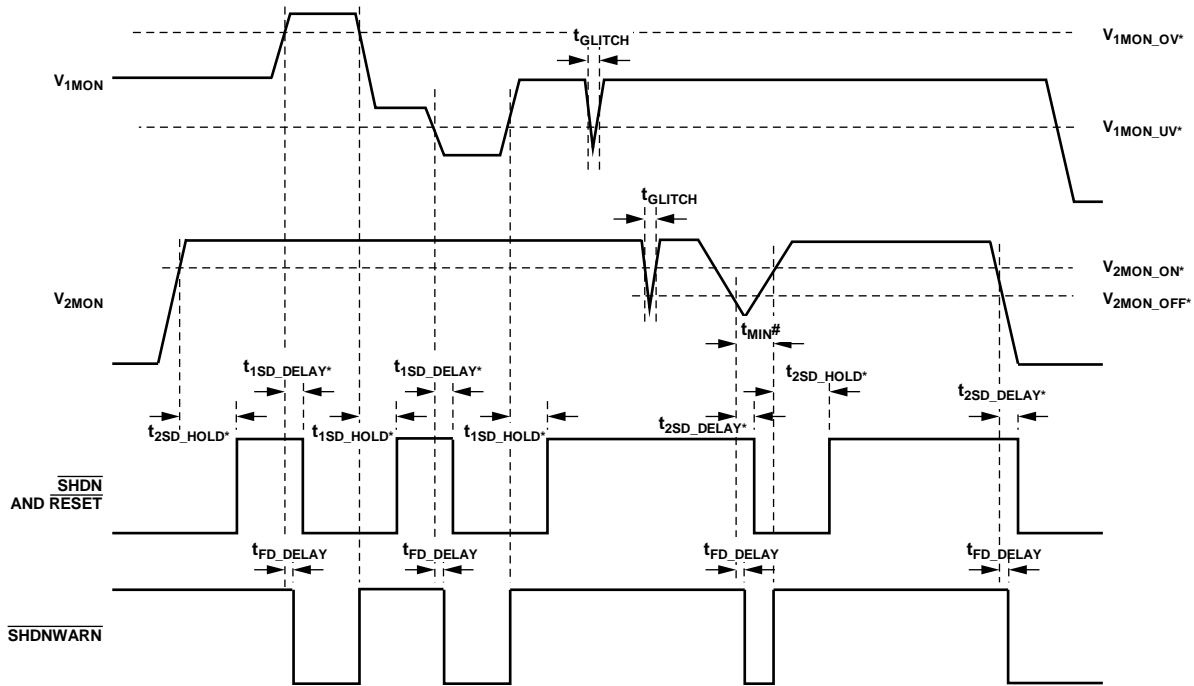
The  $\overline{\text{SHDNWARN}}$  output transitions low for signaling before the shutdown output,  $\overline{\text{SHDN}}$ , activates. The timing of the  $\overline{\text{SHDN}}$  output is dependent on how long the shutdown-programmed delay ( $t_{\text{ISD\_DELAY}}$ ) is set relative to the  $\overline{\text{SHDNWARN}}$  propagation delay ( $t_{\text{FD\_DELAY}}$ ). This feature attempts to allow the system to finish any critical housekeeping tasks before shutting down the external device.

The  $V_{1MON}$ , shutdown, and shutdown warning timing diagrams are shown in Figure 7.

The ranges of OV and UV thresholds are shown in Table 6, and the programming codes for the selected thresholds are found in Table 7. The defaulted OV threshold is 18.00 V and, for UV threshold, it is 8.43 V. Similarly, the ranges of shutdown hold and delay times are shown in Table 8, and the programming codes for the selected timings are shown in Table 9.

$V_{1MON}$  exhibits typical input resistance of 55 k $\Omega$  that users should take into account for loading effect.

The voltage at  $V_{1MON}$  provides the power for the AD5100, but a valid signal on  $V_{2MON}$  must be present before the internal power rail,  $V_{\text{REG}}$ , starts operation. Details are explained in the Power Requirements section.



NOTES

1. \* = PROGRAMMABLE.
2. # = THE DURATION OF THE  $t_{MIN\#}$  MUST BE SHORTER THAN  $t_{VREG\_OFF\_DELAY}$  OR ELSE THE AD5100 WILL BE POWERED OFF.

Figure 7.  $V_{1MON}$  and  $V_{2MON}$  Shutdown Timing Diagrams in Level-Sensitive Mode (Note that  $\overline{RESET}$  Follows  $\overline{SHDN}$ )

**$V_{2MON}$**

$V_{2MON}$  is a high voltage monitoring input that controls the  $\overline{SHDN}$  and  $\overline{RESET}$  functions of the external devices.  $V_{2MON}$  monitors inputs from 3 V to 30 V. It has a 16-level programmable turn-on and turn-off (on, off) hysteresis thresholds (Register 0x03 and Register 0x04), with an 8-step 0.07 ms to 200 ms shutdown hold time ( $t_{2SD\_HOLD}$ ) and 0.07 ms to 1200 ms shutdown delay ( $t_{2SD\_DELAY}$ ).

The  $V_{2MON}$  pin is monitored by two comparators, one for turn-on and one for turn-off detection, in the level-sensitive power-up mode. Both are designed with 1.5% hysteresis. Only the turn-on monitoring comparator is used if the rising edge triggered wake-up mode is selected.

When the  $V_{2MON}$  input goes above the programmed  $V_{2MON}$  on threshold, the comparator becomes active immediately, indicating that an on condition has occurred. Due to hysteresis, the  $V_{2MON}$  input must be brought below the programmed threshold by 1.5% before the comparator becomes inactive, indicating that the on condition has gone away (see Figure 8).

When the  $V_{2MON}$  input drops below the programmed threshold, the comparator becomes active immediately, indicating that a  $V_{2MON}$  off condition has occurred. Similarly, due to hysteresis, the  $V_{2MON}$  input must be brought above the programmed threshold by 1.5% before the comparator becomes inactive, indicating that the off condition has gone away.

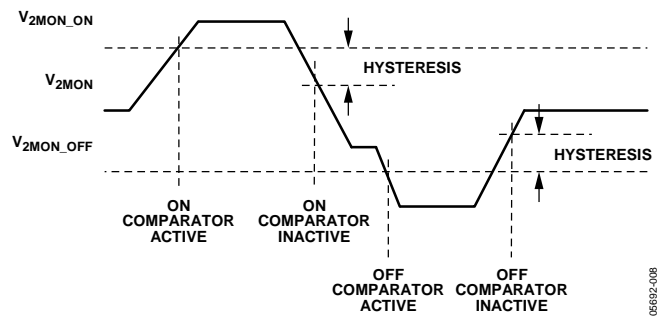


Figure 8.  $V_{2MON}$  Hysteresis

By default,  $V_{2MON}$  is level sensitive and the on and off thresholds are both monitored. The on threshold chosen must be greater than the off threshold.

When the  $\overline{SHDN}$  output is activated by the input reaching the  $V_{2MON\_OFF}$  threshold, such fault condition is temporarily recorded in the fault detection register. The  $\overline{SHDNWARN}$  output transitions low for signaling before the shutdown output,  $\overline{SHDN}$ , activates. The timing of the  $\overline{SHDN}$  output is dependent on how long the shutdown programmed delay ( $t_{2SD\_DELAY}$ ) is set relative to the  $\overline{SHDNWARN}$  propagation delay ( $t_{FD\_DELAY}$ ). This feature allows the system to finish any critical housekeeping tasks before shutting down the external device.  $\overline{SHDN}$  activates once the voltage on  $V_{2MON}$  is outside the threshold for a time longer than  $t_{GLITCH}$ .  $\overline{RESET}$  follows  $\overline{SHDN}$  delay and hold timings when triggered by  $V_{2MON}$ .

The  $V_{2MON}$ , shutdown, and shutdown warning timing diagrams are shown in Figure 7.

The ranges of on and off thresholds are shown in Table 6 and the programming codes for the selected-thresholds are found in Table 7. The default on threshold is 7.47 V and off threshold is 6.95 V. Similarly, the ranges of shutdown hold and delay times are shown in Table 8, and the programming codes of the selected timings are found in Table 9. The default shutdown hold time is 10 ms and the delay time is 100 ms.

$V_{2MON\_OFF}$  is ignored if  $V_{2MON\_OFF}$  is greater than  $V_{2MON\_ON}$  but  $V_{2MON\_OFF}$  cannot equal  $V_{2MON\_ON}$ .

If  $V_{2MON}$  is selected with rising edge triggered wake-up mode, only the on threshold is monitored and the off threshold is ignored.  $V_{2MON}$  is put into rising edge triggered mode by setting  $V_{2MON}$  off threshold, Register 0x04[3:0] to 1001

The voltage at  $V_{1MON}$  provides the power for the AD5100, but a valid signal on  $V_{2MON}$  must be present before the internal  $V_{REG}$  starts operating. Details are explained in the Power Requirements section.

$V_{2MON}$  exhibits typical input resistance of 675 k $\Omega$  that users should take into account for loading effect.

**$V_{3MON}$**

$V_{3MON}$  is a low voltage monitoring input that controls the  $\overline{RESET}$  function of an external device.

The  $V_{3MON}$  pin is monitored by a comparator to detect an undervoltage condition. It is designed with 1.5% hysteresis. When the  $V_{3MON}$  input drops below the programmed UV threshold, the comparator becomes active immediately, indicating that a UV condition has occurred. Due to hysteresis, the  $V_{3MON}$  input must be brought above the programmed UV threshold by 1.5% before the comparator becomes inactive, indicating that the UV condition has gone away (see Figure 9).

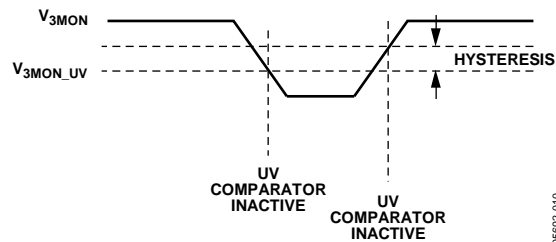


Figure 9.  $V_{3MON}$  Hysteresis

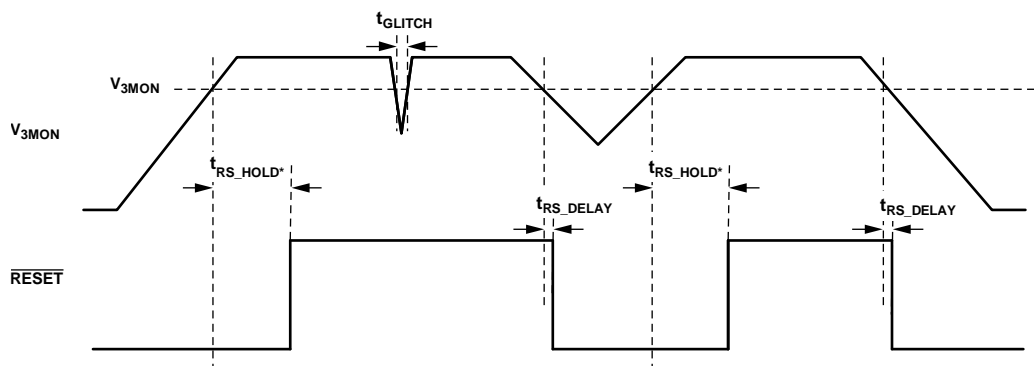
The  $V_{3MON}$  comparator is used (in conjunction with a hold timer) to control the  $\overline{RESET}$  pin.

$V_{3MON}$  monitors inputs from 2.0 V to 5.5 V. It has an 8-step programmable reset threshold (Register 0x05) with an 8-step 0.1 ms to 200 ms reset hold time ( $t_{RS\_HOLD}$ ). The reset hold time means that the  $\overline{RESET}$  output remains activate when  $V_{3MON}$  goes above its UV threshold, until  $t_{RS\_HOLD}$  has elapsed. This allows the reset of an external device to be held until the programmed time is reached.

The  $V_{3MON}$  and  $\overline{RESET}$  timing diagrams are shown in Figure 10. The range of thresholds is shown in Table 6 and the programming code for the selected threshold is found in Table 7. The range of reset hold times is shown in Table 8 and the programming code of the selected timing is found in Table 9.

$V_{3MON}$  exhibits typical input resistance of 130 k $\Omega$  that users should take into account for loading effect.

The  $\overline{MR}$  input has an internal resistor pull-up to  $V_{3MON}$ . The  $\overline{RESET}$  output is push-pull, between  $V_{3MON}$  and GND.



NOTES  
1. \* = PROGRAMMABLE

Figure 10.  $V_{3MON}$ ,  $\overline{RESET}$  Timing Diagrams

## V<sub>4MON</sub>

V<sub>4MON</sub> is a low voltage monitoring input that controls the  $\overline{\text{RESET}}$  function of an external device or provides a comparator output, V<sub>4OUT</sub>. The V<sub>4MON</sub> pin is monitored by a comparator to detect an undervoltage condition. It is designed with 5% hysteresis.

When the V<sub>4MON</sub> input drops below the programmed UV threshold, the comparator becomes active immediately, indicating that a UV condition has occurred. Due to hysteresis, the V<sub>4MON</sub> input must be brought above the programmed UV threshold by 5% before the comparator becomes inactive, indicating that the UV condition has gone away (see Figure 11).

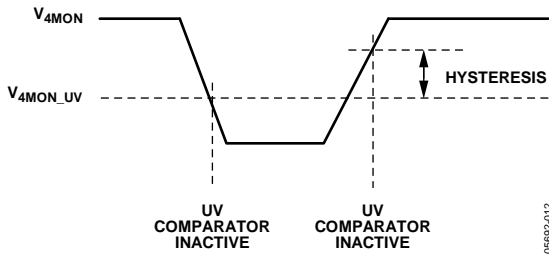


Figure 11. V<sub>4MON</sub> Hysteresis

The V<sub>4MON</sub> comparator is used to control the V<sub>4OUT</sub> pin and (in conjunction with a hold timer) to control the  $\overline{\text{RESET}}$  pin. To configure V<sub>4MON</sub> to control the  $\overline{\text{RESET}}$  pin, set Register 0x0D[3] to 0. Setting this bit to 1 prevents V<sub>4MON</sub> from causing  $\overline{\text{RESET}}$  to activate. The default setting is V<sub>4MON</sub> does not cause  $\overline{\text{RESET}}$  to activate.

V<sub>4MON</sub> input voltage range is up to 30 V. It has an 8-step programmable reset threshold (Register 0x06) from 1.67 V to 7.96 V, with an 8-step 0.1 ms to 200 ms reset hold time (t<sub>RS\_HOLD</sub>).

The V<sub>4MON</sub>,  $\overline{\text{RESET}}$ , and V<sub>4OUT</sub> timing diagrams are shown in Figure 12. The range of thresholds is shown in Table 6, and the programming code for the selected threshold is found in Table 8. The default monitoring threshold is 7.54 V. Similarly, the range of reset hold time is shown in Table 8, and the programming code of the selected timing is found in Table 9.

V<sub>4MON</sub> exhibits typical input resistance of 675 kΩ that users should take into account for loading effect.

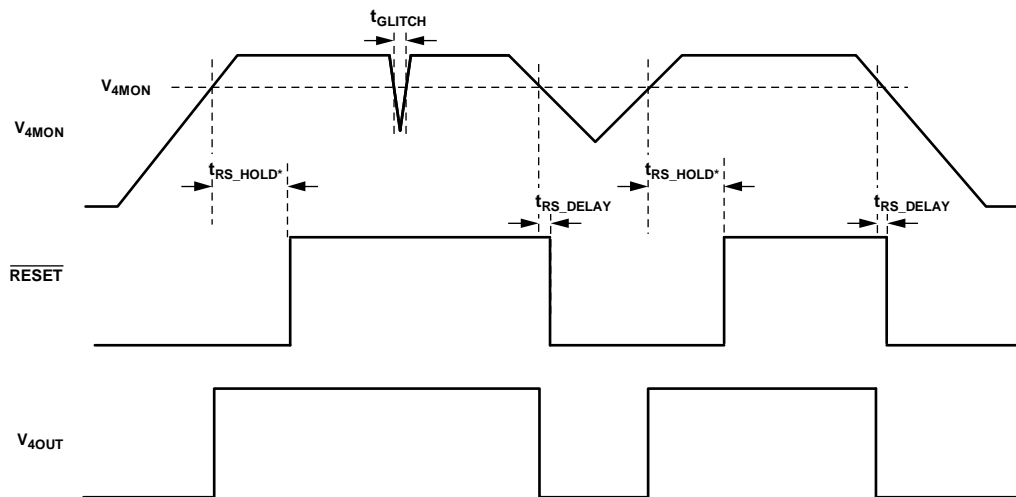
## WATCHDOG INPUT

The watchdog input (WDI) circuit attempts to reset the system to a known good state if a software or hardware glitch renders the system processor inactive for a duration that is longer than the timeout period. The timeout period, t<sub>WD</sub>, is programmable in eight steps from 100 ms to 2000 ms. The watchdog circuit is independent of any CPU clock that the watchdog is monitoring.

The range of watchdog timeout is shown in Table 8, and the programming code of the selected timeout is found in Table 9. The default timeout is 1500 ms.

The watchdog is disabled during power-up. WDI starts monitoring once  $\overline{\text{RESET}}$  is high. The AD5100 provides a standard or advanced watchdog monitoring function. Register 0x0F[3] sets the watchdog function to either standard or advanced mode. This bit can be fixed in OTP memory.

- Register 0x0F[3] = 0: standard watchdog mode (Default)
- Register 0x0F[3] = 1: advanced watchdog mode



### NOTES

1. \* = PROGRAMMABLE.
2. MOST APPLICATIONS USING V<sub>4OUT</sub> REQUIRE DISABLING OF V<sub>4MON</sub> TRIGGERED RESET.

Figure 12. V<sub>4MON</sub>,  $\overline{\text{RESET}}$ , and V<sub>4OUT</sub> Timing Diagrams



**Standard Watchdog Mode**

In the default standard watchdog mode, if WDI remains either high or low for longer than the timeout period,  $t_{WD}$ , a  $\overline{\text{RESET}}$  pulse is generated in an attempt to allow the system processor to reestablish the WDI signal. The  $\overline{\text{RESET}}$  pulses continue indefinitely until a valid watchdog signal, a rising or falling edge signal at the WDI, is received. The internal watchdog timer clears whenever a reset is asserted. The standard WDI and  $\overline{\text{RESET}}$  timing diagrams are shown in Figure 13.

**Advanced Watchdog Mode**

The AD5100 can be programmed into an advanced watchdog mode. In this mode, if WDI remains either high or low for longer than the timeout period,  $t_{WD}$ , a  $\overline{\text{RESET}}$  pulse is generated, as per standard mode. However, if the WDI input remains inactive after three such  $\overline{\text{RESET}}$  pulses, concurrent with the fourth  $\overline{\text{RESET}}$  pulse,  $\overline{\text{SHDN}}$  is also asserted.  $\overline{\text{SHDN}}$  is released after 1 second. These actions repeat indefinitely (unless action is taken by the user), if the processor is not responding. The advanced WDI and  $\overline{\text{RESET}}$  timing diagrams are shown in Figure 14.

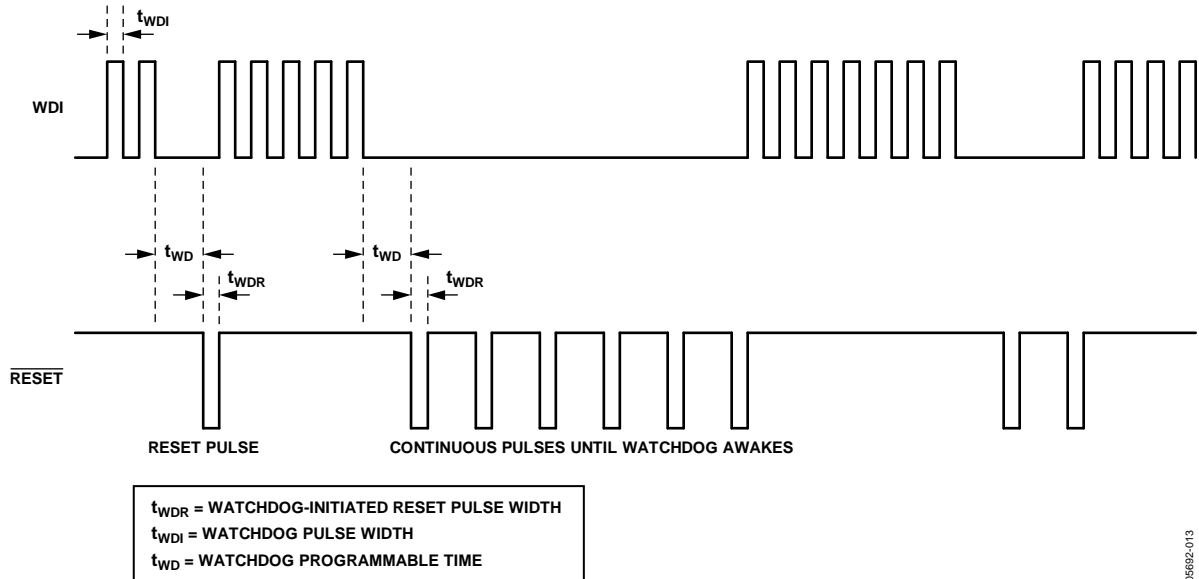


Figure 13. Standard Watchdog—Pulsing Reset Until Watchdog Awakes

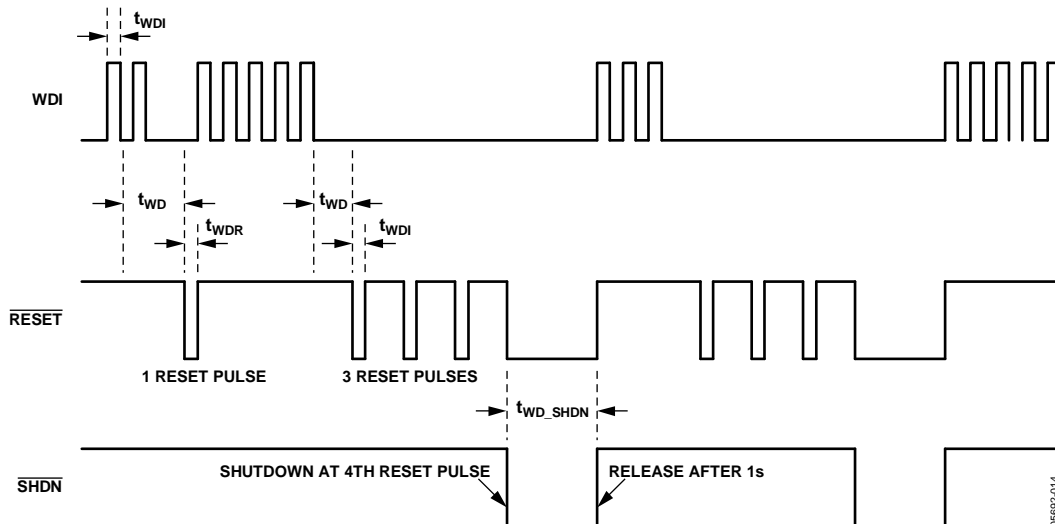


Figure 14. Advanced Watchdog— $\overline{\text{SHDN}}$  Asserted After Three Trials of Resetting the Watchdog ( $\overline{\text{SHDN}}$  Released After 1 Second and the Cycle Repeats)

## Floating WDI Input

If the WDI pin is floating, the watchdog function is disabled by default. However, floating watchdog can be enabled in the RESET configuration register such that a broken WDI connection or any unusual condition that makes WDI float triggers the reset.

- Register 0x0D[3] = 0: floating WDI input does not activate RESET (Default)
- Register 0x0D[3] = 1: floating WDI input activates RESET

This feature is fixed in OTP memory. Enabling or disabling the floating WDI feature can be changed dynamically, using the OTP overridden function is selected.

## MANUAL RESET INPUT

Manual reset ( $\overline{MR}$ ) is an active low input to the AD5100 and has an internal pull-up resistor to  $V_{3MON}$ . If the input signal on the  $\overline{MR}$  pin goes low, RESET is activated.  $\overline{MR}$  can be driven from a CMOS logic signal.

The  $\overline{MR}$  and RESET timing diagrams are shown in Figure 15. Note that RESET is activated after  $t_{MR\_DELAY}$  and is held for  $t_{RS\_HOLD}$  after the  $\overline{MR}$  signal has gone high again.

$\overline{MR}$  has the highest priority in triggering the RESET over any other monitoring inputs.

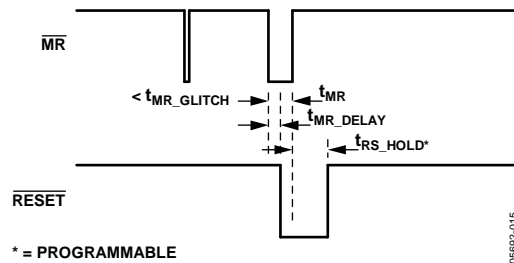


Figure 15. Manual Reset ( $\overline{MR}$ ) Timing Diagram

## OUTPUTS

### SHUTDOWN OUTPUT, $\overline{\text{SHDN}}$

The shutdown output,  $\overline{\text{SHDN}}$ , is triggered by  $V_{1\text{MON}}$  or  $V_{2\text{MON}}$  over- or underthreshold values, or as the result of a failed watchdog input.  $\overline{\text{SHDN}}$  can also be asserted low at any time by writing to certain registers on the AD5100.

The shutdown generator asserts a logic low  $\overline{\text{SHDN}}$  signal based on the following conditions:

- During power-up
- When  $V_{1\text{MON}}$  goes over or under the threshold (see Figure 7)
- When  $V_{2\text{MON}}$  is below the turn-on threshold during the rising edge or the turn-off threshold during the falling edge in level-sensitive mode (see Figure 7)
- When the external monitoring processor cannot issue the necessary WDI signal and advanced WDI mode is selected (see Figure 10 and Figure 9)
- I<sup>2</sup>C<sup>®</sup> programmed shutdown

To activate  $\overline{\text{SHDN}}$  by writing to the part, the user must first enable this feature by writing to Register 0x18[4].

- Register 0x18[4] = 0: enable software control of  $\overline{\text{SHDN}}$
- Register 0x18[4] = 1: disable software control of  $\overline{\text{SHDN}}$

Once the feature is enabled, control of  $\overline{\text{SHDN}}$  is achieved by writing to Register 0x16[2].

- Register 0x16[2] = 0:  $\overline{\text{SHDN}}$  output not controlled by software
- Register 0x16[2] = 1:  $\overline{\text{SHDN}}$  output is pulled low

The  $\overline{\text{SHDN}}$  signal is released after the programmable hold time,  $t_{\text{SD\_HOLD}}$ . The  $\overline{\text{SHDN}}$  output is push-pull configured with an I<sup>2</sup>C-selectable rail voltage of either  $V_{1\text{MON}}$  in default or internal  $V_{\text{REG}}$ . Register 0x0E[3] controls the voltage rail for  $\overline{\text{SHDN}}$ . This bit can be fixed in OTP memory.

- Register 0x0E[3] = 0:  $\overline{\text{SHDN}}$  uses  $V_{1\text{MON}}$  rail (Default)
- Register 0x0E[3] = 1:  $\overline{\text{SHDN}}$  uses  $V_{\text{REG}}$  rail

Figure 16 shows the  $\overline{\text{SHDN}}$  output configuration. Pull-down Resistor R1 ensures that  $\overline{\text{SHDN}}$  is pulled to ground when the AD5100 is not powered. When AD5100 is powered, M2a and M2b are both on. M2a has relatively lower impedance than M2b and R1 so the  $\overline{\text{SHDN}}$  remains low at shutdown. When the AD5100 settles, SW1 is turned on. M1 is stronger than M2a so  $\overline{\text{SHDN}}$  is pulled to the rail, which takes AD5100 out of the shutdown mode.

In some applications, the AD5100 may monitor and control power regulators where the input and enable pins are next to each other in a fine pitch. This may pose reliability concerns under some abnormal conditions. To prevent errors from happening, the AD5100 shutdown output features smart-load detection to ensure that the shutdown responds. For example, if the car battery has not started for a long time, a resistive dendrite may

have formed across the  $\overline{\text{SHDN}}$  pin and the battery terminal ( $V_{1\text{MON}}$ ). The dendrite is blown immediately because M2a is designed with adequate current sinking capability and remains in the on position to offer such protection. In another situation, if the  $\overline{\text{SHDN}}$  pin is hard-short-circuited to the 12 V battery, the short-circuit detector opens SW2 and limits the current by the high impedance M2b.

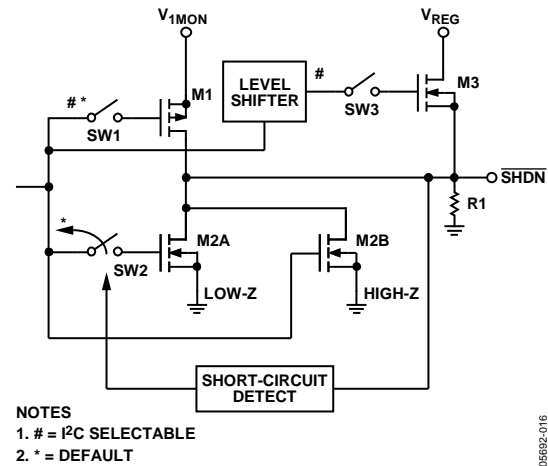


Figure 16. Shutdown Output

### RESET OUTPUT, $\overline{\text{RESET}}$

The reset output,  $\overline{\text{RESET}}$ , is triggered by  $V_{3\text{MON}}$  or  $V_{4\text{MON}}$  underthreshold values.  $\overline{\text{RESET}}$  activation can also be the result of the processor not generating the proper watchdog signal, if  $\overline{\text{MR}}$  input is triggered, or if  $\overline{\text{SHDN}}$  is activated.

The reset generator asserts the  $\overline{\text{RESET}}$  signal based on the following conditions:

- During power-up
- When  $V_{3\text{MON}}$  drops below the threshold (see Figure 10)
- When  $V_{4\text{MON}}$  drops below the threshold (see Figure 12)
- When  $\overline{\text{SHDN}}$  output is asserted (see Figure 7 and Figure 14);  $\overline{\text{RESET}}$  follows  $\overline{\text{SHDN}}$  hold and delay timings if triggered by the  $\overline{\text{SHDN}}$  output
- When the external monitoring processor cannot issue the necessary WDI signal (see Figure 13 and Figure 14)
- When  $\overline{\text{MR}}$  is asserted (see Figure 15)

$\overline{\text{RESET}}$  is active low by default, but can be configured for active high operation. Register 0x0D[1] controls the activation polarity of  $\overline{\text{RESET}}$ . It is possible to fix the value of this bit in OTP memory.

- Register 0x0D[1] = 0:  $\overline{\text{RESET}}$  is active low (Default)
- Register 0x0D[1] = 1:  $\overline{\text{RESET}}$  is active high

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The  $\overline{\text{RESET}}$  signal is asserted and maintained except when it is triggered by the  $\overline{\text{WDI}}$ , which is described in the Watchdog Input section. The  $\overline{\text{RESET}}$  signal is released after the programmable hold time,  $t_{\text{RS\_HOLD}}$ .

As shown in Figure 17, the  $\overline{\text{RESET}}$  output is push-pull configured with the rail voltage of  $V_{3\text{MON}}$ .

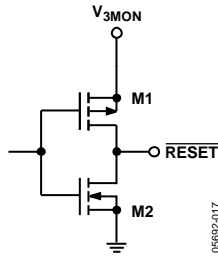


Figure 17. Reset Output

## SHUTDOWN WARNING, $\overline{\text{SHDNWARN}}$

An early shutdown warning is available for the system processor to identify the source of failure and take appropriate action before shutting down the external devices. Whenever the

voltage at  $V_{1\text{MON}}$  is detected as overvoltage or undervoltage, or the voltage at  $V_{2\text{MON}}$  falls below the threshold,  $\overline{\text{SHDNWARN}}$  outputs a Logic 0. If the processor sees a logic low on this pin, the processor may issue an I<sup>2</sup>C read command to identify the cause of failure reported in the fault detect/status register, at Address 0x19. The processor may store the information in external EEPROM as a record of failure history.

## $V_{4\text{OUT}}$ OUTPUT

$V_{4\text{OUT}}$  is an open-drain output triggered by  $V_{4\text{MON}}$  with a minimum propagation delay,  $t_{V4\text{OUT\_DELAY}}$ .  $V_{4\text{OUT}}$  can be used as a PWM control over an external device or used as a monitoring signal.

Most applications using  $V_{4\text{OUT}}$  require disabling of the  $V_{4\text{MON}}$  triggered reset function. This function is disabled by writing to Register 0x0D[2], and it is possible to fix the value of this bit in OTP memory.

Register 0x0D[2] = 0: enables  $V_{4\text{MON}}$  under threshold to activate  $\overline{\text{RESET}}$

- Register 0x0D[2] = 1: prevents  $V_{4\text{MON}}$  under threshold from activating  $\overline{\text{RESET}}$

## POWER REQUIREMENTS

### INTERNAL POWER, $V_{REG}$

The AD5100 internal power,  $V_{REG}$ , is derived from  $V_{1MON}$  and becomes active when  $V_{2MON}$  reaches 2.2 V.  $V_{2MON}$  is used to turn AD5100 on and off with a different behavior depending on the  $V_{2MON}$  monitoring mode selection.

By default, the AD5100 turns on when the voltage at  $V_{2MON}$  rises above the logic threshold,  $V_{2MON\_ON}$ . When  $V_{2MON}$  falls below the logic threshold,  $V_{2MON\_OFF}$ , AD5100 turns off 2 seconds after  $\overline{SHDN}$  is deasserted. Note that AD5100 requires 5  $\mu$ s to start up and that  $V_{1MON}$  must be applied before  $V_{2MON}$ . Extension of the AD5100 turn-off allows the system to complete any housekeeping tasks before the system is powered off. Figure 18 shows the default  $V_{2MON}$  and  $V_{REG}$  waveforms.

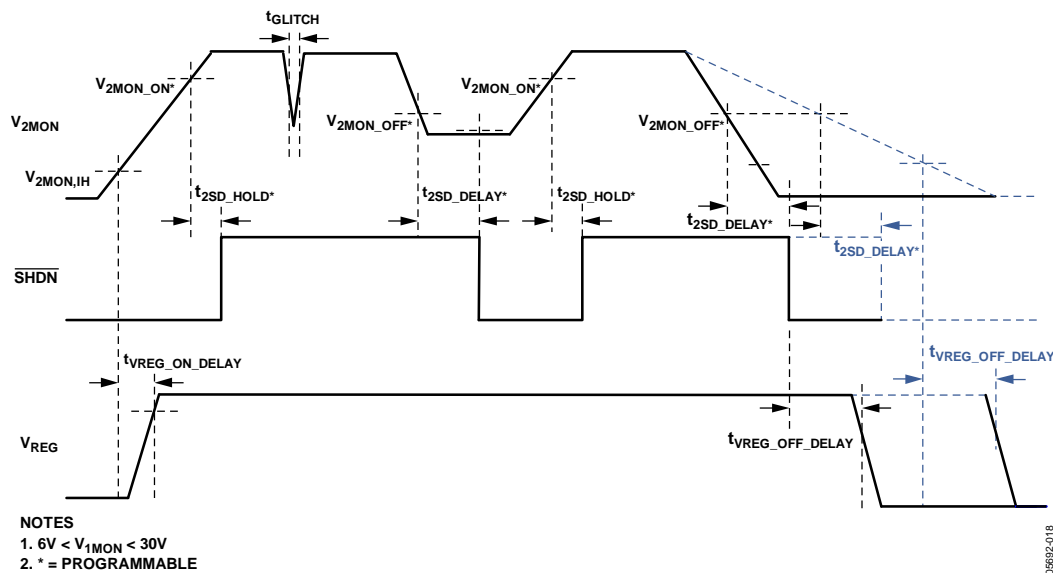


Figure 18. Internal Power  $V_{REG}$  vs.  $V_{2MON}$  Timing Diagrams (Default)

### Rising Edge Triggered Wake-Up Mode

If rising edge triggered wake-up  $V_{2MON}$  mode is selected instead, the AD5100 does not turn off when  $V_{2MON}$  returns to a logic low. To configure the part into rising edge triggered mode, set the  $V_{2MON}$  off threshold register, Register 0x04[3:1], to 1001.

In this mode, once the part is powered on, it can only be powered down by an I<sup>2</sup>C power-down instruction or by removing the supply on the  $V_{1MON}$  pin. To power down the part over the I<sup>2</sup>C bus while in rising edge triggered mode, the user must first ensure that the software power down feature is enabled.

- Register 0x18[3] = 0: enable software power-down feature
- Register 0x18[3] = 1: disable software power-down feature

The user must then write to Register 0x17[0], to actually power down the AD5100.

- Register 0x17[0] = 0: AD5100 not in software power-down
- Register 0x17[0] = 1: power down AD5100

This feature is for applications that use a wake-up signal.

## PROTECTION

For automotive applications, proper external protections on the AD5100 are needed to ensure reliable operation. The  $V_{1MON}$  is likely to be used for battery monitoring. The  $V_{2MON}$  is likely to be used for ignition switch or other critical inputs. As a result, these inputs may need additional protections such as EMI, load dump, and ESD protections. In addition, battery input requires reverse battery protection and short-circuit fuse protection (see Figure 19).

### Overcurrent Protection

If the  $V_{1MON}$  is shorted internally in the AD5100 to GND, the short-circuit protection kicks in and limits subsequent current to 150 mA in normal operation.

### Thermal Shutdown

When the AD5100 junction temperature is near the junction temperature limit, it automatically shuts down and cuts out the power from  $V_{1MON}$ . The part resumes operation when the device junction temperature returns to normal.

### ESD Protection

It is common to require a contact rating of  $\pm 8$  kV and a no contact or air rating of  $\pm 15$  kV ESD protection for the automotive electronics. As a result, an ESD-rated protection device must be used, such as MMBZ27VCL, a dual 40 W transient voltage suppressor (TVS) at the  $V_{1MON}$  and  $V_{2MON}$ .

### Load Dump Protection

A load dump is a severe overvoltage surge that occurs when the car battery is being disconnected from a spinning alternator and a resulting long duration, high voltage surge is introduced into the supply line. Therefore, external load dump protection is recommended. Typically, the load dump overvoltage lasts for a few hundred milliseconds and peaks at around 40 V to 70 V, while current can be as high as 1 A. As a result, a load dump-rated TVS D1 and D2, such as SMCJ17, are used to handle the surge energy. A series resistor is an inline current limiting resistor; it should be adequate to limit the current without significant drop and yet small enough to not affect the input monitoring accuracy.

### Reverse Battery Protection

Reverse battery protection can be provided by a regular diode if the battery monitoring accuracy can be relaxed. Otherwise, a 60 V P-channel power MOSFET, like the NDT2955, can be used. Because of the MOSFET internal diode, the battery first conducts through the P1 body diode as soon as the voltage reaches its source terminal. The voltage divider provides adequate gate-to-source voltage to turn on P1, and the voltage drop across the FET is negligible. The resistor divider values are chosen such that the maximum  $V_{GS}$  of the P1 is not violated and the current drawn through the battery is only a few microamps.

### EMI Protection

For EMI protection, a ferrite bead or EMC rated inductor, such as DR331-7-103, can be used.

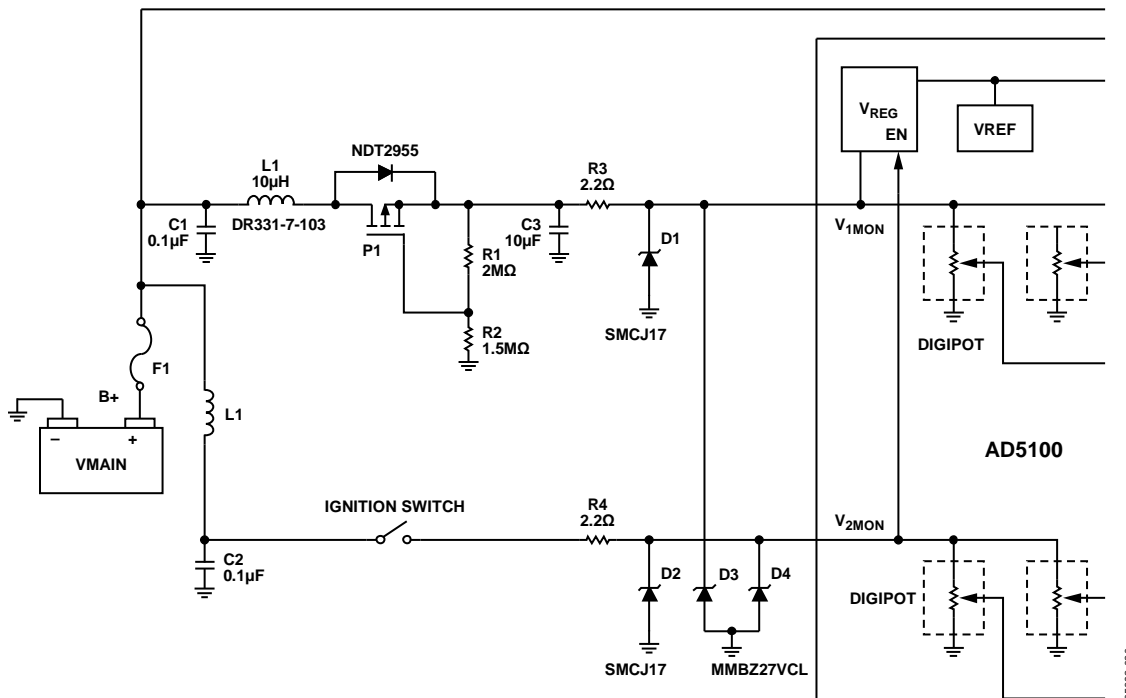


Figure 19. Protection Circuits

## AD5100 REGISTER MAP

Table 11 outlines the AD5100 register map, used to configure and control all parameters and functions in the AD5100, and indicates whether registers are writable, readable, or permanently settable. All registers have the same address for read and write operations.

The AD5100 ships from the factory with default power-up values set in OTP memory. These default values are different for each AD5100 model. However, nonprogrammed samples are available for evaluation purposes. The user can experiment with different settings in the various threshold, delay, and configuration registers.

Once evaluation is complete, the user should contact Analog Devices with their desired OTP memory default values. Analog Devices will create an AD5100 model with the desired default settings and factory program the AD5100 OTP memory with these defaults.

Some users may use the AD5100 as a set-and-forget device, that is, program some default values and never need to change these over the life of the application. However, some users may require on-the-fly flexibility, that is, the ability to change settings to values other than those they choose as their defaults. Register writing, reading, OTP, and override are explained in the I<sup>2</sup>C Serial Interface section.

**Table 11. AD5100 Register Map**

Register Address	Read/Write	Permanently Settable	Register Name and Bit Description		NonOTP Power-On Default <sup>1</sup>
0x01	R/W	Yes	V <sub>1MON</sub> Overvoltage threshold		0x00 (18.00 V)
			<b>Bit No.</b>	<b>Description</b>	
			[3:0] [7:4]	Four bits used to program V <sub>1MON</sub> OV threshold Reserved	
0x02	R/W	Yes	V <sub>1MON</sub> undervoltage threshold		0x00 (8.43 V)
			<b>Bit No.</b>	<b>Description</b>	
			[3:0] [7:4]	Four bits used to program V <sub>1MON</sub> UV threshold Reserved	
0x03	R/W	Yes	V <sub>2MON</sub> turn-on threshold		0x00 (7.47 V)
			<b>Bit No.</b>	<b>Description</b>	
			[3:0] [7:4]	Four bits used to program V <sub>2MON</sub> on threshold Reserved	
0x04	R/W	Yes	V <sub>2MON</sub> turn-off threshold		0x00 (6.95 V)
			<b>Bit No.</b>	<b>Description</b>	
			[3:0] [7:4]	Four bits used to program V <sub>2MON</sub> off threshold Reserved	
0x05	R/W	Yes	V <sub>3MON</sub> RESET Threshold		0x00 (2.93 V)
			<b>Bit No.</b>	<b>Description</b>	
			[2:0] [7:3]	Three bits used to program V <sub>3MON</sub> $\overline{\text{RESET}}$ threshold Reserved	
0x06	R/W	Yes	V <sub>4MON</sub> RESET threshold		0x00 (7.54 V)
			<b>Bit No.</b>	<b>Description</b>	
			[2:0] [7:3]	Three bits used to program V <sub>4MON</sub> $\overline{\text{RESET}}$ threshold Reserved	
0x07	R/W	Yes	V <sub>1MON</sub> OV/UV triggered $\overline{\text{SHDN}}$ hold (t <sub>1SD_HOLD</sub> )		0x00 (200 ms)
			<b>Bit No.</b>	<b>Description</b>	
			[2:0] [7:3]	Three bits used to program V <sub>1MON</sub> OV/UV triggered $\overline{\text{SHDN}}$ hold time Reserved	
0x08	R/W	Yes	V <sub>1MON</sub> OV/UV triggered $\overline{\text{SHDN}}$ delay (t <sub>1SD_DELAY</sub> )		0x00 (1200 ms)
			<b>Bit No.</b>	<b>Description</b>	
			[2:0] [7:3]	Three bits used to program V <sub>1MON</sub> OV/UV triggered $\overline{\text{SHDN}}$ delay time Reserved	

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Register Address	Read/Write	Permanently Settable	Register Name and Bit Description	NonOTP Power-On Default <sup>1</sup>	
0x09	R/W	Yes	V <sub>2MON</sub> turn-on triggered SHDN hold (t <sub>2SD_HOLD</sub> )	0x00 (10 ms)	
			<b>Bit No.</b>		<b>Description</b>
			[2:0] [7:3]		Three bits used to program V <sub>2MON</sub> t <sub>ON</sub> triggered SHDN hold time Reserved
0x0A	R/W	Yes	V <sub>2MON</sub> turn-off triggered SHDN delay (t <sub>2SD_DELAY</sub> )	0x00 (100 ms)	
			<b>Bit No.</b>		<b>Description</b>
			[2:0] [7:3]		Three bits used to program V <sub>2MON</sub> t <sub>OFF</sub> triggered SHDN delay time Reserved
0x0B	R/W	Yes	RESET hold (t <sub>RS_HOLD</sub> )	0x00 (200 ms)	
			<b>Bit No.</b>		<b>Description</b>
			[2:0] [7:3]		Three bits used to program RESET hold time Reserved
0x0C	R/W	Yes	Watchdog timeout (t <sub>WD</sub> )	0x00 (1500 ms)	
			<b>Bit No.</b>		<b>Description</b>
			[2:0] [7:3]		Three bits used to program watchdog timeout time Reserved
0x0D	R/W	Yes	RESET configuration	0x00	
			<b>Bit No.</b>		<b>Description</b>
			[0]		0: $\overline{\text{RESET}}$ is active when $\overline{\text{SHDN}}$ is active 1: $\overline{\text{RESET}}$ is not active when $\overline{\text{SHDN}}$ is active
			[1]		0: $\overline{\text{RESET}}$ active low 1: $\overline{\text{RESET}}$ active high
			[2]		0: enables V <sub>4MON</sub> under threshold, causing $\overline{\text{RESET}}$ 1: prevents V <sub>4MON</sub> under threshold from causing $\overline{\text{RESET}}$ (for V <sub>4OUT</sub> applications)
			[3] [7:4]		0: floating WDI does not activate $\overline{\text{RESET}}$ 1: floating WDI activates $\overline{\text{RESET}}$ Reserved
0x0E	R/W	Yes	SHDN rail voltage configuration	0x00	
			<b>Bit No.</b>		<b>Description</b>
			[2:0] [3]		Reserved 0: $\overline{\text{SHDN}}$ rail = V <sub>1MON</sub> 1: $\overline{\text{SHDN}}$ rail = V <sub>REG</sub>
			[7:4]		Reserved
0x0F	R/W	Yes	Watchdog mode	0x00	
			<b>Bit No.</b>		<b>Description</b>
			[2:0] [3]		Reserved 0: standard mode 1: advanced mode
			[7:4]		Reserved
0x15	R/W	Yes	Program lock (inhibit further programming)	0x00	
			<b>Bit No.</b>		<b>Description</b>
			[2:0] [3] [7:4]		Reserved Reserved Reserved



Register Address	Read/Write	Permanently Settable	Register Name and Bit Description	NonOTP Power-On Default <sup>1</sup>	
0x16	R/W	No	Special function 1	0x00	
			<b>Bit No.</b>		<b>Description</b>
			[0]		Reserved
			[1]		Reserved
			[2]		0: software assertion of $\overline{\text{SHDN}}$ pin is inactive 1: pulls $\overline{\text{SHDN}}$ pin low
[3]	0: override of permanent settings inactive 1: override of permanent settings active				
[7:4]	Reserved				
0x17	R/W	No	Special function 2	0x00	
			<b>Bit No.</b>		<b>Description</b>
			[0]		0: software power-down of AD5100 inactive 1: software power-down of AD5100 active <sup>2</sup>
			[7:1]		Reserved
0x18	R/W	No	Disable special functions <sup>3</sup>	0x00	
			<b>Bit No.</b>		<b>Description</b>
			[0]		0: allows override of any of the registers in memory except Register 0x16 Bit[2:0] and Register 0x17 Bit[0] 1: disables override of any of the registers in memory except Register 0x16 Bit[2:0] and Register 0x17 Bit[0]
			[1]		Reserved
			[2]		Reserved
			[3]		0: allows software power-down function 1: disables software power-down function
[4]	0: allows software assertion of $\overline{\text{SHDN}}$ pin 1: disables software assertion of $\overline{\text{SHDN}}$ pin				
[7:5]	Reserved				
0x19	Read-only	No	Fault detect and status (Bits[3:0] are level triggered bits that indicate the current state of the comparators monitoring the $V_{1\text{MON}}$ and $V_{2\text{MON}}$ input pins; Bits[6:4] are edge triggered fault detection bits that indicate what error conditions were present when a $\overline{\text{SHDN}}$ event occurred)	0x40	
			<b>Bit No.</b>		<b>Description</b>
			[0]		1 = $V_{2\text{MON}}$ input < $V_{2\text{MON}}$ off threshold
			[1]		1 = $V_{2\text{MON}}$ input > $V_{2\text{MON}}$ on threshold
			[2]		1 = $V_{1\text{MON}}$ input < $V_{1\text{MON}}$ UV threshold
[3]	1 = $V_{1\text{MON}}$ input > $V_{1\text{MON}}$ OV threshold				
[6:4]	000: none 001: $V_{1\text{MON}}$ UV only 010: $V_{1\text{MON}}$ OV only 011: never occurred 100: $V_{2\text{MON}}$ below off only (default) 101: $V_{1\text{MON}}$ UV and $V_{2\text{MON}}$ below off both occurred 110: $V_{1\text{MON}}$ OV and $V_{2\text{MON}}$ below off both occurred 111: never occurred				
[7]	Reserved				

<sup>1</sup> Default settings of AD5100-0 evaluation model only.

<sup>2</sup>  $V_{2\text{MON}}$  must be 0 V (that is,  $V_{2\text{MON}}$  must be configured in edge sensitive mode) for software power-down.

<sup>3</sup> These register bits are set only. To clear them, the AD5100 must be power cycled. In some cases, the AD5100 can be connected to an I<sup>2</sup>C bus with lots of activity. Setting these bits is an added means of ensuring that any erroneous activity on the bus does not cause AD5100 special functions to become active.

## I<sup>2</sup>C SERIAL INTERFACE

Control of the AD5100 is via an I<sup>2</sup>C-compatible serial bus. The AD5100 is connected to this bus as a slave device (the AD5100 has no master capabilities).

The 2-wire serial bus protocol operates as follows:

1. The master initiates data transfer by establishing a start condition, which occurs when SDA goes from high to low while SCL is high. The following byte is the slave address byte, which consists of the 7-bit slave address followed by an R/W bit that determines whether data is read from or written to the slave device
2. Data is transmitted over the serial bus in sequences of nine clock pulses (eight data bits followed by an acknowledge bit). The transitions on the SDA line must occur during the low period of SCL and remain stable during the high period of SCL.
3. When all data bits have been read or written, a stop condition is established by the master. A stop condition is defined as a low-to-high transition on the SDA line while SCL is high. In write mode, the master pulls the SDA line high during the 10<sup>th</sup> clock pulse to establish a stop condition. In the read mode, the master issues a no acknowledge for the ninth clock pulse (that is, the SDA line remains high). The master then brings the SDA line low before the 10<sup>th</sup> clock pulse and high during the 10<sup>th</sup> clock pulse to establish a stop condition.

For the AD5100, write operations contain either one or two bytes, while read operations contain one byte. The AD5100 makes use of an address pointer register. This address pointer sets up one of the other registers for the second byte of the write operation or for a subsequent read operation. Table 12 shows the structure of the address pointer register. Bits [6:0] signify the address of the register that is to be written to or read from. Bit 7 is a reserved bit and should be 0 for normal write/read operations.

**Table 12. Address Pointer Register Structure**

Bit Number	Function
7	Reserved
6	Address Bit 6
5	Address Bit 5
4	Address Bit 4
3	Address Bit 3
2	Address Bit 2
1	Address Bit 1
0	Address Bit 0 (LSB)

### SCL

The serial input register clock pin shifts in one bit at a time on positive clock edges. An external 2.2 kΩ to 10 kΩ pull-up resistor is needed. The pull-up resistor should be tied to V<sub>3MON</sub>, provided V<sub>3MON</sub> is sub-5 V.

### SDA

The serial data input/output pin shifts in one bit at a time on positive clock edges, with the MSB loaded first. An external 2.2 kΩ to 10 kΩ pull-up resistor is needed. The pull-up resistor should be tied to V<sub>3MON</sub>, provided V<sub>3MON</sub> is sub-5 V.

### AD0

The AD5100 has a 7-bit slave address. The six MSBs are 010111, and the LSB is determined by the state of the AD0 pin. When the I<sup>2</sup>C slave address pin, AD0, is low, the 7-bit AD5100 slave address is 0101110. When AD0 is high, the 7-bit AD5100 slave address is 0101111 (pulled up to 3.3 V maximum).

The AD0 pin allows the user to connect two AD5100 devices to the same I<sup>2</sup>C bus. Table 13 and Figure 20 show an example of two AD5100 devices operating on the same serial bus independently.

**Table 13. Slave Address Decoding Scheme**

AD0 Programming Bit	AD0 Device Pin	Device Addressed
0	0 V	0x2E (U1)
1	3.3 V max	0x2F (U2)

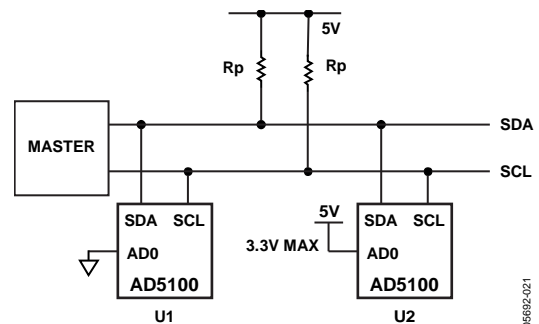


Figure 20. Two AD5100 Devices on One Bus

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## WRITING DATA TO AD5100

When writing data to the AD5100, the user begins by writing an address byte followed by the R/W bit set to 0. The AD5100 acknowledges (if the correct address byte is used) by pulling the SDA line low during the ninth clock pulse. The user then follows with two data bytes. The first data byte is the address of the internal data register to be written to, which is stored in the address pointer register. The second byte is the data to be written to the internal data register. After each byte, the AD5100 acknowledges by pulling the SDA line low during the ninth clock pulse. Figure 21 illustrates this operation.

## READING DATA FROM AD5100

When reading data from an AD5100 register, there are two possibilities.

- If the AD5100 address pointer register value is unknown or not at the desired value, it is first necessary to set it to the correct value before data can be read from the desired data register. This is done by performing a write to the AD5100, but only a value containing the register address is sent because data is not to be written to the register. This is shown in Figure 22. A read operation is then performed consisting of the serial bus address, R/W bit set to 1, followed by the data byte from the data register. This is shown in Figure 23.

- If the address pointer is known to be already at the desired address, data can be read from the corresponding data register without first writing to the address pointer register.

Table 14 shows the readback data byte structure. Bits[6:0] contain the data from the register just read. Bit 7 is a reserved bit and should be ignored for normal read operations. The majority of AD5100 registers are four bits wide, with only the fault detect and status register and disable special functions register at seven bits and five bits wide, respectively.

**Table 14. Readback Data Byte Structure**

Bit Number	Function
7	Reserved
6	D6
5	D5
4	D4
3	D3
2	D2
1	D1
0	D0 (LSB)

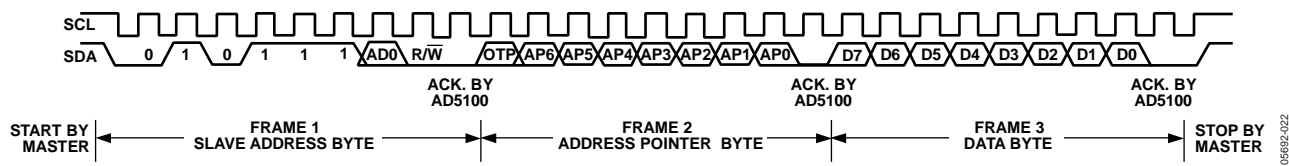


Figure 21. Writing a Register Address to the Address Pointer Register, Then Writing Data to the Selected Register

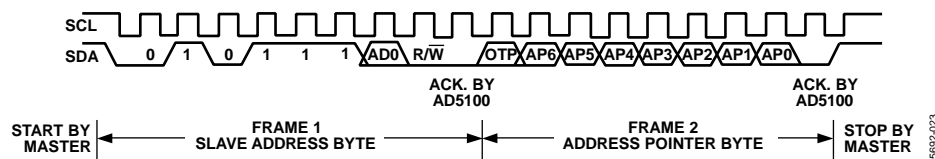


Figure 22. Dummy Write to Set Proper Address Pointer

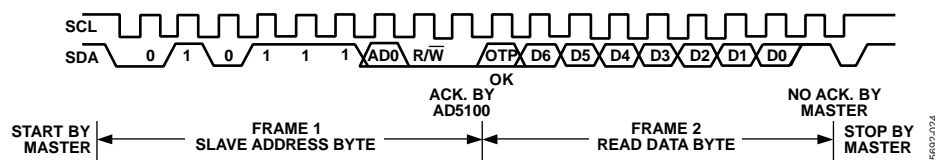


Figure 23. Read Data from the Address Pointer Register

## TEMPORARY OVERRIDE OF DEFAULT SETTINGS

Even with OTP-Programmed parts, it is possible to temporarily override the default values of any of the permanently programmable registers. To override a permanent setting in a particular register (when the lock bit is programmed), the following sequence should be used:

1. Set Bit 3 = 1 in Register 0x16 (special function 1).
2. Write the desired temporary data to the register of choice.

While the override bit (Bit 3) is set in Register 0x16, the user can override any registers by simply writing to them with new data.

To reset an overridden register to its default setting, the following sequence should be used:

1. Set Bit 3 = 0 in Register 0x16.
2. Write a dummy byte to the register of choice.

Clearing the override bit in Register 0x16 does not cause all overridden registers to revert to their defaults at the same time. For example, imagine that the user overrides Register 0x01, Register 0x02, and Register 0x03.

If the user subsequently clears the override bit in Register 0x16 and writes a dummy byte to Register 0x01, Register 0x01 reverts to its default value. However, Register 0x02 and Register 0x03 still contain their override data. To revert both registers to their default values, the user must write dummy data to each register individually.

Power cycling the AD5100 also resets all registers to their programmed defaults.

## **APPLICATIONS INFORMATION**

### **CAR BATTERY AND INFOTAINMENT SYSTEM SUPPLY MONITORING**

The AD5100 has two high voltage monitoring inputs with shutdown and reset controls over external devices. For example, the V1MON and V2MON can be used to monitor the signals from a car battery and an ignition key in an automobile, respectively (see Figure 24). The shutdown output can be connected to the

shutdown pin of an external regulator to prevent false conditions such as a weak battery or overcharging of a battery by an alternator. The reset output can be used to reset the processor in the event of a hardware or software malfunction. An example of the input and output responses of this circuit is shown in Figure 25.

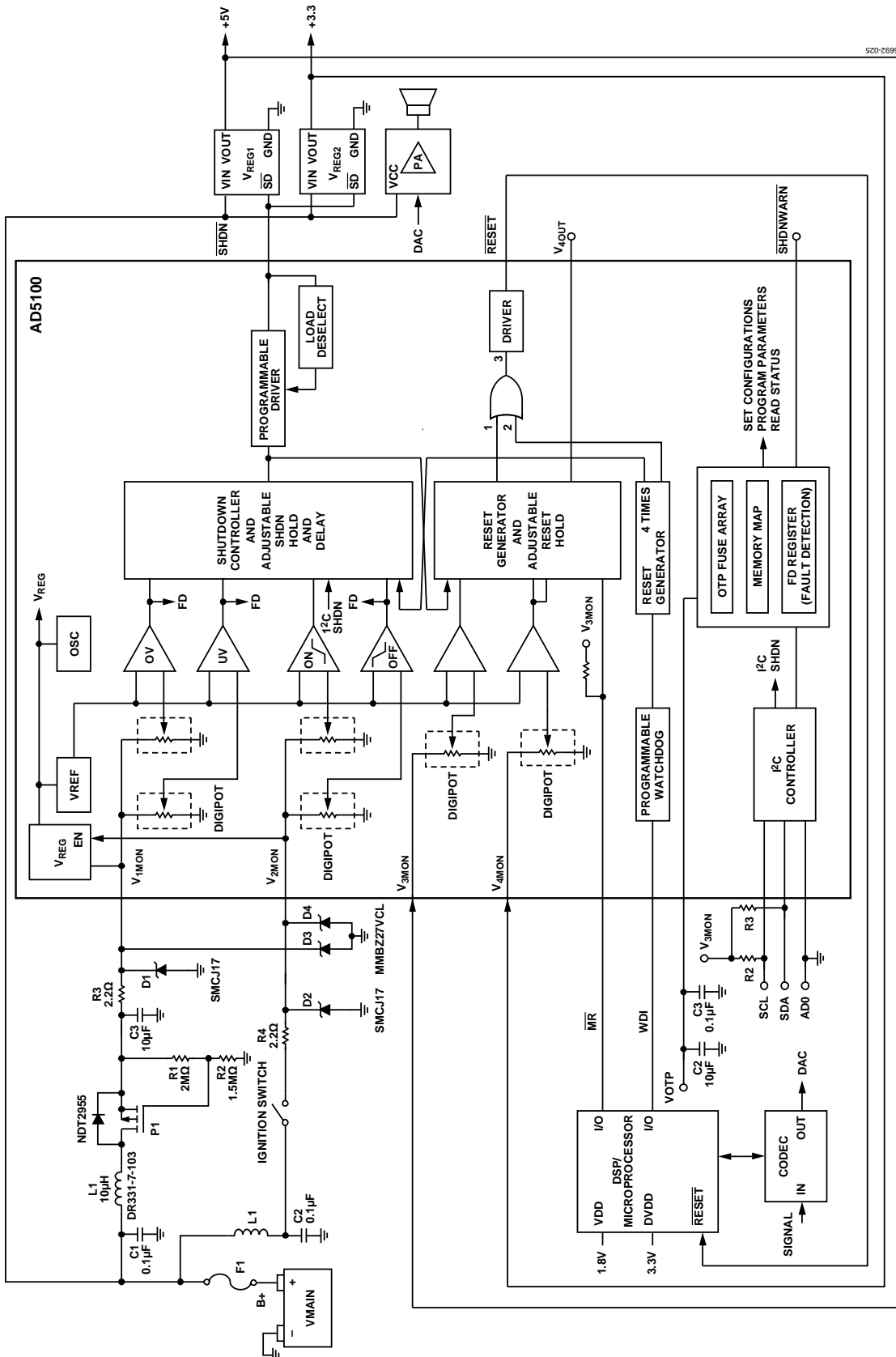


Figure 24. Typical DSP in Car Infotainment Application

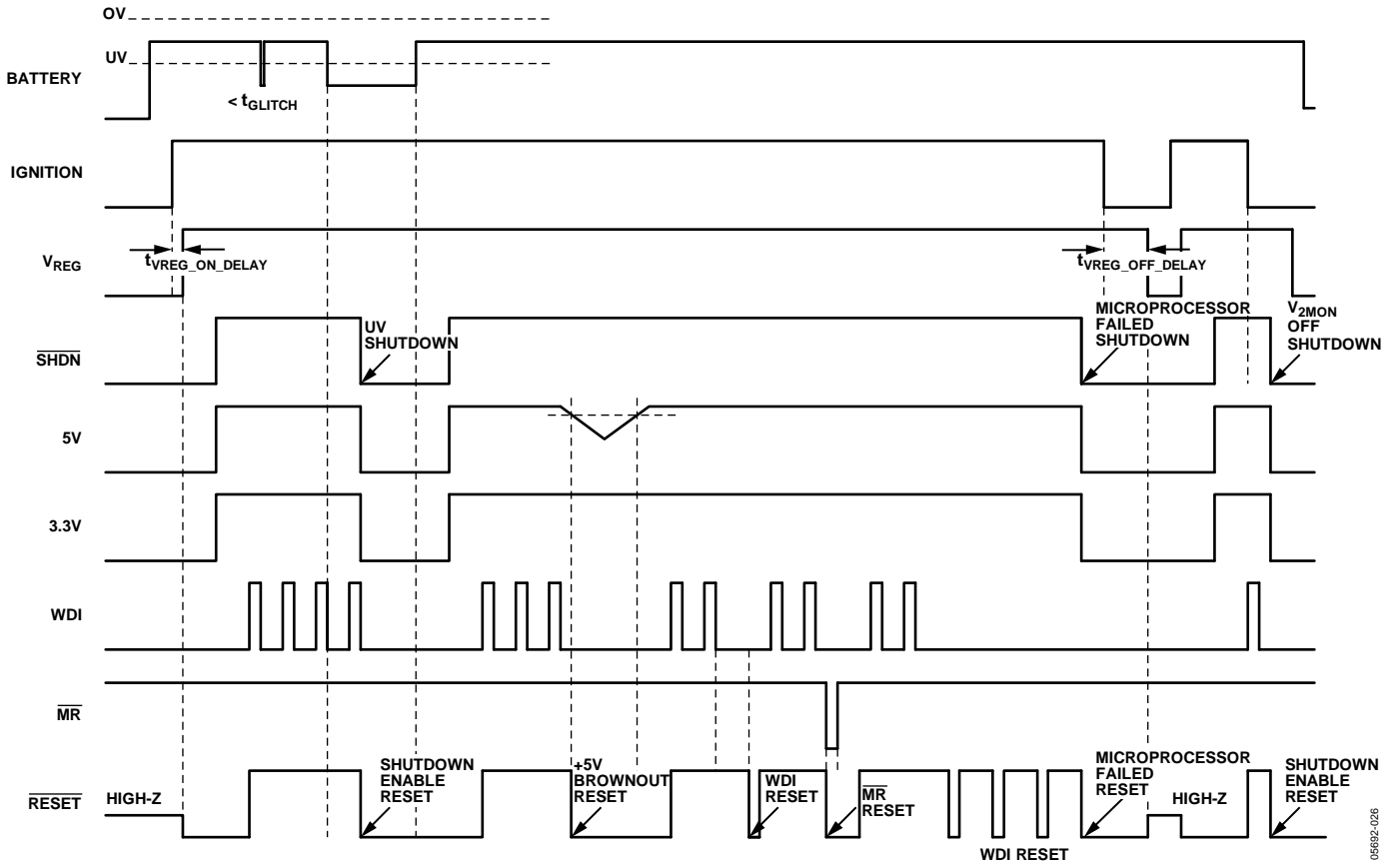


Figure 25. Example of  $\overline{SHDN}$  and  $\overline{RESET}$  Responses of Circuit Shown in Figure 24

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## BATTERY MONITORING WITH FAN CONTROL

$V_{4MON}$  can be used with  $V_{4OUT}$  in tandem to form a simple PWM control circuit. For example, as shown in Figure 26, when a temperature sensor output connects to the  $V_{4MON}$  input, with the proper threshold level set,  $V_{4OUT}$  outputs high whenever the temperature goes above the threshold. This turns on the FET switch, which activates the fan. When  $V_{TEMP}$  drops below the threshold,  $V_{4OUT}$  decreases, which turns off the fan.

## BATTERY STATE OF CHARGE INDICATOR AND SHUTDOWN EARLY WARNING MONITORING

In the automotive application, the system designer may set the battery threshold to the lowest level to allow an automobile to start at the worst-case condition. If the battery remains at the low voltage level, it is indeed a poor battery. However, there is no way to warn the driver. As a result, the system designer can use  $V_{4OUT}$  as the battery warning indicator. By stepping down the battery voltage monitored at  $V_{4MON}$ , the LED is lit, which gives a battery replacement warning. The circuit is shown in Figure 28.

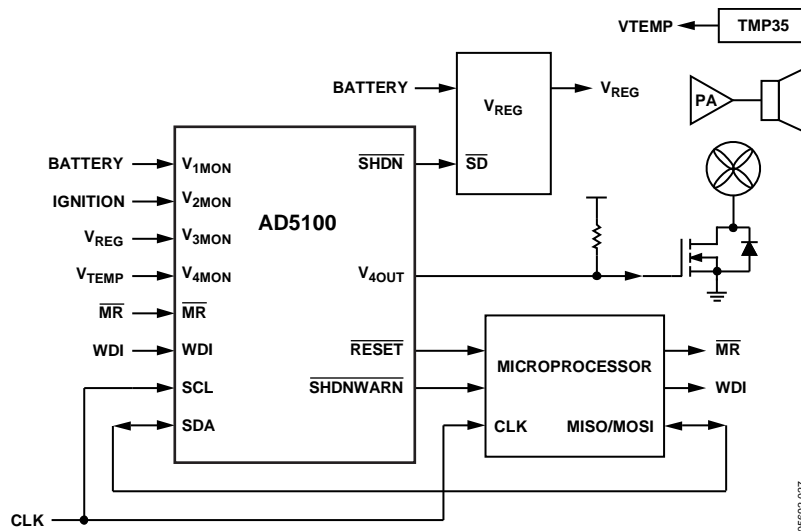
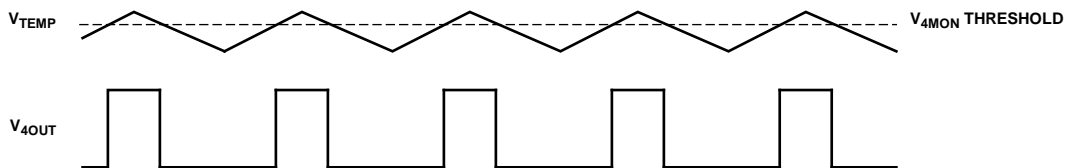


Figure 26. Power Amp Monitoring and Fan Control



- NOTES  
1.  $V_{4MON}$  RESET DISABLED.

Figure 27.  $V_{4OUT}$  with Respect to  $V_{TEMP}$ , with  $V_{4MON}$  RESET Disabled in Circuit Shown in Figure 26

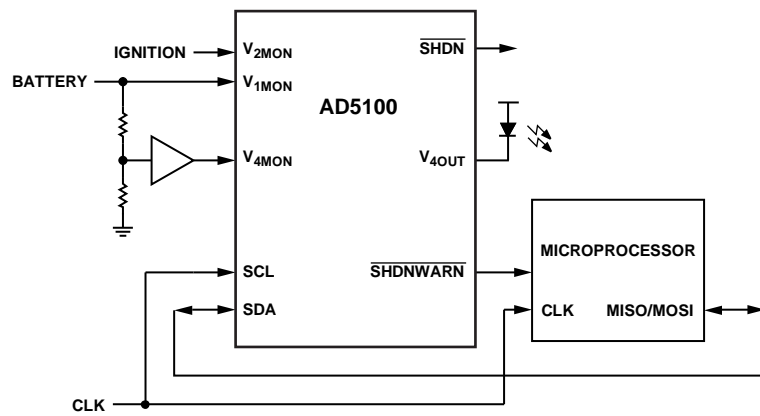


Figure 28. Battery State of Charge Indication



### RISING EDGE TRIGGERED WAKE-UP MODE

As indicated in Figure 29, the microprocessor can control its own power-down sequence using the rising edge triggered wake-up signal. The operator must select the rising edge triggered wake-up mode setting for the  $V_{2MON}$  turn-off threshold value, as shown in Table 6, by setting Register  $0x04[3:1] = 1001$ .

When the rising edge wake-up signal is detected by  $V_{2MON}$ , the AD5100 is powered up with the  $\overline{SHDN}$  pin pulled high. The external regulator is turned on to supply power to the microprocessor. A reset pulse train is generated at the reset

output if there is no watchdog activity. The pulse continues until the correct watchdog signal appears at the AD5100 WDI pin. The shutdown pin remains high as long as the AD5100 continues to receive the correct watchdog signal.

When the microprocessor finishes its housekeeping tasks or powers down the software routine, it stops sending a watchdog signal. In response, the AD5100 generates a reset. The shutdown pin is pulled low 2 seconds after, and the regulator output drops to 0 V, which shuts down the microprocessor. At that point, the AD5100 enters sleep mode.

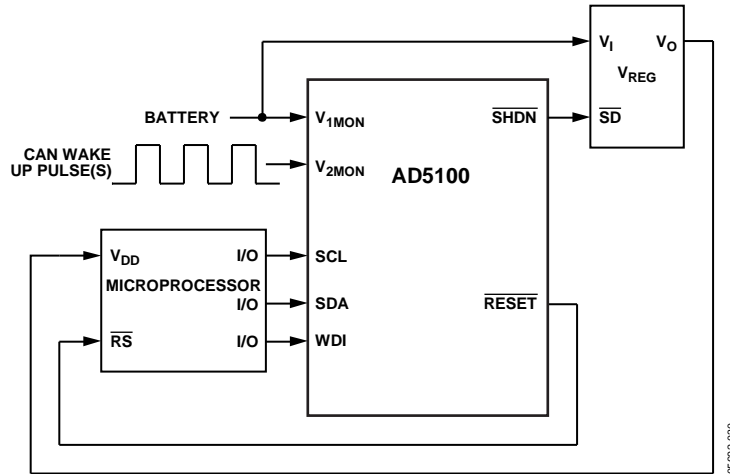
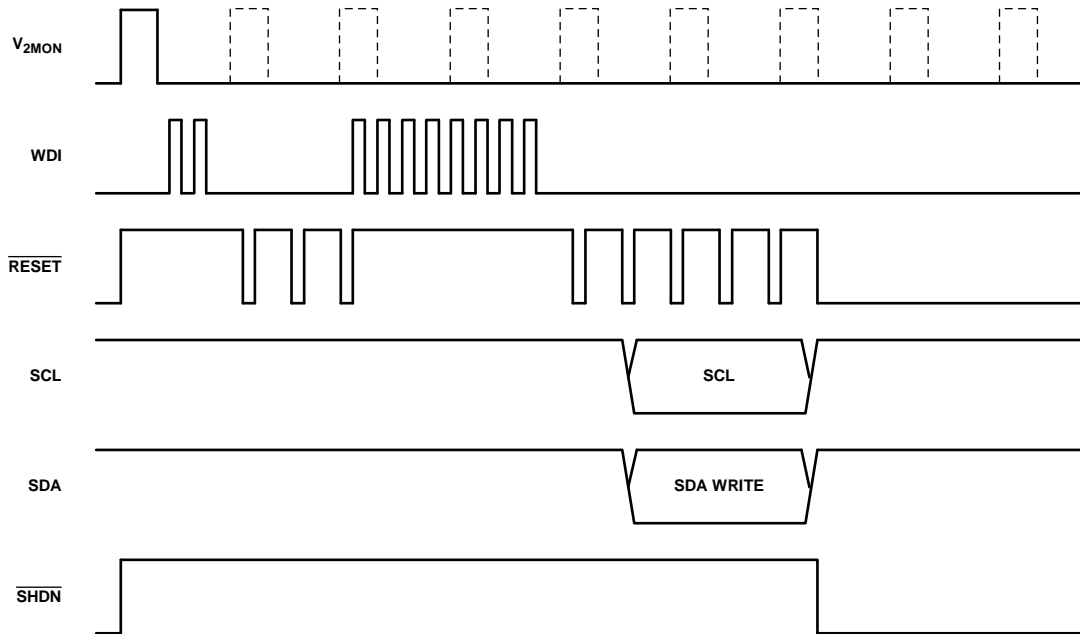


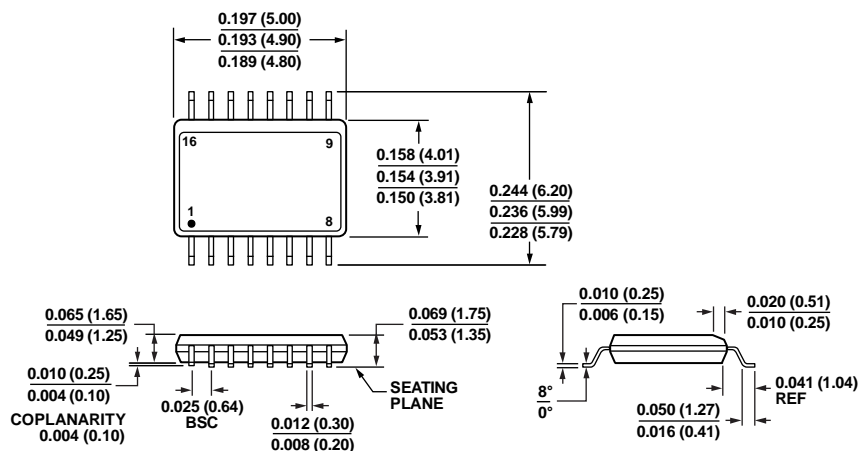
Figure 29. Rising Edge Triggered Wake-Up Mode



- NOTES
1.  $6V < V_{1MON} < 30V$ .
  2. SELECT  $V_{2MON\_OFF}$  = RISING EDGE TRIGGER/CAN WAKE UP MODE.

Figure 30. Rising Edge Triggered Operation of Circuit Shown in Figure 29

## OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-137-AB  
 CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETERS DIMENSIONS  
 (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR  
 REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 31. 16-Lead Shrink Small Outline Package [QSOP]  
 (RQ-16)

Dimensions shown in inches

012808-A

## ORDERING GUIDE

Model <sup>1,2</sup>	Temperature Range	Package Description	Package Option	Ordering Quantity
AD5100YRQZ-0	-40°C to +125°C	16-Lead QSOP	RQ-16	
AD5100YRQZ-1RL7	-40°C to +125°C	16-Lead QSOP	RQ-16	1,000
AD5100YRQZ-1REEL	-40°C to +125°C	16-Lead QSOP	RQ-16	2,500
EVAL-AD5100EBZ		Evaluation Board		

<sup>1</sup> Z = RoHS Compliant Part.

<sup>2</sup> AD5100YRQZ-0 = Non-OTP programmed part, intended for evaluation purposes only.

## AUTOMOTIVE PRODUCTS

The AD5100 models are available with controlled manufacturing to support the quality and reliability requirements of automotive applications. Note that these automotive models may have specifications that differ from the commercial models; therefore, designers should review the Specifications section of this data sheet carefully. Only the automotive grade products shown are available for use in automotive applications. Contact your local Analog Devices account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for these models.

**NOTES**

I<sup>2</sup>C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).

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