# D1U54-D-650-12-HBxC Series

## 54mm 1U Front End DC-DC Power Supply Converter

## PRODUCT OVERVIEW

The D1U54-D-650-12-HBxC products are very high efficiency DC input 650 watt front end supplies provided with a 12V main and a 12V Standby output. An active (analogue) current share characteristic is provided to allow units to be operated in parallel. The power supply may be hot plugged; recovers from overtemperature faults, and has status LEDs on the front panel in addition to hardware signal logic and PMBus™ status signals. The low profile 1U package and 21.4W/cubic inch power density make them ideal for delivering reliable, efficient power to networking equipment, workstations, storage systems and other 12V distributed power architectures.

**ORDERING GUIDE**

| Part Number | Murata Internal Part Number | Power Output -44 to -72Vdc | Main Output | Standby Output | Airflow |
|---|---|---|---|---|---|
| D1U54-D-650-12-HB3C | M1879 | 650W | 12Vdc | 12Vdc | Front to Back |
| D1U54-D-650-12-HB4C | M1878 | | | | Back to front |

## FEATURES

- 650W output power
- 93% efficiency at 50% load
- 12V main output
- 12V standby output
- 1U height:
- 2.15" x 9.00" x 1.57"
- 54.5mm x 228.6mm x 40mm
- 21.4 Watts per cubic inch density
- N+1 redundancy capable, including hot plugging
- Active (analogue) current sharing on 12V main output; ORing FET
- Overvoltage, Overcurrent, Overtemperature protection
- Internal cooling fan (variable speed)
- PMBus™/I2C interface with status indicators
- RoHS compliant
- Two Year Warranty


**Available now at: www.murata-ps.com/en/3d/acdc.html**

**INPUT CHARACTERISTICS**

| Parameter | Conditions | Min. | Nom. | Max. | Units |
|---|---|---|---|---|---|
| Input Source Voltage Operating Range | | -44 | -53 | -72 | Vdc |
| Turn-on Input Voltage | Ramp up | -42.5 | -43 | -43.5 | Vdc |
| Turn-off Input Voltage | Ramp down | -37.5 | -38 | -39.5 | |
| Input current at Vin = -53Vdc | 650W | | 13.6 | | Adc |
| Inrush Current | Cold start (25°C) between 0 to 200ms | | | 25 | Apk |
| Efficiency (-53Vdc) excluding fan load | 20% load | 90 | | | % |
| | 50% load | 93 | | | |
| | 100% load | 92 | | | |

**OUTPUT VOLTAGE CHARACTERISTICS**

| Nominal Output Voltage | Parameter | Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| 12V | Output Set Point Accuracy | 50% load; Tamb =25°C | 11.96 | 12.00 | 12.04 | Vdc |
| | Line and Load Regulation | Setpoint; temperature; line and load | -1.0% | | +1.0 % | % |
| | Ripple Voltage & Noise[1, 2] | 20MHz Bandwidth | | | 120 | mV p-p |
| | Output Current Range | | 0 | | 54.2 | A |
| | Load Capacitance | | 500 | | 4000 | µF |
| 12VSB | Output Set Point Accuracy | 50% load; Tamb = 25°C | 11.96 | 12.00 | 12.04 | Vdc |
| | Line and Load Regulation | Setpoint; temperature; line and load | 11.7 | | 12.3 | |
| | Ripple Voltage & Noise[1] | 20MHz Bandwidth | | | 120 | mV p-p |
| | Output Current | | 0 | | 2 | A |

[1] Ripple and noise is measured with a parallel combination 0.1µF of ceramic and 10µF of tantalum capacitance on each measurement node.

[2] Measurements assume the use of the minimum load capacitance as specified for the main 12V output and a minimum load of 5%. Below 5% loading the overall voltage deviation shall be within ±2.5%.

For full details go to www.murata-ps.com/rohs

Test Certificate and Test Report

## OUTPUT CHARACTERISTICS

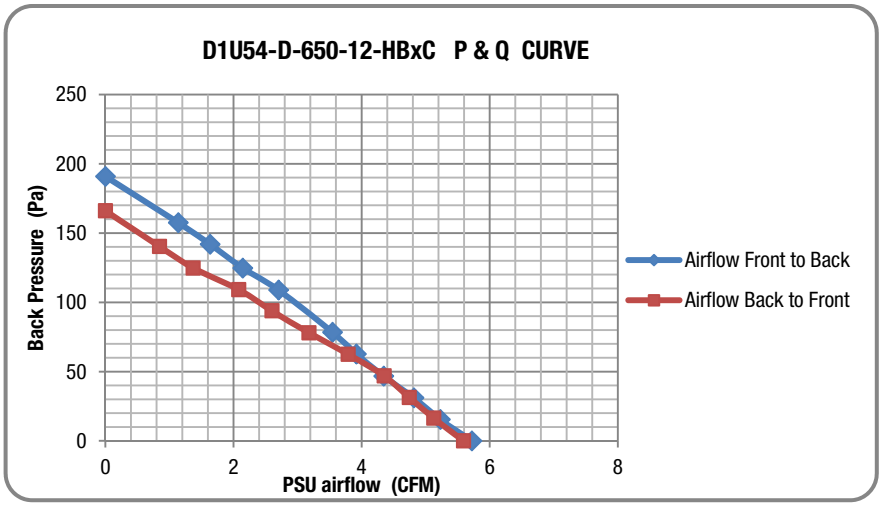
| Parameter | Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| Startup Time | DC ramp up | | | 3 | s |
| Transient Response | Main 12V, 50% load step, 1A/µs di/dt | | | ±5 | % |
| | 12VSB, 50% load step, 1A/µs di/dt | | | 500 | µs |
| Current sharing accuracy | >10% load; *of maximum output current capability | | | ±5* | % |
| Hot Swap Transients | All outputs remain in regulation | | | ± | % |
| Holdup Time (Total Effective Hold Up - See Timing Waveforms) | Full DC Input Source Range; 100% load | 2 | | 4 | ms |

## ENVIRONMENTAL CHARACTERISTICS

| Parameter | Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| Storage Temperature Range | | -40 | | 70 | °C |
| Operating Temperature Range | | -5 | | 50 | |
| Operating Humidity | Noncondensing; +45°C | 5 | | 90 | % |
| Storage Humidity | | 5 | | 95 | |
| Altitude (without derating at 40°C) | | | | 3000 | m |
| Shock | 30G non-operating | | | | |
| Operational Vibration | Sine sweep; 5-200Hz, 2G;<br>random vibration, 5-500Hz, 1.11G | | | | |
| MTBF(Target) | Per Telcordia SR-332 Issue 3 M1C3 @40°C | | 619K | | hrs |
| Safety Approvals | CAN/CSA C22.2 No 60950-1-07, Am.1:2011<br>UL 60950-1-2011, 2nd Ed.<br>IEC60950-1:2005 (2nd Ed.) w A1:2009<br>EN 60950-1:2006+A11+A1+A12+A2<br>CCC GB4943.1-2011; GB9254-1-2008; GB17625, 1-2012 | | | | |
| Input Fuse | Power Supply has an internal 25A/100Vdc fast blow fuse in the DC input negative line. | | | | |
| Weight | 1.74 lbs (0.789 kg) | | | | |

## AIRFLOW; PRESSURE VS. FLOW (PQ) CURVES

D1U54-D-650-12-HB3C & D1U54-D-650-12-HB4C




Notes:
1. The above curves represent performance based upon a the use of a 20mm thickness fan.
2. Curves recorded at room ambient (circa 25°C).
3. Curves generated with internal fan running at 100% duty cycle

## PROTECTION CHARACTERISTICS

| Output | Parameter | Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| | Overtemperature | Autorestart with 4°C hysteresis for recovery (warning issued at 70°C) | | 75 | | °C |
| 12V | Overvoltage | Latching | 13 | | 14.5 | °C |
| | Overcurrent (Target) | The output shall shutdown when an overcurrent condition is detected.<br>It will auto restart after 1sec; however if the overcurrent condition is redetected the output will once again shutdown.<br>The output will once again re-start, however if the overcurrent condition persists it will latch of after the fifth unsuccessful attempt.<br>To reset the latch it will be necessary to toggle the PS_ON_L signal (B4) or recycle the incoming DC source. | 60 | | 70 | A |
| 12VSB | Overvoltage | Latching | 13.0 | | 14.5 | V |
| | Overcurrent | The output shall shutdown when an overcurrent is detected.<br>It will auto restart after 2sec; however if the overcurrent is re-detected the output will once again shutdown.<br>This cycle will occur indefinitely while the overcurrent condition persists. | 2.2 | | 2.8 | A |

## ISOLATION CHARACTERISTICS

| Parameter | Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| Insulation Safety Rating | Input to Output | 1000 | | | Vdc |
| | Input to Chassis | 1000 | | | Vdc |
| Isolation | Output to Chassis | 500 | | | Vdc |

## EMISSIONS AND IMMUNITY

| | | |
|---|---|---|
| Conducted Emissions | FCC 47 CFR Part 15/CISPR 22/EN55022 | Class A with 6dB margin |
| ESD Immunity | IEC/EN 61000-4-2 | Level 4 criteria A |
| Radiated Field Immunity | IEC/EN 61000-4-3 | Level 3 criteria B |
| Electrical Fast Transients/Burst Immunity | IEC/EN 61000-4-4 | Level 3 criteria B |
| Surge Immunity | IEC/EN 61000-4-5 | ±1kV common mode and differential mode, unit passes criteria A (normal performance)* |
| RF Conducted Immunity | IEC/EN 61000-4-6 | Level 3 criteria A |
| Magnetic Field Immunity | IEC/EN 61000-4-8 | 3 A/m criteria B |
| Voltage Dips, Interruptions | ---- | -53Vin, 80% load, Dip 100% Duration 4ms,Criteria (A) |

* Impedance is 2 ohms for differential and common mode.

## STATUS INDICATORS

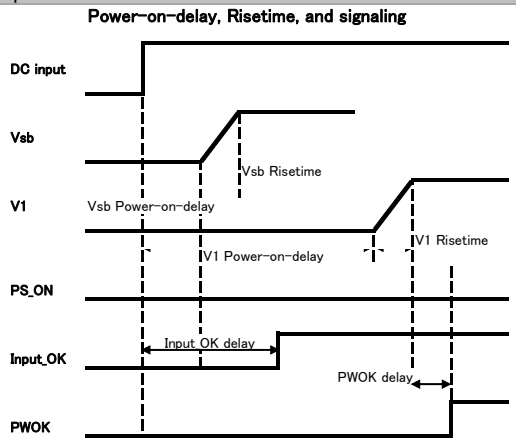
| LED NAME | LED MODE | LED STATE/OPERATION | DESCRIPTION |
|---|---|---|---|
| Input | OK | Solid Green | Input voltage operating within normal specified range |
| Input | OV/UV WARNING | Blinking Green | Input voltage operating in:<br>1) overvoltage warning, or<br>2) undervoltage warning range |
| Input | OFF OR FAULT | Off | Input voltage operating:<br>1) above overvoltage range, or<br>2) below undervoltage range, or<br>3) not present |
| | | | |
| Output | POWER GOOD | Solid Green | Main output and standby output enabled with no power supply warning or fault detected |
| Output | STANDBY | Blinking Green | Standby output enabled with no power supply warning or fault detected |
| Output | WARNING | Blinking Amber | Power supply warning detected as per PMBus STATUS_X reporting bytes• |
| Output | FAULT | Solid Amber | Power supply fault detected as per PMBus STATUS_X reporting bytes• |

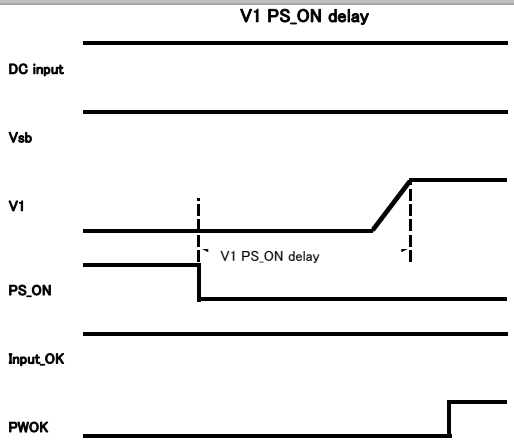
•LED fault/warning operation follows PMBus fault/warning reporting status flags and will thus also be 'sticky' (i.e. even if actual fault/warning is cleared, LED will still be in FAULT or WARNING mode until PMBus status flags are cleared with the CLEAR_FAULTS command

| STATUS AND CONTROL SIGNALS | | | |
|---|---|---|---|
| Signal Name | I/O | Description | Interface Details |
| INPUT_OK (DC Source) | Output | The signal output is driven high when the input source is available and within acceptable limits. The output is driven low to indicate loss of input power. There is a minimum of 5ms pre-warning time before signal changes to a high impedance state or is driven low to indicate loss of 12V. The power supply must ensure that this interface signal provides accurate status when DC power is lost. | Pulled up internally via 10K to 3.3Vdc. A logic high >2.0Vdc; A logic low <0.8Vdc Driven low by internal CMOS buffer (open drain output). |
| PW_OK (Output OK) | Output | The signal is asserted, driven high, by the power supply to indicate that all outputs are valid. If any of the outputs fail then this output will be hi-Z or driven low. The output is driven low to indicate that the Main output is outside of lower limit of regulation. | Pulled up internally via 10K to 3.3Vdc. A logic high >2.0Vdc; A logic low <0.8Vdc Driven low by internal CMOS buffer (open drain output). |
| SMB_ALERT (FAULT/WARNING) | Output | The signal output is driven low to indicate that the power supply has detected a warning or fault and is intended to alert the system. This output must be driven high when the power is operating correctly (within specified limits). The signal will revert to a high level when the warning/fault stimulus (that caused the alert) is removed. | Pulled up internally via 10K to 3.3Vdc. A logic high >2.0Vdc;A logic low <0.8Vdc Driven low by internal CMOS buffer (open drain output). |
| PRESENT_L (Power Supply Absent) | Output | The signal is used to detect the presence (installed) of a PSU by the host system. The signal is connected to PSU logic SGND within the power module. | Passive connection to +VSB_Return. A logic low <0.8Vdc |
| PS_ON (Power Supply Enable/Disable | Input | This signal is pulled up internally to the internal housekeeping supply (within the power supply). The power supply main 12Vdc output will be enabled when this signal is pulled low to +VSB_Return. In the low state the signal input shall not source more than 1mA of current. The 12Vdc output will be disabled when the input is driven higher than 2.4V, or open circuited. Cycling this signal shall clear latched fault conditions. | Pulled up internally via 10K to 3.3Vdc. A logic high >2.0Vdc A logic low <0.8Vdc Input is via CMOS Schmitt trigger buffer. |
| PS_KILL | Input | This signal is used during hot swap to disable the main output during hot swap extraction. The input is pulled up internally to the internal housekeeping supply (within the power supply). The signal is provided on a short (lagging pin) and should be connected to +VSB_Return. | Pulled up internally via 10K to 3.3Vdc. A logic high >2.0Vdc; A logic low <0.8Vdc Input is via CMOS Schmitt trigger buffer. |
| ADDR (Address Select) | Input | An analogue input that is used to set the address of the internal slave devices (EEPROM and microprocessor) used for digital communications. Connection of a suitable resistor to +VSB_Return, in conjunction with an internal resistor divider chain, will configure the required address (see ADDR Address Selection table). | DC voltage between the limits of 0 and +3.3Vdc. |
| SCL (Serial Clock) | Both | A serial clock line compatible with PMBus™ Power Systems Management Protocol Part 1 – General Requirements Rev 1.1. No additional internal capacitance is added that would affect the speed of the bus. The signal is provided with a series isolator device to disconnect the internal power supply bus in the event that the power module is completely unpowered, | $V_{IL}$ is 0.8V maximum $V_{OL}$ is 0.4V maximum when sinking 3mA $V_{IH}$ is 2.1V minimum |
| SDA (Serial Data) | Both | A serial data line compatible with PMBus™ Power Systems Management Protocol Part 1 – General Requirements Rev 1.1. The signal is provided with a series isolator device to disconnect the internal power supply bus in the event that the power module is completely unpowered, | $V_{IL}$ is 0.8V maximum $V_{OL}$ is 0.4V maximum when sinking 3mA $V_{IH}$ is 2.1V minimum |
| V1_SENSE V1SENSE_RTN | Input | Remote sense connections intended to be connected at and sense the voltage at the point of load. The voltage sense will interact with the internal module regulation loop to compensate for voltage drops due to connection resistance between the output connector and the load. If remote sense compensation is not required then the voltage shall be configured for local sense by:<br>1. V1_SENSE directly connected to power blades 6 to 10 (inclusive)<br>2. V1_SENSE_RTN directly connected to power blades 1 to 5 (inclusive) | Compensation for up to 0.12Vdc total connection drop (output and return connections). |
| ISHARE | Bi-Directional Analogue Bus | The current sharing signal is connected between sharing units (forming an ISHARE bus). It is an input and/or an output (bi-directional analogue bus) as the voltage on the line controls the current share between sharing units. A power supply will respond to a change in this voltage but a power supply can also change the voltage depending on the load drawn from it. On a single unit the voltage on the pin (and the common ISHARE bus would read 8VDC at 100% load (module capability). For two identical units sharing the same 100% load this would read 4VDC for perfect current sharing (i.e. 50% module load capability per unit). | Analogue voltage: +8V maximum; 10K to +12V_RTN |

## TIMING SPECIFICATIONS

### Turn-On Delay & Output Rise Time:



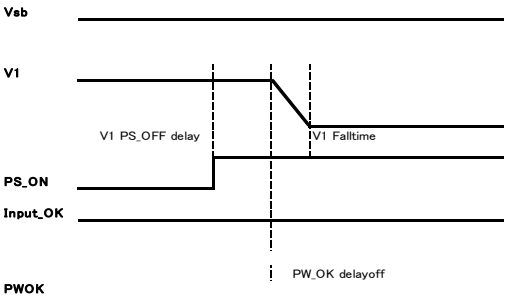




1. The turn-on delay after application of AC input within the operating range shall as defined in the following tables.
2. The output rise times shall be measured from 10% of the nominal output to the lower limit of the regulation band as defined in the following tables.

| Time | Min | Max |
|---|---|---|
| Vsb Rise time | 70ms | 170ms |
| V1 Rise time | 120ms | 220ms |
| Vsb Power-on-delay | 300ms | 700ms |
| V1 Power-on-delay | 500ms | 1500ms |
| V1 PS_ON delay | 100ms | 300ms |
| V1 PWOK delay | 300ms | 450ms |
| DCOK (Input) detect | 500ms | 1000ms |

## TIMING SPECIFICATIONS

### Turn-Off (Shutdown by PS_ON)




| Turn-Off Timing | Min | Max | Notes |
|---|---|---|---|
| V1 Fall time | - | - | Must be monotonic |
| V1 PS_OFF delay | 0ms | 6ms | |
| PW_OK delay off | 2.0ms | | |

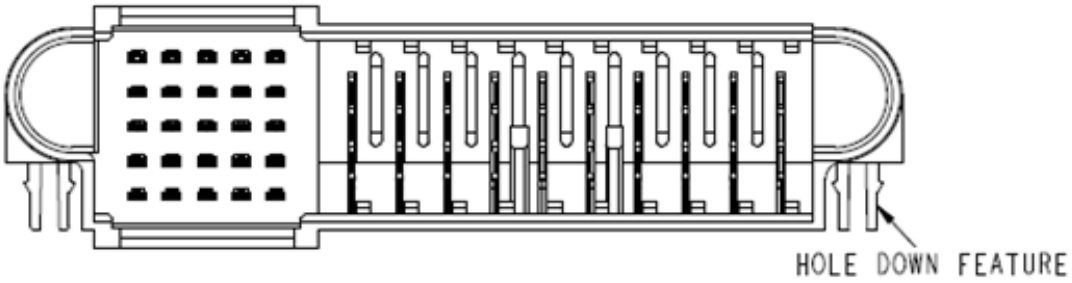
1. Note this characteristic is applicable for the main 12Vdc output shutdown from PS_ON pulled high.

## TIMING SPECIFICATIONS

### Power Removal Holdup

| Power Removal Timing | Min | Max | Notes |
|---|---|---|---|
| Vsb holdup | 20ms | 50ms | +VSB Full Load |
| V1 holdup (Total Effective) | 4ms | - | 100% load |
| DC (Input) fail detect | 400µs | 1000µs | |
| PWOK delay off | 2.0ms | | 100% load |
| PWOK Hold Up | 2.0ms | 4.0ms | |

## OUTPUT CONNECTOR & SIGNAL INTERFACE; FCI PN 10122460-005LF




| PART NUMBER | ROWS | | SIGNALS | | | | | POWERS | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 1 | 2 | 3 | 4 | 5 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | |
| 10122460-005LF 25S + 10P | E | H | 2 | 2 | 2 | 2 | 3 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | H |
| | D | | | | | | | | | | | | | | | | | |
| | C | | | | | | | | | | | | | | | | | |
| | B | | | | | | | | | | | | | | | | | |
| | A | | | | | | | | | | | | | | | | | |

NB: Reference to “3” in Column 5, refers to the shortest level signal pin; the “shortest” pins are the “last to make, first to break” in the mating sequence.

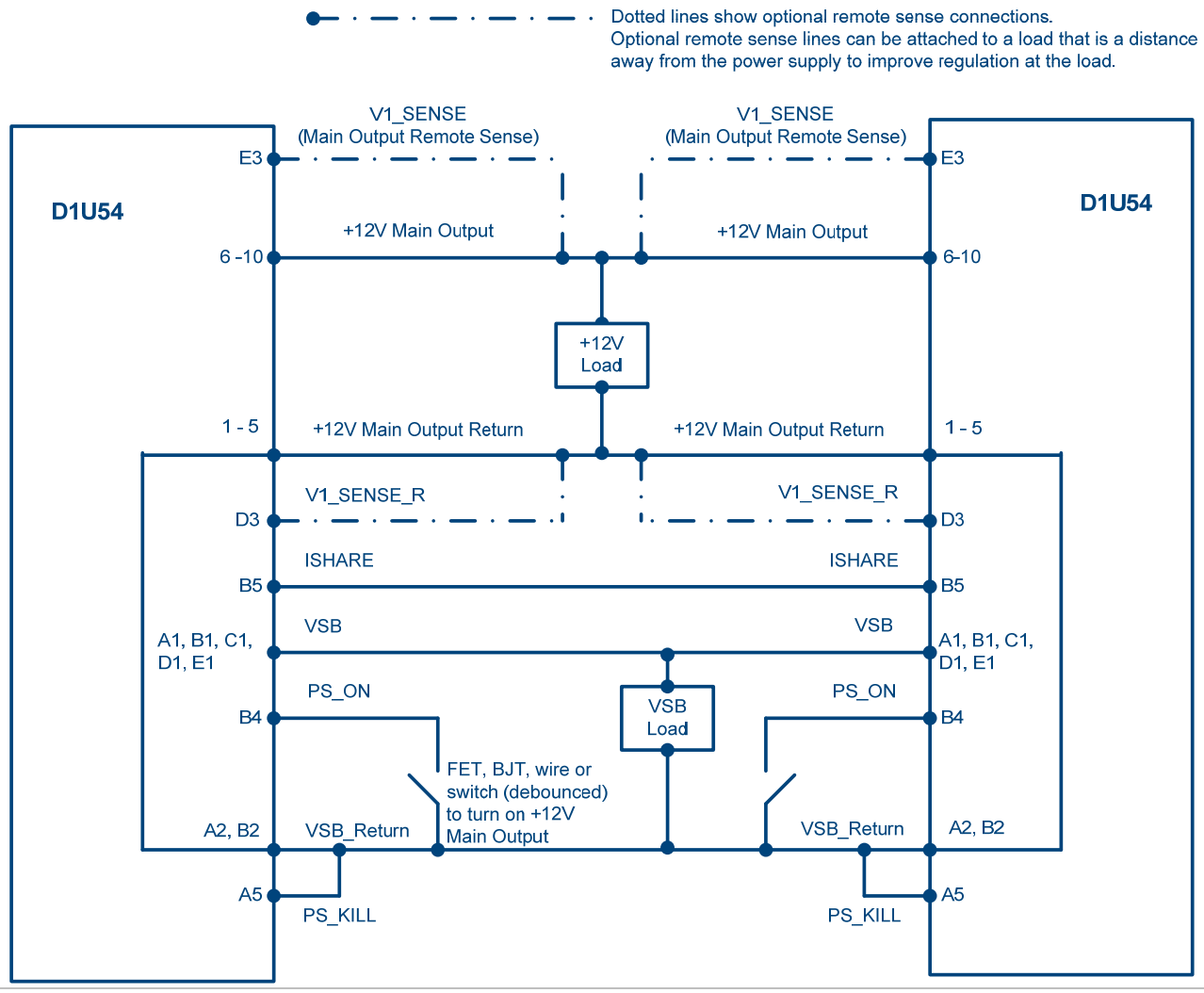
| OUTPUT CONNECTOR PIN ASSIGNMENTS - D1U54P-W-650-12-HBxC | | |
|---|---|---|
| (Power Supply) FCI PN 10122460-005LF | | |
| Pin | Signal Name | Comments |
| 6, 7, 8, 9, 10 | V1 (+12VOUT) | +12V Main Output |
| 1, 2, 3, 4, 5 | +12V RTN/PGND | +12V Main Output Return |
| A1 | +VSB | Standby Output |
| B1 | +VSB | Standby Output |
| C1 | +VSB | Standby Output |
| D1 | +VSB | Standby Output |
| E1 | +VSB | Standby Output |
| A2 | +VSB_Return | Standby Output Return |
| B2 | +VSB_Return | Standby Output Return |
| C2 | Unused | No End User Connection |
| D2 | Unused | No End User Connection |
| E2 | Unused | No End User Connection |
| A3 | APS | $I^2C$ Address Protocol Selection; (Select address by appropriate pull down resistor – See table below) |
| B3 | Unused | No End User Connection |
| C3 | SDA | $I^2C$ Serial Data Line |
| D3 | V1_SENSE_R | -VE Remote Sense Return |
| E3 | V1_SENSE | +VE Remote Sense |
| A4 | SCL | $I^2C$ Serial Clock Line |
| B4 | PS_ON_L | Remote On/Off (Enable/Disable) |
| C4 | SMB_ALERT | Alert signal to host system |
| D4 | Unused | No End User Connection |
| E4 | INPUT_OK | DC Input Source Present & “OK” |
| A5 | PS_KILL | Power Supply “kill”; short pin |
| B5 | ISHARE | Active Current Share Bus |
| C5 | PW_OK | Power “OK”; short pin |
| D5 | Unused | No End User Connection |
| E5 | PRESENT_L | Power Module Present; short pin |

| MATING CONNECTOR | |
|---|---|
| Part Number | Description |
| TE Connectivity 2-1926739-5<br>FCI 10108888-R10253SLF | Right Angle<br>Right Angle |

| APS ADDRESS SELECTION | | |
|---|---|---|
| APS pin (A3) resistor to GND (K-ohm)* | Power Supply Main Controller (Serial Communications Slave Address) | Power Supply External EEPROM (Serial Communications Slave Address) |
| 0.82 | 0xB0 | 0xA0 |
| 2.7 | 0xB2 | 0xA2 |
| 5.6 | 0xB4 | 0xA4 |
| 8.2 | 0xB6 | 0xA6 |
| 15 | 0xB8 | 0xA8 |
| 27 | 0xBA | 0xAA |
| 56 | 0xBC | 0xAC |
| 180 | 0xBE | 0xAE |

* The resistor shall be +/-5% tolerance

## WIRING DIAGRAM FOR OUTPUT

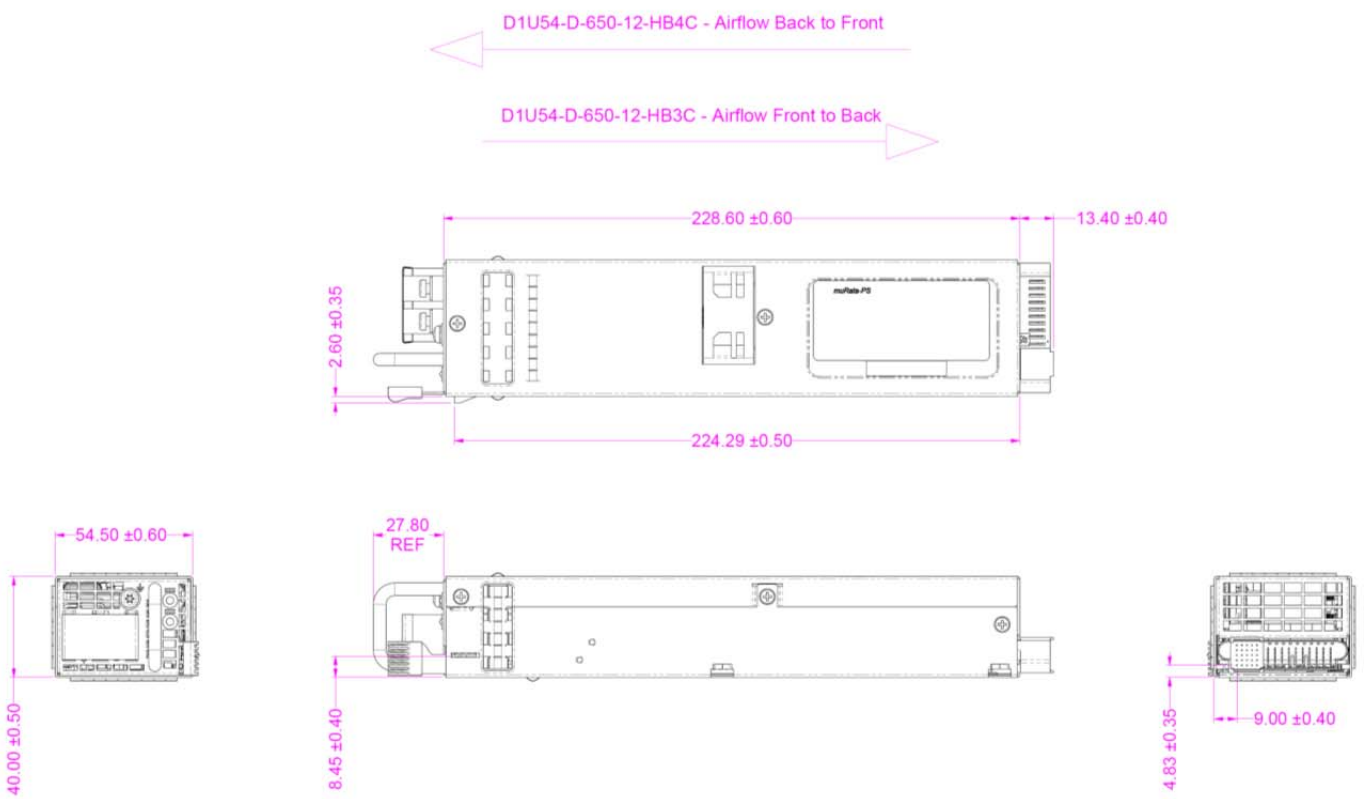



## CURRENT SHARE NOTES

1. Main Output: Current sharing is achieved using the active (analogue) current share method.
2. Current sharing can be achieved with or without the remote (V_SENSE and V_SENSE_R) connected to the common load.
3. +VSB Outputs can be tied together for redundancy but total combined output power must not exceed the rated standby power. The +VSB output has an internal ORing MOSFET for additional redundancy/internal short protection.
4. The current sharing pin B5 is connected between sharing units (forming an ISHARE bus). It is an input and/or an output (bi-directional analogue bus) as the voltage on the line controls the current share between sharing units. A power supply will respond to a change in this voltage but a power supply can also change the voltage depending on the load drawn from it. On a single unit the voltage on the pin (and the common ISHARE bus would read 8VDC at 100% (power module load capability). For two units sharing the same 100% load this would read 4VDC for perfect current sharing (i.e. 50% power module load capability per unit).

The load for both the main 12V and the VSB rails at initial startup shall not be allowed to exceed the capability of a single unit. The load can be increased after a delay of 3sec (minimum), to allow all sharing units to achieve steady state regulation.

## MECHANICAL DIMENSIONS




1. DC input connector: Dinkle Terminal Block, Dinkle Enterprise: Part No. DT-7C-B14W-02
2. Dimensions: 2.15" x 9.00" x 1.57" [54.5mm x 228.6mm x 40.0mm]
3. This drawing is a graphical representation of the product and may not show all fine details.
4. Reference File: D1U54-D-650-12-HBxC (M1878-M1879)_Drawing for Product Datasheet_20151216.pdf

## OPTIONAL ACCESSORIES

| Description | Part Number |
|---|---|
| 12V D1U54P Output Connector Card | D1U54P-12-CONC |

## APPLICATION NOTES

| Document Number | Description | Link |
|---|---|---|
| ACAN-64 | D1U54P Output Connector Card | http://power.murata.com/datasheet?/data/apnotes/acan-64.pdf |
| ACAN-60 | D1U54-x Communication Protocol | http://power.murata.com/datasheet?/data/apnotes/acan-60.pdf |

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ISO 9001 and 14001 REGISTERED

**This product is subject to the following operating requirements and the Life and Safety Critical Application Sales Policy:**
**Refer to: http://www.murata-ps.com/requirements/**

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