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April 2009

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## **FDMS7660**

# N-Channel PowerTrench<sup>®</sup> MOSFET 30 V, 2.8 m $\Omega$

#### **Features**

- Max  $r_{DS(on)}$  = 2.8 m $\Omega$  at  $V_{GS}$  = 10 V,  $I_D$  = 25 A
- Max  $r_{DS(on)}$  = 3.5 m $\Omega$  at  $V_{GS}$  = 4.5 V,  $I_D$  = 19 A
- Advanced Package and Silicon combination for low r<sub>DS(on)</sub> and high efficiency
- Next generation enhanced body diode technology, engineered for soft recovery. Provides Schottky-like performance with minimum EMI in sync buck converter applications
- MSL1 robust package design
- 100% UIL tested
- RoHS Compliant

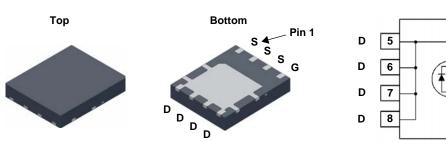


#### **General Description**

This N-Channel MOSFET has been designed specifically to improve the overall efficiency and to minimize switch node ringing of DC/DC converters using either synchronous or conventional switching PWM controllers. It has been optimized for low gate charge, low  $r_{DS(on)}$ , fast switching speed and body diode reverse recovery performance.

### **Applications**

- IMVP Vcore Switching for Notebook
- VRM Vcore Switching for Desktop and Server
- OringFET / Load Switch
- DC-DC Conversion



Power 56

#### **MOSFET Maximum Ratings** T<sub>A</sub> = 25 °C unless otherwise noted

Symbol	Parameter			Ratings	Units
$V_{DS}$	Drain to Source Voltage			30	V
$V_{GS}$	Gate to Source Voltage		(Note 4)	±20	V
	Drain Current -Continuous (Package limited)	T <sub>C</sub> = 25 °C		42	
	-Continuous (Silicon limited)	T <sub>C</sub> = 25 °C		144	^
ID	-Continuous	T <sub>A</sub> = 25 °C	(Note 1a)	25	- A
	-Pulsed			150	
E <sub>AS</sub>	Single Pulse Avalanche Energy		(Note 3)	128	mJ
Б	Power Dissipation	T <sub>C</sub> = 25 °C		78	W
$P_{D}$	Power Dissipation	T <sub>A</sub> = 25 °C	(Note 1a)	2.5	VV
T <sub>J</sub> , T <sub>STG</sub>	Operating and Storage Junction Temperature R	ange		-55 to +150	°C

#### **Thermal Characteristics**

$R_{ heta JC}$	Thermal Resistance, Junction to Case		1.6	0C/M
$R_{\theta,JA}$	Thermal Resistance, Junction to Ambient (Not	te 1a)	50	°C/W

#### **Package Marking and Ordering Information**

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMS7660	FDMS7660	Power 56	13 "	12 mm	3000 units

# **Electrical Characteristics** $T_J = 25$ °C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Тур	Max	Units
Off Chara	cteristics					
$BV_DSS$	Drain to Source Breakdown Voltage	$I_D = 250 \mu A, V_{GS} = 0 V$	30			V
$\frac{\Delta BV_{DSS}}{\Delta T_{J}}$	Breakdown Voltage Temperature Coefficient	$I_D$ = 250 $\mu$ A, referenced to 25 °C		17		mV/°C
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> = 24 V, V <sub>GS</sub> = 0 V			1	μΑ
I <sub>GSS</sub>	Gate to Source Leakage Current, Forward	V <sub>GS</sub> = 20 V, V <sub>DS</sub> = 0 V			100	nA

#### On Characteristics

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$ , $I_D = 250 \mu A$	1.25	1.9	3.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D$ = 250 $\mu$ A, referenced to 25 °C		-7		mV/°C
r <sub>DS(on)</sub>	Static Drain to Source On Resistance	V <sub>GS</sub> = 10 V , I <sub>D</sub> = 25 A		1.9	2.8	
		$V_{GS} = 4.5 \text{ V}, I_D = 19 \text{ A}$		2.7	3.5	mΩ
		$V_{GS} = 10 \text{ V}, I_D = 25 \text{ A}, T_J = 125 ^{\circ}\text{C}$		2.5	3.7	
9 <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> = 5 V, I <sub>D</sub> = 25 A		250		S

#### **Dynamic Characteristics**

C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> = 15 V, V <sub>GS</sub> = 0 V, f = 1 MHz	4185	5565	рF
Coss	Output Capacitance		1380	1830	pF
C <sub>rss</sub>	Reverse Transfer Capacitance		125	190	pF
$R_g$	Gate Resistance		0.9	2.0	Ω

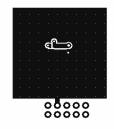
#### **Switching Characteristics**

t <sub>d(on)</sub>	Turn-On Delay Time		17	31	ns
t <sub>r</sub>	Rise Time	V <sub>DD</sub> = 15 V, I <sub>D</sub> = 25A,	9	18	ns
t <sub>d(off)</sub>	Turn-Off Delay Time	$V_{GS} = 10 \text{ V}, R_{GEN} = 6 \Omega$	37	60	ns
t <sub>f</sub>	Fall Time		7	13	ns
$Q_g$	Total Gate Charge	V <sub>GS</sub> = 0 V to 10 V	60	84	nC
Qg	Total Gate Charge	$V_{GS} = 0 \text{ V to } 4.5 \text{ V}$ $V_{DD} = 15 \text{ V},$	27	38	nC
$Q_{gs}$	Gate to Source Charge	I <sub>D</sub> = 25 A	12.3		nC
$Q_{gd}$	Gate to Drain "Miller" Charge		7.2		nC

#### **Drain-Source Diode Characteristics**

V <sub>SD</sub>	Source to Drain Diode Forward Voltage	$V_{GS} = 0 \text{ V}, I_S = 2.1 \text{ A}$ (Note 2)	0.7	0.95	V
	Source to Drain Diode Forward Voltage	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 25 A (Note 2)	0.8	1.1	
t <sub>rr</sub>	Reverse Recovery Time		46	74	ns
$Q_{rr}$	Reverse Recovery Charge		26	42	nC
t <sub>a</sub>	Reverse Recovery Fall Time	I <sub>F</sub> = 25 A, di/dt = 100 A/μs	19		nC
t <sub>b</sub>	Reverse Recovery Rise Time		27		nC
S	Softness (t <sub>b</sub> /t <sub>a</sub> )		1.4		
t <sub>rr</sub>	Reverse Recovery Time	I <sub>F</sub> = 25 A, di/dt = 300 A/μs	36	58	ns
$Q_{rr}$	Reverse Recovery Charge	1 <sub>F</sub> = 25 A, αι/αι = 300 A/μS	43	68	nC
Notes:	•	<u>'</u>			

<sup>1</sup> R<sub>0JA</sub> is determined with the device mounted on a 1in<sup>2</sup> pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. R<sub>0JC</sub> is guaranteed by design while R<sub>0CA</sub> is determined by the user's board design.



a. 50 °C/W when mounted on a 1 in<sup>2</sup> pad of 2 oz copper.



b. 125 °C/W when mounted on a minimum pad of 2 oz copper.

<sup>2.</sup> Pulse Test: Pulse Width < 300  $\mu\text{s},$  Duty cycle < 2.0%.

<sup>3.</sup> E<sub>AS</sub> of 128 mJ is based on starting T<sub>J</sub> = 25 °C, L = 1 mH, I<sub>AS</sub> = 16 A, V<sub>DD</sub> = 27 V, V<sub>GS</sub> = 10 V. 100% test at L = 0.3 mH, I<sub>AS</sub> = 23 A.

<sup>4.</sup> As an N-ch device, the negative Vgs rating is for low duty cycle pulse occurrence only. No continuous rating is implied.

## **Typical Characteristics** $T_J = 25$ °C unless otherwise noted

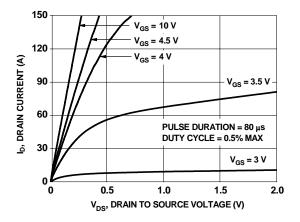


Figure 1. On-Region Characteristics

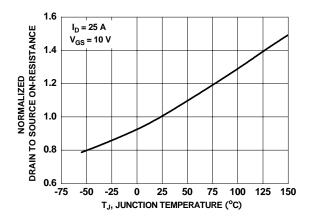


Figure 3. Normalized On-Resistance vs Junction Temperature

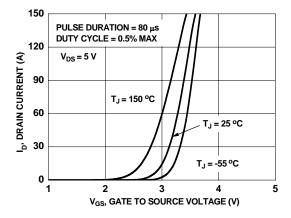


Figure 5. Transfer Characteristics

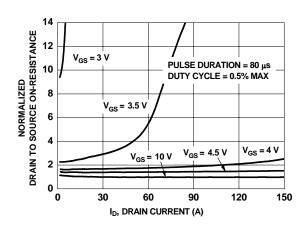


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

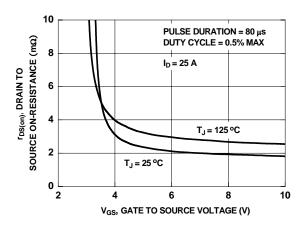


Figure 4. On-Resistance vs Gate to Source Voltage

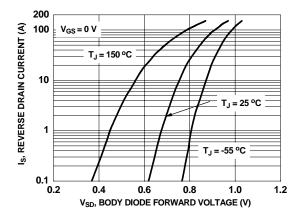


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

## Typical Characteristics $T_J = 25^{\circ}C$ unless otherwise noted

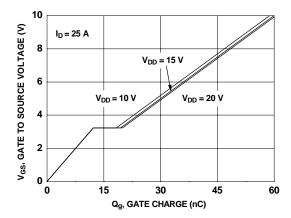


Figure 7. Gate Charge Characteristics

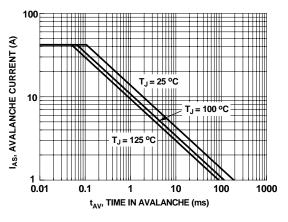


Figure 9. Unclamped Inductive Switching Capability

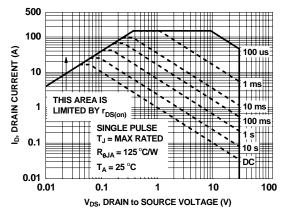


Figure 11. Forward Bias Safe Operating Area

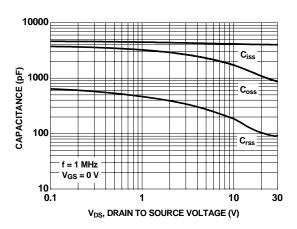


Figure 8. Capacitance vs Drain to Source Voltage

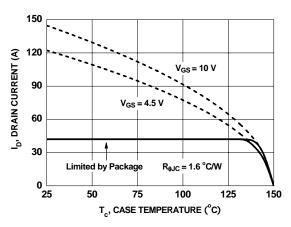


Figure 10. Maximum Continuous Drain Current vs Case Temperature

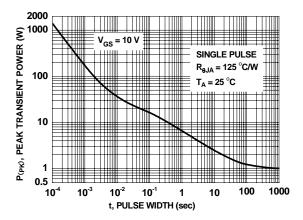


Figure 12. Single Pulse Maximum Power Dissipation

## **Typical Characteristics** $T_J = 25$ °C unless otherwise noted

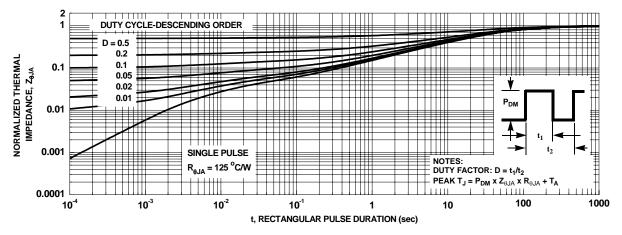


Figure 13. Junction-to-Ambient Transient Thermal Response Curve

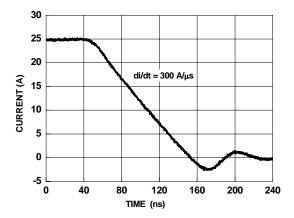


Figure 14. Body Diode Reverse Recovery Characteristics



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