High Speed Difference Amplifier with Input Short to Battery Protection

Data Sheet

ADA4830-1

FEATURES

Input overvoltage (short to battery) protection of up to 18 V
Short to battery output flag for wire diagnostics
Wide input common-mode range with single 5 V supply
High performance video amplifier with 0.5 V/V gain
−3 dB bandwidth of 84 MHz
220 V/µs slew rate (2 V step)
Excellent video specifications
0.1 dB flatness to 20 MHz
SNR of 73 dB to 15 MHz
Differential gain of 0.1%
Differential phase of 0.1°
Wide supply range: 2.9 V to 5.5 V
Power-down mode
Space saving 3 mm × 3 mm LFCSP package
Wide operating temperature range: −40°C to +125°C

APPLICATIONS

Automotive vision systems
Automotive infotainment
Surveillance systems

FUNCTIONAL BLOCK DIAGRAM

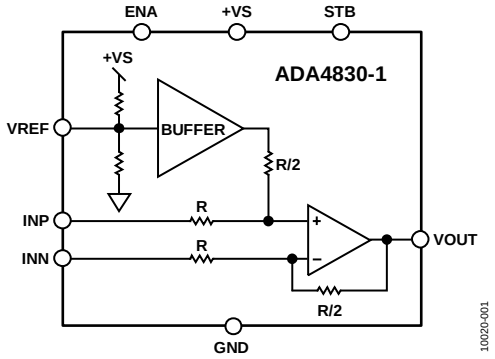

Figure 1.

GENERAL DESCRIPTION

The ADA4830-1 is a monolithic high speed difference amplifier that integrates input overvoltage (short to battery) protection of up to 18 V with a wide input common-mode voltage range and excellent ESD robustness. The ADA4830-1 is intended for use as a receiver for differential or pseudo differential CVBS and other high speed video signals in harsh, noisy environments such as automotive infotainment and vision systems. The ADA4830-1 combines the high speed and the precision that allow accurate reproduction of CVBS video signals, yet rejects unwanted common-mode error voltages.

The short to battery protection that is integrated into the ADA4830-1 employs fast switching circuitry to clamp and hold internal voltage nodes at a safe level when an input overvoltage condition is detected. This protection allows the inputs of the ADA4830-1 to be directly connected to a remote video source, such as a rearview camera, without the need for large expensive series capacitors. The ADA4830-1 can withstand direct short to battery voltages as high as 18 V on its input pins.

The ADA4830-1 is designed to operate at supply voltages as low as 2.9 V and as high as 5.5 V, using only 6.8 mA of supply current per channel. The device provides true single-supply capability, allowing the input signal to extend 8.5 V below the negative rail and to 8.5 V above ground on a single 5 V supply. At the output, the amplifier can swing to within 250 mV of either supply rail into a 150 Ω load.

The ADA4830-1 presents a gain of 0.5 V/V at its output. This is designed to keep the video signal within the allowed range of the video decoder, which is typically 1 V p-p or less.

The ADA4830-1 is available in a 3 mm × 3 mm, 8-lead LFCSP package and is specified for operation over the automotive temperature range of −40°C to +125°C.

Rev. 0

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REVISION HISTORY

10/11—Revision 0: Initial Version

SPECIFICATIONS

5 V OPERATION

T_A = 25°C, $+V_S$ = 5 V, R_L = 1 kΩ, V_{REF} = 2.5 V (floating), $V_{INCM} = +V_S/2$, R_{STB} = 5 kΩ to $+V_S$, unless otherwise specified.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
−3 dB Large Signal Bandwidth	V_{OUT} = 0.5 V p-p, R_L = 150 Ω		71		MHz
	V_{OUT} = 0.1 V p-p, R_L = 1 kΩ		84		MHz
	V_{OUT} = 0.1 V p-p, R_L = 150 Ω		74		MHz
Bandwidth for 0.1 dB Flatness	V_{OUT} = 0.5 V p-p, R_L = 150 Ω		28		MHz
Slew Rate (t_R/t_F)	V_{OUT} = 2 V step		220		V/µs
Settling Time to 0.1%	V_{OUT} = 2 V step		25		ns
NOISE/DISTORTION PERFORMANCE					
Output Voltage Noise	f = 1 MHz		28		nV/√Hz
Differential Gain Error (NTSC)	R_L = 150 Ω, V_{IN} = 1 V p-p		0.1		%
Differential Phase Error (NTSC)	R_L = 150 Ω, V_{IN} = 1 V p-p		0.1		Degrees
Signal-to-Noise Ratio	f = 100 kHz to 15 MHz, V_{OUT} = 0.5 V p-p		73		dB
DC PERFORMANCE					
Nominal Gain	V_{IN} to V_{OUT}	0.49	0.50	0.51	V/V
Output Bias Voltage		2.45	2.50	2.55	V
INPUT CHARACTERISTICS					
Input Resistance (Differential Mode)			7		kΩ
Input Resistance (Common Mode)			2		kΩ
Input Common-Mode Voltage Range			±8.5		V
Common-Mode Rejection (CMR)	V_{IN} = ±5 V	45	65		dB
SHORT TO BATTERY CHARACTERISTICS					
Input Current	V_{IN} = 18 V (short to battery)		4.1		mA
Protected Input Voltage Range		−9		+20	V
Short to Battery Output Flag Trigger Level	Signals an input fault condition	9.8	10.3	10.8	V
VOLTAGE REFERENCE INPUT					
Input Voltage Range			0.2 to 3.9		V
Input Resistance			20		kΩ
Gain	V_{REF} to V_{OUT}		1		V/V
LOGIC OUTPUT/INPUT CHARACTERISTICS					
STB V_{OH}	Input voltage ≤ 9.75 V (normal operation)		5.0		V
STB V_{OL}	Input voltage ≥ 10.75 V (fault condition)		110		mV
ENA V_{IH}	Voltage to enable device		≥3.0		V
ENA V_{IL}	Voltage to disable device		≤1.0		V
OUTPUT CHARACTERISTICS					
Output Voltage Swing	R_L = 150 Ω to GND		0.01 to 4.75		V
Output Current			125		mA
Short-Circuit Current	Sourcing/sinking		248/294		mA
Capacitive Load Drive	Peaking ≤ 3 dB		47		pF
POWER SUPPLY					
Operating Range	Operation outside of this range results in performance degradation	2.9		5.5	V
Quiescent Current per Amplifier	Enabled (ENA = 5 V), no load		6.8	10	mA
	Disabled (ENA = 0 V)		90		µA
	V_{IN} = 18 V (short to battery)		5.3		mA
Power Supply Rejection Ratio (PSRR)	$+V_S$ = 4.5 V to 5.5 V, VREF is forced to 2.5 V		53		dB
OPERATING TEMPERATURE RANGE		−40		+125	°C

3.3 V OPERATION

T_A = 25°C, $+V_S$ = 3.3 V, R_L = 1 kΩ, V_{REF} = 2.5 V (floating), V_{INCM} = $+V_S$/2, R_{STB} = 5 kΩ to +Vs, unless otherwise specified.

Table 2.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
−3 dB Large Signal Bandwidth	V_{OUT} = 0.5 V p-p, R_L = 150 Ω		73		MHz
	V_{OUT} = 0.1 V p-p, R_L = 1 kΩ		89		MHz
	V_{OUT} = 0.1 V p-p, R_L = 150 Ω		76		MHz
Bandwidth for 0.1 dB Flatness	V_{OUT} = 0.5 V p-p, R_L = 150 Ω		25		MHz
Slew Rate (t_R/t_F)	V_{OUT} = 1 V step		220		V/µs
Settling Time to 0.1%	V_{OUT} = 1 V step		25		ns
NOISE/DISTORTION PERFORMANCE					
Output Voltage Noise	f = 1 MHz		28		nV/√Hz
Differential Gain Error (NTSC)	R_L = 150 Ω, V_{IN} = 1 V p-p		0.1		%
Differential Phase Error (NTSC)	R_L = 150 Ω, V_{IN} = 1 V p-p		0.1		Degrees
Signal-to-Noise Ratio	f = 100 kHz to 15 MHz, V_{OUT} = 0.5 V p-p		73		dB
DC PERFORMANCE					
Nominal Gain	V_{IN} to V_{OUT}	0.49	0.50	0.51	V/V
Output Bias Voltage		1.60	1.65	1.70	V
INPUT CHARACTERISTICS					
Input Resistance (Differential Mode)			7		kΩ
Input Resistance (Common Mode)			2		kΩ
Input Common-Mode Voltage Range			±5.5		V
Common-Mode Rejection (CMR)	V_{IN} = ±3.3 V	43	54		dB
SHORT TO BATTERY CHARACTERISTICS					
Input Current	V_{IN} = 18 V (short to battery)		4.4		mA
Protected Input Voltage Range		−9		+20	V
Short to Battery Output Flag Trigger Level	Signals an input short to battery event	7.4	7.8	8.2	V
VOLTAGE REFERENCE INPUT					
Input Voltage Range			0.2 to 2.2		V
Input Resistance			20		kΩ
Gain	V_{REF} to V_{OUT}		1		V/V
LOGIC OUTPUT/INPUT CHARACTERISTICS					
STB V_{OH}	Input voltage ≤ 7.25 V (normal operation)		3.3		V
STB V_{OL}	Input voltage ≥ 8.25 V (fault condition)		85		mV
ENA V_{IH}	Voltage to enable device		≥1.8		V
ENA V_{IL}	Voltage to disable device		≤0.8		V
OUTPUT CHARACTERISTICS					
Output Voltage Swing	R_L = 150 Ω to GND		0.01 to 3.08		V
Output Current			50		mA
Short-Circuit Current	Sourcing/sinking		85/180		mA
Capacitive Load Drive	Peaking ≤ 4 dB		47		pF
POWER SUPPLY					
Operating Range	Operation outside of this range results in performance degradation	2.9		5.5	V
Quiescent Current per Amplifier	Enabled (ENA = 3.3 V), no load		5.5	8.0	mA
	Disabled (ENA = 0 V)		60		µA
	V_{IN} = 18 V (short to battery)		4.3		mA
Power Supply Rejection Ratio (PSRR)	$+V_S$ = 3.0 V to 3.6 V, VREF forced to 1.65 V		42		dB
OPERATING TEMPERATURE RANGE		−40		+125	°C

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Supply Voltage (+VS pin)	6 V
Input Voltage Positive Direction (INN, INP)	22 V
Input Voltage Negative Direction (INN, INP)	−10 V
Reference Voltage (VREF pin)	$+V_S$ + 0.3 V
Power Dissipation	See Figure 2
Storage Temperature Range	−65°C to +125°C
Operating Temperature Range	−40°C to +125°C
Lead Temperature (Soldering, 10 sec)	260°C
Junction Temperature	150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the device soldered to a high thermal conductivity, 4-layer (2s2p) circuit board, as described in EIA/JESD 51-7.

Table 4.

Package Type	θ_{JA}	Unit
8-Lead LFCSP	116	°C/W

MAXIMUM POWER DISSIPATION

The maximum safe power dissipation in the ADA4830-1 package is limited by the associated rise in junction temperature (T_J) on the die. At approximately 150°C, which is the glass transition temperature, the plastic changes its properties. Exceeding a junction temperature of 150°C for an extended time can result in changes in the silicon devices, potentially causing failure.

The power dissipated in the package (P_D) is the sum of the quiescent power dissipation and the power dissipated in the package due to the load drive for all outputs. The quiescent power is the voltage between the supply pins (V_S) times the quiescent current (I_S). The power dissipated due to load drive depends on the particular application. The power due to load drive is calculated by multiplying the load current by the associated voltage drop across the device. RMS voltages and currents must be used in these calculations.

Airflow increases heat dissipation, effectively reducing θ_{JA}.

Figure 2 shows the maximum power dissipation in the package vs. the ambient temperature for the 8-lead LFCSP (116°C/W) on a JEDEC standard 4-layer board. θ_{JA} values are approximate.

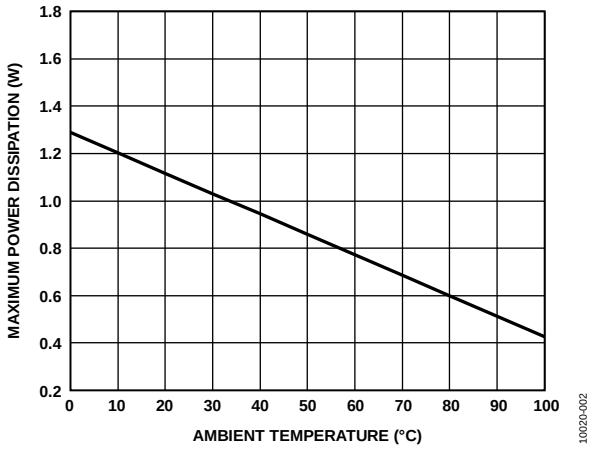

Figure 2. Maximum Power Dissipation vs. Ambient Temperature for a 4-Layer Board

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

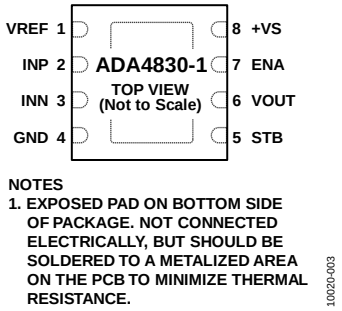

Figure 3. Pin Configuration

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	VREF	Voltage Reference Input. Sets the output dc bias voltage. Internally biased to +Vs/2 when left floating. See the Applications Information section.
2	INP	Positive Input.
3	INN	Negative Input.
4	GND	Power Supply Ground Pin.
5	STB	Short to Battery Indicator Pin. A logic low indicates an overvoltage condition (short to battery), whereas a logic high indicates normal operation. An open-drain configuration requires external pull-up resistor.
6	VOUT	Video Amplifier Output.
7	ENA	Enable. Connect to +VS or float for normal operation. Connect to GND for device disable.
8	+VS	Positive Power Supply. Bypass this pin with a 0.1 µF capacitor to GND.
	EPAD	Exposed Pad. The exposed pad is located on bottom side of package. The pad is not connected electrically but should be soldered to a metalized area on the PCB to minimize thermal resistance.

TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, $+V_S$ = 5 V, R_L = 1 kΩ, V_{REF} = 2.5 V (floating), V_{INCM} = $+V_S$/2, R_{STB} = 5 kΩ to $+V_S$ unless otherwise specified.

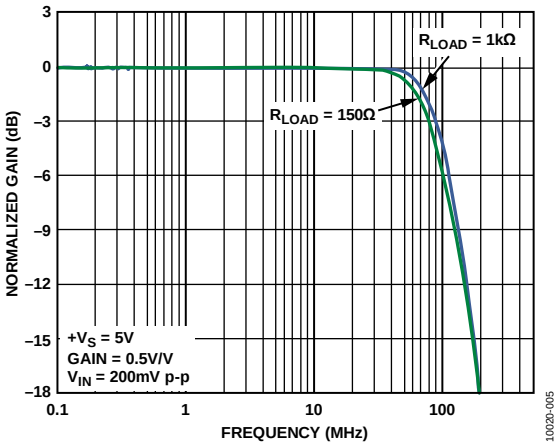

Figure 4. Small Signal Frequency Response vs. Load

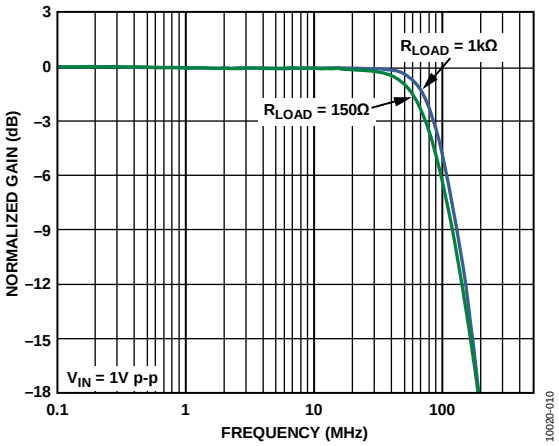

Figure 7. Large Signal Frequency Response vs. Load

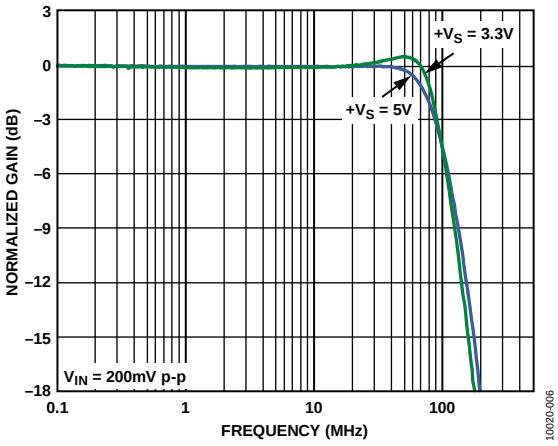

Figure 5. Small Signal Frequency Response vs. Supply Voltage

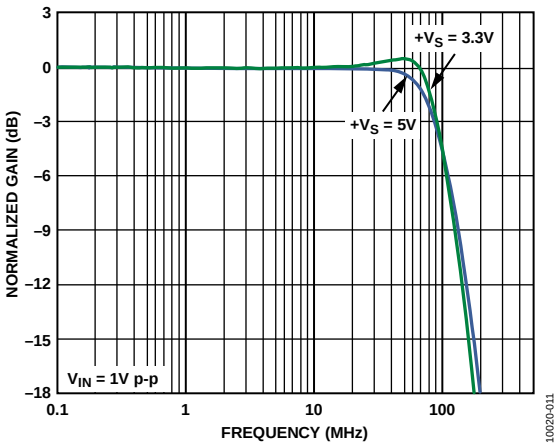

Figure 8. Large Signal Frequency Response vs. Supply Voltage

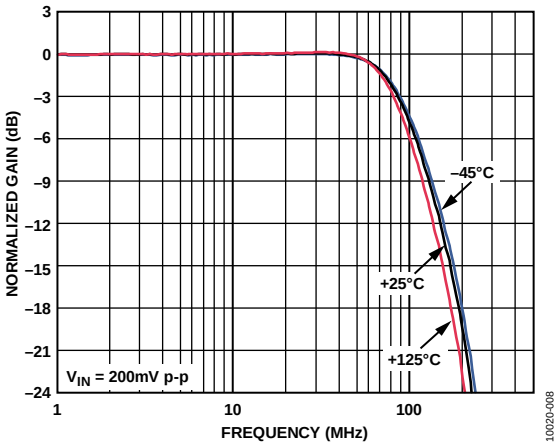

Figure 6. Small Signal Frequency Response for Various Temperatures, $+V_S$ = 5 V

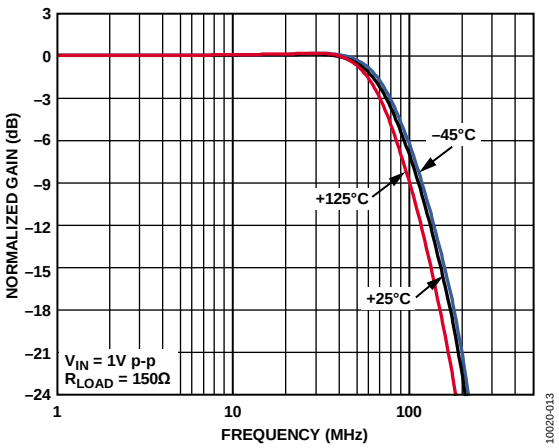

Figure 9. Large Signal Frequency Response for Various Temperatures, $+V_S$ = 3.3 V

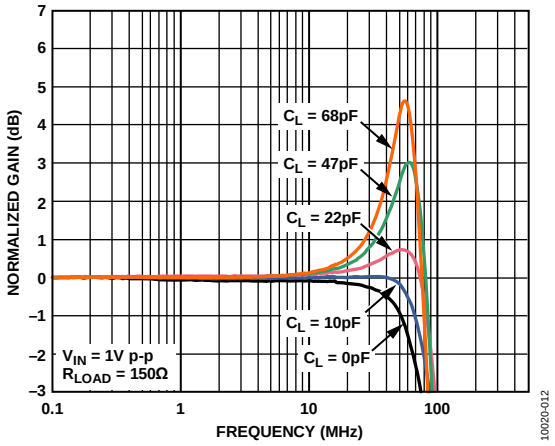

Figure 10. Large Signal Frequency Response for Various Capacitor Loads

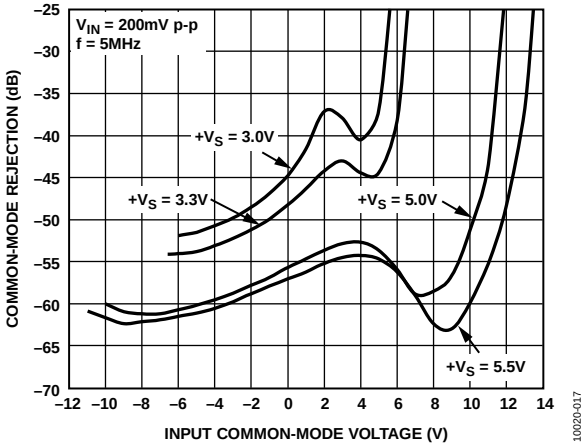

Figure 13. Small Signal CMR vs. V_{INCM} and Supply Voltage

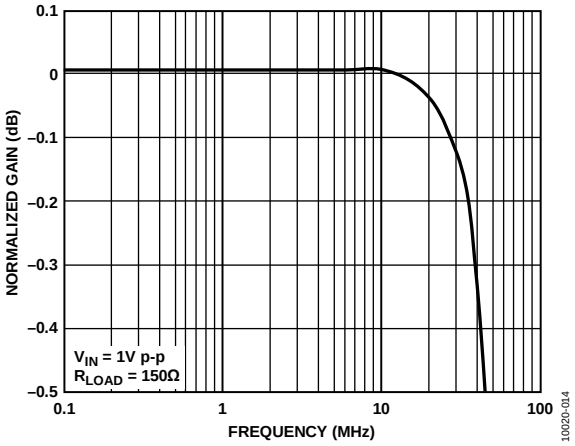

Figure 11. 0.1 dB Flatness

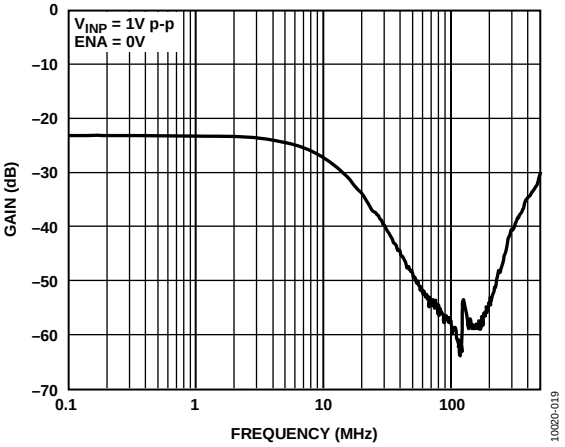

Figure 14. Disabled Response: Input to Output

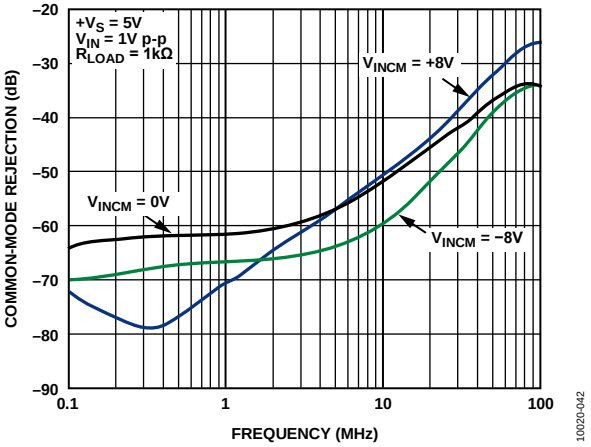

Figure 12. CM Frequency Response vs. Input Common-Mode Voltage

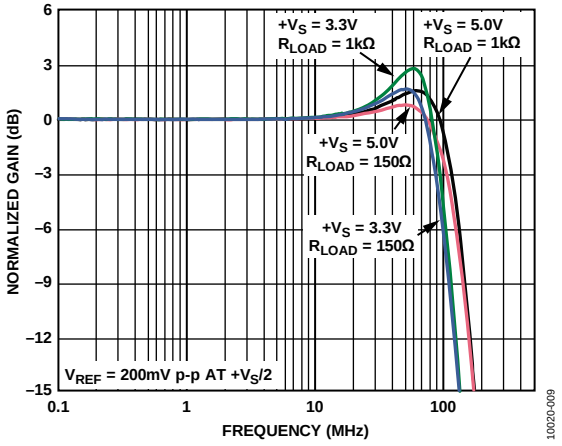

Figure 15. Small Signal Response: V_{REF} to V_{OUT}

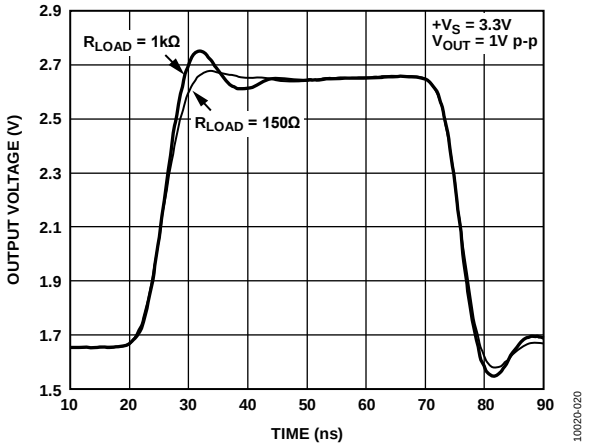

Figure 16. Pulse Response at $+V_S$ = 3.3 V

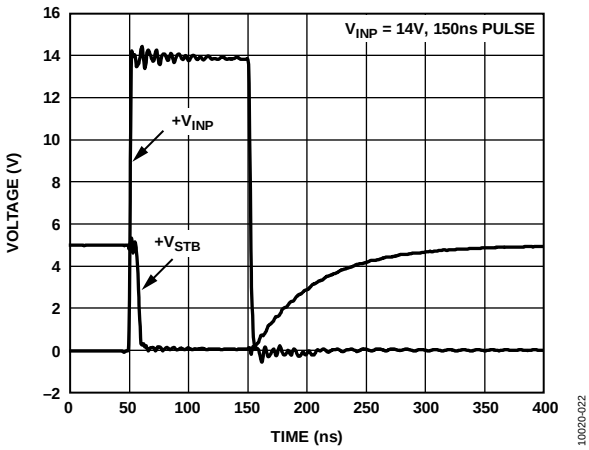

Figure 17. STB Flag Response

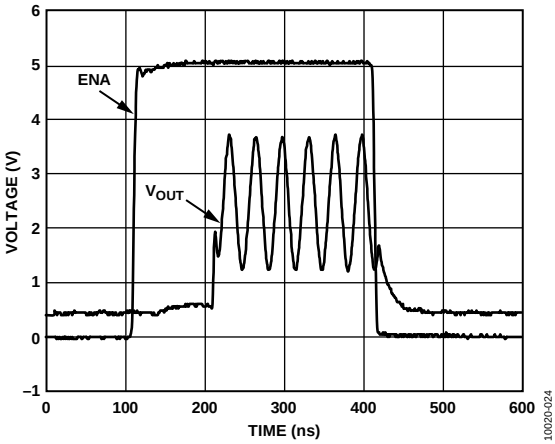

Figure 18. Enable Pin Turn-on/Turn-off Time

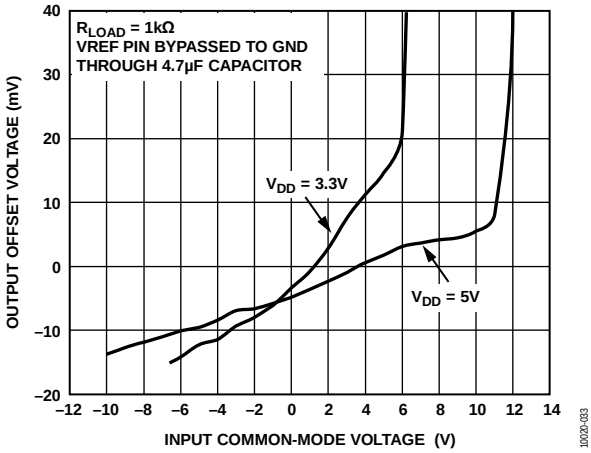

Figure 19. Output Offset Voltage : $V_{OUT} - V_{REF}$

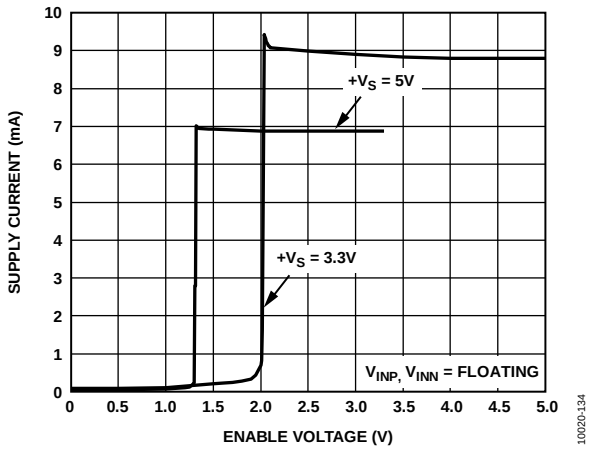

Figure 20. Supply Current vs. Enable Voltage

THEORY OF OPERATION

CORE AMPLIFIER

At the core of the ADA4830-1 is a high speed, rail-to-rail op amp that is built on a 0.35 µm CMOS process. Together with the core amplifier, the ADA4830-1 combines four highly matched on-chip resistors into a difference amplifier function. Common-mode range extension at its inputs is achieved by employing a resistive attenuator. The closed-loop differential to single-ended gain of the video channel is internally fixed at 0.5 V/V (−6 dB) to ensure compatibility with video decoders whose input range is constrained to 1 V p-p or less. The transfer function of the ADA4830-1 is

$$V_{OUT} = \frac{V_{IN+} - V_{IN-}}{2} + V_{REF}$$

where:
V_{OUT} is the voltage at the output pin, VOUT.
V_{IN+} and V_{IN-} are the input voltages at Pin INP and Pin INN, respectively.
V_{REF} is the voltage at the VREF pin.

OVERVOLTAGE (SHORT TO BATTERY) PROTECTION

Robust inputs guarantee that sensitive internal circuitry is not subjected to extreme voltages or currents during a stressful event. A short to battery condition usually consists of a voltage on either input (or both inputs) that is significantly higher than the power supply voltage of the amplifier. Duration may vary from a short transient to a continuous fault.

The ADA4830-1 can withstand voltages of up to 18 V on the inputs. Critical internal nodes are protected from exposure to high voltages by circuitry that clamps the inputs at a safe level and limits internal currents. This protection is available whether the device is enabled or disabled, even when the supply voltage is removed.

SHORT TO BATTERY OUTPUT FLAG

The short to battery output flag (STB pin) is functionally independent of the short to battery protection. Its purpose is to indicate an overvoltage condition on either input. Because protection is provided passively, it is always available; the flag merely indicates the presence or absence of a fault condition.

ESD PROTECTION

All pins on the ADA4830-1 are protected with internal ESD protection structures connected to the power supply pins (+VS and GND). These structures provide protection during the handling and manufacturing process.

The inputs (INN and INP) of the ADA4830-1 can be exposed to dc voltages well above the supply voltage; therefore, conventional ESD structure protection cannot be used.

The ADA4830-1 employs Analog Devices, Inc., proprietary ESD devices at the input pins (INN, INP) to allow for a wide common-mode voltage range and ESD protection well beyond the handling and manufacturing requirements.

APPLICATIONS INFORMATION

METHODS OF TRANSMISSION

Pseudo Differential Mode (Unbalanced Source Termination)

The ADA4830-1 can be operated in a pseudo differential configuration with an unbalanced input signal. This allows the receiver to be driven by any single-ended source. Pseudo differential mode uses a single conductor to carry an unbalanced signal, and connects the negative input terminal to the ground reference of the source.

Use the positive wire or coaxial center conductor to connect the source output to the positive input (INP) of the ADA4830-1. Next, connect the negative wire or coaxial shield from the negative input (INN) back to a ground reference on the source printed circuit board (PCB). The input termination should match the source impedance and be referenced to the remote ground. An example of this configuration is shown in Figure 21.

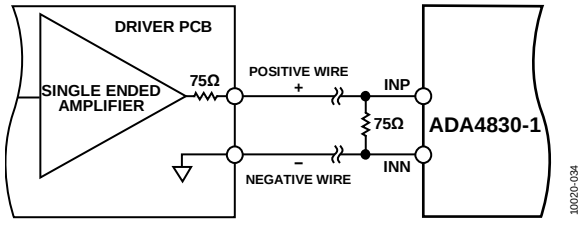

Figure 21. Pseudo Differential Mode

Pseudo Differential Mode (Balanced Source Impedance)

Pseudo differential signaling is typically implemented using unbalanced source termination as shown in Figure 21. With this arrangement, however, common-mode signals on the positive and negative inputs receive different attenuation due to unbalanced termination at the source. This effectively converts some of the common-mode signal into differential mode signal, degrading the overall common-mode rejection of the system. System common-mode rejection can be improved by balancing the output impedance of the driver as shown in Figure 22. Splitting the source termination resistance evenly between the hot and cold conductors results in matched attenuation of the common-mode signals, ensuring maximum rejection.

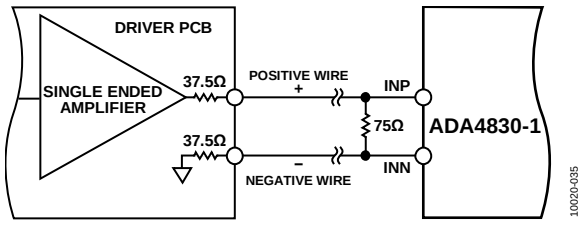

Figure 22. Pseudo Differential Mode with Balanced Source Impedance

Fully Differential Mode

The differential inputs of the ADA4830-1 allow full balanced transmission using any differential source. In this configuration, the differential input termination is equal to twice the source impedance of each output. For example, a source with 37.5 Ω back termination resistors in each leg should be terminated with a differential resistance of 75 Ω. An illustration of this arrangement is shown in Figure 23.

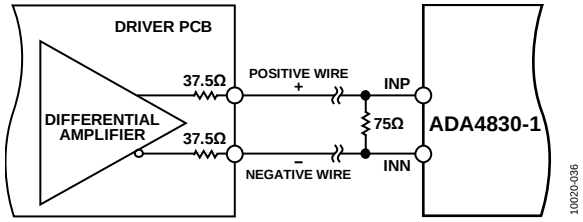

Figure 23. Fully Differential Mode

VOLTAGE REFERENCE (VREF PIN)

An internal reference level determines the output voltage when the differential input voltage is zero. This is set by a resistor divider connected between the supply rails. Built with a matched pair of 40 kΩ resistors, the divider sets this voltage to $+V_S/2$.

The voltage reference pin (VREF) normally floats at its default value of $+V_S/2$. However, it can be used to vary the output reference level from this default value. A voltage applied to VREF appears at the output with unity gain, within the bandwidth limit of the internal reference buffer.

Any noise on the $+V_S$ supply rail appears at the output with only 6 dB of attenuation (the divide-by-two provided by the reference divider). Even when this pin is floating, it is recommended that an external capacitor be connected from the reference node to ground to provide further attenuation of noise on the power supply line. A 4.7 µF capacitor combined with the internal 40 kΩ resistor sets the low-pass corner at under 1 Hz and results in better than 40 dB of supply noise attenuation at 100 Hz.

INPUT COMMON-MODE RANGE

In a standard four resistor difference amplifier with 0.5 V/V gain, the input common-mode (CM) range is three times the CM range of the core amplifier. In the ADA4830-1, however, the input CM has been extended to more than 17 V (with a 5 V supply). The input CM range can be approximated by using the following formulas:

Maximum CM voltage

$$5(+V_S - 1.25) - 4V_{REF} \approx V_{INCM(MAX)} \leq 9.5\ V$$

Minimum CM voltage

$$-10\ V \leq V_{INCM(MIN)} \approx -(1 + 4V_{REF})$$

Approximate minimum and maximum CM voltages are shown in Table 6 for several common supply voltages.

Table 6.

$+V_S$ (V)	V_{REF} (V)	$V_{INCM(MIN)}$ (V)	$V_{INCM(MAX)}$ (V)
3.0	1.5[1]	−7.0	2.8
3.0	0.97	−4.9	4.9
3.3	1.67[1]	−7.6	3.6
3.3	1.15	−5.6	5.6
3.6	1.8[1]	−8.2	4.5
3.6	1.34	−6.4	6.4
5.0	2.5[1]	−10	8.7
5.0	2.22	−9.9	9.9

[1] Floating (default condition).

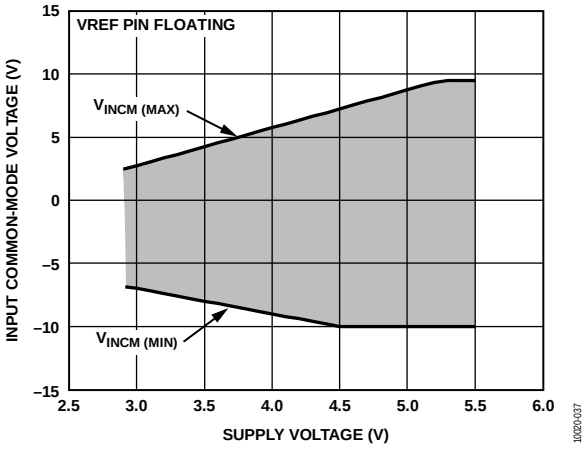

Figure 24. Input Common-Mode Range vs. Supply Voltage

SHORT TO BATTERY OUTPUT FLAG PIN

The flag output (STB pin) is of an active low, open-drain logic style. A low level on this output indicates that more than 11 V has been detected on either the positive or the negative input. Flags from multiple chips may be wire-or'ed to form a single fault detection signal. The output is driven by a grounded source NMOS device, capable of sinking approximately 10 mA while pulling within 100 mV of ground. The output high level is set with an external pull-up resistor connected to the supply voltage of the logic family that is used to monitor the state of the flag.

The speed with which the flag output responds primarily depends, in the falling direction, on the external capacitance attached to this node and the sink current that can be provided. For example, if the load is 10 pF, and the external pull-up voltage is 3.3 V, the fall time is a few nanoseconds. In the rising direction, the speed is determined by external capacitance and the magnitude of the pull-up resistor. For the case of 10 pF of external capacitance and a pull-up of 5 kΩ, the time constant of the rising edge is approximately 50 ns.

Table 7. STB Pin Function

STB Pin Output	Device State
High (Logic 1)	Normal operation
Low (Logic 0)	STB fault condition

ENABLE/DISABLE MODES (ENA PIN)

The power-down, or enable/disable (ENA) pin, is internally pulled up to $+V_S$ through a 250 kΩ resistor. When the voltage on this pin is high, the amplifier is enabled; pulling ENA low disables the channel. With no external connection, this pin floats high, enabling the amplifier channel.

Table 8. ENA Pin Function

ENA Pin Input	Device State
High (Logic 1)	Enabled
Low (Logic 0)	Disabled

PCB LAYOUT

As with all high speed applications, attention to PCB layout is of paramount importance. Adhere to standard high speed layout practices in designs using the ADA4830-1. A solid ground plane is recommended, and placing a 0.1 µF surface-mount, ceramic power supply, decoupling capacitor as close as possible to the supply pin is recommended.

Connect the GND pin(s) to the ground plane with a trace that is as short as possible. In cases where the ADA4830-1 drives transmission lines, series terminate the outputs and use controlled impedance traces of the shortest length possible to connect to the signal I/O pins, which should not pass over any voids in the ground plane.

EXPOSED PADDLE (EPAD) CONNECTION

The ADA4830-1 has an exposed thermal pad (EPAD) on the bottom of the package. This pad is not electrically connected to the die and can be left floating or connected to the ground plane. Should heat dissipation be a concern, thermal resistance can be minimized by soldering the EPAD to a metalized pad on the PCB. Connect this pad to the ground plane with multiple vias. Note that the thermal resistance (θ_{JA}) of the device is specified with the EPAD soldered to the PCB.

TYPICAL APPLICATIONS CIRCUITS

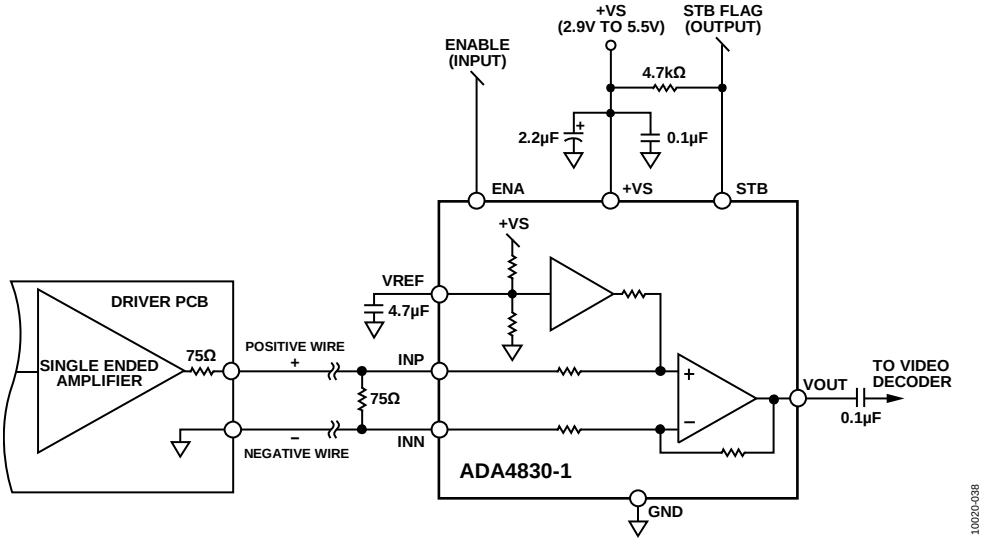

Figure 25. Typical Application with Pseudo Differential Input

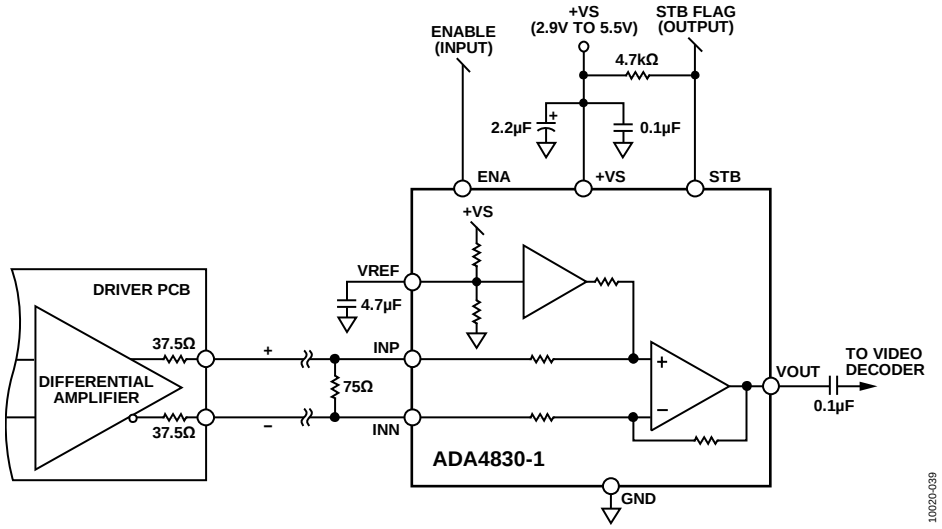

Figure 26. Typical Application with Fully Differential Input

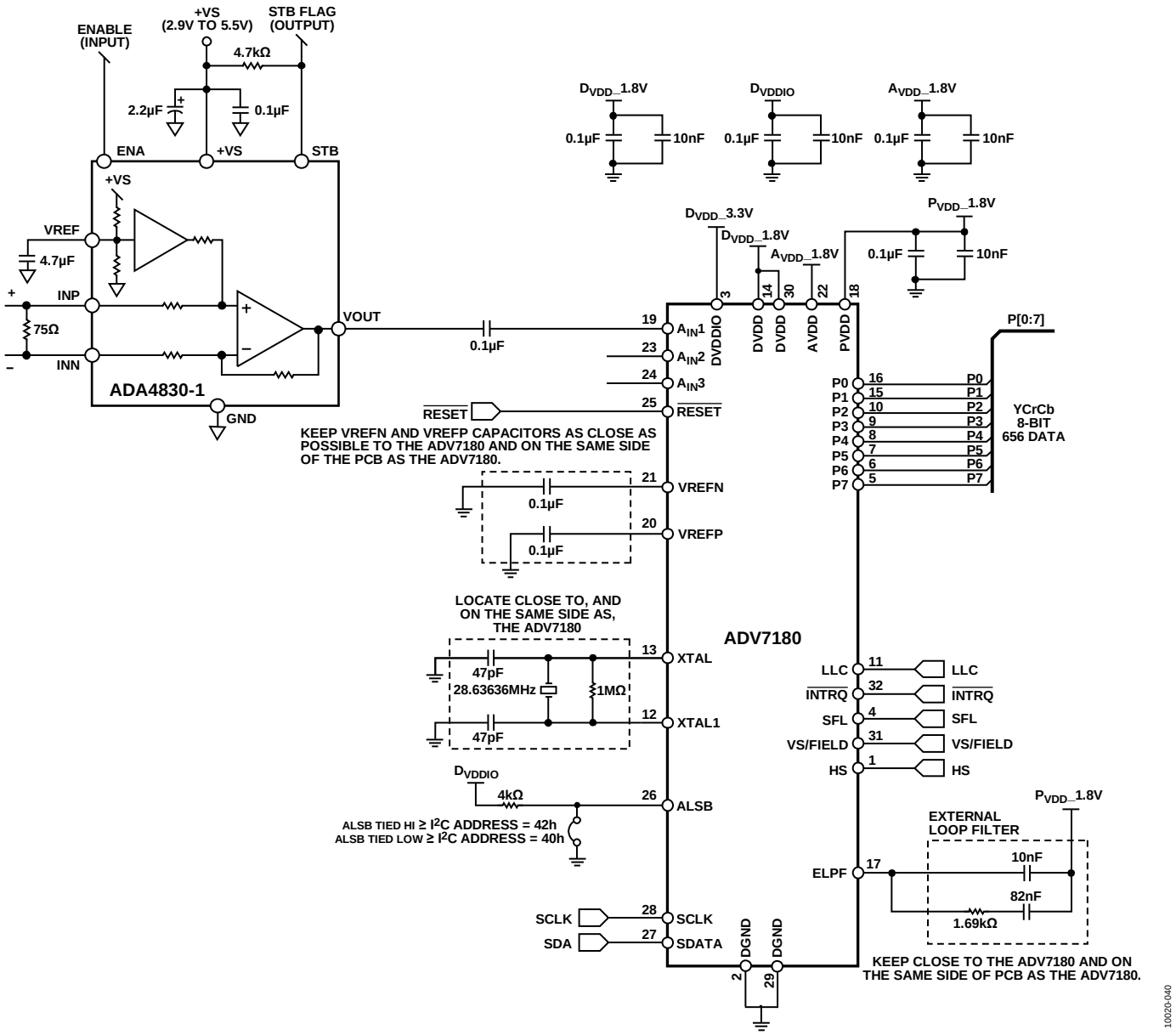

Figure 27. ADA4830-1 Driving an ADV7180 Video Decoder

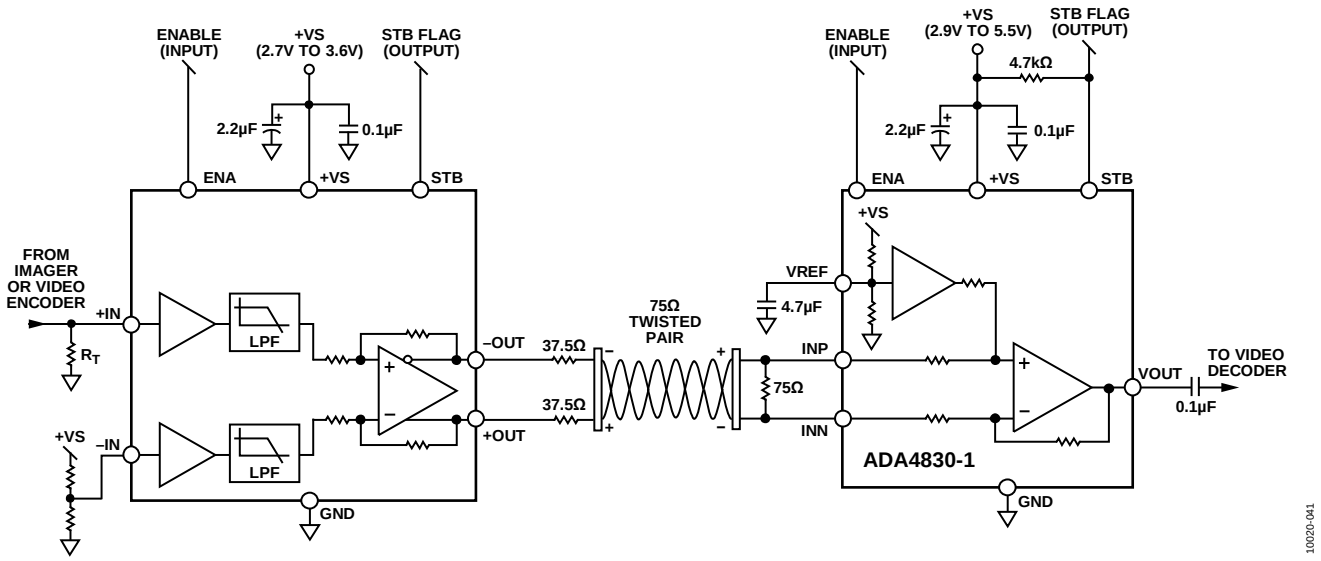

Figure 28. Differential Video Filter Driver and ADA4830-1 Difference Amplifier

PACKAGING AND ORDERING INFORMATION

OUTLINE DIMENSIONS

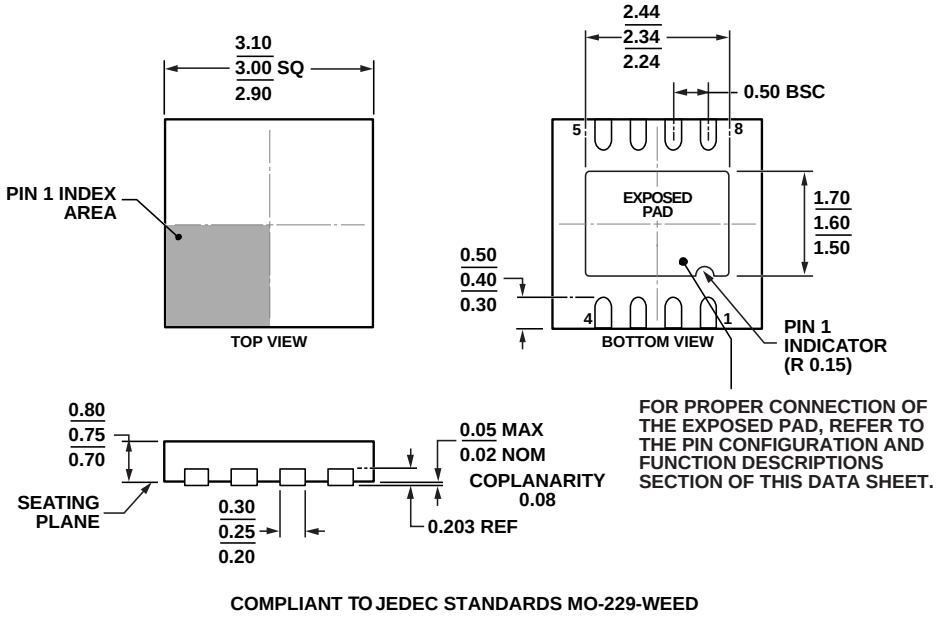

Figure 29.8-Lead Lead Frame Chip Scale Package [LFCSP]
(CP-8-11)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option	Branding	Ordering Quantity
ADA4830-1BCPZ-R7	−40°C to +125°C	8-Lead Lead Frame Chip Scale Package [LFCSP]	CP-8-11	H30	1,500
ADA4830-1BCPZ-R2	−40°C to +125°C	8-Lead Lead Frame Chip Scale Package [LFCSP]	CP-8-11	H30	250
ADA4830-1BCP-EBZ		Evaluation Board			

[1] Z = RoHS Compliant Part.

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