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November 2015

FCH125N60E

N-Channel SuperFET[®] II Easy-Drive MOSFET 600 V, 29 A, 125 m Ω

Features

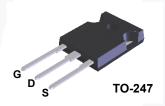
- 650 V @T_J = 150°C
- Typ. $R_{DS(on)}$ = 102 $m\Omega$
- Ultra Low Gate Charge (Typ. Q_g = 75 nC)
- Low Effective Output Capacitance (Typ. C_{oss(eff)} = 258 pF)
- · 100% Avalanche Tested
- · RoHS Compliant

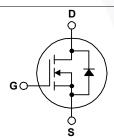
Applications

- · Telecom / Sever Power Supplies
- · Industrial Power Supplies

Description

SuperFET® II MOSFET is Fairchild Semiconductor's brand-new high voltage super-junction (SJ) MOSFET family that is utilizing charge balance technology for outstanding low on-resistance and lower gate charge performance. This technology is tailored to minimize conduction loss, provide superior switching performance, dv/dt rate and higher avalanche energy. Consequently, SuperFET II MOSFET easy-drive series offers slightly slower rise and fall times compared to the SuperFET II MOSFET series. Noted by the "E" part number suffix, this family helps manage EMI issues and allows for easier design implementation. For faster switching in applications where switching losses must be at an absolute minimum, please consider the SuperFET II MOSFET series.





Absolute Maximum Ratings T_C = 25°C unless otherwise noted.

Symbol		Parameter		FCH125N60E	Unit
V _{DSS}	Drain to Source Voltage			600	V
		- DC		±20	V
V_{GSS}	Gate to Source Voltage	- AC	(f > 1 Hz)	±30	V
	Drain Current	- Continuous (T _C = 25°C)		29	Δ.
ID	Drain Current	- Continuous (T _C = 100°C)		18	_ A
I _{DM}	Drain Current	- Pulsed	(Note 1)	87	Α
E _{AS}	Single Pulsed Avalanche Energy (Note 2)		720	mJ	
I _{AR}	Avalanche Current		(Note 1)	6	Α
E _{AR}	Repetitive Avalanche Energy	Repetitive Avalanche Energy (Note 1)		2.78	mJ
	MOSFET dv/dt			100	\//m=
dv/dt	Peak Diode Recovery dv/dt		(Note 3)	20	V/ns
D	Davis a Dia sin efficie	(T _C = 25°C)		278	W
P_{D}	Power Dissipation - Derate Above 25°C			2.2	W/°C
T _J , T _{STG}	Operating and Storage Temperature Range			-55 to +150	οС
T _L	Maximum Lead Temperature for	Soldering, 1/8" from Case for 5 S	econds	300	°C

Thermal Characteristics

Symbol	Parameter FCH125N60E			
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	0.45	°C/W	
$R_{ heta JA}$	Thermal Resistance, Junction to Ambient, Max.	40	*C/VV	

Package Marking and Ordering Information

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FCH125N60E	FCH125N60E	TO-247	Tube	N/A	N/A	30 units

Electrical Characteristics $T_C = 25^{\circ}C$ unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
Off Charac	cteristics					
BV _{DSS}	Drain to Source Breakdown Voltage	$V_{GS} = 0 \text{ V}, I_D = 10 \text{ mA}, T_J = 25^{\circ}\text{C}$	600	-	-	V
DVDSS	Drain to Source Breakdown voltage	$V_{GS} = 0 \text{ V}, I_D = 10 \text{ mA}, T_J = 150^{\circ}\text{C}$	650	-	-	V
ΔBV _{DSS} / ΔT _J	Breakdown Voltage Temperature Coefficient	I _D = 10 mA, Referenced to 25°C	-	0.7	-	V/°C
1	Zero Gate Voltage Drain Current	V _{DS} = 600 V, V _{GS} = 0 V	-	-	1	μА
IDSS	Zero Gate Voltage Drain Current	$V_{DS} = 480 \text{ V}, V_{GS} = 0 \text{ V}, T_{C} = 125^{\circ}\text{C}$	-	2	-	μΑ
I _{GSS}	Gate to Body Leakage Current	$V_{GS} = \pm 20 \text{ V}, V_{DS} = 0 \text{ V}$	-	-	±100	nA

On Characteristics

V _{GS(th)}	Gate Threshold Voltage	$V_{GS} = V_{DS}, I_{D} = 250 \mu A$	2.5	-	3.5	V
R _{DS(on)}	Static Drain to Source On Resistance	$V_{GS} = 10 \text{ V}, I_D = 14.5 \text{ A}$	-	102	125	mΩ
9 _{FS}	Forward Transconductance	$V_{DS} = 20 \text{ V}, I_{D} = 14.5 \text{ A}$	-	25	-	S

Dynamic Characteristics

C _{iss}	Input Capacitance	V 200 V V 0 V	-	2250	2990	pF
C _{oss}	Output Capacitance	$V_{DS} = 380 \text{ V}, V_{GS} = 0 \text{ V},$ f = 1 MHz		60	80	pF
C _{rss}	Reverse Transfer Capacitance	1 1 1 1 1 2	-\	17	-	pF
Coss(eff.)	Effective Output Capacitance	$V_{DS} = 0 \text{ V to } 480 \text{ V}, V_{GS} = 0 \text{ V}$	- \	258	-	pF
Q _{g(tot)}	Total Gate Charge at 10V	V _{DS} = 380 V, I _D = 14.5 A,	- \	75	95	nC
Q_{gs}	Gate to Source Gate Charge	V _{GS} = 10 V	-	10	-	nC
Q_{gd}	Gate to Drain "Miller" Charge	(Note 4)	-	33	-	nC
ESR	Equivalent Series Resistance	f = 1 MHz	-	3.5	-	Ω

Switching Characteristics

t _{d(on)}	Turn-On Delay Time			-	23	56	ns
t _r	Turn-On Rise Time	$V_{DD} = 380 \text{ V}, I_D = 14.5 \text{ A},$		- /	20	50	ns
t _{d(off)}	Turn-Off Delay Time	V_{GS} = 10 V, R_g = 4.7 Ω		-/	106	222	ns
t _f	Turn-Off Fall Time		(Note 4)	-	23	56	ns

Drain-Source Diode Characteristics

I _S	Maximum Continuous Drain to Source Dio	Maximum Continuous Drain to Source Diode Forward Current		-	29	Α
I _{SM}	Maximum Pulsed Drain to Source Diode Fo	Maximum Pulsed Drain to Source Diode Forward Current		-	87	Α
V_{SD}	Drain to Source Diode Forward Voltage	V _{GS} = 0 V, I _{SD} = 14.5 A	-	-	1.2	V
t _{rr}	Reverse Recovery Time	V _{GS} = 0 V, I _{SD} = 14.5 A,	-	376	-	ns
Q _{rr}	Reverse Recovery Charge	dI _F /dt = 100 A/μs	-	6.5	-	μС

Notes:

- 1. Repetitive rating: pulse width limited by maximum junction temperature.
- 2. I_{AS} = 6.0 A, R_{G} = 25 Ω , Starting T_{J} = 25°C
- 3. I $_{SD} \leq$ 14.5 A, di/dt \leq 200 A/µs, V $_{DD} \leq$ 380 V, Starting T $_{J}$ = 25°C
- 4. Essentially independent of operating temperature.

Typical Performance Characteristics

Figure 1. On-Region Characteristics

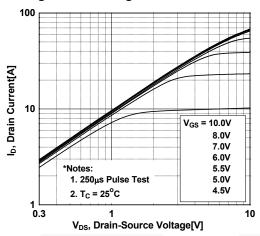


Figure 3. On-Resistance Variation vs.

Drain Current and Gate Voltage

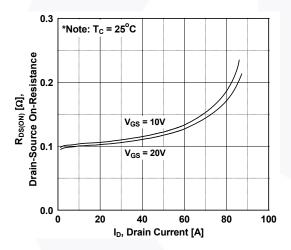


Figure 5. Capacitance Characteristics

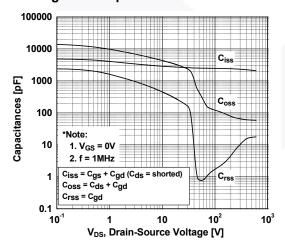


Figure 2. Transfer Characteristics

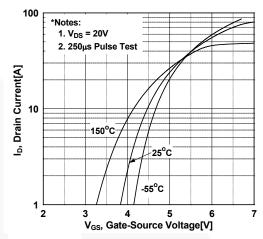


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

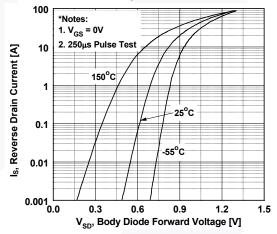
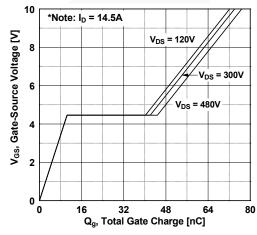


Figure 6. Gate Charge Characteristics



Typical Performance Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

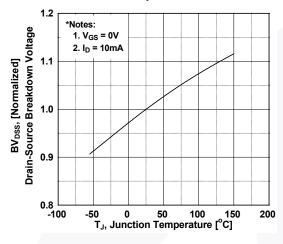


Figure 9. Maximum Safe Operating Area

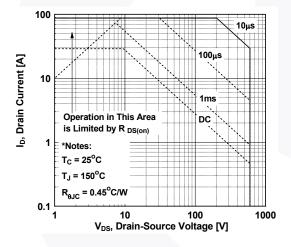


Figure 11. Eoss vs. Drain to Source Voltage

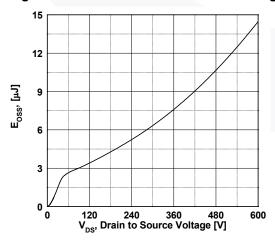


Figure 8. On-Resistance Variation vs. Temperature

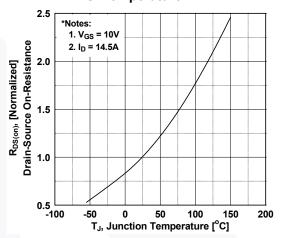
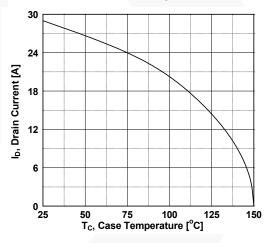
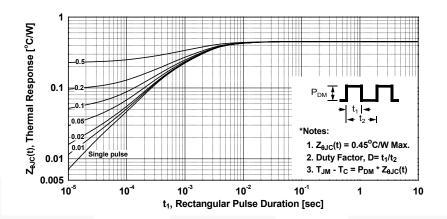


Figure 10. Maximum Drain Current vs. Case Temperature



Typical Performance Characteristics (Continued)

Figure 12. Transient Thermal Response Curve



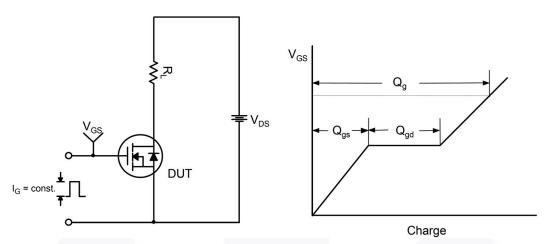


Figure 13. Gate Charge Test Circuit & Waveform

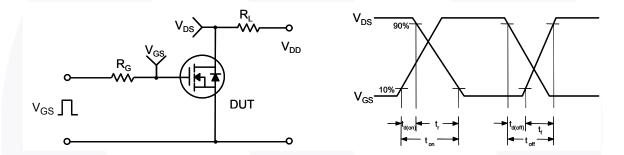


Figure 14. Resistive Switching Test Circuit & Waveforms

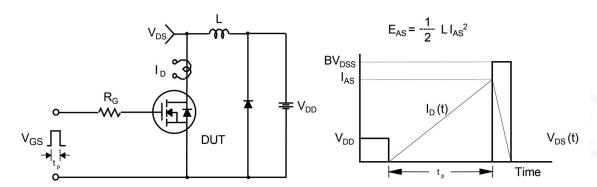


Figure 15. Unclamped Inductive Switching Test Circuit & Waveforms

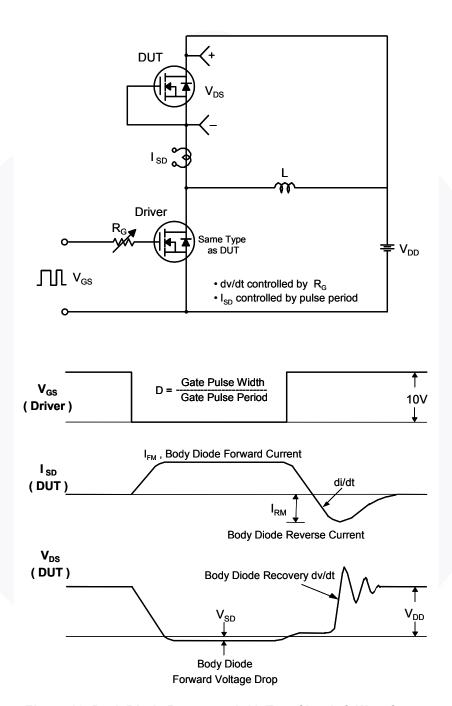
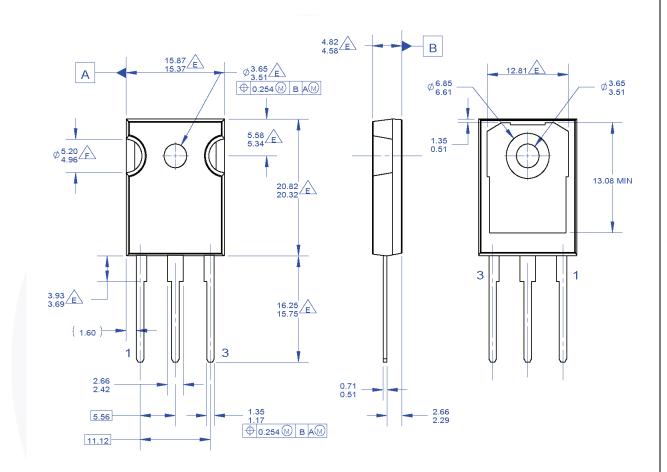


Figure 16. Peak Diode Recovery dv/dt Test Circuit & Waveforms

Mechanical Dimensions



NOTES: UNLESS OTHERWISE SPECIFIED.

- A. PACKAGE REFERENCE: JEDEC TO-247,
 ISSUE E, VARIATION AB, DATED JUNE, 2004.
 B. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
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- E DOES NOT COMPLY JEDEC STANDARD VALUE
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 - DRAWING FILENAME: MKT-TO247A03_REV03

Figure 17. TO-247, Molded, 3-Lead, Jedec Variation AB

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Definition of Terms

Datasheet Identification	Product Status	Definition
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