



# IS31PW8200

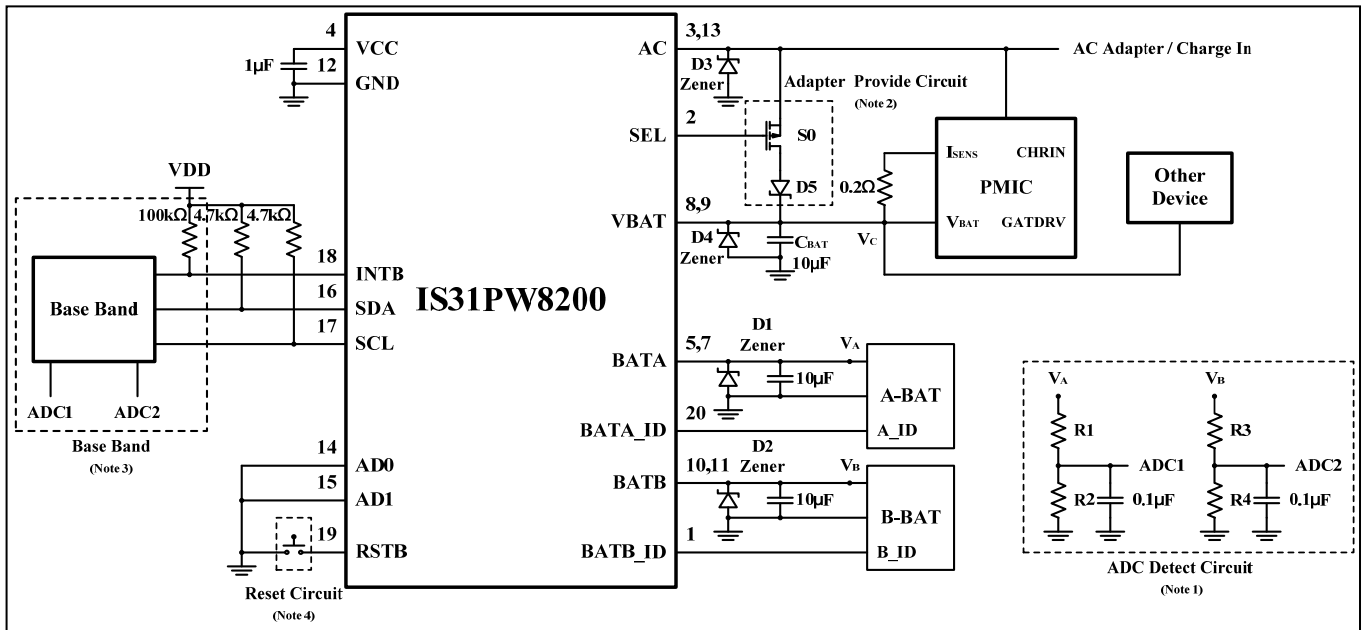


Figure 2 Typical Application Circuit

**Note 1:** Two ADC circuits can be used to detect the battery voltage. Connecting to the VC point if only one ADC. This circuit can be connected or not.

In MTK Platform, R1=R3=470kΩ, R2=R4=300kΩ. In Zhanxun Platform, R1=R3=470kΩ, R2=R4=100kΩ.

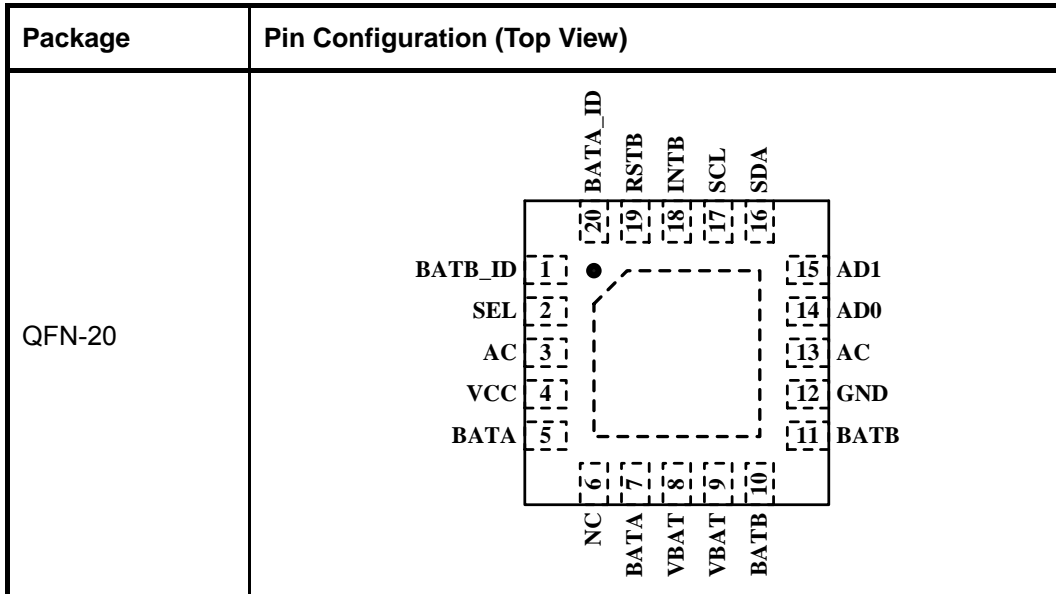
**Note 2:** The adapter provides power for system when the adapter plugs in and no batteries connected. Please refer to Page 12 to get the detail information. This circuit can be connected or not.

**Note 3:** Base Band can control and read the dual batteries information. Please refer to Page 9 to get the detail information. This circuit can be connected or not. Register configuration is default if there is no connection.

**Note 4:** If use the two-pin battery, BATA\_ID and BATB\_ID pins should connect a 10kΩ resistor to ground. Three-pin battery is recommended.

# IS31PW8200

## PIN CONFIGURATION



## PIN DESCRIPTION

Pin	Name	Function
1	BATB_ID	Indication that Li-ion Battery B is inserted.
2	SEL	Control output to the gate of the external PMOS for AC adapter input as power source.
3, 13	AC	AC adapter input.
4	VCC	Power supply.
5, 7	BATA	Battery A connection.
6	NC	No connect.
8, 9	VBAT	Current source output.
10, 11	BATB	Battery B connection.
12	GND	Ground.
14	AD0	Address input. Select device slave address.
15	AD1	Address input. Select device slave address.
16	SDA	I2C compatible serial data.
17	SCL	I2C compatible serial clock.
18	INTB	Interrupt output. Active low.
19	RSTB	Reset input. Active low. Cut the power path to PMU and reset I2C.
20	BATA_ID	Indication that Li-ion Battery A is inserted.
	Thermal Pad	Connect to GND.



# IS31PW8200

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## ORDERING INFORMATION

**INDUSTRIAL RANGE: -40°C TO +85°C**

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Order Part No.	Package	QTY/Reel
IS31PW8200-QFLS2-TR	QFN-20, Lead-free	2500

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# IS31PW8200

## ABSOLUTE MAXIMUM RATINGS

Supply voltage, AC, BATA, BATB	-0.3V ~ +6.0V
Voltage at any input pin	-0.3V ~ +6.0V
Maximum junction temperature, $T_{JMAX}$	150°C
Operating temperature range, $T_A$	-40°C ~ +85°C
Storage temperature range, $T_{STG}$	-65°C ~ +150°C
ESD (HBM)	1kV
ESD (CDM)	1kV

### Note:

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## DC CHARACTERISTICS

$T_A = -40^\circ\text{C} \sim +85^\circ\text{C}$ ,  $V_{CC} = 2.4\text{V} \sim 5.5\text{V}$ , unless otherwise noted. Typical value are  $T_A = +25^\circ\text{C}$ . (Note 5)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
$V_{CC}$	Supply voltage		2.4		5.5	V
$V_{TH1}$	Switch threshold voltage 1	$V_{TH1}$ bit set to "0" in Configuration Register(01h)	3.44	3.5	3.56	V
$V_{TH2}$	Switch threshold voltage 2	$V_{TH2}$ bit set to "0" in Configuration Register(01h)		3.2		V
$V_{HY}$	$V_{TH1}$ hysteresis voltage	HV bit set to "0" in Configuration Register(01h)		0.1		V
$I_{CC}$	Quiescent current	$V_{BATA} = V_{BATB} = 4.2\text{V}$ Without adapter plugging in		100		$\mu\text{A}$
		$V_{BATA} = V_{BATB} = 4.2\text{V}$ With Adapter plugging in			5	mA
$t_D$	$V_{TH1}$ switching timing delay	Page 11		2		ms
$I_{CH}$	Charge current		95	120	155	mA
$V_{OVP}$	Over voltage protect			4.1	4.3	V
$R_{DS(ON)}$	On resistance of MOSFET			100		m $\Omega$
$t_{SW}$	Switching delay		120	150	180	ns

### Logic Electrical Characteristics (SDA, SCL, AD0, AD1, INTB)

$V_{IH}$	Input high voltage		1.4			V
$V_{IL}$	Input low voltage				0.4	V
$I_{IH}, I_{IL}$	Input leakage current		-0.2		0.2	$\mu\text{A}$
$C_{IN}$	Input capacitance(Note 6)			10		pF
$V_{OLSDA}$	Output low voltage SDA	$I_{SINK} = 6\text{mA}$			180	mV
$V_{OLINT}$	Output low-voltage INTB	$I_{SINK} = 5\text{mA}$			180	mV

# IS31PW8200

## DIGITAL INPUT SWITCHING CHARACTERISTICS (Note 6)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
$f_{SCL}$	Serial-Clock frequency				400	kHz
$t_{BUF}$	Bus free time between a STOP and a START condition		1.3			$\mu$ s
$t_{HD, STA}$	Hold time (repeated) START condition		0.6			$\mu$ s
$t_{SU, STA}$	Repeated START condition setup time		0.6			$\mu$ s
$t_{SU, STO}$	STOP condition setup time		0.6			$\mu$ s
$t_{HD, DAT}$	Data hold time	(Note 7)			0.9	$\mu$ s
$t_{SU, DAT}$	Data setup time		100			ns
$t_{LOW}$	SCL clock low period		1.3			$\mu$ s
$t_{HIGH}$	SCL clock high period		0.7			$\mu$ s
$t_R$	Rise time of both SDA and SCL signals, receiving	(Note 8)		$20+0.1C_b$	300	ns
$t_F$	Fall time of both SDA and SCL signals, receiving	(Note 8)		$20+0.1C_b$	300	ns
$t_{F, TX}$	Fall time of SDA transmitting	(Note 8)		$20+0.1C_b$	250	ns
$t_{SP}$	Pulse width of spike suppressed	(Note 9)		50		ns
$C_b$	Capacitive load for each bus line				400	pF
$t_W$	RSTB pulse width		500			ns
$t_{RSTB}$	RSTB rising to START condition setup time		1			ns

**Note 5:** All parameters are tested at  $T_A = 25^\circ\text{C}$ . Specifications over temperature are guaranteed by design.

**Note 6:** Guaranteed by design.

**Note 7:** A master device must provide a hold time of at least 300ns for the SDA signal (referred to  $V_{IL}$  of the SCL signal) in order to bridge the undefined region of SCL's falling edge.

**Note 8:**  $C_b$  = total capacitance of one bus line in pF.  $I_{SINK} \leq 6\text{mA}$ .  $t_R$  and  $t_F$  measured between  $0.3 \times V_{CC}$  and  $0.7 \times V_{CC}$ .

**Note 9:** Input filters on the SDA and SCL inputs suppress noise spikes less than 50ns.

# IS31PW8200

## DETAILED DESCRIPTION

### I2C INTERFACE

The IS31PW8200 uses a serial bus, which conforms to the I2C protocol, to control the chip's functions with two wires: SCL and SDA. The IS31PW8200 has a 7-bit slave address (A7:A1), followed by the R/W bit, A0. Set A0 to "0" for a write command and set A0 to "1" for a read command. The bit A2:A1 are selected by the connection of AD1/AD0 pin.

The complete slave address is:

**Table 1 Slave Address:**

Bit	A7:A3	A2	A1	A0
Value	10111	AD1	AD0	1/0

AD1/AD0 connects to VCC, AD1/AD0=1;

AD1/AD0 connects to GND, AD1/AD0=0;

The SCL line is uni-directional. The SDA line is bi-directional (open-collector) with a pull-up resistor (typically 4.7kΩ). The maximum clock frequency specified by the I2C standard is 400kHz. In this discussion, the master is the microcontroller and the slave is the IS31PW8200.

The timing diagram for the I2C is shown in Figure 3. The SDA is latched in on the stable high level of the SCL. When there is no interface activity, the SDA line should be held high.

The "START" signal is generated by lowering the SDA signal while the SCL signal is high. The start signal will alert all devices attached to the I2C bus to check the incoming address against their own chip address.

The 8-bit chip address is sent next, most significant bit first. Each address bit must be stable while the SCL level is high.

After the last bit of the chip address is sent, the master checks for the IS31PW8200's acknowledge. The

master releases the SDA line high (through a pull-up resistor). Then the master sends an SCL pulse. If the IS31PW8200 has received the address correctly, then it holds the SDA line low during the SCL pulse. If the SDA line is not low, then the master should send a "STOP" signal (discussed later) and abort the transfer.

Following acknowledge of IS31PW8200, the register address byte is sent, most significant bit first. IS31PW8200 must generate another acknowledge indicating that the register address has been received.

Then 8-bit of data byte are sent next, most significant bit first. Each data bit should be valid while the SCL level is stable high. After the data byte is sent, the IS31PW8200 must generate another acknowledge to indicate that the data was received.

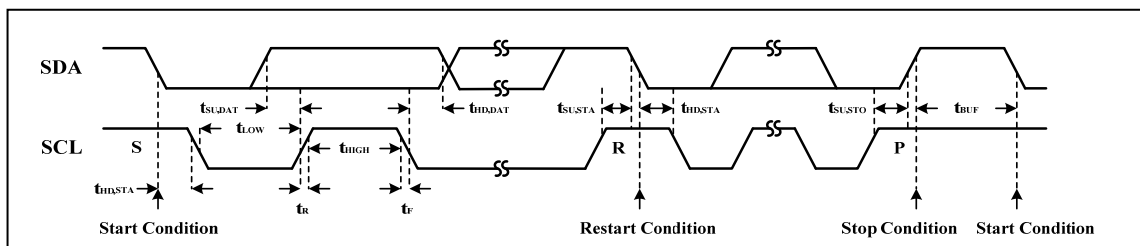
The "STOP" signal ends the transfer. To signal "STOP", the SDA signal goes high while the SCL signal is high.

### WRITING TO THE REGISTERS

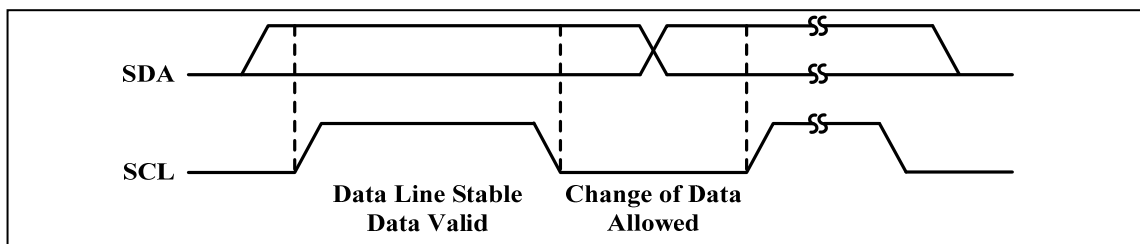
Transmit data to the IS31PW8200 by sending the device slave address and setting the LSB to "0". The command byte is sent after the address and determines which registers receive the data following the command byte.

### READING PORT REGISTERS

To read the device data, the bus master must first send the IS31PW8200 address with the R/W bit set to "0", followed by the command byte, which determines which register is accessed. After a restart, the bus master must then send the IS31PW8200 address with the R/W bit set to "1". Data from the register defined by the command byte is then sent from the IS31PW8200 to the master (Figure 6).



**Figure 3** Interface Timing



**Figure 4** Bit Transfer

# IS31PW8200

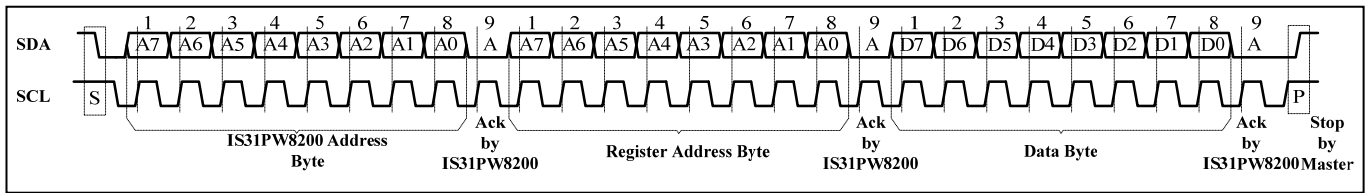


Figure 5 Writing to IS31PW8200

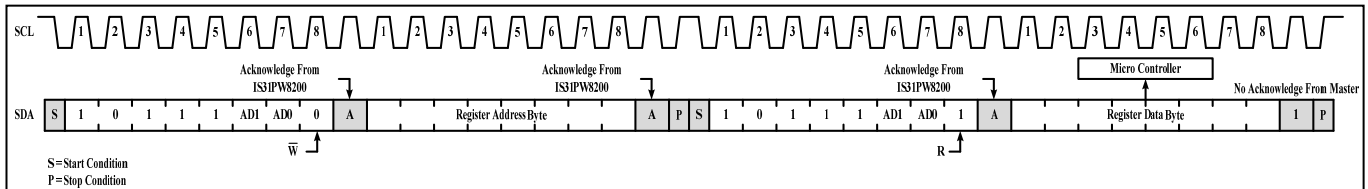


Figure 6 Reading from IS31PW8200

## REGISTERS DEFINITIONS

Table 2 Register Function

Address	Name	Function	Table	R/W	Default
00h	State Register	Store the state of batteries	3	R	-
01h	Configuration Register	Set the operation voltage and power selection	4	R/W	xx00 0000
0Fh	Reset Register	Reset all registers to default value	-	W	xxxx xxxx

Table 3 00h State Register (Read only)

Bit	D7	D6	D5:D4	D3:D2	D1:D0
Name	BI	AI	BS	BVD	AVD
R/W	R				
Default	-				

The State Register stores the state information for A-BAT and B-BAT.

**BI** B-BAT ID Connection  
 0 Battery in (BATB-ID is high)  
 1 Battery out (BATB-ID is low)

**AI** A-BAT ID Connection  
 0 Battery in (BATA-ID is high)  
 1 Battery out (BATA-ID is low)

**BS** Battery State  
 00 A-BAT Connect  
 01 B-BAT Connect  
 11 Both A-BAT and B-BAT disconnect and AC adapter supply power  
 Others Not available

**BVD** B-BAT Voltage Detection  
 00  $V_{B-BAT} < V_{TH2}$   
 01  $V_{TH2} < V_{B-BAT} < V_{TH1}$   
 10  $V_{TH1} < V_{B-BAT} < 4.2V$   
 11  $V_{B-BAT} \geq 4.2V$

**AVD** A-BAT Voltage Detection  
 00  $V_{A-BAT} < V_{TH2}$   
 01  $V_{TH2} < V_{A-BAT} < V_{TH1}$   
 10  $V_{TH1} < V_{A-BAT} < 4.2V$   
 11  $V_{A-BAT} \geq 4.2V$



# IS31PW8200

**Table 4 01h Configuration Register**

Bit	D7	D5	D5:D4	D3:D2	D1	D0
Name	SB	SA/CS	PS	HV	V <sub>TH1</sub>	V <sub>TH2</sub>
R/W	R	R/W	W	W	W	W
Default	-	-/0	00	00	0	0

The Configuration Register sets operating mode and the power source.

**SB** Internal Charger Charge up for B-BAT (Read only)

0 Charge  
1 Off

**SA(R)** Hysteresis Voltage Charge up for A-BAT (Read only)

0 Charge  
1 Off

**CS(W)** Internal Charger Control

0 On  
1 Off

**PS** Power Selection

00 Default  
01 A-BAT  
10 B-BAT  
Others Not available

**HV** Hysteresis Voltage for V<sub>TH1</sub>

00 0.10V  
10 0.05V  
Others Not available

**V<sub>TH1</sub>** Threshold Voltage 1

0 3.5V  
1 3.6V

**V<sub>TH2</sub>** Threshold Voltage 2

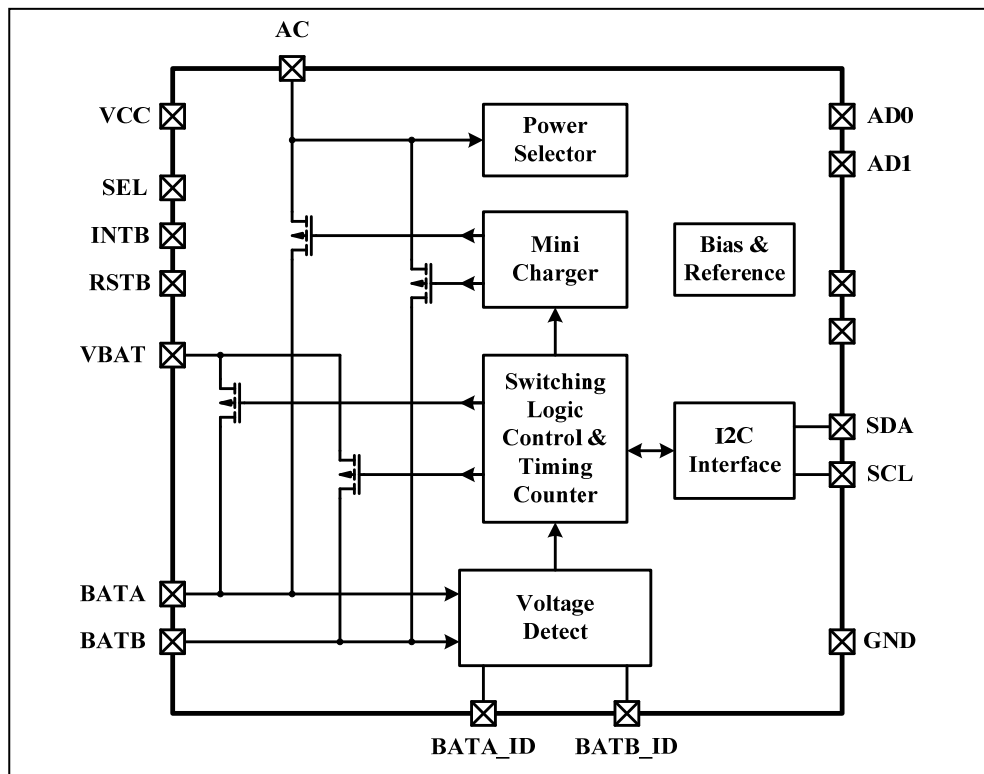
0 3.2V  
1 3.3V

### 0Fh Reset Register

Once user writes "0000 0000" data to the Reset Register, IS31PW8200 will reset all registers to their default value. On initial power-up, the IS31PW8200 registers are reset to their default values.

# IS31PW8200

## FUNCTIONAL BLOCK DIAGRAM



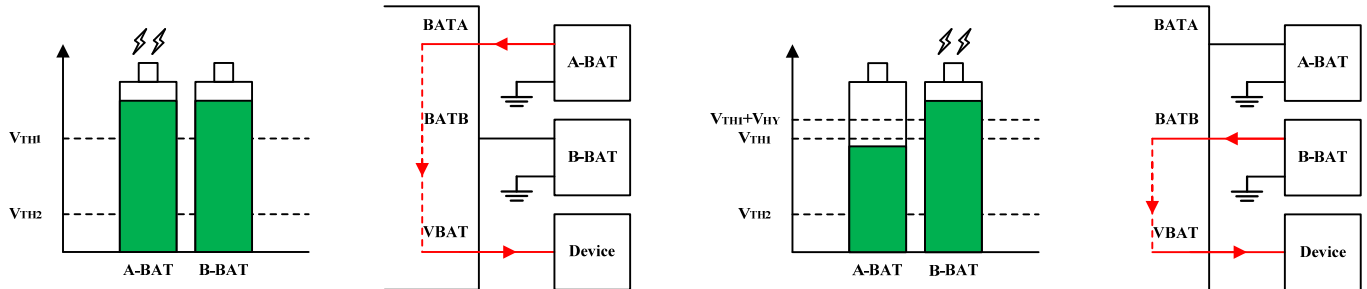
# IS31PW8200

## APPLICATION INFORMATION

### DUAL BATTERIES SWITCHING FOR PROVIDING POWER

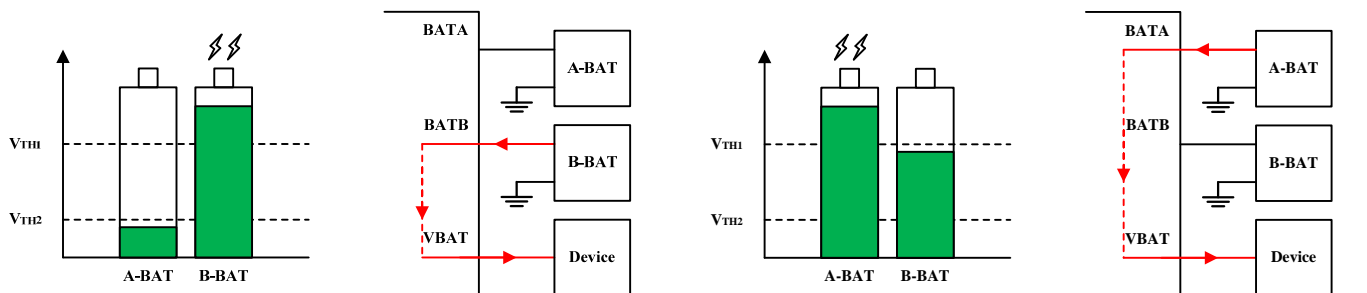
The IS31PW8200 highly integrated IC serves as the control logic for a system with multiple power sources. It selects the power path for the system and manages dual battery sources for charge and discharge.

#### SWITCH CONDITION IN DISCHARGE MODE (WITHOUT ADAPTER PLUGGED IN):



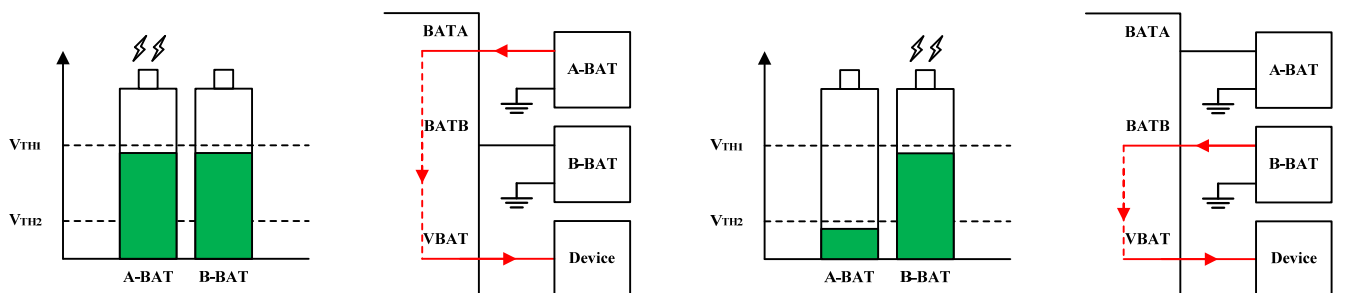
State 1: If  $V_{A-BAT} \geq V_{TH1}$  and  $V_{B-BAT} \geq V_{TH1}$ , A-BAT provides power.

State 2: If  $V_{A-BAT} \leq V_{TH1}$  and lasts for  $t_D$  and  $V_{B-BAT} \geq V_{TH1} + V_{HY}$ , switch to B-BAT providing power.



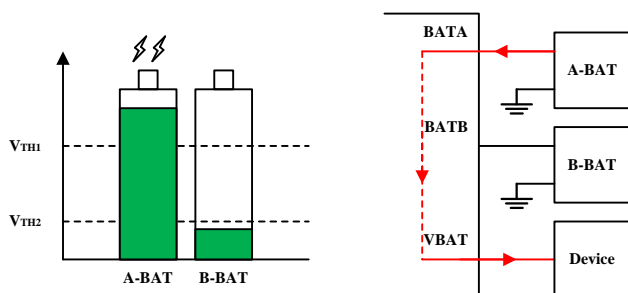
State 3: If  $V_{A-BAT} \leq V_{TH2}$  and  $V_{B-BAT} \geq V_{TH1}$ , switch to B-BAT providing power immediately.

State 4: If  $V_{A-BAT} \geq V_{TH1}$  and  $V_{TH2} \leq V_{B-BAT} \leq V_{TH1}$ , A-BAT provides power.



State 5: If  $V_{TH2} \leq V_{A-BAT} \leq V_{TH1}$  and  $V_{TH2} \leq V_{B-BAT} \leq V_{TH1}$ , A-BAT provides power.

State 6: If  $V_{A-BAT} \leq V_{TH2}$  and  $V_{TH2} \leq V_{B-BAT} \leq V_{TH1}$ , switch to B-BAT providing power.



State 7: If  $V_{B-BAT} \leq V_{TH2}$ , A-BAT provides power all the time.

Note: When  $V_{A-BAT}$  and  $V_{B-BAT}$  are both higher than  $V_{TH2}$ , IS31PW8200 can force switching the battery source by setting the PS bit in Configuration Register (01h).

After forcing a battery selection, the system will continue to automatically choose the supply battery in accordance with the conditions as described if the battery's voltage falls below  $V_{TH2}$ , until the voltage returns back to  $V_{TH2}$  again making the selected battery available.

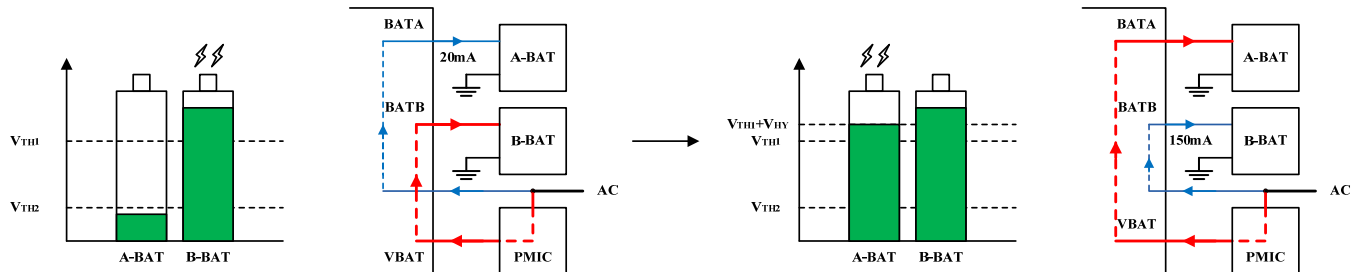
# IS31PW8200

## SWITCH CONDITION IN CHARGE MODE (WITH ADAPTER PLUGGED IN):

Charge rules:

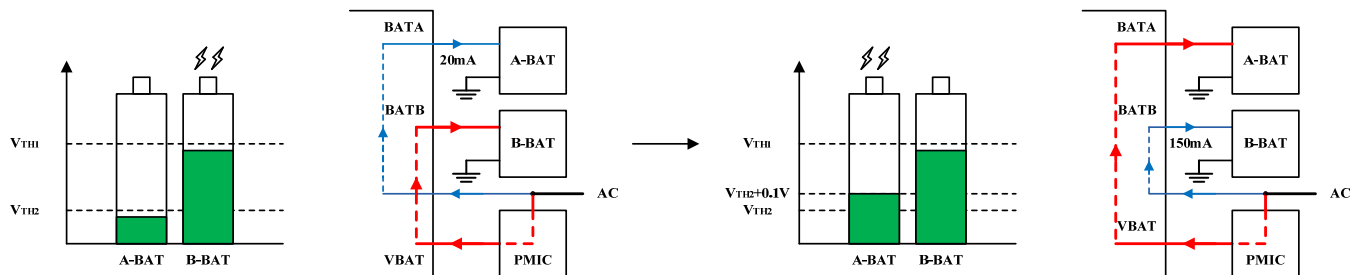
When the adapter is plugged in, the PMIC charges the supply battery and the internal charger provides a small current for the unused battery. Internal charger provides a 20mA current for the unused battery which below  $V_{TH2}$  until the voltage of the battery reaches  $V_{TH2}$  then provides a 150mA current.

The voltage of battery changes during charging. The charging rules should follow the switch condition below. The internal charger will disconnect automatically if batteries are both full.



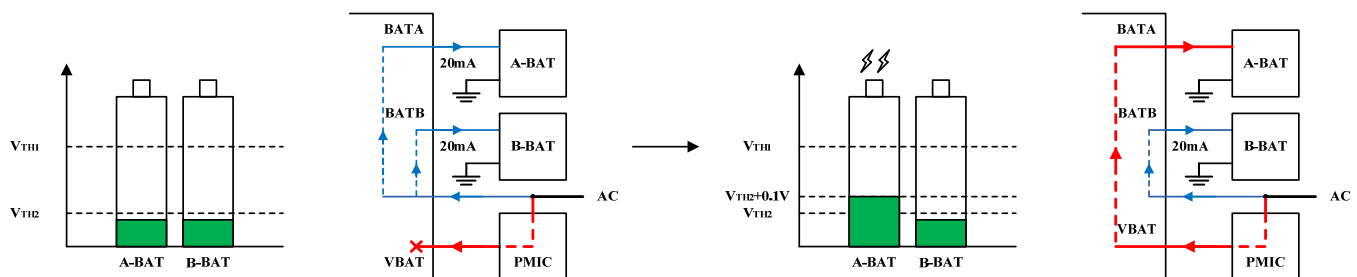
**State 1:** If  $V_{A-BAT} \leq V_{TH2}$  and  $V_{B-BAT} \geq V_{TH1}$ , B-BAT provides power. The PMIC charges up B-BAT and IS31PW8200 provides small current (20mA) for A-BAT by internal charger at the same time. The battery source will not switch until  $V_{A-BAT}$  reaches to  $V_{TH1}+V_{HY}$ .

**State 2:** If  $V_{A-BAT}$  charges up to  $V_{TH1}+V_{HY}$  and  $V_{B-BAT} \geq V_{TH1}$ , switch to A-BAT providing power. The PMIC charges up A-BAT and IS31PW8200 provides small current (150mA) for B-BAT by internal charger at the same time until batteries are both full.



**State 3:** If  $V_{A-BAT} \leq V_{TH2}$  and  $V_{TH2} \leq V_{B-BAT} \leq V_{TH1}$ , B-BAT provides power. The PMIC charges up for B-BAT and IS31PW8200 provides small current (20mA) for A-BAT by internal charger at the same time. The battery source will not switch until  $V_{A-BAT}$  reaches  $V_{TH2}+0.1V$ .

**State 4:** If  $V_{A-BAT}$  charges up to  $V_{TH2}+0.1V$  and  $V_{TH2} \leq V_{B-BAT} \leq V_{TH1}$ , switch to A-BAT providing power. The PMIC charges up for A-BAT and IS31PW8200 provides small current (150mA) for B-BAT by internal charger at the same time until batteries are both full.



**State 5:** If  $V_{A-BAT} \leq V_{TH2}$  and  $V_{B-BAT} \leq V_{TH2}$ , dual batteries disconnect with VBAT. At this moment, the PMIC doesn't charge up any batteries and IS31PW8200 provides small current (20mA) for dual batteries by internal charger until one of batteries is charged up to  $V_{TH2}+0.1V$  and offer power by this battery.

**State 6:** If  $V_{A-BAT}$  charges up to  $V_{TH2}+0.1V$  first and  $V_{B-BAT} \leq V_{TH2}$ , A-BAT provides power. The PMIC charges up A-BAT and IS31PW8200 provides small current (20mA) for B-BAT by internal charger at the same time until batteries are both full. It operates opposition situation if  $V_{B-BAT}$  charges up to  $V_{TH2}+0.1V$  first.

Note: Stop charging when the B-BAT is full. If  $V_{B-BAT}$  falls below 4.0V for a period of more than 2s, B-BAT resumes charging again.

## APPLICATIONS

IS31PW8200 can be used in multiple application configurations, for example, as shown in Figure 1 and Figure 2. Switching between the batteries follows the switching conditions as described above.

1. External battery: A-BAT is the external battery, such as in a cell phone cover, and B-BAT is the internal battery.
2. Built-in battery: A-BAT is a removable battery, and B-BAT is the permanent battery, both located inside of the mobile device.
3. Single battery: Either A-BAT and B-BAT can be used.

Note, for different cell phone systems, a low power warning or shutdown warning may occur even if the major battery's voltage doesn't fall below  $V_{TH1}$ . To handle this situation, forced switching of the supply battery via I2C interface by setting the PS bit in Configuration Register (01h) is available.

## HYSTERESIS VOLTAGE

The hysteresis voltage is used to prevent continual switching between the two batteries and to ensure that A-BAT provides power as the major power source. If the voltage of the providing battery drops below the threshold voltage causing the power path to switch, it will switch back when the voltage returns to the threshold voltage plus the hysteresis voltage.

Setting the HV bits of Configuration Register (01h) configures the hysteresis voltage,  $V_{HY}$ . If the HV bits are set to "00",  $V_{HY} = 0.1V$ . If the HV bits are set to "01",  $V_{HY} = 0.05V$ .  $V_{HY}$  is the hysteresis voltage for  $V_{TH1}$  and the hysteresis voltage of  $V_{TH2}$  is fixed at 0.1V.

## REGISTER FUNCTION CONFIGURATION

Configure the operating mode by setting the Configuration Register (01h).

By setting the CS bit to "0", the internal charger is on. When the CS bit is set to "1", the internal charger is off.

The PS bit is used to configure the power supply source. If the PS bits are set to "00", the system selects the power supply source automatically in accordance with the switch conditions described earlier. If the PS bits are set to "01", the system forces A-BAT to be the power supply source, and, finally, if the PS bits are set to "10" the system selects B-BAT to be the power supply source. Note that the forced power source selection is only valid if both  $V_{A-BAT}$  and  $V_{B-BAT}$  are higher than  $V_{TH2}$ . When both  $V_{A-BAT}$  and  $V_{B-BAT}$  are lower than  $V_{TH2}$  the cell phone will normally be shutdown. After connecting the charger, both  $V_{A-BAT}$  and  $V_{B-BAT}$  will begin charging. After both  $V_{A-BAT}$  and  $V_{B-BAT}$  are higher than  $V_{TH2}$  the IS31PW8200 will select the appropriate battery based on the existing

register content.

The  $V_{TH1}$  bit is used to set the threshold voltage,  $V_{TH1}$ . If  $V_{TH1}$  is set to "0",  $V_{TH1} = 3.5V$ . If  $V_{TH1}$  is set to "1",  $V_{TH1} = 3.6V$ .

The  $V_{TH2}$  bit is used to set the threshold voltage,  $V_{TH2}$ . If  $V_{TH2}$  is set to "0",  $V_{TH2} = 3.2V$ . If  $V_{TH2}$  is set to "1",  $V_{TH2} = 3.3V$ .

## BATTERIES STATE INFORMATION

State Register (00h) is a read-only register, storing the state information for both batteries.

The BI bit indicates the B-BAT connection state. If BATB\_ID is pulled to high, the BI bit is set to "0". If BATB\_ID is pulled to low, the BI bit is set to "1".

The AI bit indicates the A-BAT connection state. If BATA\_ID is pulled to high, the AI bit is set to "0". If BATA\_ID is pulled to low, the AI bit is set to "1".

The BS bits are used to show the battery state. If A-BAT provides power, the BS bits are set to "00". If B-BAT provides power, the BS bits are set to "01". If the power supply is provided by the adapter and no connection with A-BAT and B-BAT, the BS bits are set to "11".

The BVD bits show the voltage state of B-BAT. If  $V_{B-BAT} < V_{TH2}$ , the BVD bits are set to "00". If  $V_{TH2} < V_{B-BAT} < V_{TH1}$ , the BVD bits are set to "01". If  $V_{TH1} < V_{B-BAT} < 4.2V$ , the BVD bits are set to "10". If  $V_{B-BAT} \geq 4.2V$ , the BVD bits are set to "11".

The AVD bits show the voltage state of A-BAT. If  $V_{A-BAT} < V_{TH2}$ , the AVD bits are set to "00". If  $V_{TH2} < V_{A-BAT} < V_{TH1}$ , the AVD bits are set to "01". If  $V_{TH1} < V_{A-BAT} < 4.2V$ , the AVD bits are set to "10". If  $V_{A-BAT} \geq 4.2V$ , the AVD bits are set to "11".

The SA and SB bits are the read-only bit, storing the charging state of the internal charger.

The SA bit shows the A-BAT charging state of the internal charger. If the internal charger is charging A-BAT, the SA bit is set to "0". Conversely if the internal charger is not charging A-BAT, the SA bit is set to "1".

The SB bit shows the B-BAT charging state by internal charger. If the internal charger is charging B-BAT, the SB bit is set to "0". Conversely if the internal charger is not charging B-BAT, the SB bit is set to "1".

Note, the SA bit and the CS bit are the same bit in Configuration Register (01h) which corresponding to reading and writing operation (Table 4). The internal charger can be controlled by the CS bit. Setting the CS bit to "1" shuts down the internal charger and, thus, it will not charge either of the batteries. In this case, both the SA and SB bits will be set to "1". If the internal charger is on, the SA and SB bits will indicate which batteries are being charged by the internal charger.

# IS31PW8200

## INTERRUPT FUNCTION

A latching interrupt output, INTB, is programmed to flag battery status changes. At start up, the IS31PW8200 will always assert the INTB. This ensures that the baseband will read the initial status of the batteries, as well as clear the interrupt signal. Any subsequent changes to the battery status will cause the INTB to be asserted. The state register will report the current status of the batteries even if the event causing the interrupt to be asserted has been cleared prior to the baseband reading the register and clearing the latched INTB signal.

## BATTERY HOT-SWAP SOLUTION

The IS31PW8200 supports battery hot-swapping to ensure that the cell phone will not be shutdown during a battery change. IS31PW8200 will switch to the other battery as the power source if the supply battery is removed. In this case, the system will assert the interrupt indicating the batteries state changes.

## HARDWARE RESET FUNCTION

IS31PW8200 has hardware reset function to handle the case where mobile device operating system is locked-up. Pulling the RSTB pin to low resets the IS31PW8200 to the default conditions and will follow the normal startup procedure once the RSTB pin is returned to a high level.

## SINGLE BATTERY APPLICATION

For platform applications, there are certain cases where a single platform may be used for either single battery or dual battery applications. In the single battery applications, there is no need for the IS31PW8200 to be installed. Figure 7 shows the application circuit for a single battery. There is a 0Ω resistor between A-BAT/B-BAT and VBAT which must be installed for single battery applications.

**Note:** For dual battery applications, the IS31PW8200 is installed and the 0Ω resistors are not.

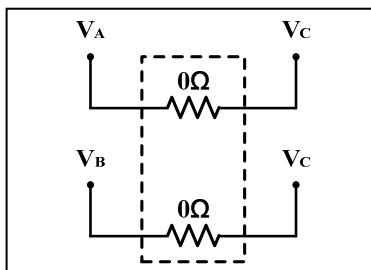


Figure 7 Single Battery Application Circuit

## DESIGN NOTE

### COMPONENT SELECTION

D1~D4 are the zener diodes using to prevent destroying the IC by high voltage. They should be placed close to the IC. D3 is used to prevent damage resulting from high voltage on the AC pin. The SOD-323 package is recommended.

When using the single battery configuration (Figure 7), take care to ensure a sufficient current rating for the 0Ω resistor(s). Three parallel 0Ω resistors in 0402 package or one 0Ω resistor in 0805 package are recommended.

The switching speed of IS31PW8200 can be 150ns.  $C_{BAT}$  in 10μF should be recommended.

All the capacitors should have a voltage rating of at least 10V.

In certain mobile applications it is acceptable to drive the mobile device directly from the AC adapter output. In these cases, the adapter providing circuit (PMOS + diode) must be installed. The FDFMA2P853 integrates a PMOS and diode into a single package to apply the AC adapter output directly to the VBAT pin. Please refer to the datasheet of the FDFMA2P853 to get more detailed information.

### PCB LAYOUT

The zener diode, D1~D4 and the capacitors for A-BAT and B-BAT should be placed close to the IC. The trace of BAT-ID should be shielded to reduce interference and noise. All the traces connected to the BATA, BATB and VBAT pins should be as short and wide as possible.

Trace width should be at least 0.8mm when the current reaches 2A. Trace width should be at least 1.5mm when the current reaches 4A. Trace width should be at least 1.0mm for the power supply and the ground plane.

# IS31PW8200

## CLASSIFICATION REFLOW PROFILES

Profile Feature	Pb-Free Assembly
<b>Preheat &amp; Soak</b> Temperature min (T <sub>smn</sub> ) Temperature max (T <sub>smax</sub> ) Time (T <sub>smn</sub> to T <sub>smax</sub> ) (t <sub>s</sub> )	150°C 200°C 60-120 seconds
Average ramp-up rate (T <sub>smax</sub> to T <sub>p</sub> )	3°C/second max.
Liquidous temperature (T <sub>L</sub> ) Time at liquidous (t <sub>L</sub> )	217°C 60-150 seconds
Peak package body temperature (T <sub>p</sub> )*	Max 260°C
Time (t <sub>p</sub> )** within 5°C of the specified classification temperature (T <sub>c</sub> )	Max 30 seconds
Average ramp-down rate (T <sub>p</sub> to T <sub>smax</sub> )	6°C/second max.
Time 25°C to peak temperature	8 minutes max.

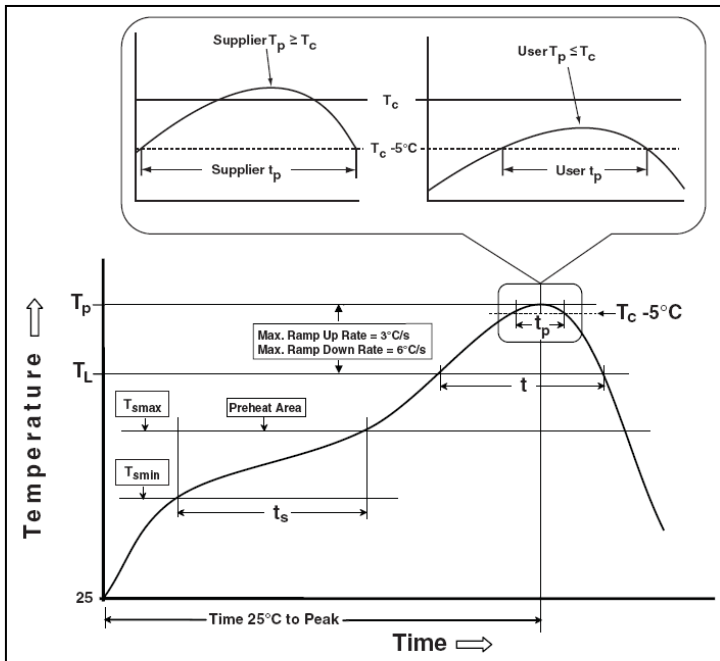
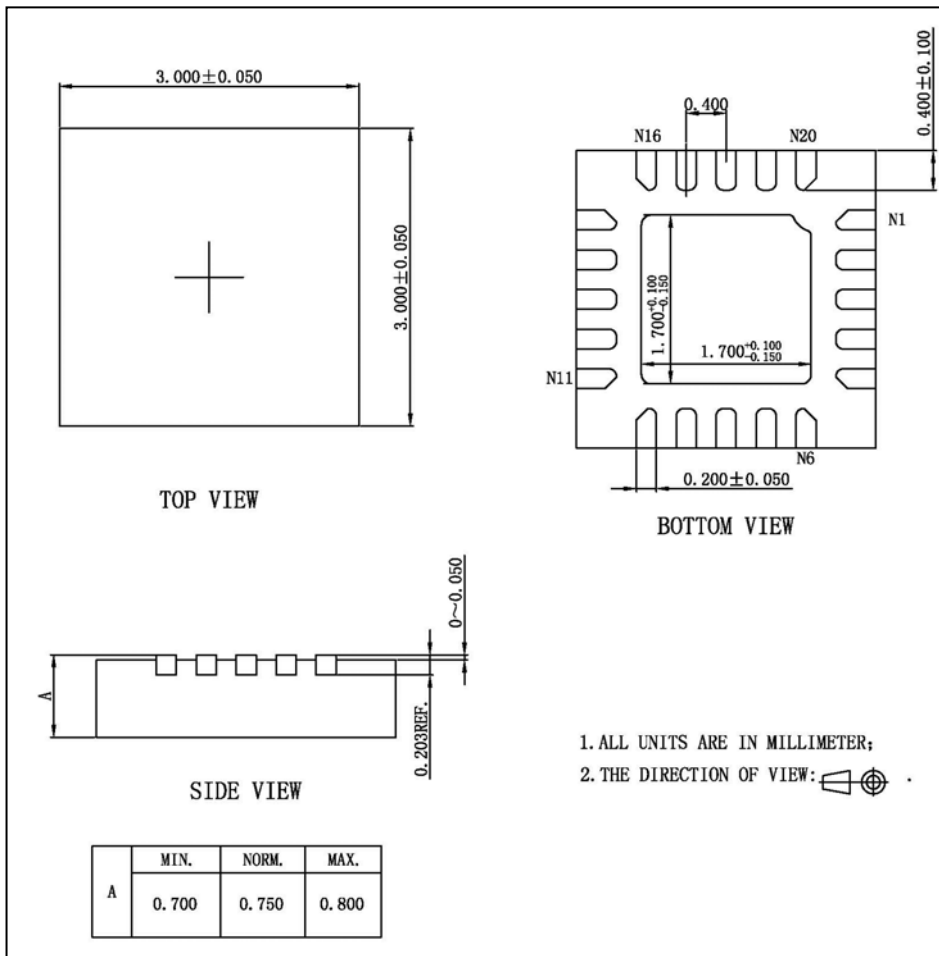


Figure 8 Classification Profile

# IS31PW8200

## PACKAGE INFORMATION

### QFN-20



**Note:** All dimensions in millimeters unless otherwise stated.



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