EMC1438

1°C Multiple Temperature Sensor with Hardware Controlled Standby & Hottest of Multiple Zones

PRODUCT FEATURES

Datasheet

General Description

The EMC1438 is a high accuracy, low cost, System Management Bus (SMBus) temperature sensor. Advanced features such as Resistance Error Correction (REC), Beta Compensation (to CPU diodes requiring the BJT or transistor model) and automatic diode type detection combine to provide a robust solution for complex environmental monitoring applications. Additionally, the hardware controlled STANDBY pin allows for system level power shutdown to support energy saving initiatives.

The EMC1438 monitors up to eight temperature channels (up to seven external and one internal). The device provides ±1°C accuracy for the internal and external diode temperatures.

Temperature monitoring includes two tiers of protection: one that can be masked and causes the ALERT pin to be asserted, and the other that cannot be masked and causes the THERM pin to be asserted.

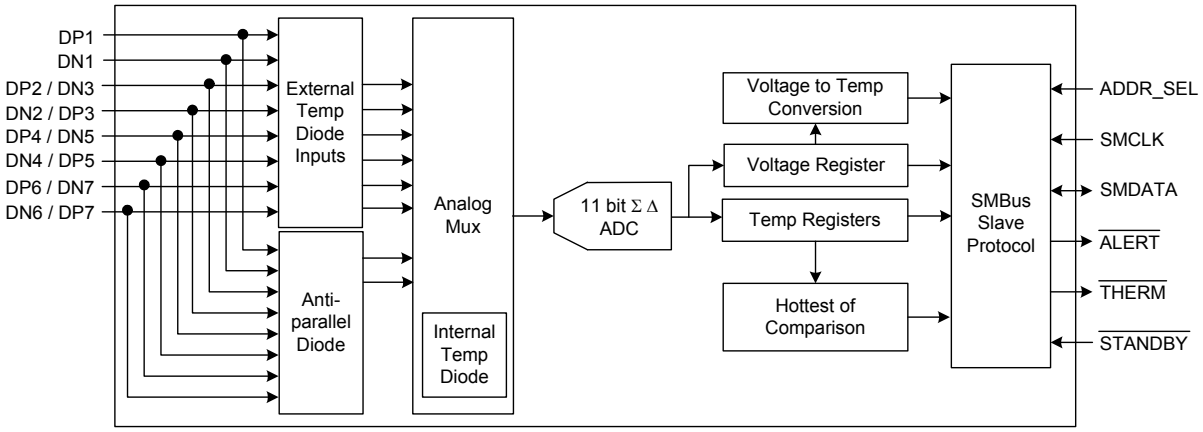
Applications

- Notebook Computers
- Desktop Computers
- Industrial
- Embedded Applications

Features

- Hardware Set Standby Mode
  - 200uA (typical) quiescent current in Standby
- Designed to support 45nm, 65nm, and 90nm CPU diodes
- Supports diodes requiring the BJT or transistor model
- Resistance Error Correction (up to 100 Ohms)
- Up to seven External Temperature Monitors
  - ±1°C Accuracy (40°C < T_{DIODE} < 110°C)
  - 0.125°C Resolution
  - Supports up to 2.2nF filter capacitor
  - Anti-parallel diodes for extra diode support and compact design
- Internal Temperature Monitor
  - ±1°C Accuracy
  - 0.125°C Resolution
- Programmable temperature limits for ALERT and THERM
- 3.3V Supply Voltage
- SMBus 2.0 interface
  - Pin-selectable SMBus address
  - Block Read and Write
- Available in a 16-pin 4mm x 4mm QFN Lead-free RoHS Compliant package

Block Diagram



Ordering Information:

ORDERING NUMBER	PACKAGE	FEATURES
EMC1438-1-AP-TR	16-pin QFN 4mm x 4mm (Lead-free RoHS compliant)	Up to 7 external diodes. "Hottest Of" temperature comparison. ALERT and THERM outputs. Standby low power state. ALERT pin masked and APDs enabled at power up.
EMC1438-2-AP-TR	16-pin QFN 4mm x 4mm (Lead-free RoHS compliant)	Up to 7 external diodes. "Hottest Of" temperature comparison. ALERT and THERM outputs. Standby low power state. ALERT pin masked and APDs disabled at power up.

REEL SIZE IS 4,000 PIECES

This product meets the halogen maximum concentration values per IEC61249-2-21

For RoHS compliance and environmental information, please visit www.smsc.com/rohs

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Chapter 1 Delta

1.1 Delta from EMC1428 to EMC1438

1. Order numbers EMC1438-1 and EMC1438-2.
2. Pin 5 was changed from TRIP_SET to ADDR_SEL.
3. Pin 6 was changed from $\overline{\text{SYS\_SHDN}}$ to $\overline{\text{THERM}}$.
4. Pin 13 was changed from N/C to $\overline{\text{STANDBY}}$.
5. Added Standby low power state (see Section 5.2, "Power States") and STANDBY register bit (see Section 6.4, "Configuration Register").
6. Added pin-selectable SMBus address (see Section 4.1.2, "SMBus Address and RD / WR Bit").
7. Added support for SMBus block read and write.
8. Changed default for MASK_ALL bit to 1, which prevents ALERT# pin assertion in interrupt mode (see Section 6.4, "Configuration Register").
9. Removed SYS_SHDN Configuration Register 1Dh.
10. Changed default Channel Interrupt Mask Register 1Fh from F0h to 00h so all of the enabled channels will assert the $\overline{\text{ALERT}}$ pin in comparator mode (see Section 6.11, "Channel Interrupt Mask Register").
11. EMC1438-1 changed default Channel Configuration Register 3Bh from 00h to 0Eh so all of the DPx/DNx and DNx/DPx pins power up with APD enabled, thereby enabling all temperature channels at power up (see Section 6.21, "Channel Configuration Register"). EMC1438-2 leaves the register default set at 00h.

Chapter 2 Pin Description

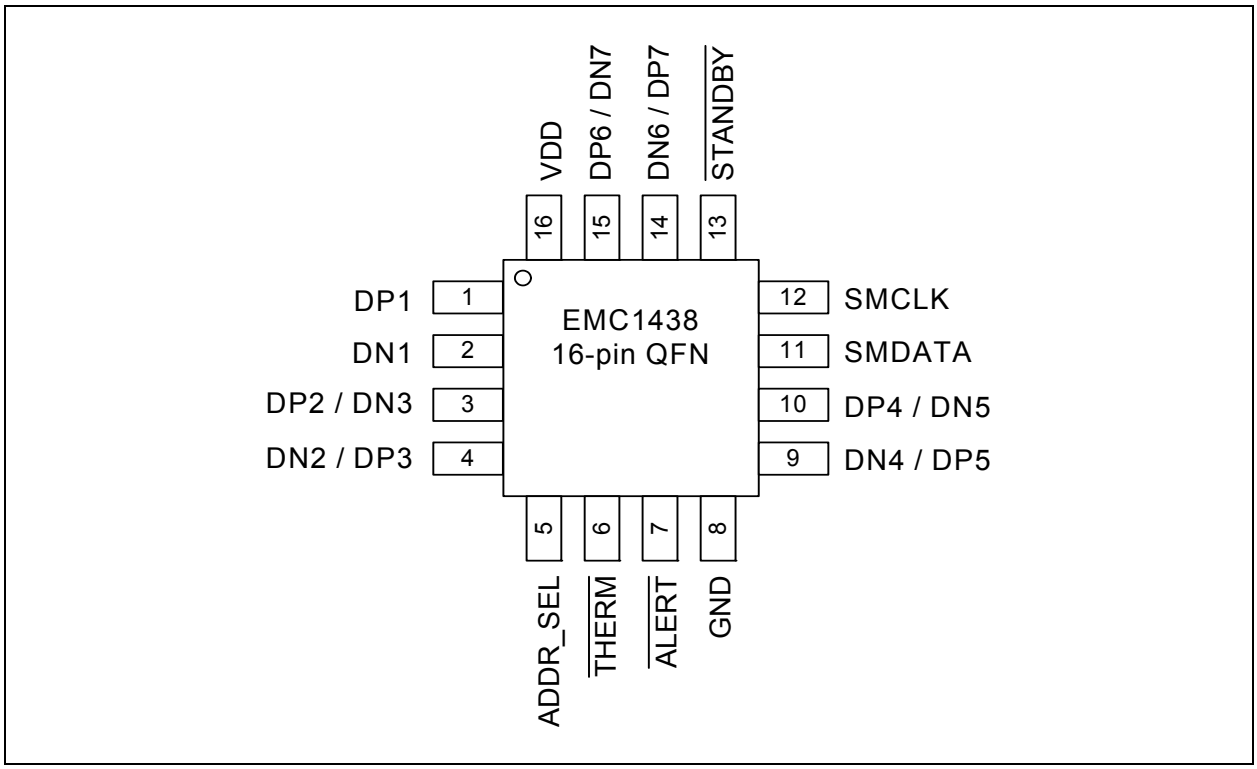


Figure 2.1 EMC1438 Pin Diagram

Table 2.1 EMC1438 Pin Description

PIN NUMBER	NAME	FUNCTION	TYPE
1	DP1	DP1 - External Diode 1 positive (anode) connection.	AIO
2	DN1	External Diode 1 negative (cathode) connection.	AIO
3	DP2 / DN3	External Diode 2 positive (anode) connection and External Diode 3 negative (cathode) connection	AIO
4	DN2 / DP3	External diode 2 negative (cathode) connection and External Diode 3 positive (anode) connection	AIO
5	ADDR_SEL	Selects SMBus address via pull-down resistor.	AI
6	$\overline{\text{THERM}}$	Active low output - requires pull-up resistor. If not used, connect to Ground.	OD (5V)
7	$\overline{\text{ALERT}}$	Active low interrupt - requires pull-up resistor. If not used, connect to Ground.	OD (5V)
8	GND	Ground Connection	Power

Table 2.1 EMC1438 Pin Description (continued)

PIN NUMBER	NAME	FUNCTION	TYPE
9	DN4 / DP5	External diode 4 negative (cathode) connection and External Diode 5 positive (anode) connection	AIO
10	DP4 / DN5	External Diode 4 positive (anode) connection and External Diode 5 negative (cathode) connection	AIO
11	SMDATA	SMBus Data input/output - requires pull-up resistor	DIOD (5V)
12	SMCLK	SMBus Clock input - requires pull-up resistor	DI (5V)
13	$\overline{\text{STANDBY}}$	Active low input that places the device into the Standby state. If not used, connect to V_{DD}.	DI (5V)
14	DN6 / DP7	External diode 6 negative (cathode) connection and External Diode 7 positive (anode) connection	AIO
15	DP6 / DN7	External Diode 6 positive (anode) connection and External Diode 7 negative (cathode) connection	AIO
16	VDD	Power supply	Power

The pin types are described Table 2.2. All pins labeled (5V) are 5V tolerant.

APPLICATION NOTE: For the 5V tolerant pins that have a pull-up resistor, the voltage difference between VDD and the pull-up voltage must never exceed 3.6V.

Table 2.2 Pin Type

PIN TYPE	FUNCTION
Power	Used to supply either VDD or GND to the device
DI	5V tolerant digital input
OD	5V tolerant Open drain digital output. Requires a pull-up resistor
DIOD	5V tolerant bi-directional digital input / open-drain output. Requires a pull-up resistor.
AIO	Analog input / output used for external diodes or analog inputs
AI	Analog Input - this pin is used as an input for analog signals.

Chapter 3 Electrical Specifications

3.1 Absolute Maximum Ratings

Table 3.1 Absolute Maximum Ratings

DESCRIPTION	RATING	UNIT
Supply Voltage (V_{DD})	-0.3 to 4.0	V
Voltage on 5V tolerant pins (V_{5VT_pin})	-0.3 to 5.5	V
Voltage on 5V tolerant pins ($\|V_{5VT\_pin} - V_{DD}\|$) (see Note 3.1)	0 to 3.6	V
Voltage on any other pin to Ground	-0.3 to V_{DD} +0.3	V
Operating Temperature Range	-40 to +125	°C
Storage Temperature Range	-55 to +150	°C
Lead Temperature Range	Refer to JEDEC Spec. J-STD-020	
QFN-16 Package Power Dissipation (see Note 3.2)	0.5W up to T_A = 85°C	W
Junction to Ambient (θ_{JA}) (see Note 3.3)	58	°C/W
ESD Rating, All pins HBM	2000	V

Note: Stresses at or above those listed could cause permanent damage to the device. This is a stress rating only and functional operation of the device at any other condition above those indicated in the operation sections of this specification is not implied. Prolonged stresses above the stated operating levels and below the Absolute Maximum Ratings may degrade device performance and lead to permanent damage.

Note 3.1 For the 5V tolerant pins that have a pull-up resistor, the pull-up voltage must not exceed 3.6V when the device is unpowered.

Note 3.2 The Package Power Dissipation specification assumes a thermal via design with the thermal landing soldered to the PCB ground plane with four 12 mil vias.

Note 3.3 Junction to Ambient (JA) is dependent on the design of the thermal vias. Without thermal vias and a thermal landing, the θ_{JA} is approximately 60°C/W including localized PCB temperature increase.

3.2 Electrical Specifications

Table 3.2 Electrical Specifications

V_{DD} = 3.0V to 3.6V, T_A = -40°C to 125°C, all typical values at T_A = 27°C unless otherwise noted.						
CHARACTERISTIC	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNITS**	**CONDITIONS**
DC Power						
Supply Voltage	V_{DD}	3.0	3.3	3.6	V	
Supply Current	I_{DD}		395	450	uA	1 conversion / sec, dynamic averaging disabled
	I_{DD}		700	960	uA	4 conversions / sec, dynamic averaging enabled
Standby Supply Current	I_{STBY}		200		uA	Monitoring disabled.
Internal Temperature Monitor						
Temperature Accuracy			±0.25	±1	°C	0°C < T_A < 100°C
				±2	°C	-40°C < T_A < 125°C
Temperature Resolution			0.125		°C	
External Temperature Monitor						
Temperature Accuracy			±0.25	±1	°C	+40°C < T_{DIODE} < +110°C 0°C < T_A < 110°C
			±0.5	±2	°C	-40°C < T_{DIODE} < 127°C
Temperature Resolution			0.125		°C	
Conversion Time all Channels	t_{CONV}		170		ms	default settings
Capacitive Filter	C_{FILTER}		2.2	2.7	nF	Connected across external diode
Resistance Error Correction	R_{SERIES}			100	Ω	In series with DP and DN lines
$\overline{\text{ALERT}}$ and $\overline{\text{THERM}}$ pins						
Output Low Voltage	V_{OL}			0.4	V	I_{SINK} = 8mA
Leakage Current	I_{LEAK}			±5	uA	powered or unpowered T_A < 85°C pull-up voltage ≤ 3.6V
SMCLK, SMDATA, and $\overline{\text{STANDBY}}$ pins						
Input High Voltage	V_{IH}	2.0		V_{DD}	V	5V Tolerant
Input Low Voltage	V_{IL}	-0.3		0.8	V	5V Tolerant
Input High/Low Current	I_{IH} / I_{IL}			±5	uA	Powered or unpowered T_A < 85°C

Table 3.2 Electrical Specifications (continued)

V_{DD} = 3.0V to 3.6V, T_A = -40°C to 125°C, all typical values at T_A = 27°C unless otherwise noted.						
CHARACTERISTIC	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNITS**	**CONDITIONS**
Power Up Timing						
First conversion ready	t_{CONV_f}			300	ms	Time after power up before all channels updated with valid data
SMBus delay	t_{SMB_d}			25	ms	Delay before SMBus communications should be sent by host

3.3 SMBus Electrical Characteristics

Table 3.3 SMBus Electrical Specifications

V_{DD} = 3.0V to 3.6V, T_A = -40°C to 125°C, all typical values are at T_A = 27°C unless otherwise noted.						
CHARACTERISTIC	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNITS**	**CONDITIONS**
SMBus Interface						
Hysteresis			420		mV	
Input Capacitance	C_{IN}		5		pF	
Output Low Sink Current	I_{OL}	8.2		15	mA	SMDATA = 0.4V
SMBus Timing						
Clock Frequency	f_{SMB}	10		400	kHz	
Spike Suppression	t_{SP}			50	ns	
Bus free time Start to Stop	t_{BUF}	1.3			us	
Hold Time: Start	$t_{HD:STA}$	0.6			us	
Setup Time: Start	$t_{SU:STA}$	0.6			us	
Setup Time: Stop	$t_{SU:STP}$	0.6			us	
Data Hold Time	$t_{HD:DAT}$	0			us	
Data Setup Time	$t_{SU:DAT}$	100			ns	
Clock Low Period	t_{LOW}	1.3			us	
Clock High Period	t_{HIGH}	0.6			us	
Clock/Data Fall time	t_{FALL}			300	ns	Min = 20+0.1C_{LOAD} ns
Clock/Data Rise time	t_{RISE}			300	ns	Min = 20+0.1C_{LOAD} ns f_{SMB} > 100kHz
Clock/Data Rise time	t_{RISE}			1000	ns	Min = 20+0.1C_{LOAD} ns $f_{SMB} \leq$ 100kHz
Capacitive Load	C_{LOAD}			400	pF	per bus line

Chapter 4 System Management Bus Interface Protocol

4.1 System Management Bus Interface Protocol

The EMC1438 communicates with a host controller, such as an SMSC SIO, through the SMBus. The SMBus is a two-wire serial communication protocol between a computer host and its peripheral devices. A detailed timing diagram is shown in Figure 4.1. Stretching of the SMCLK signal is supported; however, the EMC1438 will not stretch the clock signal.

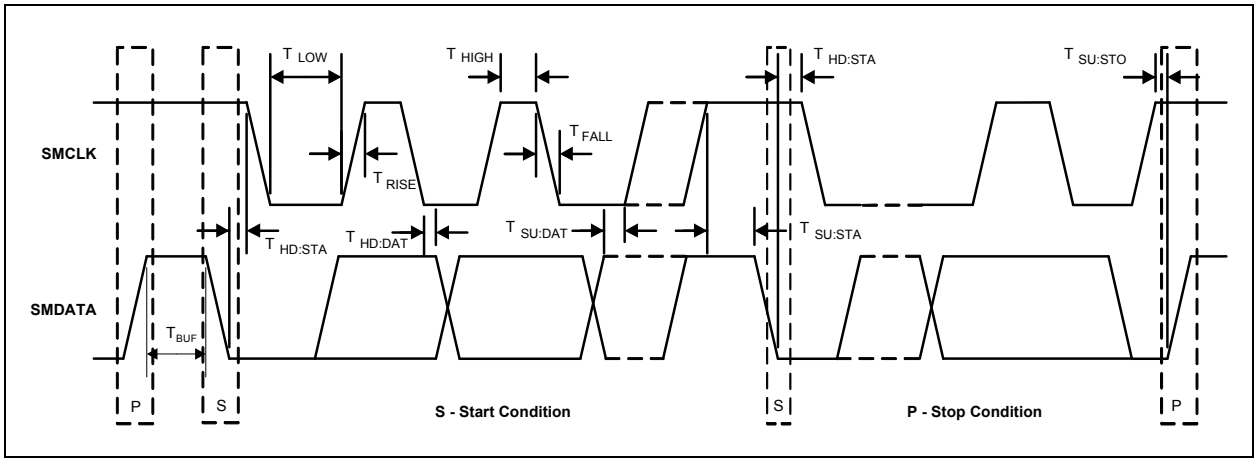


Figure 4.1 SMBus Timing Diagram

4.1.1 SMBus Start Bit

The SMBus Start bit is defined as a transition of the SMBus Data line from a logic ‘1’ state to a logic ‘0’ state while the SMBus Clock line is in a logic ‘1’ state.

4.1.2 SMBus Address and RD / $\overline{WR}$ Bit

The SMBus Address Byte consists of the 7-bit client address followed by a 1-bit RD / $\overline{WR}$ indicator. If this RD / $\overline{WR}$ bit is a logic ‘0’, the SMBus host is writing data to the client device. If this RD / $\overline{WR}$ bit is a logic ‘1’, the SMBus host is reading data from the client device.

The EMC1438 SMBus address is determined by a single resistor connected between ground and the ADDR_SEL pin, as shown in Table 4.1.

Table 4.1 ADDR_SEL Resistor Setting

RESISTOR (+/-10%)	SMBUS ADDRESS	RESISTOR (+/- 10%)	SMBUS ADDRESS
GND	1001_100(r/w)	1500	1001_001(r/w)
270	1001_101(r/w)	2700	1001_010(r/w)
560	1001_110(r/w)	5600	1001_011(r/w)
1000	1001_111(r/w)	≥18000	0011_000(r/w)

All SMBus Data bytes are sent most significant bit first and composed of 8-bits of information.

4.1.3 SMBus ACK and NACK Bits

The SMBus client will acknowledge all data bytes that it receives (as well as the client address if it matches and the ARA address if the ALERT pin is asserted). This is done by the client device pulling the SMBus Data line low after the 8th bit of each byte that is transmitted.

The host will NACK (not acknowledge) the data received from the client by holding the SMBus data line high after the 8th data bit has been sent.

4.1.4 SMBus Stop Bit

The SMBus Stop bit is defined as a transition of the SMBus Data line from a logic ‘0’ state to a logic ‘1’ state while the SMBus clock line is in a logic ‘1’ state. When the EMC1438 detects an SMBus Stop bit, and it has been communicating with the SMBus protocol, it will reset its client interface and prepare to receive further communications.

4.1.5 SMBus Time-out

The EMC1438 includes an SMBus time-out feature. Following a 30ms period of inactivity on the SMBus, the device will time-out and reset the SMBus interface.

The time-out functionality defaults to disabled and can be enabled by writing to the TIMEOUT bit (see Section 6.12, "Consecutive ALERT Register").

4.1.6 SMBus and I^2C Compliance

The major differences between SMBus and I^2C devices are highlighted here. For complete compliance information, refer to the SMBus 2.0 specification.

1. Minimum frequency for SMBus communications is 10kHz.
2. The client protocol will reset if the clock is held at a logic ‘0’ for longer than 30ms. This time-out functionality is disabled by default.
3. The client protocol will reset if both the clock and data lines are held at a logic ‘1’ for longer than 150us. This function is disabled by default.
4. I^2C devices do not support the Alert Response Address functionality (which is optional for SMBus).

4.2 SMBus Protocols

The EMC1438 is SMBus 2.0 compatible and supports Send Byte, Read Byte, Receive Byte, Write Byte, Block Read, and Block Write as valid protocols. It will respond to the Alert Response Address protocol but is not in full compliance.

All of the below protocols use the convention in Table 4.2.

Table 4.2 Protocol Format

DATA SENT TO DEVICE	DATA SENT TO THE HOST

Attempting to communicate with the EMC1438 SMBus interface with an invalid slave address or invalid protocol will result in no response from the device and will not affect its register contents.

4.2.1 Write Byte

The Write Byte is used to write one byte of data to the registers as shown below Table 4.3:

Table 4.3 Write Byte Protocol

START	SLAVE ADDRESS	WR	ACK	REGISTER ADDRESS	ACK	REGISTER DATA	ACK	STOP
1 -> 0	YYYY_YYY	0	0	XXh	0	XXh	0	0 -> 1

4.2.2 Read Byte

The Read Byte protocol is used to read one byte of data from the registers as shown in Table 4.4.

Table 4.4 Read Byte Protocol

START	SLAVE ADDRESS	WR	ACK	REGISTER ADDRESS	ACK	START	SLAVE ADDRESS	RD	ACK	REGISTER DATA	NACK	STOP
1-> 0	YYYY_YYY	0	0	XXh	0	0 -> 1	YYYY_YYY	1	0	XXh	1	0 -> 1

4.2.3 Send Byte

The Send Byte protocol is used to set the internal address register pointer to the correct address location. No data is transferred during the Send Byte protocol as shown in Table 4.5.

Table 4.5 Send Byte Protocol

START	SLAVE ADDRESS	WR	ACK	REGISTER ADDRESS	ACK	STOP
1 -> 0	YYYY_YYY	0	0	XXh	0	1 -> 0

4.2.4 Receive Byte

The Receive Byte protocol is used to read data from a register when the internal register address pointer is known to be at the right location (e.g. set via Send Byte). This is used for consecutive reads of the same register as shown in Table 4.6.

Table 4.6 Receive Byte Protocol

START	SLAVE ADDRESS	RD	ACK	REGISTER DATA	NACK	STOP
1 -> 0	YYYY_YYY	1	0	XXh	1	1 -> 0

4.2.5 Block Write

The Block Write is used to write multiple data bytes to a group of contiguous registers, as shown in Table 4.7. It is an extension of the Write Byte Protocol.

Table 4.7 Block Write Protocol

START	SLAVE ADDRESS	WR	ACK	REGISTER ADDRESS	ACK	REGISTER DATA	ACK
1 ->0	YYYY_YYY	0	0	XXh	0	XXh	0
REGISTER DATA	**ACK**	**REGISTER DATA**	**ACK**	**. . .**	**REGISTER DATA**	**ACK**	**STOP**
XXh	0	XXh	0	. . .	XXh	0	0 -> 1

4.2.6 Block Read

The Block Read is used to read multiple data bytes from a group of contiguous registers, as shown in Table 4.8. It is an extension of the Read Byte Protocol.

Table 4.8 Block Read Protocol

START	SLAVE ADDRESS	WR	ACK	REGISTER ADDRESS	ACK	START	SLAVE ADDRESS	RD	ACK	REGISTER DATA
1->0	YYYY_YYY	0	0	XXh	0	1 ->0	YYYY_YYY	1	0	XXh
ACK	**REGISTER DATA**	**ACK**	**REGISTER DATA**	**ACK**	**REGISTER DATA**	**ACK**	**. . .**	**REGISTER DATA**	**NACK**	**STOP**
0	XXh	0	XXh	0	XXh	0	. . .	XXh	1	0 -> 1

4.2.7 Alert Response Address

The $\overline{\text{ALERT}}$ output can be used as a processor interrupt or as an SMBus Alert.

When it detects that the $\overline{\text{ALERT}}$ pin is asserted, the host will send the Alert Response Address (ARA) to the general address of 0001_100b. All devices with active interrupts will respond with their client address as shown in Table 4.9.

Table 4.9 Alert Response Address Protocol

START	ALERT RESPONSE ADDRESS	RD	ACK	DEVICE ADDRESS	NACK	STOP
1 -> 0	0001_100	1	0	YYYY_YYY	1	1 -> 0

The EMC1438 will respond to the ARA in the following way if the $\overline{\text{ALERT}}$ pin is asserted:

1. Send Slave Address and verify that full slave address was sent (i.e. the SMBus communication from the device was not prematurely stopped due to a bus contention event).
2. Set the MASK bit to clear the $\overline{\text{ALERT}}$ pin.

APPLICATION NOTE: The ARA does not clear the Status Register. If the MASK bit is cleared prior to the Status Register being cleared, the $\overline{\text{ALERT}}$ pin will be reasserted.

Chapter 5 Product Description

The EMC1438 is an SMBus temperature sensor that monitors up to seven (7) external diodes and one internal diode.

Thermal management is performed in cooperation with a host device. This consists of the host reading the temperature data of both the external and internal temperature diodes of the EMC1438 and using that data to control the speed of one or more fans.

The EMC1438 provides two levels of monitoring. The first EMC1438 provides a maskable $\overline{\text{ALERT}}$ signal to the host when measured temperatures meet or exceed user programmable limits. This allows the EMC1438 to be used as an independent thermal watchdog to warn the host of temperature hot spots without constant monitoring by the host. The second level of monitoring provides a non-maskable interrupt on the $\overline{\text{THERM}}$ pin if the measured values meet or exceed a second programmable limit.

Because the EMC1438 automatically corrects for temperature errors due to series resistance in temperature diode lines, there is greater flexibility in where external diodes are positioned and better measurement accuracy than previously available devices without resistance error correction. As well, the automatic beta detection feature means that there is no need to program the device according to which type of diode is present. Therefore, the device can power up ready to operate for any system configuration including those diodes that require the BJT or transistor model.

Figure 5.1 shows a system level block diagram of the EMC1438.

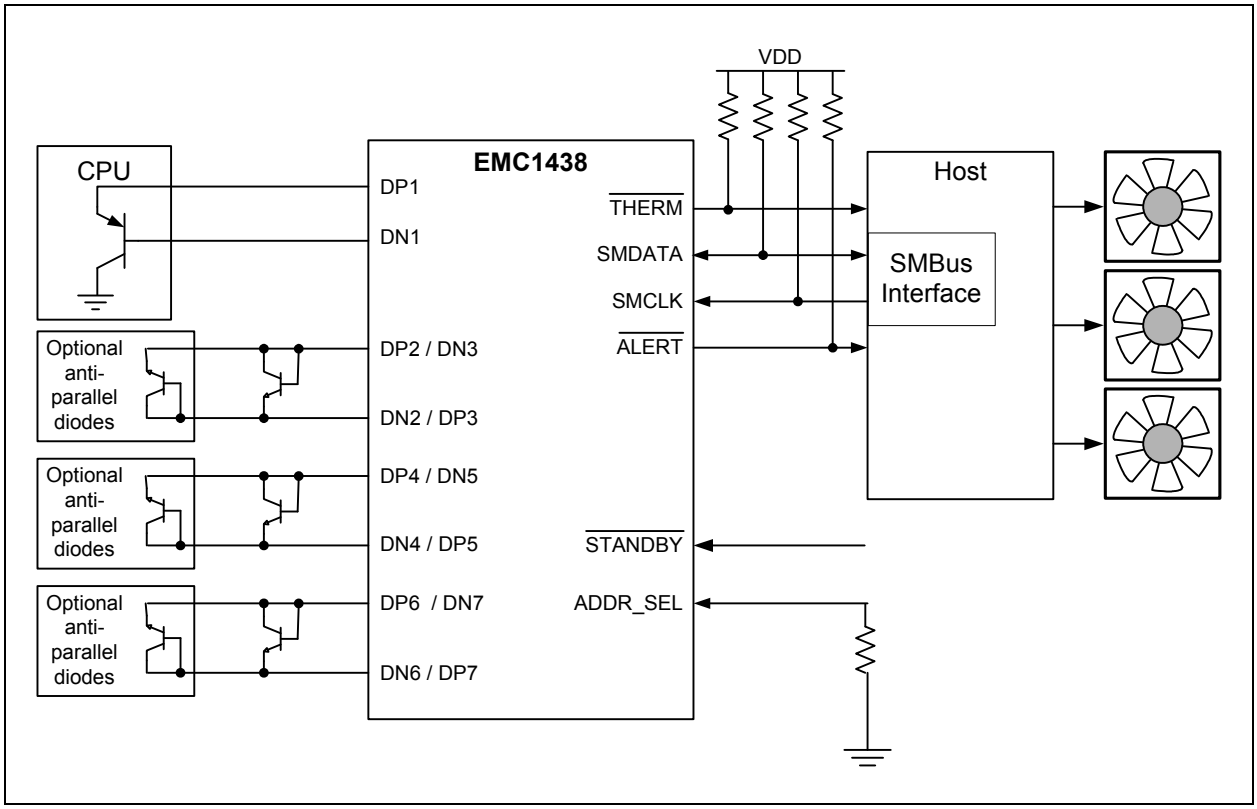


Figure 5.1 System Diagram for EMC1438

5.1 Register Bits

Unless otherwise stated when a bit is “set”, it is written to a logic ‘1’. Likewise when a bit is “cleared”, it is written to a logic ‘0’.

5.2 Power States

The EMC1438 contains two power states that are determined by the $\overline{\text{STANDBY}}$ pin. They are:

1. Active - This power state is enabled when the $\overline{\text{STANDBY}}$ pin is held at a logic '1' and when the STANDBY bit is cleared (see Section 6.4, "Configuration Register"). In this state, the device is fully active and monitoring all active channels.
2. Standby - This power state is enabled when the $\overline{\text{STANDBY}}$ pin is held at a logic '0' or when the STANDBY bit is set (see Section 6.4, "Configuration Register"). In this state, the device is powered down. It will not sample any of the channels nor will it check limits or assert the $\overline{\text{ALERT}}$ or $\overline{\text{THERM}}$ pin. The device will respond to SMBus commands normally and the user may initiate a "One-Shot" command (see Section 6.7, "One Shot Register") which will cause the device to measure all active channels and then return to the Standby state. It will compare the measured temperature against the limits, but will not assert the $\overline{\text{ALERT}}$ or $\overline{\text{THERM}}$ pins.

APPLICATION NOTE: To clear status bits while the device is in Standby, initiate the "One-Shot" command with the error conditions removed and read the status registers. When the device is returned to the Active state, the Status registers will be cleared and then updated after the first conversion time. The $\overline{\text{ALERT}}$ and $\overline{\text{THERM}}$ pins cannot be asserted until after the first conversion is completed after coming out of Standby.

5.3 Temperature Monitoring

The EMC1438 can monitor the temperature of up to seven (7) externally connected diodes as well as the internal or ambient temperature.

5.3.1 Status

The EMC1438 provides a register that summarizes error conditions (see Section 6.3, "Status Register") as well as separate registers to identify the specific channel(s) causing specific error conditions (see Section 6.15, "Hottest Temperature Status Register", Section 6.16, "High Limit Status Register", Section 6.17, "Low Limit Status Register", Section 6.10, "External Diode Fault Register", and Section 6.18, "THERM Limit Status Register").

The summary Status Register bits are set whenever a bit is set in one of the specific status registers. These bits are set regardless of masking.

5.3.2 Limits and Fault Queues

The EMC1438 provides programmable high, low, and therm limits for each channel (see Section 6.6, "Temperature Limit Registers" and Section 6.9, "Therm Limit Registers"). When a temperature channel limit is exceeded for a programmable number of consecutive readings (fault queue - see below), the specific limit status register is updated as well as the summary Status Register.

The EMC1438 contains multiple fault queue counters. Each out of limit error and diode fault condition has its own counter associated with it. The counters are user programmable and determine the number of consecutive measurements that a temperature channel must be out-of-limit or reporting a diode fault before the corresponding status bits are set (see Section 6.12, "Consecutive ALERT Register"). Each counter is incremented whenever the corresponding channel exceeds the appropriate limit (e.g. if External Diode 1 exceeds its high limit, it will increment its high counter). Additionally, each counter is reset if the condition has been removed.

The THERM fault counter is incremented whenever any of the measurements exceed the corresponding THERM Limit. If the temperature drops below the THERM limit minus the corresponding hysteresis (see Section 6.8, "Therm Hysteresis Register"), the counter is reset. If the programmed number of consecutive measurements exceed the THERM Limit, the corresponding THERM Limit status bit is set. Once the status bit is set, the consecutive THERM counter will not reset until the corresponding temperature drops below the appropriate limit minus the corresponding hysteresis.

When the ALERT pin is configured as a comparator (see Section 5.4.2, "ALERT Pin Comparator Mode"), only the high limit fault counter is used; it is incremented if the measured temperature meets or exceeds the High Limit. The fault queue counters for low limit and diode fault are not used, so the applicable status bits are updated after a single out-of-limit or diode fault and the ALERT pin will **not** be asserted. Once the high limit fault counter reaches the programmed limit, the ALERT pin will be asserted (if not masked), but the counter will not be reset. It will remain set until the temperature drops below the High Limit minus the THERM Hysteresis value (see Section 6.8, "Therm Hysteresis Register").

The following is an example of how the counters work. If the CALRT[2:0] bits are set for 4 consecutive alerts on an EMC1438 device, the high limits are set at 70°C, and none of the channels are masked, the status bits will be asserted after the following four measurements:

1. Internal Diode reads 71°C and both external diodes read 69°C. Consecutive alert counter for INT is incremented to 1.
2. Both the Internal Diode and the External Diode 1 read 71°C and External Diode 2 reads 68°C. Consecutive alert counter for INT is incremented to 2 and for EXT1 is set to 1.
3. The External Diode 1 reads 71°C and both the Internal Diode and External Diode 2 read 69°C. Consecutive alert counter for INT and EXT2 are cleared and EXT1 is incremented to 2.
4. The Internal Diode reads 71°C and both external diodes read 71°C. Consecutive alert counter for INT is set to 1, EXT2 is set to 1, and EXT1 is incremented to 3.
5. The Internal Diode reads 71°C and both the external diodes read 71°C. Consecutive alert counter for INT is incremented to 2, EXT2 is set to 2, and EXT1 is incremented to 4. The HIGH status bit are set for EXT1 and the ALERT pin is asserted. The EXT1 counter is reset to 0 and all other counters hold the last value until the next temperature measurement.

5.3.3 "Hottest Of" Comparison

At the end of every measurement cycle, the EMC1438 compares all of the user selectable External Diode channels (see Section 6.20, "Hottest Configuration Register") to determine which of these channels is reporting the hottest temperature. The hottest temperature is stored in the Hottest Temperature Registers and the appropriate status bit in the Hottest Status Register is set (see Section 6.15, "Hottest Temperature Status Register"). If multiple temperature channels measure the same temperature and are equal to the hottest temperature, the hottest status will be based on the measurement order.

As an optional feature, the EMC1438 can also flag an event if the hottest temperature channel changes (see Section 6.21, "Channel Configuration Register"). For example, suppose that External Diode channels 1, 3, and 4 are programmed to be compared in the "Hottest Of" Comparison. If the External Diode 1 channel reports the hottest temperature of the three, its temperature is copied into the Hottest Temperature Registers (in addition to the External Diode 1 Temperature registers) and it is flagged in the Hottest Status bit. If, on the next measurement, the External Diode 3 channel temperature has increased such that it is now the hottest temperature, the EMC1438 can flag this event as an interrupt condition and assert the ALERT pin.

5.3.4 Diode Faults

The EMC1438 actively detects an open and short condition on each measurement channel. When a diode fault is detected and meets the criteria (see Section 5.3.2, "Limits and Fault Queues"), the temperature data MSByte is forced to a value of 80h, the FAULT bit is set in the Status Register, and the bit corresponding to the channel is set in the External Diode Fault Register (see Section 6.10,

"External Diode Fault Register"). When an external diode channel is configured to operate in APD mode, the circuitry will detect independent open fault conditions; however, a short condition will be shared between the APD channels.

5.4 $\overline{\text{ALERT}}$ Output

The $\overline{\text{ALERT}}$ pin is an open drain output and has two modes of operation: interrupt mode and comparator mode. The mode of the $\overline{\text{ALERT}}$ output is selected via the ALERT / COMP bit (see Section 6.4, "Configuration Register").

5.4.1 $\overline{\text{ALERT}}$ Pin Interrupt Mode

When configured to operate in interrupt mode and enabled, the $\overline{\text{ALERT}}$ pin asserts low when an out of limit measurement ($\geq$ high limit or < low limit) is detected on any diode or when a diode fault is detected. The $\overline{\text{ALERT}}$ pin will remain asserted as long as an out-of-limit condition remains. Once the out-of-limit condition has been removed, the $\overline{\text{ALERT}}$ pin will remain asserted until the appropriate specific status register bits are cleared (Section 5.3.1, "Status"). Each channel is subject to the fault queue (see Section 5.3.2, "Limits and Fault Queues").

The MASK_ALL bit (see Section 6.4, "Configuration Register") can be set to '1', so the $\overline{\text{ALERT}}$ pin is masked. Alternatively, the MASK_ALL bit can be set to '0' and individual channels can be masked by setting corresponding bits in the Channel Interrupt Mask Register (see Section 6.11, "Channel Interrupt Mask Register"). When the $\overline{\text{ALERT}}$ pin is masked, it is de-asserted and remains de-asserted until the mask is removed by the user.

The $\overline{\text{ALERT}}$ pin is used as an interrupt signal or as an SMBus Alert signal that allows an SMBus slave to communicate an error condition to the master. One or more $\overline{\text{ALERT}}$ outputs can be hard-wired together.

5.4.2 $\overline{\text{ALERT}}$ Pin Comparator Mode

When the $\overline{\text{ALERT}}$ pin is configured to operate in comparator mode, it will be asserted if any of the measured temperatures meets or exceeds the respective high limit. Low temperature out of limit and diode faults will not assert the $\overline{\text{ALERT}}$ pin. The $\overline{\text{ALERT}}$ pin will remain asserted until all temperatures drop below the corresponding high limit minus the THERM Hysteresis value. Each channel is subject to the high limit fault queue (see Section 5.3.2, "Limits and Fault Queues").

When the $\overline{\text{ALERT}}$ pin is asserted in comparator mode, the HIGH status bit in the Status Register and the appropriate bit in the High Limit Status Register will be set. Reading these bits will not clear them until the $\overline{\text{ALERT}}$ pin is deasserted. Once the $\overline{\text{ALERT}}$ pin is deasserted, the status bits will be automatically cleared.

The MASK_ALL bit will not block the $\overline{\text{ALERT}}$ pin in this mode; however, the individual channel masks (see Section 6.11, "Channel Interrupt Mask Register") will prevent the respective channel from asserting the $\overline{\text{ALERT}}$ pin, although the status bits will still be set.

5.5 $\overline{\text{THERM}}$ Output

The $\overline{\text{THERM}}$ pin is asserted independently of the $\overline{\text{ALERT}}$ pin and cannot be masked. The temperature is compared against the corresponding THERM Limit (see Section 6.9, "Therm Limit Registers"). Whenever any of the measured temperatures linked to the $\overline{\text{THERM}}$ pin meet or exceed the THERM criteria (see Section 5.3.2, "Limits and Fault Queues"), the $\overline{\text{THERM}}$ pin is asserted. Once it has been asserted, it will remain asserted until all measured temperatures drop below the THERM Limit minus the programmable THERM Hysteresis (see Section 6.8, "Therm Hysteresis Register").

5.6 System Configuration Controls

Each channel can be configured to use Resistance Error Correction, Beta Compensation, and Digital Averaging based on user settings and system requirements. Conversion rates and Dynamic Averaging are also configurable.

5.6.1 Resistance Error Correction

The EMC1438 includes active Resistance Error Correction to remove the effect of up to 100 ohms of series resistance. Without this automatic feature, voltage developed across the parasitic resistance in the remote diode path causes the temperature to read higher than the true temperature is. The error induced by parasitic resistance is approximately +0.7°C per ohm. Sources of series resistance include bulk resistance in the remote temperature transistor junctions, series resistance in the CPU, and resistance in the printed circuit board traces and package leads. Resistance error correction in the EMC1438 eliminates the need to characterize and compensate for parasitic resistance in the remote diode path.

5.6.2 Beta Compensation

The forward current gain, or beta, of a transistor is not constant as emitter currents change. As well, it is not constant over changes in temperature. The variation in beta causes an error in temperature reading that is proportional to absolute temperature. Compensating for this error is also known as implementing the BJT or transistor model for temperature measurement.

For discrete transistors configured with the collector and base shorted together, the beta is generally sufficiently high such that the percent change in beta variation is very small. For example, a 10% variation in beta for two forced emitter currents with a transistor whose ideal beta is 50 would contribute approximately 0.25°C error at 100°C. However, for substrate transistors where the base-emitter junction is used for temperature measurement and the collector is tied to the substrate, the proportional beta variation will cause large error. For example, a 10% variation in beta for two forced emitter currents with a transistor whose ideal beta is 0.5 would contribute approximately 8.25°C error at 100°C.

The Beta Compensation circuitry in the EMC1438 corrects for this beta variation to eliminate any error which would normally be induced. It automatically detects the appropriate beta setting to use.

5.6.3 Digital Averaging

To reduce the effect of noise and temperature spikes on the reported temperature, all of the external diode channels can use digital averaging. This averaging acts as a running average using the previous four measured values.

The default setting is to have digital averaging disabled for all channels. It can be enabled for each channel individually by the Filter Control Register (Section 6.22, "Filter Control Register").

5.6.4 Conversion Rates

The EMC1438 may be configured for different conversion rates based on the system requirements. The conversion rate is configured as described in Section 6.5, "Conversion Rate Register". The default conversion rate is 4 conversions per second. Other available conversion rates are shown in Table 6.7.

5.6.5 Dynamic Averaging

Dynamic averaging causes the EMC1438 to measure the external diode channels for an extended time based on the selected conversion rate. This functionality can be disabled for increased power savings at the lower conversion rates (see Section 6.4, "Configuration Register"). When dynamic averaging is enabled, the device will automatically adjust the sampling and measurement time for the external diode channels. This allows the device to average 2x or 4x longer than the normal 11 bit operation (nominally 21ms per channel) while still maintaining the selected conversion rate. The benefits of dynamic

averaging are improved noise rejection due to the longer integration time as well as less random variation of the temperature measurement.

When enabled, the dynamic averaging will affect the average supply current based on the chosen conversion rate as shown in Table 5.1 for EMC1438.

Table 5.1 Supply Current vs. Conversion Rate for EMC1438

CONVERSION RATE	AVERAGE SUPPLY CURRENT		AVERAGING FACTOR (BASED ON 11-BIT OPERATION)	
	DYNAMIC AVERAGING ENABLED (DEFAULT)	DYNAMIC AVERAGING DISABLED	DYNAMIC AVERAGING ENABLED (DEFAULT)	DYNAMIC AVERAGING DISABLED
1 / sec	715uA	450uA	4x	1x
2 / sec	750uA	550uA	2x	1x
4 / sec (default)	900uA	815uA	1x	1x
Continuous (see Table 6.8)	950uA	950uA	0.5x	0.5x

5.7 Diode Connections

The diode connection for the External Diode 1 channel can support a discrete diode-connected transistor (such as a 2N3904) or a substrate transistor (such as those found in a CPU or GPU). Anti-parallel diodes are supported on all diode channels, except the External Diode 1 channel. Figure 5.2 shows examples of diode connections.

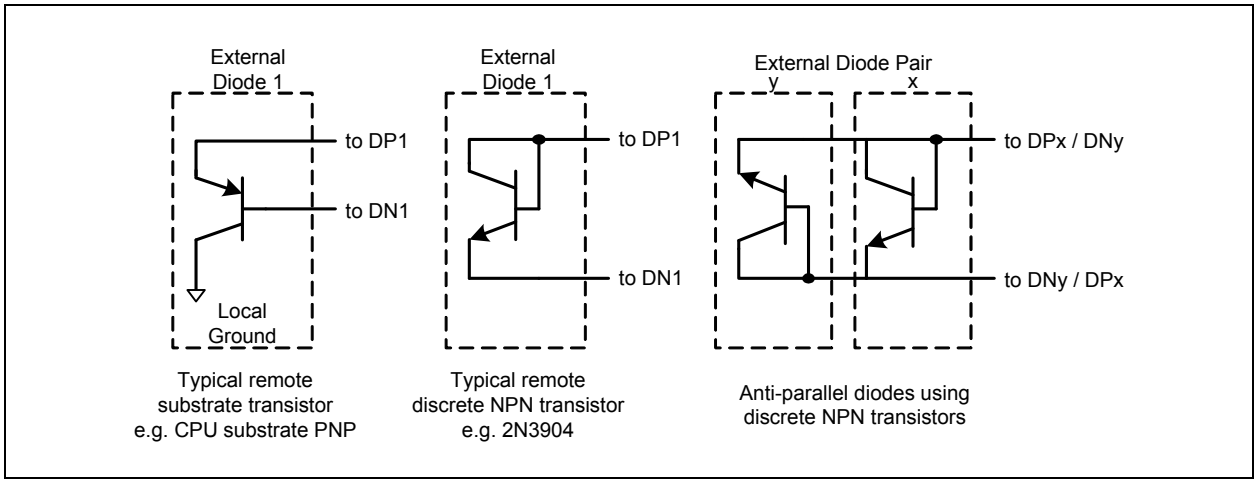


Figure 5.2 Diode Connections

Chapter 6 Register Description

The registers shown in Table 6.1 are accessible through the SMBus. An entry of '-' indicates that the bit is not used and will always read '0'.

In some registers, the EMC1438-1 and EMC1438-2 have different defaults. Due to space limitations, these are noted in the DEFAULT VALUE columns using "(-1)" for EMC1438-1 and "(-2)" for EMC1438-2.

Table 6.1 Register Set in Hexadecimal Order

REGISTER ADDRESS	R/W	REGISTER NAME	FUNCTION	DEFAULT VALUE	PAGE
00h	R	Internal Diode Data High Byte	Stores the integer data for the Internal Diode	00h	Page 28
01h	R	External Diode 1 Data High Byte	Stores the integer data for the External Diode 1	00h	Page 28
02h	R-C	Status	Reports general error conditions	00h	Page 29
03h	R/W	Configuration	Controls the general operation of the device (mirrored at address 09h)	80h	Page 30
04h	R/W	Conversion Rate	Controls the conversion rate for updating temperature data (mirrored at address 0Ah)	06h (4/sec)	Page 31
05h	R/W	Internal Diode High Limit	Stores the 8-bit high limit for the Internal Diode (mirrored at address 0Bh)	55h (85°C)	Page 31
06h	R/W	Internal Diode Low Limit	Stores the 8-bit low limit for the Internal Diode (mirrored at address 0Ch)	00h (0°C)	Page 31
07h	R/W	External Diode 1 High Limit High Byte	Stores the integer portion of the high limit for the External Diode 1 (mirrored at register 0Dh)	55h (85°C)	Page 31
08h	R/W	External Diode 1 Low Limit High Byte	Stores the integer portion of the low limit for the External Diode 1 (mirrored at register 0Eh)	00h (0°C)	Page 31
09h	R/W	Configuration	Controls the general operation of the device (mirrored at address 03h)	80h	Page 30
0Ah	R/W	Conversion Rate	Controls the conversion rate for updating temperature data (mirrored at address 04h)	06h (4/sec)	Page 31
0Bh	R/W	Internal Diode High Limit	Stores the 8-bit high limit for the Internal Diode (mirrored at address 05h)	55h (85°C)	Page 31
0Ch	R/W	Internal Diode Low Limit	Stores the 8-bit low limit for the Internal Diode (mirrored at address 06h)	00h (0°C)	Page 31

Table 6.1 Register Set in Hexadecimal Order (continued)

REGISTER ADDRESS	R/W	REGISTER NAME	FUNCTION	DEFAULT VALUE	PAGE
0Dh	R/W	External Diode 1 High Limit High Byte	Stores the integer portion of the high limit for the External Diode 1 (mirrored at register 07h)	55h (85°C)	Page 31
0Eh	R/W	External Diode 1 Low Limit High Byte	Stores the integer portion of the low limit for the External Diode 1 (mirrored at register 08h)	00h (0°C)	Page 31
0Fh	W	One shot	A write to this register during Standby initiates a one shot update.	00h	Page 34
10h	R	External Diode 1 Data Low Byte	Stores the fractional data for the External Diode 1	00h	Page 28
13h	R/W	External Diode 1 High Limit Low Byte	Stores the fractional portion of the high limit for the External Diode 1	00h	Page 31
14h	R/W	External Diode 1 Low Limit Low Byte	Stores the fractional portion of the low limit for the External Diode 1	00h	Page 31
15h	R/W	External Diode 2 High Limit High Byte	Stores the integer portion of the high limit for External Diode 2	55h (85°C)	Page 31
16h	R/W	External Diode 2 Low Limit High Byte	Stores the integer portion of the low limit for External Diode 2	00h (0°C)	Page 31
17h	R/W	External Diode 2 High Limit Low Byte	Stores the fractional portion of the high limit External Diode 2	00h	Page 31
18h	R/W	External Diode 2 Low Limit Low Byte	Stores the fractional portion of the low limit for External Diode 2	00h	Page 31
19h	R/W	External Diode 1 THERM Limit	Stores the 8-bit critical temperature limit for the External Diode 1	55h (85°C)	Page 35
1Ah	R/W	External Diode 2 THERM Limit	Stores the 8-bit critical temperature limit for External Diode 2	55h (85°C)	Page 35
1Bh	R-C	External Diode Fault	Stores status bits indicating which external diode detected a diode fault	00h	Page 36
1Fh	R/W	Interrupt Mask Register	Controls the masking of the $\overline{\text{ALERT}}$ pin for individual channels	00h	Page 36
20h	R/W	Internal Diode THERM Limit	Stores the 8-bit critical temperature limit for the Internal Diode	55h (85°C)	Page 35
21h	R/W	THERM Hysteresis	Stores the 8-bit hysteresis value that applies to all THERM limits	0Ah (10°C)	Page 35
22h	R/W	Consecutive ALERT	Controls the number of out-of-limit conditions that must occur before the status bit is asserted	70h	Page 37
23h	R	External Diode 2 Data High Byte	Stores the integer data for External Diode 2	00h	Page 28
24h	R	External Diode 2 Data Low Byte	Stores the fractional data for External Diode 2	00h	Page 28

Table 6.1 Register Set in Hexadecimal Order (continued)

REGISTER ADDRESS	R/W	REGISTER NAME	FUNCTION	DEFAULT VALUE	PAGE
25h	R/W	External Diode 1 Beta Configuration	Stores the Beta Compensation circuitry settings for External Diode 1	08h	Page 38
26h	R/W	External Diode 2 Beta Configuration	Stores the Beta Compensation circuitry settings for External Diode 2	08h	Page 38
29h	R	Internal Diode Data Low Byte	Stores the fractional data for the Internal Diode	00h	Page 28
2Ah	R	External Diode 3 High Byte	Stores the integer data for External Diode 3	00h	Page 28
2Bh	R	External Diode 3 Low Byte	Stores the fractional data for External Diode 3	00h	Page 28
2Ch	R/W	External Diode 3 High Limit High Byte	Stores the integer portion of the high limit for External Diode 3	55h (85°C)	Page 31
2Dh	R/W	External Diode 3 Low Limit High Byte	Stores the integer portion of the low limit for External Diode 3	00h (0°C)	Page 31
2Eh	R/W	External Diode 3 High Limit Low Byte	Stores the fractional portion of the high limit for External Diode 3	00h	Page 31
2Fh	R/W	External Diode 3 Low Limit Low Byte	Stores the fractional portion of the low limit for External Diode 3	00h	Page 31
30h	R/W	External Diode 3 THERM Limit	Stores the 8-bit critical temperature limit for External Diode 3	55h (85°C)	Page 35
32h	R	Hottest Diode High Byte	Stores the integer data for the hottest temperature	80h	Page 39
33h	R	Hottest Diode Low Byte	Stores the fractional data for the hottest temperature	00h	Page 39
34h	R-C	Hottest Status	Status bits indicating which external diode is hottest	00h	Page 39
35h	R-C	High Limit Status	Status bits for the High Limits	00h	Page 39
36h	R-C	Low Limit Status	Status bits for the Low Limits	00h	Page 40
37h	R	THERM Limit Status	Status bits for the THERM Limits	00h	Page 41
39h	R/W	REC Configuration	Controls REC for all channels	00h	Page 42
3Ah	R/W	Hottest Config	Controls which external diode channels are used in the “hottest of “comparison	00h	Page 42
3Bh	R/W	Channel Config	Controls which channels are enabled	0Eh (-1) 00h (-2)	Page 42
40h	R/W	Filter Control	Controls the digital filter setting for the External Diode 1 channel	00h	Page 43
41h	R	External Diode 4 Data High Byte	Stores the integer data for the External Diode 4 channel	00h	Page 28

Table 6.1 Register Set in Hexadecimal Order (continued)

REGISTER ADDRESS	R/W	REGISTER NAME	FUNCTION	DEFAULT VALUE	PAGE
42h	R	External Diode 4 Data Low Byte	Stores the fractional data for the External Diode 4 channel	00h	Page 28
43h	R	External Diode 5 Data High Byte	Stores the integer data for the External Diode 5 channel	00h	Page 28
44h	R	External Diode 5 Data Low Byte	Stores the fractional data for the External Diode 5 channel	00h	Page 28
45h	R	External Diode 6 Data High Byte	Stores the integer data for the External Diode 6 channel	00h	Page 28
46h	R	External Diode 6 Data Low Byte	Stores the fractional data for the External Diode 6 channel	00h	Page 28
47h	R	External Diode 7 Data High Byte	Stores the integer data for the External Diode 7 channel	00h	Page 28
48h	R	External Diode 7 Data Low Byte	Stores the fractional data for the External Diode 7 channel	00h	Page 28
50h	R/W	External Diode 4 High Limit High Byte	Stores the integer data for the high limit for the External Diode 4 channel	55h (85°C)	Page 31
51h	R/W	External Diode 4 Low Limit High Byte	Stores the integer data for the low limit for the External Diode 4 channel	00h (0°C)	Page 31
52h	R/W	External Diode 4 HIgh Limit Low Byte	Stores the fractional data for the low limit for the External Diode 4 channel	00h	Page 31
53h	R/W	External Diode 4 Low Limit Low Byte	Stores the fractional data for the low limit for the External Diode 4 channel	00h	Page 31
54h	R/W	External Diode 5 High Limit High Byte	Stores the integer data for the high limit for the External Diode 5 channel	55h (85°C)	Page 31
55h	R/W	External Diode 5 Low Limit High Byte	Stores the integer data for the low limit for the External Diode 5 channel	00h (0°C)	Page 31
56h	R/W	External Diode 5 HIgh Limit Low Byte	Stores the fractional data for the low limit for the External Diode 5 channel	00h	Page 31
57h	R/W	External Diode 5 Low Limit Low Byte	Stores the fractional data for the low limit for the External Diode 5 channel	00h	Page 31
58h	R/W	External Diode 6 High Limit High Byte	Stores the integer data for the high limit for the External Diode 6 channel	55h (85°C)	Page 31
59h	R/W	External Diode 6 Low Limit High Byte	Stores the integer data for the low limit for the External Diode 6 channel	00h (0°C)	Page 31

Table 6.1 Register Set in Hexadecimal Order (continued)

REGISTER ADDRESS	R/W	REGISTER NAME	FUNCTION	DEFAULT VALUE	PAGE
5Ah	R/W	External Diode 6 HIgh Limit Low Byte	Stores the fractional data for the low limit for the External Diode 6 channel	00h (0°C)	Page 31
5Bh	R/W	External Diode 6 Low Limit Low Byte	Stores the fractional data for the low limit for the External Diode 6 channel	00h (0°C)	Page 31
5Ch	R/W	External Diode 7 High Limit High Byte	Stores the integer data for the high limit for the External Diode 7 channel	55h (85°C)	Page 31
5Dh	R/W	External Diode 7 Low Limit High Byte	Stores the integer data for the low limit for the External Diode 7 channel	00h (0°C)	Page 31
5Eh	R/W	External Diode 7 HIgh Limit Low Byte	Stores the fractional data for the low limit for the External Diode 7 channel	00h	Page 31
5Fh	R/W	External Diode 7 Low Limit Low Byte	Stores the fractional data for the low limit for the External Diode 7 channel	00h	Page 31
64h	R/W	External Diode 4 THERM Limit	Stores the 8-bit critical temperature limit for External Diode 4	55h (85°C)	Page 31
65h	R/W	External Diode 5 THERM Limit	Stores the 8-bit critical temperature limit for External Diode 5	55h (85°C)	Page 31
66h	R/W	External Diode 6 THERM Limit	Stores the 8-bit critical temperature limit for External Diode 6	55h (85°C)	Page 31
67h	R/W	External Diode 7 THERM Limit	Stores the 8-bit critical temperature limit for External Diode 7	55h (85°C)	Page 31
71h	R/W	External Diode 4 Beta Configuration	Stores the Beta Compensation circuitry settings for External Diode 4	08h	Page 38
72h	R/W	External Diode 6 Beta Configuration	Stores the Beta Compensation circuitry settings for External Diode 6	08h	Page 38
FDh	R	Product ID	Stores a fixed value that identifies each product	59h	Page 44
FEh	R	Manufacturer ID	Stores a fixed value that represents SMSC	5Dh	Page 44
FFh	R	Revision	Stores a fixed value that represents the revision number	00h	Page 44

6.1 Data Read Interlock

When any temperature channel high byte register is read, the corresponding low byte is copied into an internal 'shadow' register. The user is free to read the low byte at any time and be guaranteed that it will correspond to the previously read high byte. Regardless if the low byte is read or not, reading from the same high byte register again will automatically refresh this stored low byte data.

6.2 Temperature Data Registers

Table 6.2 Temperature Data Registers

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
00h	R	Internal Diode High Byte	Sign	64	32	16	8	4	2	1	00h
29h	R	Internal Diode Low Byte	0.5	0.25	0.125	-	-	-	-	-	00h
01h	R	External Diode 1 High Byte	Sign	64	32	16	8	4	2	1	00h
10h	R	External Diode 1 Low Byte	0.5	0.25	0.125	-	-	-	-	-	00h
23h	R	External Diode 2 High Byte	Sign	64	32	16	8	4	2	1	00h
24h	R	External Diode 2 Low Byte	0.5	0.25	0.125	-	-	-	-	-	00h
2Ah	R	External Diode 3 High Byte	Sign	64	32	16	8	4	2	1	00h
2Bh	R	External Diode 3 Low Byte	0.5	0.25	0.125	-	-	-	-	-	00h
41h	R	External Diode 4 High Byte	Sign	64	32	16	8	4	2	1	00h
42h	R	External Diode 4 Low Byte	0.5	0.25	0.125	-	-	-	-	-	00h
43h	R	External Diode 5 High Byte	Sign	64	32	16	8	4	2	1	00h
44h	R	External Diode 5 Low Byte	0.5	0.25	0.125	-	-	-	-	-	00h
45h	R	External Diode 6 High Byte	Sign	64	32	16	8	4	2	1	00h
46h	R	External Diode 6 Low Byte	0.5	0.25	0.125	-	-	-	-	-	00h
47h	R	External Diode 7 High Byte	Sign	64	32	16	8	4	2	1	00h
48h	R	External Diode 7 Low Byte	0.5	0.25	0.125	-	-	-	-	-	00h

All temperatures are stored as an 11-bit value with the high byte representing the integer value and the low byte representing the fractional value left justified to occupy the MSBits. The data format is standard 2's complement from -64°C to 127.875°C as shown in Table 6.3.

Table 6.3 Temperature Data Format

TEMPERATURE (°C)	BINARY	HEX (AS READ BY REGISTERS)
Diode Fault	1000_0000_000b	80_00h
-64	1100_0000_000b	C0_00h
-63.875	1100_0000_001b	C0_20h
-1	1111_1111_000b	FF_00h
-0.125	1111_1111_111b	FF_E0h
0	0000_0000_000b	00_00h
0.125	0000_0000_001b	00_20h
1	0000_0001_000b	01_00h
63	0011_1111_000b	3F_00h
64	0100_0000_000b	40_00h
127	0111_1111_000b	7F_00h
127.875	0111_1111_111b	7F_E0h

6.3 Status Register

Table 6.4 Status Register

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
02h	R	Status	BUSY	HOTTEST	-	HIGH	LOW	FAULT	THERM	-	00h

The Status Register reports general error conditions (see Section 5.3.1, "Status").

Bit 7 - BUSY - This bit indicates that the ADC is currently converting. This bit does not cause the ALERT pin to be asserted. This bit is set and cleared by the device.

Bit 6 - HOTTEST - This bit is set if the REM_HOT bit is set and the hottest channel changes (see Section 5.3.3, ""Hottest Of" Comparison"). This bit is cleared when this register is read.

Bit 4 - HIGH - This bit is set when any one of the temperature channels meets or exceeds its programmable high limit criteria (see Section 5.3.2, "Limits and Fault Queues"). If the ALERT pin is in interrupt mode, reading from the High Limit Status Register will clear this bit if the error condition has been removed. If the ALERT pin is in comparator mode, this bit is cleared when the ALERT pin is deasserted (see Section 5.4.2, "ALERT Pin Comparator Mode").

Bit 3 - LOW - This bit is set when any one of the temperature channels drops below its programmed low limit criteria (see Section 5.3.2, "Limits and Fault Queues"). Reading from the Low Limit Status Register will clear this bit if the error condition has been removed.

Bit 2 - FAULT - This bit is asserted when a diode fault is detected on any one of the external diode channels (see Section 5.3.4, "Diode Faults"). Reading from the External Diode Fault Register will clear this bit if the error condition has been removed.

Bit 1 - THERM - This bit is set when any one of the external diode channels meets or exceeds its THERM limit criteria (see Section 5.3.2, "Limits and Fault Queues").

6.4 Configuration Register

Table 6.5 Configuration Register

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
03h	R/W	Config	MASK_ ALL	STANDBY	ALERT/ COMP	-	-	-	DAVG_ DIS	-	80h
09h											

The Configuration Register controls the basic operation of the device. This register is fully accessible at either address.

Bit 7 - MASK_ALL - Masks the $\overline{\text{ALERT}}$ pin from asserting.

- '0' - The $\overline{\text{ALERT}}$ pin is not masked. If any of the appropriate status bits are set, the $\overline{\text{ALERT}}$ pin will be asserted.
- '1' (default) - The $\overline{\text{ALERT}}$ pin is masked. It will not be asserted for any interrupt condition, although it may be asserted if the $\overline{\text{ALERT}}$ pin is configured to operate in comparator mode (see Section 5.4.2, "ALERT Pin Comparator Mode"). The Status Registers will be updated normally.

Bit 6 - STANDBY - Enables the Standby state without using the $\overline{\text{STANDBY}}$ pin (see Section 5.2, "Power States").

Note: The $\overline{\text{STANDBY}}$ pin has no effect on this bit. If asserted, it will not set this bit to '1'.

- '0' (default) - The EMC1438 is in the Active state if the $\overline{\text{STANDBY}}$ pin is not asserted.
- '1' - The EMC1438 is in the Standby state.

Bit 5 - ALERT/COMP - Controls the operation of the $\overline{\text{ALERT}}$ pin.

- '0' (default) - The $\overline{\text{ALERT}}$ pin acts in interrupt mode as described in Section 5.4.1.
- '1' - The $\overline{\text{ALERT}}$ pin acts in comparator mode as described in Section 5.4.2. In this mode the MASK_ALL bit is ignored.

Bit 1 - DAVG_DIS - Disables the dynamic averaging feature on all temperature channels (see Section 5.6.5, "Dynamic Averaging").

- '0' (default) - The dynamic averaging feature is enabled. All temperature channels will be converted with an averaging factor that is based on the conversion rate as shown in Table 5.1.
- '1' - The dynamic averaging feature is disabled. All temperature channels will be converted with a maximum averaging factor of 1x (equivalent to 11-bit conversion). For higher conversion rates (i.e. more conversions per second), this averaging factor will be reduced as shown in Table 5.1.

6.5 Conversion Rate Register

Table 6.6 Conversion Rate Register

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
04h	R/W	Conversion Rate	-	-	-	-		CONV[2:0]			06h (4/sec)
0Ah											

The Conversion Rate Register controls how often the temperature measurement channels are updated and compared against the limits. This register is fully accessible at either register address.

Bits 3-0 - CONV[3:0] - Determines the conversion rate as shown in Table 6.7.

Table 6.7 Conversion Rate

CONV[2:0]			CONVERSIONS / SECOND
2	1	0	
1	0	0	1
1	0	1	2
1	1	0	4 (default)
1	1	1	Continuous
All Others			4

The actual conversion rate for Continuous conversions will depend on the number of diode channels enabled and is shown in Table 6.8.

Table 6.8 Maximum Conversion Rate Per Temperature Channels

NUMBER OF EXTERNAL DIODE CHANNELS	MAX CONVERSION RATE
4	15 / sec
5	13 / sec
6	11 / sec
7	10 / sec

6.6 Temperature Limit Registers

Table 6.9 Temperature Limit Registers

ADDR.	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
05h	R/W	Internal Diode High Limit	Sign	64	32	16	8	4	2	1	55h (85°C)
0Bh											

Table 6.9 Temperature Limit Registers (continued)

ADDR.	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
06h 0Ch	R/W	Internal Diode Low Limit	Sign	64	32	16	8	4	2	1	00h (0°C)
07h 0Dh	R/W	External Diode 1 High Limit High Byte	Sign	64	32	16	8	4	2	1	55h (85°C)
13h	R/W	External Diode 1 High Limit Low Byte	0.5	0.25	0.125	-	-	-	-	-	00h
08h 0Eh	R/W	External Diode 1 Low Limit High Byte	Sign	64	32	16	8	4	2	1	00h (0°C)
14h	R/W	External Diode 1 Low Limit Low Byte	0.5	0.25	0.125	-	-	-	-	-	00h
15h	R/W	External Diode 2 High Limit High Byte	Sign	64	32	16	8	4	2	1	55h (85°C)
16h	R/W	External Diode 2 Low Limit High Byte	Sign	64	32	16	8	4	2	1	00h (0°C)
17h	R/W	External Diode 2 High Limit Low Byte	0.5	0.25	0.125	-	-	-	-	-	00h
18h	R/W	External Diode 2 Low Limit Low Byte	0.5	0.25	0.125	-	-	-	-	-	00h
2Ch	R/W	External Diode 3 High Limit High Byte	Sign	64	32	16	8	4	2	1	55h (85°C)
2Dh	R/W	External Diode 3 Low Limit High Byte	Sign	64	32	16	8	4	2	1	00h (0°C)
2Eh	R/W	External Diode 3 High Limit Low Byte	0.5	0.25	0.125	-	-	-	-	-	00h

Table 6.9 Temperature Limit Registers (continued)

ADDR.	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
2Fh	R/W	External Diode 3 Low Limit Low Byte	0.5	0.25	0.125	-	-	-	-	-	00h
50h	R/W	External Diode 4 High Limit High Byte	Sign	64	32	16	8	4	2	1	55h (85°C)
51h	R/W	External Diode 4 Low Limit High Byte	Sign	64	32	16	8	4	2	1	00h (0°C)
52h	R/W	External Diode 4 High Limit Low Byte	0.5	0.25	0.125	-	-	-	-	-	00h
53h	R/W	External Diode 4 Low Limit Low Byte	0.5	0.25	0.125	-	-	-	-	-	00h
54h	R/W	External Diode 5 High Limit High Byte	Sign	64	32	16	8	4	2	1	55h (85°C)
55h	R/W	External Diode 5 Low Limit High Byte	Sign	64	32	16	8	4	2	1	00h (0°C)
56h	R/W	External Diode 5 High Limit Low Byte	0.5	0.25	0.125	-	-	-	-	-	00h
57h	R/W	External Diode 5 Low Limit Low Byte	0.5	0.25	0.125	-	-	-	-	-	00h
58h	R/W	External Diode 6 High Limit High Byte	Sign	64	32	16	8	4	2	1	55h (85°C)
59h	R/W	External Diode 6 Low Limit High Byte	Sign	64	32	16	8	4	2	1	00h (0°C)
5Ah	R/W	External Diode 6 High Limit Low Byte	0.5	0.25	0.125	-	-	-	-	-	00h

Table 6.9 Temperature Limit Registers (continued)

ADDR.	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
5Bh	R/W	External Diode 6 Low Limit Low Byte	0.5	0.25	0.125	-	-	-	-	-	00h
5Ch	R/W	External Diode 7 High Limit High Byte	Sign	64	32	16	8	4	2	1	55h (85°C)
5Dh	R/W	External Diode 7 Low Limit High Byte	Sign	64	32	16	8	4	2	1	00h (0°C)
5Eh	R/W	External Diode 7 High Limit Low Byte	0.5	0.25	0.125	-	-	-	-	-	00h
5Fh	R/W	External Diode 7 Low Limit Low Byte	0.5	0.25	0.125	-	-	-	-	-	00h

The device contains both high and low limits for all temperature channels. If the measured temperature meets or exceeds the high limit, the corresponding status bits are set (see Section 5.3.1, "Status") and the $\overline{\text{ALERT}}$ pin may be asserted (see Section 5.4, "ALERT Output"). Likewise, if the measured temperature is less than the low limit, the corresponding status bits are set and the $\overline{\text{ALERT}}$ pin may be asserted.

The limit registers with multiple register addresses are fully accessible at either address.

When the device is in the Standby state, updating the limit registers will have no effect until the next conversion cycle occurs. This can be initiated via a write to the One Shot Register (see Section 6.7, "One Shot Register").

6.7 One Shot Register

Table 6.10 One Shot Register

ADDR.	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
0Fh	W	One Shot	Writing to this register in Standby initiates a single conversion cycle. Data is not stored and always reads 00h								00h

The One Shot Register is used to initiate a one shot command. Writing to the one shot register, when the device is in the Standby state (see Section 5.2, "Power States") and the BUSY bit (see Section 6.3, "Status Register") is '0', will immediately cause the ADC to update all temperature measurements. Writing to the One Shot Register while the device is in the Active state will have no effect.

6.8 Therm Hysteresis Register

Table 6.11 Therm Hysteresis Register

ADDR.	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
21h	R/W	THERM Hysteresis	-	64	32	16	8	4	2	1	0Ah (10°C)

The THERM Hysteresis is used in conjunction with the THERM Limit Registers to set the THERM status bits (see Section 5.5, "THERM Output"). In addition, the THERM Hysteresis Register is used with the High Limit Registers when the ALERT pin is configured to act as a comparator (see Section 5.4.2, "ALERT Pin Comparator Mode").

6.9 Therm Limit Registers

Table 6.12 Therm Limit Registers

ADDR.	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
19h	R/W	External Diode 1 THERM Limit	Sign	64	32	16	8	4	2	1	55h (85°C)
1Ah	R/W	External Diode 2 THERM Limit	Sign	64	32	16	8	4	2	1	55h (85°C)
20h	R/W	Internal Diode THERM Limit	Sign	64	32	16	8	4	2	1	55h (85°C)
30h	R/W	External Diode 3 THERM Limit	Sign	64	32	16	8	4	2	1	55h (85°C)
64h	R/W	External Diode 4 THERM Limit	Sign	64	32	16	8	4	2	1	55h (85°C)
65h	R/W	External Diode 5 THERM Limit	Sign	64	32	16	8	4	2	1	55h (85°C)
66h	R/W	External Diode 6 THERM Limit	Sign	64	32	16	8	4	2	1	55h (85°C)
67h	R/W	External Diode 7 THERM Limit	Sign	64	32	16	8	4	2	1	55h (85°C)

The THERM Limit Registers are used to set the THERM status bits and assert the $\overline{\text{THERM}}$ pin (see Section 5.5, "THERM Output").

6.10 External Diode Fault Register

Table 6.13 External Diode Fault Register

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
1Bh	R-C	External Diode Fault	E7FLT	E6FLT	E5FLT	E4FLT	E3FLT	E2FLT	E1FLT	-	00h

The External Diode Fault Register contains the status bits that are set when a temperature channel meets the diode fault criteria (see Section 5.3.4, "Diode Faults"). If any of these bits are set, the FAULT status bit in the Status Register is set. Reading from the External Diode Fault Register will clear all bits if the error condition has been removed. Reading from the register will also clear the FAULT status bit in the Status Register.

The $\overline{\text{ALERT}}$ pin, if configured in interrupt mode, may be set if any of these status bits are set (see Section 5.4, "ALERT Output").

Bit 7 - E7FLT - This bit is set if the External Diode 7 channel reported a diode fault.

Bit 6 - E6FLT - This bit is set if the External Diode 6 channel reported a diode fault.

Bit 5 - E5FLT - This bit is set if the External Diode 5 channel reported a diode fault.

Bit 4 - E4FLT - This bit is set if the External Diode 4 channel reported a diode fault.

Bit 3 - E3FLT - This bit is set if the External Diode 3 channel reported a diode fault.

Bit 2 - E2FLT - This bit is set if the External Diode 2 channel reported a diode fault.

Bit 1 - E1FLT - This bit is set if the External Diode 1 channel reported a diode fault.

6.11 Channel Interrupt Mask Register

Table 6.14 Channel Interrupt Mask Register

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
1Fh	R/W	Channel Mask	E7_ MSK	E6_ MSK	E5_ MSK	E4_ MSK	E3_ MSK	E2_ MSK	E1_ MSK	INT_ MSK	00h

The Channel Interrupt Mask Register controls individual channel masking. When a channel is masked, the $\overline{\text{ALERT}}$ pin will not be asserted when the masked channel reads a diode fault or out of limit error.

Bits 7-1 - Ex_MSK - Prevents the $\overline{\text{ALERT}}$ pin from being asserted when the External Diode X channel is out of limit or reports a diode fault. If the EXT6_APD bit is not set (see Section 6.21, "Channel Configuration Register"), the EXT7_MSK bit is ignored. Likewise, if the EXT4_APD bit is not set, then the EXT5_MSK bit is ignored, and if the EXT2_APD bit is not set (see Section 6.21), the EXT3_MSK bit is ignored.

- '0' (default) - The External Diode X channel will cause the $\overline{\text{ALERT}}$ pin to be asserted if it is out of limit or reports a diode fault.
- '1' - The External Diode X channel will not cause the $\overline{\text{ALERT}}$ pin to be asserted if it is out of limit or reports a diode fault.

Bit 0 - INT_MSK - Prevents the $\overline{\text{ALERT}}$ pin from being asserted when the Internal Diode temperature is out of limit.

- '0' (default) - The Internal Diode channel will cause the $\overline{\text{ALERT}}$ pin to be asserted if it is out of limit.

- '1' - The Internal Diode channel will not cause the $\overline{\text{ALERT}}$ pin to be asserted if it is out of limit.

6.12 Consecutive ALERT Register

Table 6.15 Consecutive ALERT Register

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
22h	R/W	Consecutive ALERT	TIME OUT	CTHERM[2:0]			CALRT[2:0]			-	70h

The Consecutive ALERT Register determines how many times an out-of-limit error or diode fault must be detected in consecutive measurements before the status registers are asserted (see Section 5.3.2, "Limits and Fault Queues").

Bit 7 - TIMEOUT - Determines whether the SMBus Timeout function is enabled.

- '0' (default) - The SMBus Timeout and idle timeout features are disabled. The SMCLK line can be held low indefinitely without the device resetting its SMBus protocol.
- '1' - The SMBus Timeout feature is enabled. If the SMCLK line is held low for more than 30ms, the device will reset the SMBus protocol. The Idle Timeout is also enabled. If both the SMCLK and SMDATA lines are held high for longer than 150us, the device will reset the SMBus protocol.

Bits 6-4 CTHERM[2:0] - Determines the number of consecutive measurements that must exceed the corresponding THERM Limit before the corresponding THERM Limit status bit is set and the $\overline{\text{THERM}}$ pin is asserted (if enabled for the channel). All temperature channels use this value to set the respective counters.

The bits are decoded as shown in Table 6.16. The default setting is 4 consecutive out of limit conversions.

Bits 3-1 - CALRT[2:0] - Determine the number of consecutive measurements that must have an out of limit condition or diode fault before the applicable status bits are asserted. All temperature channels use this value to set the respective counters. The bits are decoded as shown in Table 6.16. The default setting is 1 consecutive out-of-limit conversion or diode fault.

APPLICATION NOTE: If one of the fault queues is not cleared and the CALRT[2:0] or CTHERM[2:0] bits are updated, the update won't take effect until the fault queue is cleared. All the fault queues are independent so those that are empty will be updated immediately.

APPLICATION NOTE: If the $\overline{\text{ALERT}}$ pin is configured in comparator mode, these bits are ignored for low temperature out-of-limit and diode faults. The value used is one occurrence.

Table 6.16 Consecutive Alert Settings

2	1	0	NUMBER OF CONSECUTIVE OUT OF LIMIT MEASUREMENTS / DIODE FAULTS
0	0	0	1 (default for CALRT[2:0])
0	0	1	2
0	1	1	3
1	1	1	4 (default for CTHERM[2:0])
All Others			1 (CALRT[2:0]), 4 (CTHERM[2:0])

6.13 Beta Configuration Register

Table 6.17 Beta Configuration Register

ADDR.	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
25h	R/W	External Diode 1 Beta Configuration	-	-	-	-	AUTO1	BETA1[2:0]			08h
26h	R/W	External Diode 2 Beta Configuration	-	-	-	-	AUTO2	BETA2[2:0]			08h
71h	R/W	External Diode 4 Beta Configuration	-	-	-	-	AUTO4	BETA4[2:0]			08h
72h	R/W	External Diode 6 Beta Configuration	-	-	-	-	AUTO6	BETA6[2:0]			08h

These registers are used to set the Beta Compensation factor that is used for the External Diode channels.

Bit 3 - AUTOx - Enables the Beta Compensation factor autodetection function.

- '0' - The Beta Compensation Factor autodetection circuitry is disabled. The External Diode will always use the Beta Compensation factor set by the BETAx[2:0] bits.
- '1' (default) - The Beta Compensation factor autodetection circuitry is enabled. At the beginning of every conversion, the optimal Beta Compensation factor setting will be determined and applied. The BETAx[2:0] bits will be automatically updated to indicate the current setting.

Bit 2-0 - BETAx[2:0] - These bits always reflect the current beta configuration settings. These bits will be updated automatically and writing to these bits will have no effect.

Table 6.18 Beta Compensation Look Up Table

BETAX[2:0]			MINIMUM BETA
2	1	0	
0	0	0	$\leq$ 0.08
0	0	1	$\leq$ 0.111
0	1	0	$\leq$ 0.176
0	1	1	$\leq$ 0.29
1	0	0	$\leq$ 0.48
1	0	1	$\leq$ 0.9
1	1	0	$\leq$ 2.33
1	1	1	Disabled

6.14 Hottest Temperature Registers

Table 6.19 Hottest Temperature Registers

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
32h	R	Hottest Temperature High Byte	Sign	64	32	16	8	4	2	1	80h
33h	R	Hottest Temperature Low Byte	0.5	0.25	0.125	-	-	-	-	-	00h

The Hottest Temperature Registers store the measured hottest temperature of all the selected external diode channels (see Section 5.3.3, ""Hottest Of" Comparison"). If no External diodes are selected, the High Byte Register will read 80h. The data format is the same as the temperature channels.

6.15 Hottest Temperature Status Register

Table 6.20 Hottest Temperature Register

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
34h	R	Hottest Temperature Status	EXT7	EXT6	EXT5	EXT4	EXT3	EXT2	EXT1	INT	00h

The Hottest Temperature Status Register flags which external diode temperature is hottest (see Section 5.3.3, ""Hottest Of" Comparison").

Bit 7 - EXT7 - The External Diode 7 channel is the hottest.

Bit 6 - EXT6 - The External Diode 6 channel is the hottest.

Bit 4 - EXT5 - The External Diode 5 channel is the hottest.

Bit 3 - EXT4 - The External Diode 4 channel is the hottest.

Bit 3 - EXT3 - The External Diode 3 channel is the hottest.

Bit 2 - EXT2 - The External Diode 2 channel is the hottest.

Bit 1 - EXT1 - The External Diode 1 channel is the hottest.

Bit 0 - INT - The Internal Diode channel is the hottest.

6.16 High Limit Status Register

Table 6.21 High Limit Status Register

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
35h	R-C	High Limit Status	E7 HIGH	E6 HIGH	E5 HIGH	E4 HIGH	E3 HIGH	E2 HIGH	E1 HIGH	I HIGH	00h

The High Limit Status Register contains the status bits that are set when a temperature channel meets the high limit criteria (see Section 5.3.2, "Limits and Fault Queues"). If any of these bits are set, the HIGH status bit in the Status Register is set. If the $\overline{\text{ALERT}}$ pin is in interrupt mode, reading from the High Limit Status Register will clear all bits if the error condition has been removed, and reading from the register will also clear the HIGH status bit in the Status Register. If the $\overline{\text{ALERT}}$ pin is in comparator mode, these bits are cleared when the $\overline{\text{ALERT}}$ pin is deasserted (see Section 5.4.2, "ALERT Pin Comparator Mode").

The $\overline{\text{ALERT}}$ pin may be set if any of these status bits are set (see Section 5.4, "ALERT Output").

Bit 7 - E7HIGH - This bit is set when the External Diode 7 channel meets or exceeds its programmed high limit.

Bit 6 - E6HIGH - This bit is set when the External Diode 6 channel meets or exceeds its programmed high limit.

Bit 5 - E5HIGH - This bit is set when the External Diode 5 channel meets or exceeds its programmed high limit.

Bit 4 - E4HIGH - This bit is set when the External Diode 4 channel meets or exceeds its programmed high limit.

Bit 3 - E3HIGH - This bit is set when the External Diode 3 channel meets or exceeds its programmed high limit.

Bit 2 - E2HIGH - This bit is set when the External Diode 2 channel meets or exceeds its programmed high limit.

Bit 1 - E1HIGH - This bit is set when the External Diode 1 channel meets or exceeds its programmed high limit.

Bit 0 - IHIGH - This bit is set when the Internal Diode channel meets or exceeds its programmed high limit.

6.17 Low Limit Status Register

Table 6.22 Low Limit Status Register

ADDR.	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
36h	R-C	Low Limit Status	E7 LOW	E6 LOW	E5 LOW	E4 LOW	E3 LOW	E2 LOW	E1 LOW	ILOW	00h

The Low Limit Status Register contains the status bits that are set when a temperature channel meets the low limit criteria (see Section 5.3.2, "Limits and Fault Queues"). If any of these bits are set, the LOW status bit in the Status Register is set. Reading from the Low Limit Status Register will clear all bits if the error condition has been removed. Reading from the register will also clear the LOW status bit in the Status Register.

The $\overline{\text{ALERT}}$ pin, if configured in interrupt mode, may be set if any of these status bits are set (see Section 5.4, "ALERT Output").

Bit 7 - E7LOW - This bit is set when the External Diode 7 channel drops below its programmed low limit.

Bit 6 - E6LOW - This bit is set when the External Diode 6 channel drops below its programmed low limit.

Bit 5 - E5LOW - This bit is set when the External Diode 5 channel drops below its programmed low limit.

Bit 4 - E4LOW - This bit is set when the External Diode 4 channel drops below its programmed low limit.

Bit 3 - E3LOW - This bit is set when the External Diode 3 channel drops below its programmed low limit.

Bit 2 - E2LOW - This bit is set when the External Diode 2 channel drops below its programmed low limit.

Bit 1 - E1LOW - This bit is set when the External Diode 1 channel drops below its programmed low limit.

Bit 0 - ILOW - This bit is set when the Internal Diode channel drops below its programmed low limit.

6.18 THERM Limit Status Register

Table 6.23 THERM Limit Status Register

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
37h	R-C	THERM Limit Status	E7 THERM	E6 THERM	E5 THERM	E4 THERM	E3 THERM	E2 THERM	E1 THERM	I THERM	00h

The THERM Limit Status Register contains the status bits that are set when a temperature channel meets the THERM Limit criteria (see Section 5.3.2, "Limits and Fault Queues"). If any of these bits are set, the THERM status bit in the Status Register is set. Reading from the THERM Limit Status Register will not clear the status bits. Once the temperature drops below the THERM Limit minus the THERM Hysteresis, the corresponding status bits will be automatically cleared. The THERM bit in the Status Register will be cleared when all individual channel THERM bits are cleared.

Bit 7 - E7THERM - This bit is set when the External Diode 7 channel meets or exceeds its programmed THERM Limit.

Bit 6 - E6THERM - This bit is set when the External Diode 6 channel meets or exceeds its programmed THERM Limit.

Bit 5 - E5THERM - This bit is set when the External Diode 5 channel meets or exceeds its programmed THERM Limit.

Bit 4 - E4THERM - This bit is set when the External Diode 4 channel meets or exceeds its programmed THERM Limit.

Bit 3 - E3THERM - This bit is set when the External Diode 3 channel meets or exceeds its programmed THERM Limit.

Bit 2 - E2THERM - This bit is set when the External Diode 2 channel meets or exceeds its programmed THERM Limit.

Bit 1 - E1THERM - This bit is set when the External Diode 1 channel meets or exceeds its programmed THERM limit.

Bit 0 - ITHERM - This bit is set when the Internal Diode channel meets or exceeds its programmed THERM limit.

6.19 REC Configuration Register

Table 6.24 REC Configuration Register

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
39h	R/W	REC Config	E7 REC_n	E6_ REC_n	E5_ REC_n	E4_ REC_n	E3_ REC_n	E2_ REC_n	E1_ REC_n	-	00h

The REC Control Register controls the Resistance Error Correction circuitry for each of the external diode channels.

Bits 7 - 0 - EX_REC_n - Disables the Resistance Error Correction (REC) for the External Diode X channel.

- '0' (default) - REC is enabled.
- '1' - REC is disabled.

6.20 Hottest Configuration Register

Table 6.25 Hottest Configuration Register

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
3Ah	R/W	Hottest Config	E7HOT	E6HOT	E5HOT	E4HOT	E3HOT	E2HOT	E1HOT	IHOT	00h

The Hottest Configuration Register determines which External Diode Channels (if any) are compared during the "Hottest Of" comparison that is automatically performed at the end of every conversion cycle (see Section 5.3.3, ""Hottest Of" Comparison").

Bits 7 - 0 - ExHOT - Controls whether the External Diode X temperature data is compared during the "Hottest Of" comparison.

- '0' (default) - The External Diode X channel is not compared during the "Hottest Of" Comparison.
- '1' - The External Diode X channel temperature data is compared to all other indicated channels during the "Hottest Of" Comparison.

Bit 0 - IHOT - Controls whether the Internal Diode temperature data is compared during the "Hottest Of" comparison.

- '0' (default) - The Internal Diode channel is not compared during the "Hottest Of" Comparison.
- '1' - The Internal Diode channel temperature data is compared to all other indicated channels during the "Hottest Of" Comparison.

6.21 Channel Configuration Register

Table 6.26 Channel Configuration Register

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
3Bh	R/W	Channel Config	REM_ HOT	-	-	-	EXT6_ APD	EXT4_ APD	EXT2_ APD	-	0Eh (-1) 00h (-2)

The Channel Configuration Register determines which external diode channels are active in the device.

Bit 7 - REM_HOT - Enables circuitry that will remember the last temperature channel that was determined to be the Hottest and flag an error if the hottest temperature channel changes (see Section 5.3.3, "“Hottest Of” Comparison").

- ‘0’ (default) - The HOTTEST status bit will not be asserted if the hottest temperature channel changes.
- ‘1’ - If the hottest temperature channel changes, the HOTTEST status bit will be asserted.

Bit 3 - EXT6_APD - Enables the DP6 / DN7 and DN6 / DP7 pins to support two anti-parallel diode connections versus a single diode connection.

- ‘0’ (default - EMC1438-2) - The DP6 / DN7 and DN6 / DP7 pins do not support two anti-parallel diode connections. The pins will only monitor a single external diode (External Diode 6).
- ‘1’ (default - EMC1438-1) - The DP6 / DN7 and DN6 / DP7 pins support two anti-parallel diode connections (External Diode 6 and External Diode 7).

Bit 2 - EXT4_APD - Enables the DP4 / DN5 and DN4 / DP5 pins to support two anti-parallel diode connections versus a single diode connection.

- ‘0’ (default - EMC1438-2) - The DP4 / DN5 and DN4 / DP5 pins do not support two anti-parallel diode connections. The pins will only monitor a single external diode (External Diode 4).
- ‘1’ (default - EMC1438-1) - The DP4 / DN5 and DN4 / DP5 pins support two anti-parallel diode connections (External Diode 4 and External Diode 5).

Bit 1 - EXT2_APD - Enables the DP2 / DN3 and DN2 / DP3 pins to support two anti-parallel diode connections versus a single diode connection.

- ‘0’ (default - EMC1438-2) - The DP2 / DN3 and DN2 / DP3 pins do not support two anti-parallel diode connections. The pins will only monitor a single external diode (External Diode 2).
- ‘1’ (default - EMC1438-1) - The DP2 / DN3 and DN2 / DP3 pins support two anti-parallel diode connections (External Diode 2 and External Diode 3).

6.22 Filter Control Register

Table 6.27 Filter Control Register

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
40h	R/W	Filter Control	AVG7_ EN	AVG6_ EN	AVG5_ EN	AVG4_ EN	AVG3_ EN	AVG2_ EN	AVG1_ EN	-	00h

The Filter Configuration Register controls the digital filter on the external diode channels (see Section 5.6.3, "Digital Averaging").

Bits 7 - 0 - AVGx_EN - Control the digital averaging that is applied to the External Diode X temperature measurements.

- ‘0’ (default) - Digital Averaging is disabled.
- ‘1’ - Digital averaging is enabled as a 4x running average for the External Diode X channel.

Bit 5 - This bit is part of the test mux encoding but is ignored.

6.23 Product ID Register

Table 6.28 Product ID Register

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
FDh	R	Product ID	0	1	0	1	1	0	0	1	59h

The Product ID Register holds a unique value that identifies the device.

6.24 Manufacturer ID Register (FEh)

Table 6.29 Manufacturer ID Register

ADDR.	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
FEh	R	Manufacturer ID	0	1	0	1	1	1	0	1	5Dh

The Manufacturer ID Register holds an 8-bit word that identifies SMSC.

6.25 Revision Register (FFh)

Table 6.30 Revision Register

ADDR.	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
FFh	R	Revision	0	0	0	0	0	0	0	0	00h

The Revision register contains an 8-bit word that identifies the die revision.

Chapter 7 Package Information

7.1 EMC1438 Package Drawing

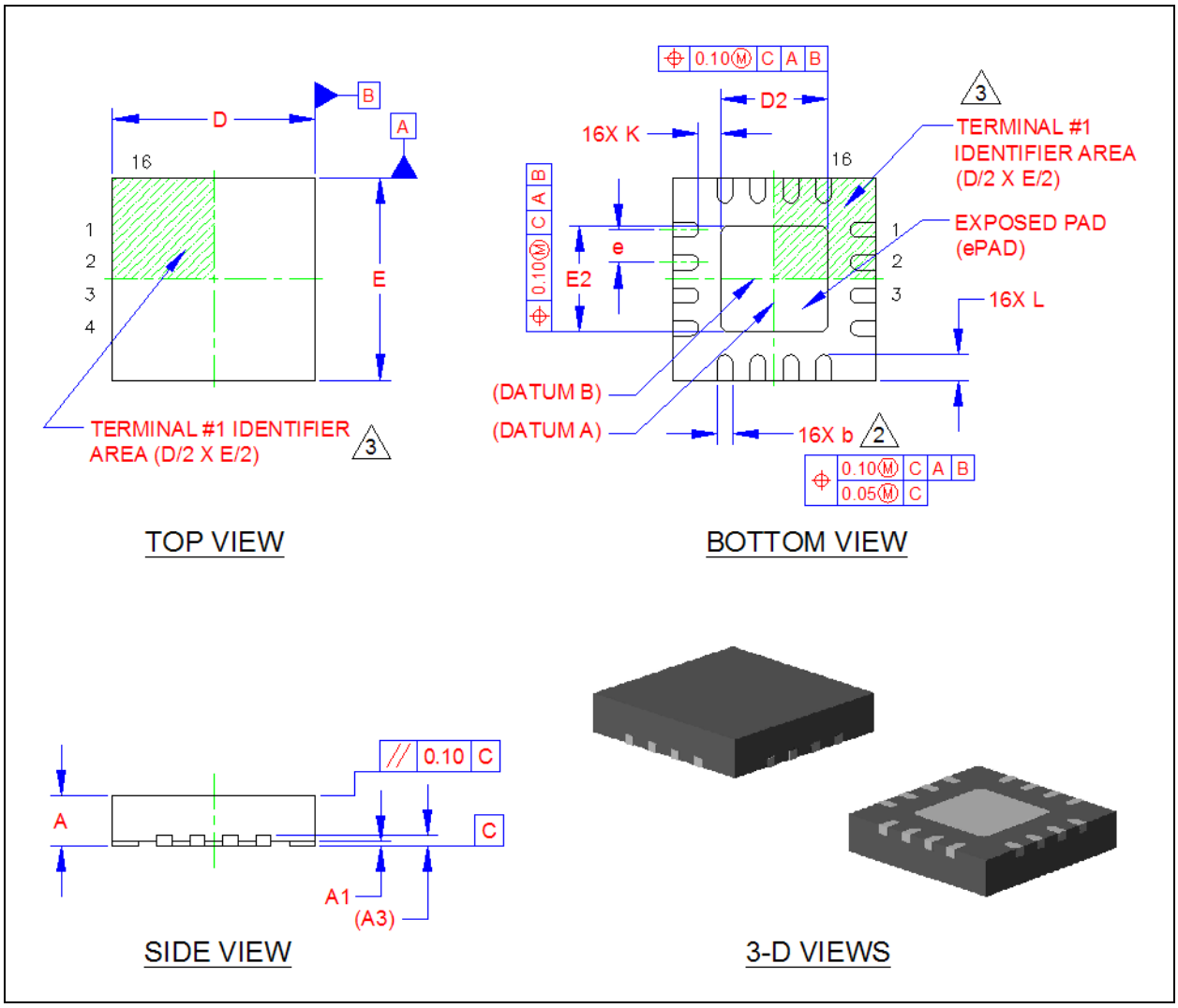
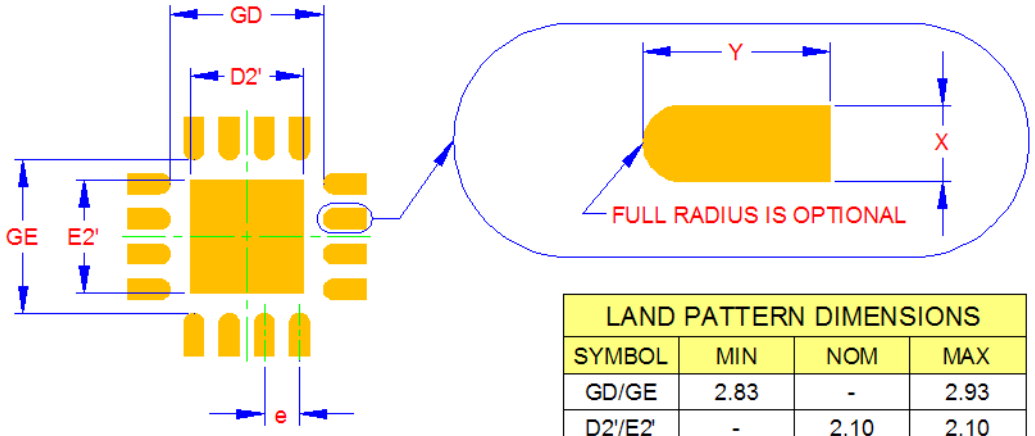


Figure 7.1 16-Pin QFN 4mm x 4mm Package Drawing



LAND PATTERN DIMENSIONS			
SYMBOL	MIN	NOM	MAX
GD/GE	2.83	-	2.93
D2'/E2'	-	2.10	2.10
X	-	-	0.37
Y	0.79	-	-
e		0.65	

PCB LAND PATTERN

Figure 7.2 16-Pin QFN 4mm x 4mm PCB Footprint

COMMON DIMENSIONS					
SYMBOL	MIN	NOM	MAX	NOTE	REMARK
A	0.80	0.85	0.90	-	OVERALL PACKAGE HEIGHT
A1	0	0.02	0.05	-	STANDOFF
A3		0.20 REF		-	LEAD-FRAME THICKNESS
D/E	3.90	4.00	4.10	-	X/Y BODY SIZE
D2/E2	2.00	2.10	2.20	-	X/Y EXPOSED PAD SIZE
L	0.40	0.50	0.60	-	TERMINAL LENGTH
b	0.25	0.30	0.35	2	TERMINAL WIDTH
K	0.35	0.45	-	-	TERMINAL TO PAD DISTANCE
e		0.65 BSC		-	TERMINAL PITCH

NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONS "b" APPLIES TO PLATED TERMINALS AND IT IS MEASURED BETWEEN 0.15 AND 0.30 mm FROM THE TERMINAL TIP.
3. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE AREA INDICATED.

Figure 7.3 16-Pin QFN 4mm x 4mm Package Dimensions

7.2 Package Markings

7.2.1 EMC1438 (16-Pin 4mm x 4mm QFN)

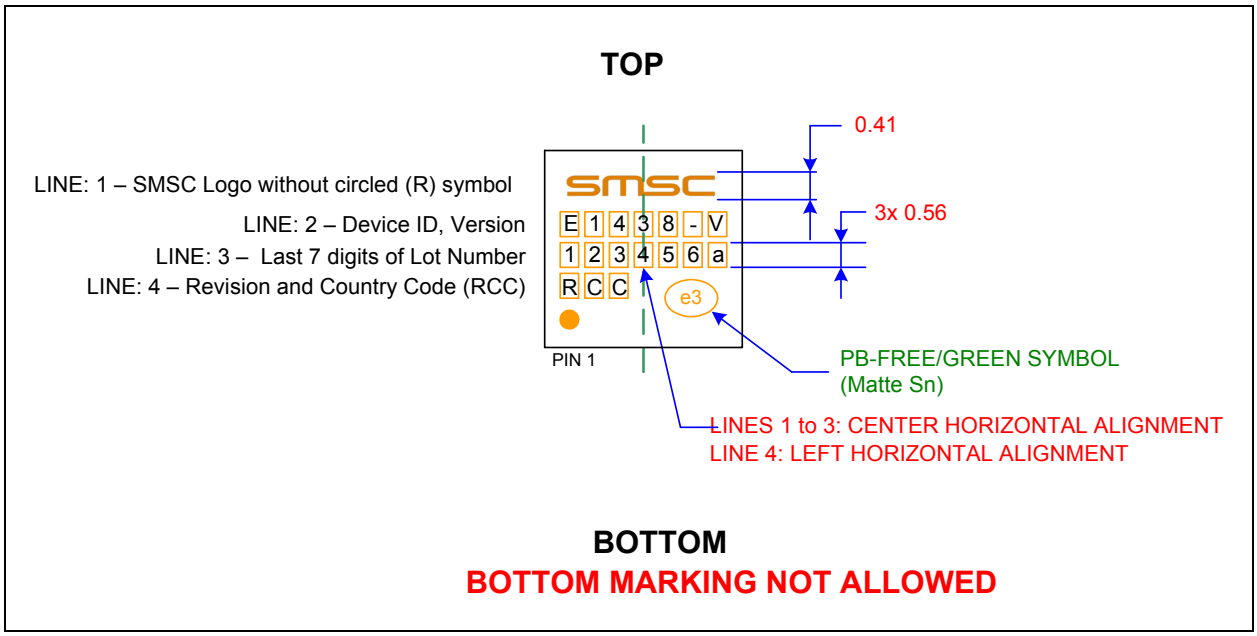


Figure 7.4 EMC1438 Package Marking

Chapter 8 Datasheet Revision History

Table 8.1 Customer Revision History

REVISION LEVEL AND DATE	SECTION/FIGURE/ENTRY	CORRECTION
Rev. 1.0 Rev. 1.0 (04-29-10)	Datasheet release	

Общество с ограниченной ответственностью «МосЧип» ИНН 7719860671 / КПП 771901001
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