# S-8204B Series

## BATTERY PROTECTION IC FOR 3-SERIES OR 4-SERIES CELL PACK

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Rev.3.9_00

The S-8204B Series includes high-accuracy voltage detection circuits and delay circuits, in single use, makes it possible for users to monitor the status of 3-series or 4-series cell lithium-ion rechargeable battery. By switching the voltage level which is applied to the SEL pin, users are able to use the S-8204B Series either for 3-series or 4-series cell pack.
By cascade connection using the S-8204B Series, it is also possible to protect 6-series or more cells[*1] lithium-ion rechargeable battery pack.

***1.** Refer to the application note for connection examples of protection circuit for 6-series or more cells.
In case of protecting 5-series cell lithium-ion rechargeable battery pack, contact our sales office.

## ■ Features

- High-accuracy voltage detection function for each cell

| | | |
|---|---|---|
| Overcharge detection voltage n (n = 1 to 4) | 3.65 V to 4.6 V (50 mV step) | Accuracy ±25 mV |
| Overcharge release voltage n (n = 1 to 4) | 3.5 V to 4.6 V[*1] | Accuracy ±50 mV |
| Overdischarge detection voltage n (n = 1 to 4) | 2.0 V to 3.0 V (100 mV step) | Accuracy ±80 mV |
| Overdischarge release voltage n (n = 1 to 4) | 2.0 V to 3.4 V[*2] | Accuracy ±100 mV |

- Discharge overcurrent detection in 3-step

| | | |
|---|---|---|
| Discharge overcurrent detection voltage 1 | 0.05 V to 0.30 V (50 mV step) | Accuracy ±15 mV |
| Discharge overcurrent detection voltage 2 | 0.5 V (fixed) | Accuracy ±100 mV |
| Load short-circuit detection voltage | 1.0 V (fixed) | Accuracy ±300 mV |

- Settable by external capacitor; overcharge detection delay time, overdischarge detection delay time, discharge overcurrent detection delay time 1, discharge overcurrent detection delay time 2
  (Load short-circuit detection delay time is internally fixed.)
- Switchable between 3-series and 4-series cell by using the SEL pin
- Independent charge and discharge control by the control pins
- Power-down function "available" / "unavailable" is selectable
- High-withstand voltage: Absolute maximum rating: 24 V
- Wide operation voltage range: 2 V to 22 V
- Wide operation temperature range: Ta = −40°C to +85°C
- Low current consumption

| | |
|---|---|
| During operation | 33 µA max. (Ta = +25°C) |
| During power-down | 0.1 µA max. (Ta = +25°C) |

- Lead-free, Sn 100%, halogen-free[*3]

***1.** Overcharge hysteresis voltage n (n = 1 to 4) is selectable in 0 V, or in 0.1 V to 0.4 V in 50 mV step.
(Overcharge hysteresis voltage = Overcharge detection voltage − Overcharge release voltage)
***2.** Overdischarge hysteresis voltage n (n = 1 to 4) is selectable in 0 V, or in 0.2 V to 0.7 V in 100 mV step.
(Overdischarge hysteresis voltage = Overdischarge release voltage − Overdischarge detection voltage)
***3.** Refer to "■ **Product Name Structure**" for details.

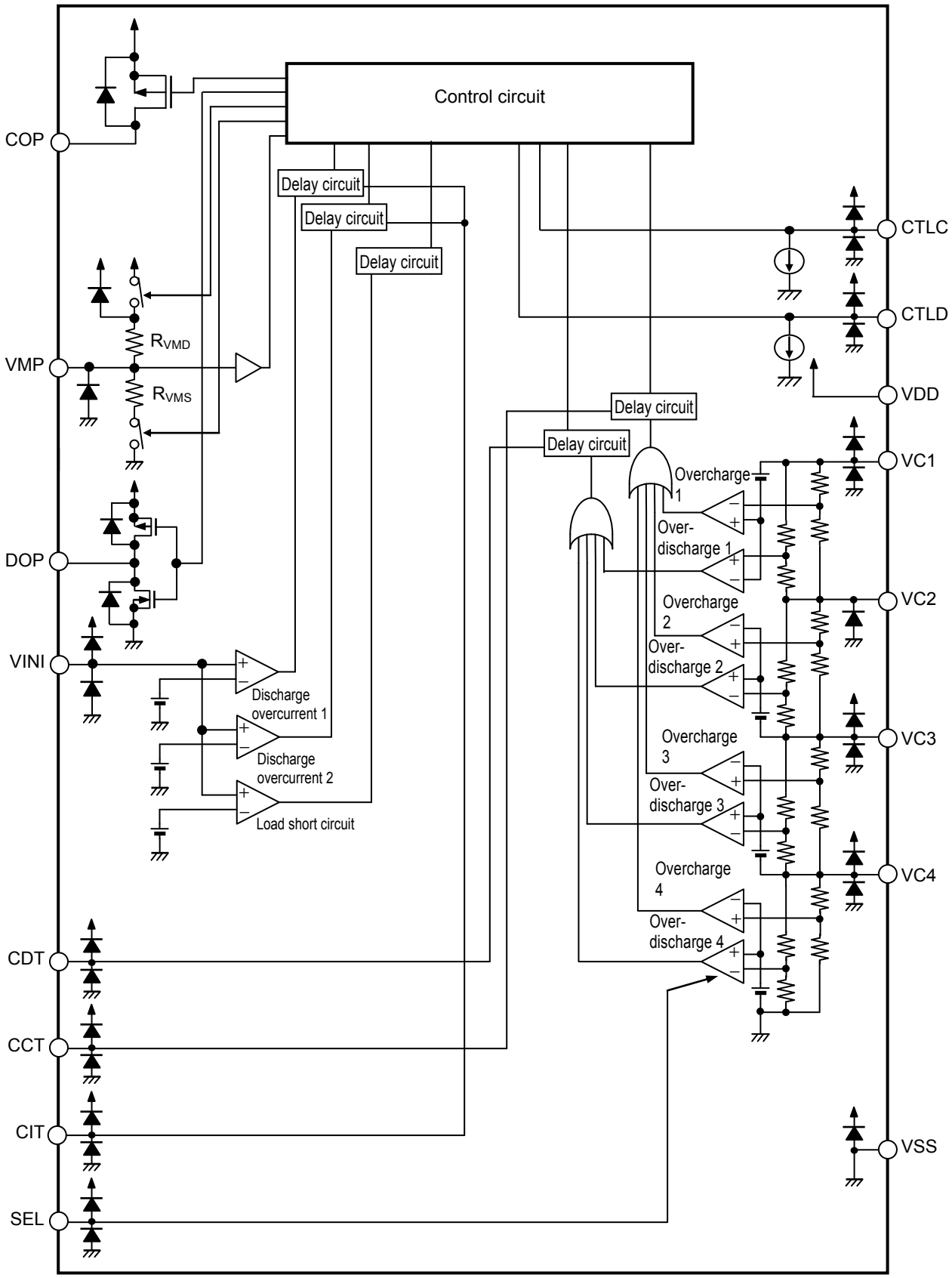
## ■ Application

- Rechargeable lithium-ion battery pack

## ■ Package

- 16-Pin TSSOP

## ■ Block Diagram

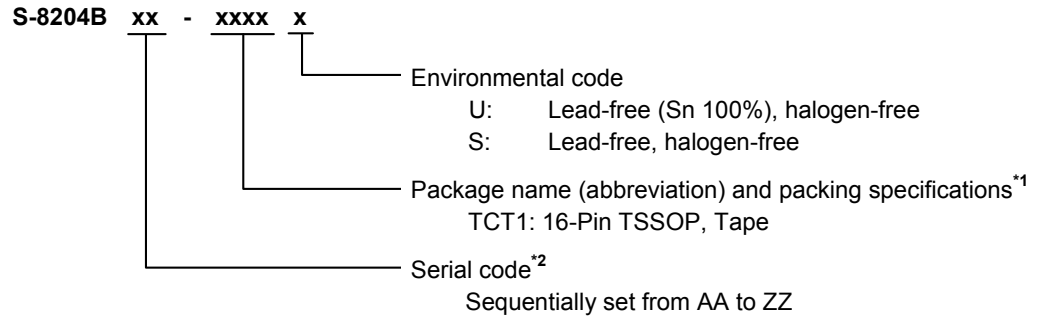



**Remark** Diodes in the figure are parasitic diodes.

**Figure 1**

## ■ Product Name Structure

### 1. Product name




***1.** Refer to the tape drawing.
***2.** Refer to "**3. Product name list**".

### 2. Package

**Table 1 Package Drawing Codes**

| Package Name | | Dimension | Tape | Reel |
|---|---|---|---|---|
| 16-Pin TSSOP | Environmental code = S | FT016-A-P-SD | FT016-A-C-SD | FT016-A-R-SD |
| | Environmental code = U | FT016-A-P-SD | FT016-A-C-SD | FT016-A-R-S1 |

### 3. Product name list

**Table 2**

| Product Name | Overcharge Detection Voltage [$V_{CU}$] | Overcharge Release Voltage [$V_{CL}$] | Overdischarge Detection Voltage [$V_{DL}$] | Overdischarge Release Voltage [$V_{DU}$] | Discharge Overcurrent Detection Voltage 1 [$V_{DIOV1}$] | 0 V Battery Charge Function | Power-down Function |
|---|---|---|---|---|---|---|---|
| S-8204BAB-TCT1y | 4.350 V | 4.150 V | 2.00 V | 2.70 V | 0.250 V | Available | Available |
| S-8204BAC-TCT1y | 4.225 V | 4.075 V | 2.30 V | 3.00 V | 0.100 V | Available | Available |
| S-8204BAD-TCT1y | 3.800 V | 3.600 V | 2.00 V | 2.30 V | 0.300 V | Available | Available |
| S-8204BAE-TCT1y | 4.350 V | 4.150 V | 2.50 V | 3.00 V | 0.250 V | Available | Available |
| S-8204BAF-TCT1y | 4.350 V | 4.150 V | 2.30 V | 3.00 V | 0.100 V | Available | Available |
| S-8204BAG-TCT1y | 4.350 V | 4.150 V | 2.80 V | 3.30 V | 0.100 V | Available | Available |
| S-8204BAH-TCT1y | 4.200 V | 4.000 V | 2.60 V | 3.00 V | 0.100 V | Available | Available |
| S-8204BAI-TCT1y | 3.900 V | 3.800 V | 2.00 V | 2.00 V | 0.150 V | Unavailable | Available |
| S-8204BAJ-TCT1y | 4.300 V | 4.100 V | 2.50 V | 2.90 V | 0.250 V | Available | Available |
| S-8204BAK-TCT1y | 3.650 V | 3.500 V | 2.40 V | 3.00 V | 0.100 V | Available | Available |
| S-8204BAL-TCT1y | 4.200 V | 4.100 V | 2.70 V | 2.90 V | 0.250 V | Available | Available |
| S-8204BAM-TCT1y | 4.400 V | 4.200 V | 2.00 V | 2.70 V | 0.250 V | Available | Available |
| S-8204BAN-TCT1y | 4.100 V | 4.100 V | 2.00 V | 2.50 V | 0.150 V | Unavailable | Available |
| S-8204BAO-TCT1y | 3.900 V | 3.600 V | 2.50 V | 2.70 V | 0.100 V | Unavailable | Available |
| S-8204BAP-TCT1y | 4.320 V | 4.120 V | 2.40 V | 3.00 V | 0.100 V | Unavailable | Available |
| S-8204BAQ-TCT1y | 3.800 V | 3.600 V | 2.00 V | 2.30 V | 0.150 V | Available | Available |
| S-8204BAR-TCT1y | 3.850 V | 3.650 V | 2.50 V | 2.70 V | 0.150 V | Available | Available |
| S-8204BAS-TCT1y | 4.250 V | 4.150 V | 2.80 V | 3.00 V | 0.150 V | Available | Available |
| S-8204BAT-TCT1y | 3.650 V | 3.500 V | 2.00 V | 2.70 V | 0.100 V | Available | Available |
| S-8204BAU-TCT1y | 4.200 V | 4.100 V | 2.70 V | 2.90 V | 0.100 V | Available | Available |
| S-8204BAV-TCT1y | 3.900 V | 3.600 V | 2.00 V | 2.70 V | 0.100 V | Available | Available |
| S-8204BAW-TCT1y | 3.800 V | 3.650 V | 2.20 V | 2.50 V | 0.100 V | Available | Available |
| S-8204BAX-TCT1y | 4.250 V | 4.250 V | 2.00 V | 2.00 V | 0.100 V | Unavailable | Available |
| S-8204BAY-TCT1y | 3.900 V | 3.600 V | 2.30 V | 2.50 V | 0.100 V | Available | Available |
| S-8204BAZ-TCT1y | 4.250 V | 4.100 V | 3.00 V | 3.30 V | 0.100 V | Available | Available |
| S-8204BBA-TCT1y | 4.250 V | 4.150 V | 2.50 V | 3.00 V | 0.100 V | Available | Available |
| S-8204BBB-TCT1y | 4.250 V | 4.150 V | 2.70 V | 3.00 V | 0.250 V | Unavailable | Available |
| S-8204BBC-TCT1y | 4.250 V | 4.100 V | 2.80 V | 3.20 V | 0.250 V | Unavailable | Available |
| S-8204BBD-TCT1y | 4.300 V | 4.200 V | 2.30 V | 3.00 V | 0.100 V | Available | Available |
| S-8204BBE-TCT1y | 3.800 V | 3.600 V | 2.00 V | 2.30 V | 0.100 V | Available | Available |
| S-8204BBF-TCT1y | 3.800 V | 3.600 V | 2.00 V | 2.30 V | 0.050 V | Available | Available |
| S-8204BBG-TCT1y | 4.250 V | 4.100 V | 2.80 V | 3.30 V | 0.100 V | Unavailable | Available |
| S-8204BBH-TCT1y | 4.250 V | 4.150 V | 2.70 V | 3.00 V | 0.125 V | Unavailable | Available |
| S-8204BBI-TCT1U | 4.250 V | 4.150 V | 2.70 V | 3.00 V | 0.125 V | Unavailable | Unavailable |
| S-8204BBJ-TCT1U | 4.250 V | 4.150 V | 2.70 V | 3.00 V | 0.150 V | Unavailable | Unavailable |
| S-8204BBK-TCT1U | 4.250 V | 4.190 V | 2.80 V | 3.00 V | 0.150 V | Available | Available |
| S-8204BBL-TCT1U | 4.230 V | 4.230 V | 2.80 V | 3.00 V | 0.150 V | Available | Available |
| S-8204BBU-TCT1U | 4.350 V | 4.150 V | 2.30 V | 3.00 V | 0.100 V | Unavailable | Available |
| S-8204BBV-TCT1U | 4.450 V | 4.300 V | 2.70 V | 3.00 V | 0.100 V | Unavailable | Available |

**Remark 1.** Please contact our sales office for products with detection voltage values other than those specified above.
**2.** y: S or U
**3.** Please select products of environmental code = U for Sn 100%, halogen-free products.

## ■ Pin Configuration

### 1. 16-Pin TSSOP

Top view

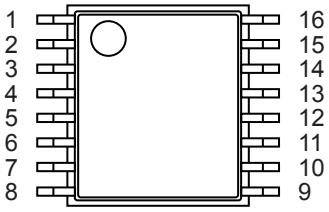



**Figure 2**

**Table 3**

| Pin No. | Symbol | Description |
|---|---|---|
| 1 | COP | Connection pin of charge control FET gate (Pch open-drain output) |
| 2 | VMP | Voltage detection pin between VDD pin and VMP pin |
| 3 | DOP | Connection pin of discharge control FET gate (CMOS output) |
| 4 | VINI | Voltage detection pin between VSS pin and VINI pin,<br>discharge overcurrent 1 / 2 detection pin, load short-circuit detection pin |
| 5 | CDT | Capacitor connection pin for delay for overdischarge detection |
| 6 | CCT | Capacitor connection pin for delay for overcharge detection |
| 7 | CIT | Capacitor connection pin for delay for discharge overcurrent 1 / 2 |
| 8 | SEL | Pin for switching 3-series or 4-series cell<br>• $V_{SS}$ level: 3-series cell<br>• $V_{DD}$ level: 4-series cell |
| 9 | VSS | Input pin for negative power supply,<br>connection pin for negative voltage of battery 4 |
| 10 | VC4 | Connection pin for negative voltage of battery 3,<br>connection pin for positive voltage of battery 4 |
| 11 | VC3 | Connection pin for negative voltage of battery 2,<br>connection pin for positive voltage of battery 3 |
| 12 | VC2 | Connection pin for negative voltage of battery 1,<br>connection pin for positive voltage of battery 2 |
| 13 | VC1 | Connection pin for positive voltage of battery 1 |
| 14 | VDD | Input pin for positive power supply,<br>connection pin for positive voltage of battery 1 |
| 15 | CTLD | Discharge FET control pin |
| 16 | CTLC | Charge FET control pin |

## ■ Absolute Maximum Ratings

**Table 4**

(Ta = +25°C unless otherwise specified)

| Item | Symbol | Applied Pin | Absolute Maximum Rating | Unit |
|---|---|---|---|---|
| Input voltage between VDD pin and VSS pin | $V_{DS}$ | – | $V_{SS}$ – 0.3 to $V_{SS}$ + 24 | V |
| Input pin voltage | $V_{IN}$ | VC1, VC2, VC3, VC4, CTLC, CTLD, SEL, CCT, CDT, CIT, VINI | $V_{SS}$ – 0.3 to $V_{DD}$ + 0.3 | V |
| VMP pin input voltage | $V_{VMP}$ | VMP | $V_{SS}$ – 0.3 to $V_{SS}$ + 24 | V |
| DOP pin output voltage | $V_{DOP}$ | DOP | $V_{SS}$ – 0.3 to $V_{DD}$ + 0.3 | V |
| COP pin output voltage | $V_{COP}$ | COP | $V_{DD}$ – 24 to $V_{DD}$ + 0.3 | V |
| Power dissipation | $P_D$ | – | 1100[*1] | mW |
| Operation ambient temperature | $T_{opr}$ | – | –40 to +85 | °C |
| Storage temperature | $T_{stg}$ | – | –40 to +125 | °C |

***1.** When mounted on board
[Mounted board]
(1) Board size: 114.3 mm × 76.2 mm × t1.6 mm
(2) Board name: JEDEC STANDARD51-7

**Caution The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any conditions.**

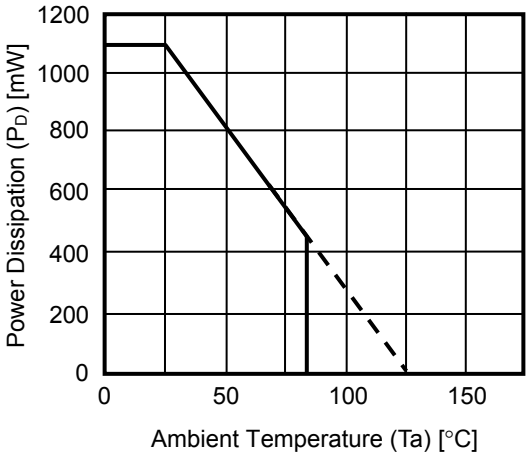



**Figure 3 Power Dissipation of Package (When Mounted on Board)**

## ■ Electrical Characteristics

**Table 5 (1 / 2)**

(Ta = +25°C unless otherwise specified)

| Item | Symbol | Condition | | Min. | Typ. | Max. | Unit | Test Circuit |
|---|---|---|---|---|---|---|---|---|
| **Detection Voltage** | | | | | | | | |
| Overcharge detection voltage n (n = 1, 2, 3, 4) | $V_{CUn}$ | 3.65 V to 4.6 V, adjustable, 50 mV step | | $V_{CUn}$ − 0.025 | $V_{CUn}$ | $V_{CUn}$ + 0.025 | V | 2 |
| Overcharge release voltage n (n = 1, 2, 3, 4) | $V_{CLn}$ | 3.5 V to 4.6 V, adjustable, 50 mV step | $V_{CL} \neq V_{CU}$ | $V_{CLn}$ − 0.05 | $V_{CLn}$ | $V_{CLn}$ + 0.05 | V | 2 |
| | | | $V_{CL} = V_{CU}$ | $V_{CLn}$ − 0.025 | $V_{CLn}$ | $V_{CLn}$ + 0.025 | V | 2 |
| Overdischarge detection voltage n (n = 1, 2, 3, 4) | $V_{DLn}$ | 2.0 V to 3.0 V, adjustable, 100 mV step | | $V_{DLn}$ − 0.08 | $V_{DLn}$ | $V_{DLn}$ + 0.08 | V | 2 |
| Overdischarge release voltage n (n = 1, 2, 3, 4) | $V_{DUn}$ | 2.0 V to 3.4 V, adjustable, 100 mV step | $V_{DL} \neq V_{DU}$ | $V_{DUn}$ − 0.10 | $V_{DUn}$ | $V_{DUn}$ + 0.10 | V | 2 |
| | | | $V_{DL} = V_{DU}$ | $V_{DUn}$ − 0.08 | $V_{DUn}$ | $V_{DUn}$ + 0.08 | V | 2 |
| Discharge overcurrent detection voltage 1 | $V_{DIOV1}$ | 0.05 V to 0.30 V, adjustable | | $V_{DIOV1}$ − 0.015 | $V_{DIOV1}$ | $V_{DIOV1}$ + 0.015 | V | 2 |
| Discharge overcurrent detection voltage 2 | $V_{DIOV2}$ | − | | 0.4 | 0.5 | 0.6 | V | 2 |
| Load short-circuit detection voltage | $V_{SHORT}$ | − | | 0.7 | 1.0 | 1.3 | V | 2 |
| Temperature coefficient 1*1 | $T_{COE1}$ | Ta = 0°C to 50°C*3 | | −1.0 | 0 | 1.0 | mV/°C | 2 |
| Temperature coefficient 2*2 | $T_{COE2}$ | Ta = 0°C to 50°C*3 | | −0.5 | 0 | 0.5 | mV/°C | 2 |
| **Delay Time Function*4** | | | | | | | | |
| CCT pin internal resistance | $R_{INC}$ | V1 = 4.7 V, V2 = V3 = V4 = 3.5 V | | 6.15 | 8.31 | 10.2 | MΩ | 3 |
| CDT pin internal resistance | $R_{IND}$ | V1 = 1.5 V, V2 = V3 = V4 = 3.5 V | | 615 | 831 | 1020 | kΩ | 3 |
| CIT pin internal resistance 1 | $R_{INI1}$ | V1 = V2 = V3 = V4 = 3.5 V | | 123 | 166 | 204 | kΩ | 3 |
| CIT pin internal resistance 2 | $R_{INI2}$ | V1 = V2 = V3 = V4 = 3.5 V | | 12.3 | 16.6 | 20.4 | kΩ | 3 |
| CCT pin detection voltage | $V_{CCT}$ | $V_{DS}$ = 15.2 V, V1 = 4.7 V, V2 = V3 = V4 = 3.5 V | | $V_{DS}$ × 0.68 | $V_{DS}$ × 0.70 | $V_{DS}$ × 0.72 | V | 3 |
| CDT pin detection voltage | $V_{CDT}$ | $V_{DS}$ = 12.0 V, V1 = 1.5 V, V2 = V3 = V4 = 3.5 V | | $V_{DS}$ × 0.68 | $V_{DS}$ × 0.70 | $V_{DS}$ × 0.72 | V | 3 |
| CIT pin detection voltage | $V_{CIT}$ | $V_{DS}$ = 14.0 V, V1 = V2 = V3 = V4 = 3.5 V | | $V_{DS}$ × 0.68 | $V_{DS}$ × 0.70 | $V_{DS}$ × 0.72 | V | 3 |
| Load short-circuit detection delay time | $t_{SHORT}$ | FET gate capacitance = 2000 pF | | 100 | 300 | 600 | μs | 3 |
| **0 V Battery Charge Function** | | | | | | | | |
| 0 V battery charge starting voltage | $V_{0CHA}$ | 0 V battery charge function "available" | | − | 1.2 | 2.0 | V | 2 |
| 0 V battery charge inhibition battery voltage | $V_{0INH}$ | 0 V battery charge function "unavailable" | | 0.4 | 0.7 | 1.1 | V | 2 |
| **Internal Resistance** | | | | | | | | |
| Resistance between VMP pin and VDD pin | $R_{VMD}$ | − | | 0.5 | 1 | 1.5 | MΩ | 4 |
| Resistance between VMP pin and VSS pin | $R_{VMS}$ | With power-down function | | 450 | 900 | 1800 | kΩ | 4 |

**Table 5 (2 / 2)**

(Ta = +25°C unless otherwise specified)

| Item | Symbol | Condition | Min. | Typ. | Max. | Unit | Test Circuit |
|---|---|---|---|---|---|---|---|
| **Input Voltage** | | | | | | | |
| Operation voltage between VDD pin and VSS pin | $V_{DSOP}$ | Fixed output voltage of DOP pin and COP pin | 2 | – | 22 | V | 2 |
| CTLC pin input voltage "H" | $V_{CTLCH}$ | V1 = V2 = V3 = V4 = 3.5 V | – | – | 13.2 | V | 2 |
| CTLC pin input voltage "L" | $V_{CTLCL}$ | V1 = V2 = V3 = V4 = 3.5 V | 10.1 | – | – | V | 2 |
| CTLD pin input voltage "H" | $V_{CTLDH}$ | V1 = V2 = V3 = V4 = 3.5 V | – | – | 13.2 | V | 2 |
| CTLD pin input voltage "L" | $V_{CTLDL}$ | V1 = V2 = V3 = V4 = 3.5 V | 10.1 | – | – | V | 2 |
| SEL pin input voltage "H" | $V_{SELH}$ | $V_{DS}$ = 14.0 V, V1 = V2 = V3 = V4 = 3.5 V | $V_{DS}$ × 0.8 | – | – | V | 2 |
| SEL pin input voltage "L" | $V_{SELL}$ | $V_{DS}$ = 14.0 V, V1 = V2 = V3 = V4 = 3.5 V | – | – | $V_{DS}$ × 0.2 | V | 2 |
| **Input Current** | | | | | | | |
| Current consumption during operation | $I_{OPE}$ | V1 = V2 = V3 = V4 = 3.5 V | – | 15 | 33 | µA | 1 |
| Current consumption during power-down | $I_{PDN}$ | With power-down function, V1 = V2 = V3 = V4 = 1.5 V | – | – | 0.1 | µA | 1 |
| Current consumption during overdischarge | $I_{OPED}$ | Without power-down function, V1 = V2 = V3 = V4 = 1.5 V | – | 14 | 32 | µA | 1 |
| VC1 pin current | $I_{VC1}$ | V1 = V2 = V3 = V4 = 3.5 V | 0.5 | 1.5 | 3.0 | µA | 4 |
| VC2 pin current | $I_{VC2}$ | V1 = V2 = V3 = V4 = 3.5 V | –0.3 | 0 | 0.3 | µA | 4 |
| VC3 pin current | $I_{VC3}$ | V1 = V2 = V3 = V4 = 3.5 V | –0.3 | 0 | 0.3 | µA | 4 |
| VC4 pin current | $I_{VC4}$ | V1 = V2 = V3 = V4 = 3.5 V | –0.3 | 0 | 0.3 | µA | 4 |
| CTLC pin current "H" | $I_{CTLCH}$ | V1 = V2 = V3 = V4 = 3.5 V, $V_{CTLC}$ = $V_{DD}$ | 0.4 | 0.6 | 0.8 | µA | 4 |
| CTLC pin current "L" | $I_{CTLCL}$ | V1 = V2 = V3 = V4 = 3.5 V, maximum current flowing from CTLC pin | –20.0 | –10.0 | –3.0 | µA | 4 |
| CTLD pin current "H" | $I_{CTLDH}$ | V1 = V2 = V3 = V4 = 3.5 V, $V_{CTLD}$ = $V_{DD}$ | 0.4 | 0.6 | 0.8 | µA | 4 |
| CTLD pin current "L" | $I_{CTLDL}$ | V1 = V2 = V3 = V4 = 3.5 V, maximum current flowing from CTLD pin | –20.0 | –10.0 | –3.0 | µA | 4 |
| SEL pin current "H" | $I_{SELH}$ | V1 = V2 = V3 = V4 = 3.5 V, $V_{SEL}$ = $V_{DD}$ | – | – | 0.1 | µA | 4 |
| SEL pin current "L" | $I_{SELL}$ | V1 = V2 = V3 = V4 = 3.5 V, $V_{SEL}$ = $V_{SS}$ | –0.1 | – | – | µA | 4 |
| **Output Current** | | | | | | | |
| COP pin source current | $I_{COH}$ | $V_{COP}$ = $V_{DD}$ – 0.5 V | 10 | – | – | µA | 4 |
| COP pin leakage current | $I_{COL}$ | $V_{COP}$ = 0 V | – | – | 0.1 | µA | 4 |
| DOP pin source current | $I_{DOH}$ | $V_{DOP}$ = $V_{DD}$ – 0.5 V | 10 | – | – | µA | 4 |
| DOP pin sink current | $I_{DOL}$ | $V_{DOP}$ = $V_{SS}$ + 0.5 V | 10 | – | – | µA | 4 |

***1.** Voltage temperature coefficient 1: Overcharge detection voltage

***2.** Voltage temperature coefficient 2: Discharge overcurrent detection voltage 1

***3.** Since products are not screened at high and low temperature, the specification for this temperature range is guaranteed by design, not tested in production.

***4.** Details of delay time function is described in "■ **Operation**".

## ■ Test Circuit

This chapter describes how to test the S-8204B Series. In case of selecting to use it for 4-series cell battery, set SEL pin = $V_{DD}$. For 3-series cell battery, set SEL pin = $V_{SS}$ and short between the VC4 pin and the VSS pin.

### 1. Current consumption during operation and power-down (Test circuit 1)

#### 1. 1 Current consumption during operation ($I_{OPE}$)

The current at the VSS pin when V1 = V2 = V3 = V4 = 3.5 V and $V_{VMP}$ = $V_{DD}$ is the current consumption during operation ($I_{OPE}$).

#### 1. 2 Current Consumption during power-down ($I_{PDN}$) (with power-down function)

The current at the VSS pin when V1 = V2 = V3 = V4 = 1.5 V and $V_{VMP}$ = $V_{SS}$ is the current consumption during power-down ($I_{PDN}$).

#### 1. 3 Current consumption during overdischarge ($I_{OPED}$) (without power-down function)

The current at the VSS pin when V1 = V2 = V3 = V4 = 1.5 V and $V_{VMP}$ = $V_{SS}$ is the current consumption during overdischarge ($I_{OPED}$).

### 2. Overcharge detection voltage, overcharge release voltage, overdischarge detection voltage, overdischarge release voltage, discharge overcurrent detection voltage 1, discharge overcurrent detection voltage 2, load short-circuit detection voltage, CTLC pin input voltage "H", CTLC pin input voltage "L", CTLD pin input voltage "H", CTLD pin input voltage "L", SEL pin input voltage "H", SEL pin input voltage "L" (Test circuit 2)

Confirm both the COP pin and the DOP pin are in "H" (its voltage level is $V_{DS} \times 0.9$ V or more) after setting $V_{VMP}$ = $V_{SEL}$ = $V_{CTLC}$ = $V_{CTLD}$ = $V_{DD}$, $V_{VINI}$ = $V_{SS}$, CCT pin = Open, CDT pin = Open, CIT pin = Open, V1 = V2 = V3 = V4 = 3.5 V. (This status is referred to as initial status.)

#### 2. 1 Overcharge detection voltage ($V_{CU1}$), overcharge release voltage ($V_{CL1}$)

The overcharge detection voltage ($V_{CU1}$) is a voltage at V1; when the COP pin's voltage is set to "L" (its voltage level is $V_{DD} \times 0.1$ V or less) after increasing a voltage at V1 gradually from the initial status. After that, decreasing a voltage at V1 gradually, a voltage at V1 when the COP pin's voltage is set to "H"; is the overcharge release voltage ($V_{CL1}$).

#### 2. 2 Overdischarge detection voltage ($V_{DL1}$), overdischarge release voltage ($V_{DU1}$)

The overdischarge detection voltage ($V_{DL1}$) is a voltage at V1; when the DOP pin's voltage is set to "L" after decreasing a voltage at V1 gradually from the initial status. After that, increasing a voltage at V1 gradually, a voltage at V1 when the DOP pin’s voltage is set to "H"; is the overdischarge release voltage ($V_{DU1}$).

By changing the voltage at Vn (n = 2 to 4), users can define the overcharge detection voltage ($V_{CUn}$), the overcharge release voltage ($V_{CLn}$), the overdischarge detection voltage ($V_{DLn}$), the overdischarge release voltage ($V_{DUn}$) as well when n = 1.

#### 2. 3 Discharge overcurrent detection voltage 1 ($V_{DIOV1}$)

The discharge overcurrent detection voltage 1 ($V_{DIOV1}$) is the VINI pin's voltage; when the DOP pin's voltage is set to "L" after increasing the VINI pin’s voltage gradually from the initial status.

#### 2. 4 Discharge overcurrent detection voltage 2 ($V_{DIOV2}$)

The discharge overcurrent detection voltage 2 ($V_{DIOV2}$) is a voltage at the VINI pin; when a flowing current from the CIT pin reaches 500 μA or more after increasing the VINI pin's voltage gradually from the initial status.

#### 2. 5 Load short-circuit detection voltage ($V_{SHORT}$)

The load short-circuit detection voltage ($V_{SHORT}$) is the VINI pin's voltage; when the DOP pin's voltage is set to "L" after increasing the VINI pin's voltage gradually after setting the CIT pin's voltage $V_{SS}$ level from the initial status.

### 2. 6 CTLC pin input voltage "H" ($V_{CTLCH}$), CTLC pin input voltage "L" ($V_{CTLCL}$)

The CTLC pin input voltage "L" ($V_{CTLCL}$) is the CTLC pin's voltage; when the COP pin's voltage is set to "L" after decreasing the CTLC pin's voltage gradually from the initial status. After that, increasing the CTLC pin's voltage gradually, the CTLC pin's voltage when the COP pin's voltage is set to "H"; is the CTLC pin input voltage "H" ($V_{CTLCH}$).

### 2. 7 CTLD pin input voltage "H" ($V_{CTLDH}$), CTLD pin input voltage "L" ($V_{CTLDL}$)

The CTLD pin input voltage "L" ($V_{CTLDL}$) is the CTLD pin's voltage; when the DOP pin's voltage is set to "L" after decreasing the CTLD pin's voltage gradually from the initial status. After that, increasing the CTLD pin's voltage gradually, the CTLD pin's voltage when the DOP pin's voltage is set to "H"; is the CTLD pin input voltage "H" ($V_{CTLDH}$).

### 2. 8 SEL pin input voltage "H" ($V_{SELH}$), SEL pin input voltage "L" ($V_{SELL}$)

Start from the initial status, set V4 = 0 V. Confirm the DOP pin is in "L". After that, decreasing the SEL pin's voltage gradually, the SEL pin's voltage when the DOP pin's voltage is set to "H"; is the SEL pin input voltage "L" ($V_{SELL}$). After that, increasing the SEL pin's voltage gradually, the SEL pin's voltage when the DOP pin's voltage is set to "L"; is the SEL pin input voltage "H" ($V_{SELH}$).

## 3. CCT pin internal resistance, CDT pin internal resistance, CIT pin internal resistance 1, CIT pin internal resistance 2, CCT pin detection voltage, CDT pin detection voltage, CIT pin detection voltage, load short-circuit detection delay time (Test circuit 3)

Confirm both the COP pin and the DOP pin are in "H" (its voltage level is $V_{DS} \times 0.9$ V or more) after setting $V_{VMP}$ = $V_{SEL}$ = $V_{CTLC}$ = $V_{CTLD}$ = $V_{DD}$, $V_{VINI}$ = CCT = CDT = CIT = $V_{SS}$, V1 = V2 = V3 = V4 = 3.5 V. (This status is referred to as initial status.)

### 3. 1 CCT pin internal resistance ($R_{INC}$)

The CCT pin internal resistance ($R_{INC}$) is $R_{INC} = V_{DS} / I_{CCT}$, $I_{CCT}$ is the current which flows from the CCT pin when setting V1 = 4.7 V from the initial status.

### 3. 2 CDT pin internal resistance ($R_{IND}$)

The CDT pin internal resistance ($R_{IND}$) is $R_{IND} = V_{DS} / I_{CDT}$, $I_{CDT}$ is the current which flows from the CDT pin when setting V1 = 1.5 V from the initial status.

### 3. 3 CIT pin internal resistance 1 ($R_{INI1}$)

The CIT pin internal resistance 1 ($R_{INI1}$) is $R_{INI1} = V_{DS} / I_{CIT1}$, $I_{CIT1}$ is the current which flows from the CIT pin when setting $V_{VINI} = V_{DIOV1}$ max. + 0.05 V from the initial status.

### 3. 4 CIT pin internal resistance 2 ($R_{INI2}$)

The CIT pin internal resistance 2 ($R_{INI2}$) is $R_{INI2} = V_{DS} / I_{CIT2}$, $I_{CIT2}$ is the current which flows from the CIT pin when setting $V_{VINI} = V_{DIOV2}$ max. + 0.05 V from the initial status.

### 3. 5 CCT pin detection voltage ($V_{CCT}$)

The CCT pin detection voltage ($V_{CCT}$) is the voltage at the CCT pin when the COP pin's voltage is set to "L" (voltage $V_{DS} \times 0.1$ V or less) after increasing the CCT pin's voltage gradually, after setting V1 = 4.7 V from the initial status.

### 3. 6 CDT pin detection voltage ($V_{CDT}$)

The CDT pin detection voltage ($V_{CDT}$) is the voltage at the CDT pin when the DOP pin's voltage is set to "L" (voltage $V_{DS} \times 0.1$ V or less) after increasing the CDT pin's voltage gradually, after setting V1 = 1.5 V from the initial status.

### 3. 7 CIT pin detection voltage ($V_{CIT}$)

The CIT pin detection voltage ($V_{CIT}$) is the voltage at the CIT pin when the DOP pin's voltage is set to "L" (voltage $V_{DS} \times 0.1$ V or less) after increasing the CIT pin's voltage gradually, after setting $V_{VINI} = V_{DIOV1}$ max. + 0.05 V from the initial status.

### 3. 8 Load short-circuit detection delay time ($t_{SHORT}$)

Load short-circuit detection delay time ($t_{SHORT}$) is a period in which the VINI pin's voltage changes from "H" to "L" by changing the VINI pin's voltage instantaneously from the initial status to $V_{SHORT}$ max. + 0.05 V.

## 4. 0 V battery charge starting voltage (0 V battery charge function "available"), 0 V battery charge inhibition battery voltage (0 V battery charge function "unavailable") (Test circuit 2)

Confirm both COP pin and DOP pin are in "H" (its voltage level is $V_{DS} \times 0.9$ V or more) after setting $V_{VMP} = V_{SEL} = V_{CTLC} = V_{CTLD} = V_{DD}$, $V_{VINI} = V_{SS}$, CCT pin = Open, CDT pin = Open, CIT pin = Open, V1 = V2 = V3 = V4 = 3.5 V. (This status is referred to as initial status.)

According to user's selection of the function to charge 0 V battery, either function of voltage for start charging 0 V battery or battery voltage for inhibit charging 0 V battery is applied to each product.

### 4. 1 0 V battery charge starting voltage ($V_{0CHA}$) (0 V battery charge function "available")

0 V battery charge starting voltage ($V_{0CHA}$) is a voltage at V1; when a voltage at the COP pin is set to "H" after increasing a voltage at V1 gradually, after setting V1 = V2 = V3 = V4 = 0 V from the initial status.

### 4. 2 0 V battery charge inhibition battery voltage ($V_{0INH}$) (0 V battery charge function "unavailable")

0 V battery charge inhibition battery voltage ($V_{0INH}$) is a voltage at V1; when a voltage at the COP pin is set to "L" after decreasing a voltage at V1 gradually from the initial status.

## 5. Resistance between VMP pin and VDD pin, resistance between VMP pin and VSS pin, VC1 pin current, VC2 pin current, VC3 pin current, VC4 pin current, CTLC pin current "H", CTLC pin current "L", CTLD pin current "H", CTLD pin current "L", SEL pin current "H", SEL pin current "L", COP pin source current, COP pin leakage current, DOP pin source current, DOP pin sink current (Test circuit 4)

Set $V_{CTLC} = V_{CTLD} = V_{VMP} = V_{SEL} = V_{DD}$, $V_{VINI} = V_{SS}$, V1 = V2 = V3 = V4 = 3.5 V, set other pins open. (This status is referred to as initial status.)

### 5. 1 Resistance between VMP pin and VDD pin ($R_{VMD}$)

The value of resistance between VMP pin and VDD pin ($R_{VMD}$) can be defined by $R_{VMD} = V_{DS} / I_{VMD}$ by using the VMP pin's current ($I_{VMD}$) when $V_{VINI} = 1.5$ V and $V_{VMP} = V_{SS}$ after the initial status.

### 5. 2 Resistance between VMP pin and VSS pin ($R_{VMS}$)

The value of resistance between VMP pin and VSS pin ($R_{VMS}$) can be defined by $R_{VMS} = V_{DS} / I_{VMS}$ by using the VMP pin's current ($I_{VMS}$) when V1 = V2 = V3 = V4 = 1.8 V after the initial status.

### 5. 3 VC1 pin current ($I_{VC1}$), VC2 pin current ($I_{VC2}$), VC3 pin current ($I_{VC3}$), VC4 pin current ($I_{VC4}$)

In the initial status, each current flows in the VC1 pin, VC2 pin, VC3 pin, VC4 pin is the VC1 pin current ($I_{VC1}$), the VC2 pin current ($I_{VC2}$), the VC3 pin current ($I_{VC3}$), the VC4 pin current ($I_{VC4}$), respectively.

### 5. 4 CTLC pin current "H" ($I_{CTLCH}$), CTLC pin current "L" ($I_{CTLCL}$)

In the initial status, a current which flows in the CTLC pin is the CTLC pin current "H" ($I_{CTLCH}$). After that, decreasing a voltage at the CTLC pin gradually, the maximum current which flows in the CTLC pin is; the CTLC pin current "L" ($I_{CTLCL}$).

### 5. 5 CTLD pin current "H" ($I_{CTLDH}$), CTLD pin current "L" ($I_{CTLDL}$)

In the initial status, a current which flows in the CTLD pin is the CTLD pin current "H" ($I_{CTLDH}$). After that, decreasing a voltage at the CTLD pin gradually, the maximum current which flows in the CTLD pin is; the CTLD pin current "L" ($I_{CTLDL}$).

### 5. 6 SEL pin current "H" ($I_{SELH}$), SEL pin current "L" ($I_{SELL}$)

In the initial status, a current which flows in the SEL pin is the SEL pin current "H" ($I_{SELH}$). After that, a current which flows in the SEL pin when setting $V_{SEL} = V_{SS}$ is; the SEL pin current "L" ($I_{SELL}$).

### 5. 7 COP pin source current ($I_{COH}$), COP pin leakage current ($I_{COL}$)

Start from the initial status, set $V_{COP} = V_{DD} - 0.5$ V, a current which flows in the COP pin is the COP pin source current ($I_{COH}$). After that, a current which flows in the COP pin when setting V1 = V2 = V3 = V4 = 5.5 V, $V_{COP} = V_{SS}$ is; the COP pin leakage current ($I_{COL}$).

### 5. 8 DOP pin source current ($I_{DOH}$), DOP pin sink current ($I_{DOL}$)

Start from the initial status, set $V_{DOP} = V_{DD} - 0.5$ V, a current which flows in the DOP pin is the DOP pin source current ($I_{DOH}$). After that, a current which flows in the DOP pin when setting V1 = V2 = V3 = V4 = 1.8 V, $V_{DOP} = V_{SS} + 0.5$ V is; the DOP pin sink current ($I_{DOL}$).

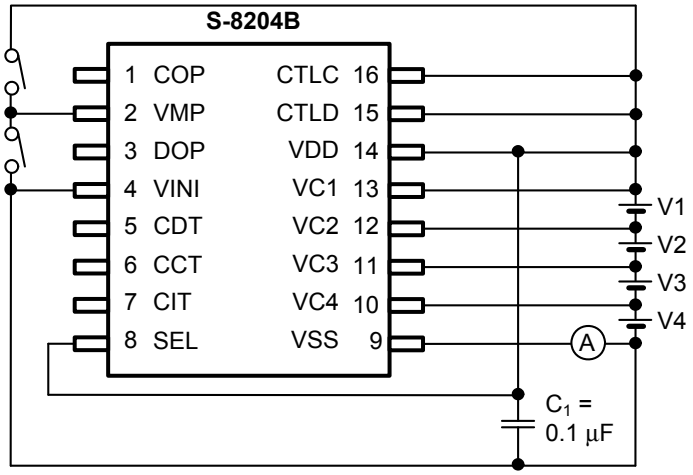



**Figure 4 Test Circuit 1**

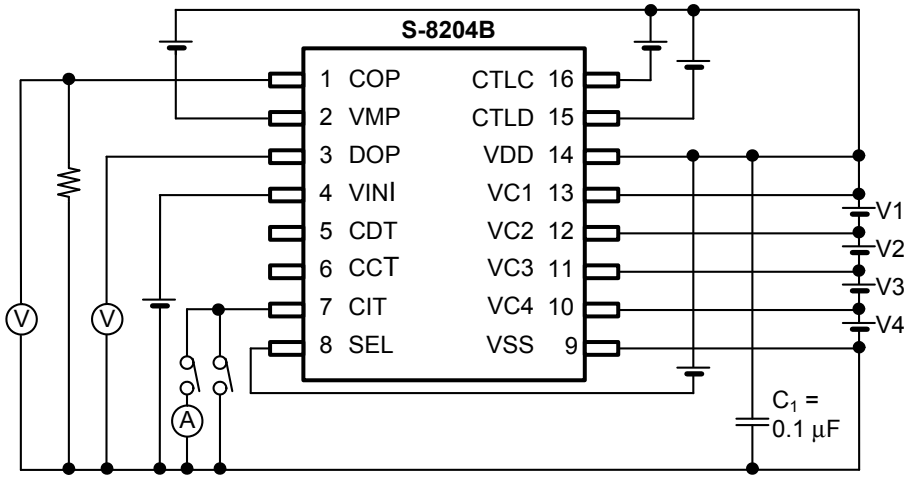



**Figure 5 Test Circuit 2**

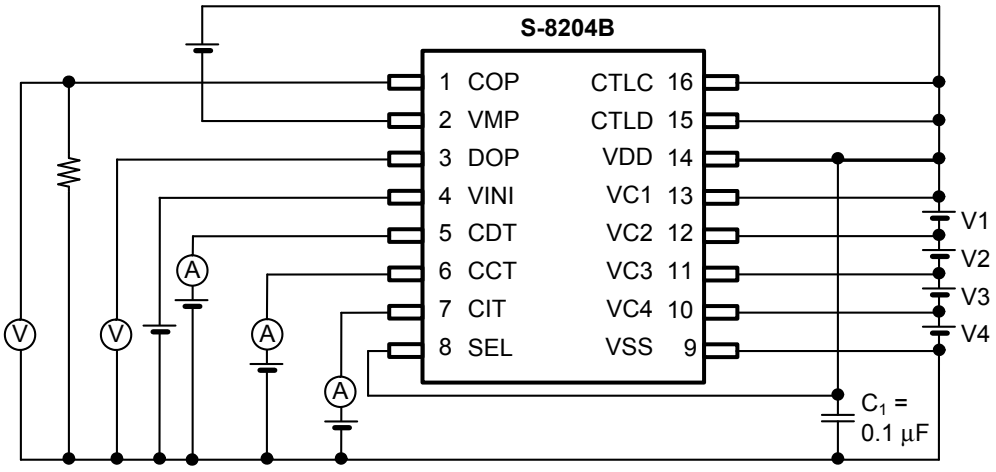



**Figure 6 Test Circuit 3**

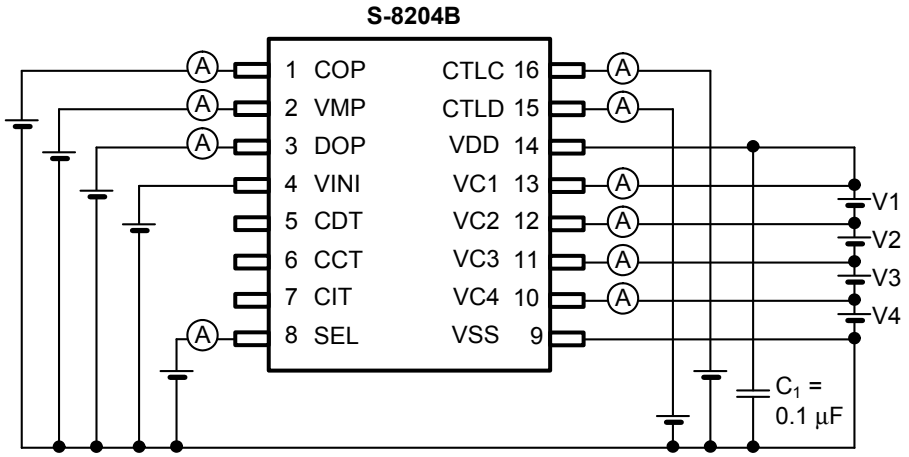



**Figure 7 Test Circuit 4**

## ■ Operation

**Remark** Refer to "■ **Connection Examples of Battery Protection IC**".

### 1. Normal status

In the S-8204B Series, both of the COP pin and the DOP pin get the $V_{DD}$ level; when the voltage of each of the batteries is in the range of overdischarge detection voltage ($V_{DLn}$) to overcharge detection voltage ($V_{CUn}$), and due to the discharge current, the VINI pin's voltage is discharge overcurrent detection voltage ($V_{DIOV1}$) or less. This is the normal status. At this time, the charge FET and discharge FET are on.

### 2. Overcharge status

In the S-8204B Series, the voltage of one of the batteries increases to the level of more than $V_{CUn}$, the COP pin is set in high impedance. This is the overcharge status. The COP pin is pulled down to EB− by an external resistor so that the charge FET is turned off and it stops charging.

This overcharge status is released if either condition mentioned below is satisfied;

(1) In case that the VMP pin voltage is 39 / 40 × $V_{DS}$ or more; the voltage of each of the batteries is in the level of overcharge release voltage ($V_{CLn}$) or less.
(2) In case that the VMP pin voltage is 39 / 40 × $V_{DS}$ or less; the voltage of each of the batteries is in the level of $V_{CUn}$ or less.

### 3. Overdischarge status

In the S-8204B Series, when the voltage of one of the batteries decreases to the level of less than $V_{DLn}$, the DOP pin voltage gets the $V_{SS}$ level. This is the overdischarge status. The discharge FET is turned off and it stops discharging.

This overcharge status is released if either condition mentioned below is satisfied;

(1) To release; the VMP pin voltage is in the level of more than $V_{DD}$, the voltage of each of the batteries is in the $V_{DLn}$ level or more.
(2) To release; the VMP pin voltage is $V_{DS}$ / 2 or more and the VMP pin voltage is in the level of less than $V_{DD}$, the voltage of each of the batteries is in the level of overdischarge release voltage ($V_{DUn}$) or more.

#### 3. 1 Power-down function

In the S-8204B Series, power-down function "available" / "unavailable" is selectable.

##### 3. 1. 1 With power-down function

When the S-8204B Series reaches the overdischarge status, the VMP pin is pulled down to the $V_{SS}$ level by a resistor between the VMP pin and the VSS pin ($R_{VMS}$). If the VMP pin voltage decreases to the level of $V_{DS}$ / 2 or less, the power-down function starts to operate and almost every circuit in the S-8204B Series stops working.

The power-down function is released if the following condition is satisfied.

(1) The VMP pin voltage gets $V_{DS}$ / 2 or more.

##### 3. 1. 2 Without power-down function

The VMP pin is not pulled down even when the S-8204B Series reaches the overdischarge status. The overdischarge status is maintained even If the VMP pin voltage decreases to the level of $V_{DS}$ / 2 or less, and the current consumption decreases to the level of current consumption during overdischarge ($I_{OPED}$) or less.

### 4. Discharge overcurrent status

In the S-8204B Series, in batteries in the normal status, the discharging current increases more than a certain value. As a result, if the status in which the VINI pin voltage increases to the level of $V_{DIOV1}$ or more, the DOP pin gets the $V_{SS}$ level. This is the discharge overcurrent status. At this time, the discharge control FET is turned off and it stops discharging.

The S-8204B Series has three levels for discharge overcurrent detection ($V_{DIOV1}$, $V_{DIOV2}$, $V_{SHORT}$). In the status of discharge overcurrent, the COP pin is set in high impedance. The VMP pin is pulled up to the $V_{DD}$ level by a resistor between the VMP pin and the VDD pin ($R_{VMD}$).
The S-8204B Series' operations against discharge overcurrent detection voltage 2 ($V_{DIOV2}$) and load short-circuit detection voltage ($V_{SHORT}$) are as well in $V_{DIOV1}$.

The discharge overcurrent status is released if the following condition is satisfied.

(1) The VMP pin voltage gets $V_{DS}$ −1.2 V (typ.) or more.

### 5. 0 V battery charge function

In the S-8204B Series, regarding how to charge a discharged battery (0 V battery), users are able to select either function mentioned below.

(1) Allow to charge a 0 V battery (enable to charge a 0 V battery)
A 0 V battery is charged when the voltage between the VDD pin and the VSS pin ($V_{DS}$) is 0 V battery charge starting voltage ($V_{0CHA}$) or more.

(2) Inhibit charging a 0 V battery (unable to charge a 0 V battery)
A 0 V battery is not charged when the battery voltage is 0 V battery charge inhibition battery voltage ($V_{0INH}$) or less.

**Caution When the VDD pin voltage is less than the minimum value of operation voltage between the VDD pin and the VSS pin ($V_{DSOP}$), the operation of the S-8204B Series is not assured.**

## 6. Delay time setting

In the S-8204B Series, users are able to set delay time for the period; from detecting the voltage of one of the batteries or detecting changes in the voltage at the VINI pin, to the output to the COP pin and the DOP pin. Each delay time is determined by a resistor in the S-8204B Series and an external capacitor.

In the overchage detection, when the voltage of one of the batteries gets $V_{CUn}$ or more, the S-8204B Series starts charging to the CCT pin's capacitor ($C_{CCT}$) via the CCT pin's internal resistor ($R_{INC}$). After a certain period, the COP pin is set in high impedance if the voltage at the CCT pin reaches the CCT pin detection voltage ($V_{CCT}$). This period is overcharge detection delay time ($t_{CU}$).

$t_{CU}$ is calculated using the following equation ($V_{DS} = V1 + V2 + V3 + V4$).

$$t_{CU} [s] = -\ln (1 - V_{CCT} / V_{DS}) \times C_{CCT} [\mu F] \times R_{INC} [M\Omega]$$
$$= -\ln (1 - 0.7 \text{ (typ.)}) \times C_{CCT} [\mu F] \times 8.31 [M\Omega] \text{ (typ.)}$$
$$= 10.0 [M\Omega] \text{ (typ.)} \times C_{CCT} [\mu F]$$

Overdischarge detection delay time ($t_{DL}$), discharge overcurrent detection delay time 1 ($t_{DIOV1}$), discharge overcurrent detection delay time 2 ($t_{DIOV2}$) are calculated using the following equations as well.

$$t_{DL} [ms] = -\ln (1 - V_{CDT} / V_{DS}) \times C_{CDT} [\mu F] \times R_{IND} [k\Omega]$$
$$t_{DIOV1} [ms] = -\ln (1 - V_{CIT} / V_{DS}) \times C_{CIT} [\mu F] \times R_{INI1} [k\Omega]$$
$$t_{DIOV2} [ms] = -\ln (1 - V_{CIT} / V_{DS}) \times C_{CIT} [\mu F] \times R_{INI2} [k\Omega]$$

In case $C_{CCT} = C_{CDT} = C_{CIT} = 0.1$ [μF], each delay time $t_{CU}$, $t_{DL}$, $t_{DIOV1}$, $t_{DIOV2}$ is calculated as follows.

$$t_{CU} [s] = 10.0 [M\Omega] \text{ (typ.)} \times 0.1 [\mu F] = 1.0 [s] \text{ (typ.)}$$
$$t_{DL} [ms] = 1000 [k\Omega] \text{ (typ.)} \times 0.1 [\mu F] = 100 [ms] \text{ (typ.)}$$
$$t_{DIOV1} [ms] = 200 [k\Omega] \text{ (typ.)} \times 0.1 [\mu F] = 20 [ms] \text{ (typ.)}$$
$$t_{DIOV2} [ms] = 20 [k\Omega] \text{ (typ.)} \times 0.1 [\mu F] = 2.0 [ms] \text{ (typ.)}$$

Load short-circuit detection delay time ($t_{SHORT}$) is fixed internally.

## 7. CTLC pin and CTLD pin

The S-8204B Series has two pins to control.
The CTLC pin controls the output voltage from the COP pin, the CTLD pin controls the output voltage from the DOP pin. Thus it is possible for users to control the output voltages from the COP pin and DOP pin independently. These controls precede the battery protection circuit.

**Table 6 Conditions Set by CTLC Pin**

| CTLC Pin | COP Pin |
|---|---|
| "H"*1 | Normal status*4 |
| Open*2 | "High-Z" |
| "L"*3 | "High-Z" |

***1.** "H"; CTLC ≥ $V_{CTLCH}$
***2.** Pulled down by $I_{CTLCH}$
***3.** "L"; CTLC ≤ $V_{CTLCL}$
***4.** The status is controlled by the voltage detection circuit.

**Table 7 Conditions Set by CTLD Pin**

| CTLD Pin | DOP Pin |
|---|---|
| "H"*1 | Normal status*4 |
| Open*2 | $V_{SS}$ level |
| "L"*3 | $V_{SS}$ level |

***1.** "H"; CTLD ≥ $V_{CTLDH}$
***2.** Pulled down by $I_{CTLDH}$
***3.** "L"; CTLD ≤ $V_{CTLDL}$
***4.** The status is controlled by the voltage detection circuit.

**Caution Note that when the power supply fluctuates, unexpected behavior might occur if an electrical potential is generated between the potentials of "H" level input to the CTLC pin / the CTLD pin and IC's $V_{DD}$ by external filters $R_{VDD1}$ and $C_{VDD1}$.**

## 8. SEL pin

The S-8204B Series has a pin to switch-control the protection for 3-cell or 4-cell battery.
The overdischarge detection for V4-cell is inhibited by setting the SEL pin "L", so that short-circuiting the V4 cell does not allow the overdischarge detection. This setting makes it possible to use the S-8204B Series for 3-cell protection. The control by this SEL pin precedes the battery protection circuit. Be sure to use the SEL pin in "H" or "L".

**Table 8 Conditions Set by SEL Pin**

| SEL Pin | Condition |
|---|---|
| "H"*1 | 4-cell protection |
| Open | Indefinite |
| "L"*2 | 3-cell protection |

***1.** "H"; SEL ≥ $V_{SELH}$
***2.** "L"; SEL ≤ $V_{SELL}$

In cascade connection, it is possible to use the S-8204B Series for protecting 6-cell, 7-cell or 8-cell battery by combining the electrical level of the SEL pin.

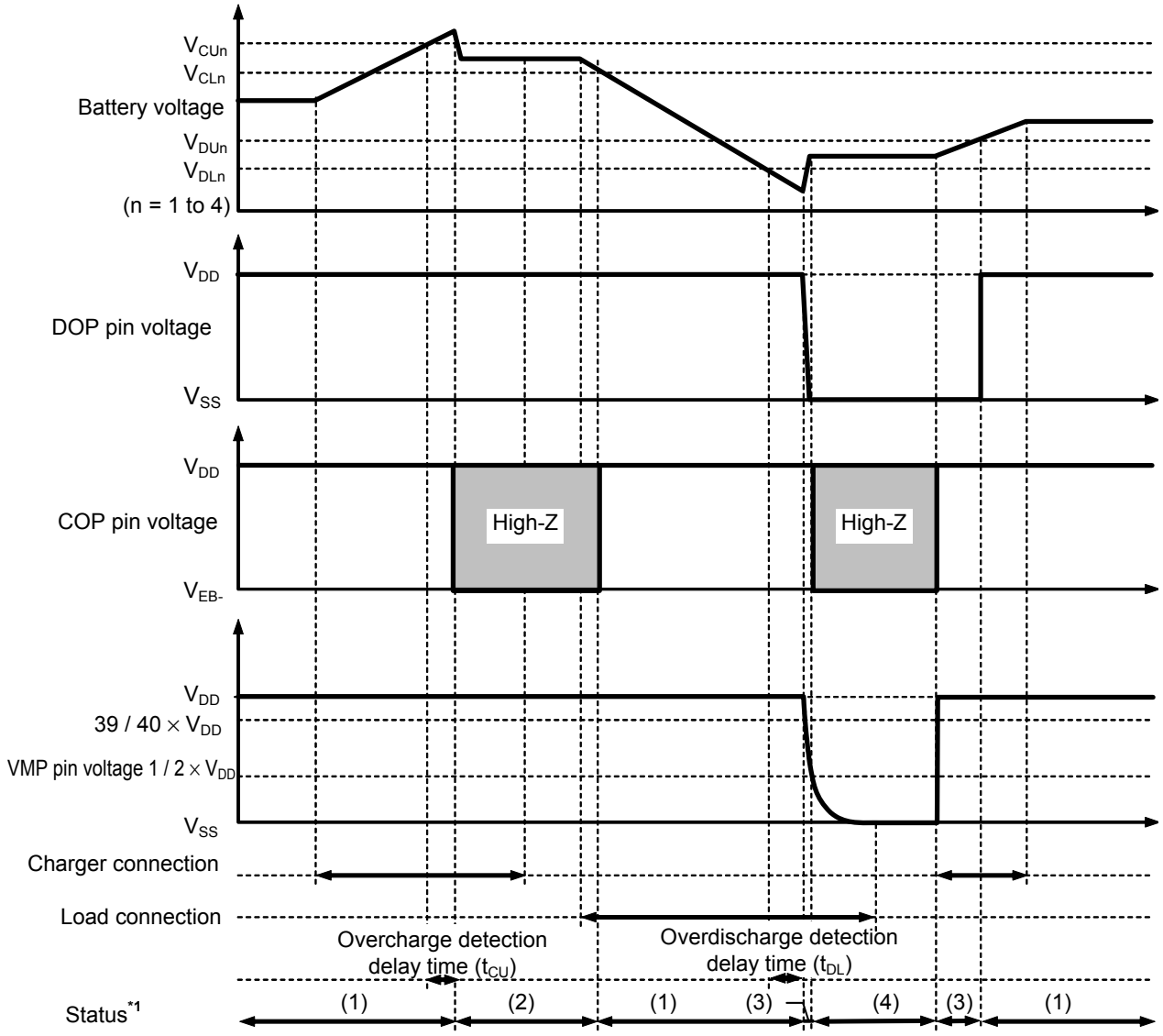
**Table 9 Conditions Set by SEL Pin in Cascade Connection**

| SEL pin in S-8204B (1) | SEL pin in S-8204B (2) | Condition |
|---|---|---|
| "L"*1 | "L"*1 | 6-series cell protection |
| "L"*1 | "H"*2 | 7-series cell protection |
| "H"*2 | "H"*2 | 8-series cell protection |

***1.** "L"; SEL ≤ $V_{SELL}$
***2.** "H"; SEL ≥ $V_{SELH}$

## ■ Timing Chart (Circuit in Figure 11)

### 1. Overcharge detection and overdischarge detection (with power-down function)

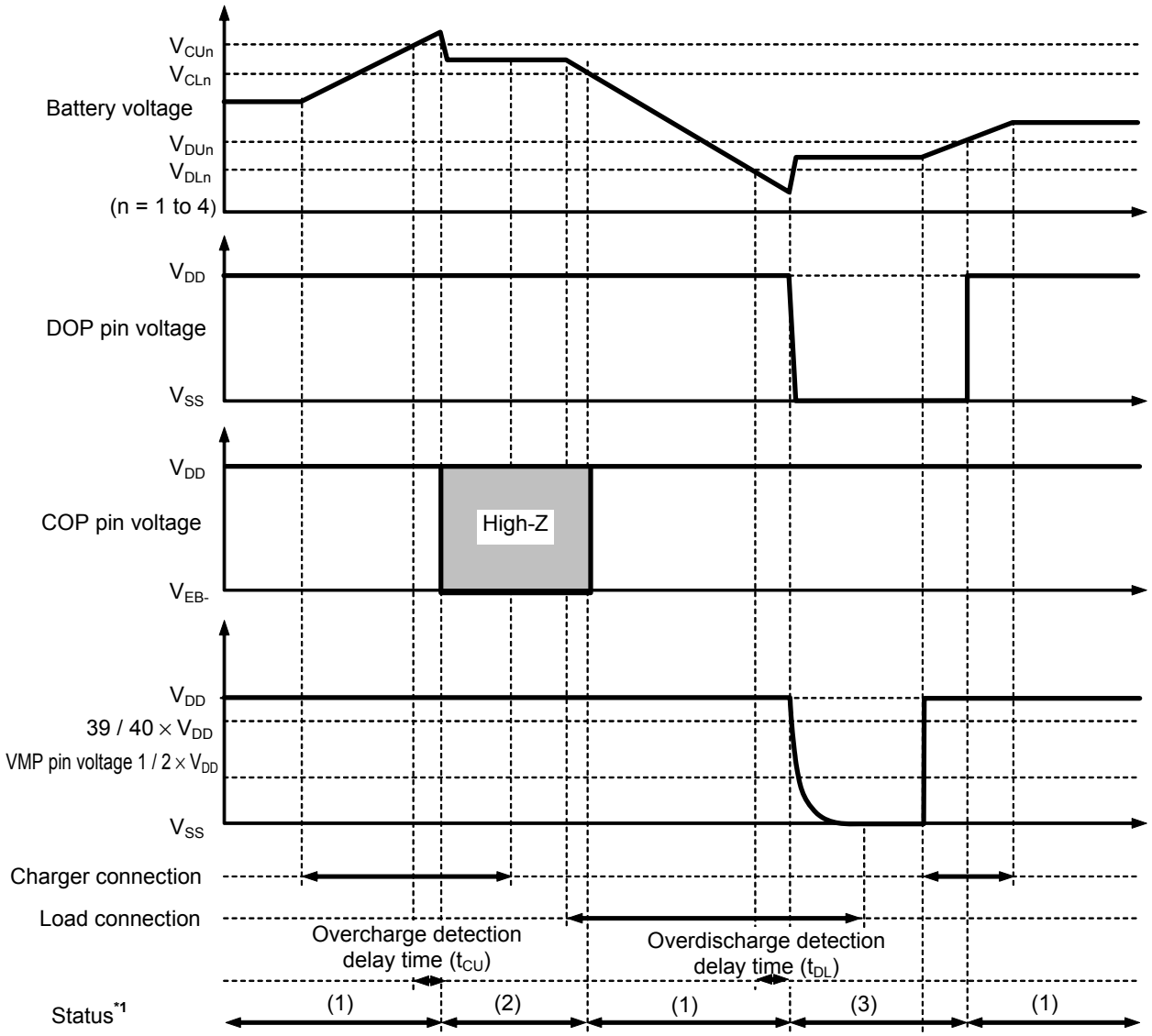



***1.** (1): Normal status
(2): Overcharge status
(3): Overdischarge status
(4): Power-down status

**Remark** The charger is assumed to charge with a constant current. $V_{EB-}$ indicates the open voltage of the charger.

**Figure 8**

**2. Overcharge detection and overdischarge detection (without power-down function)**

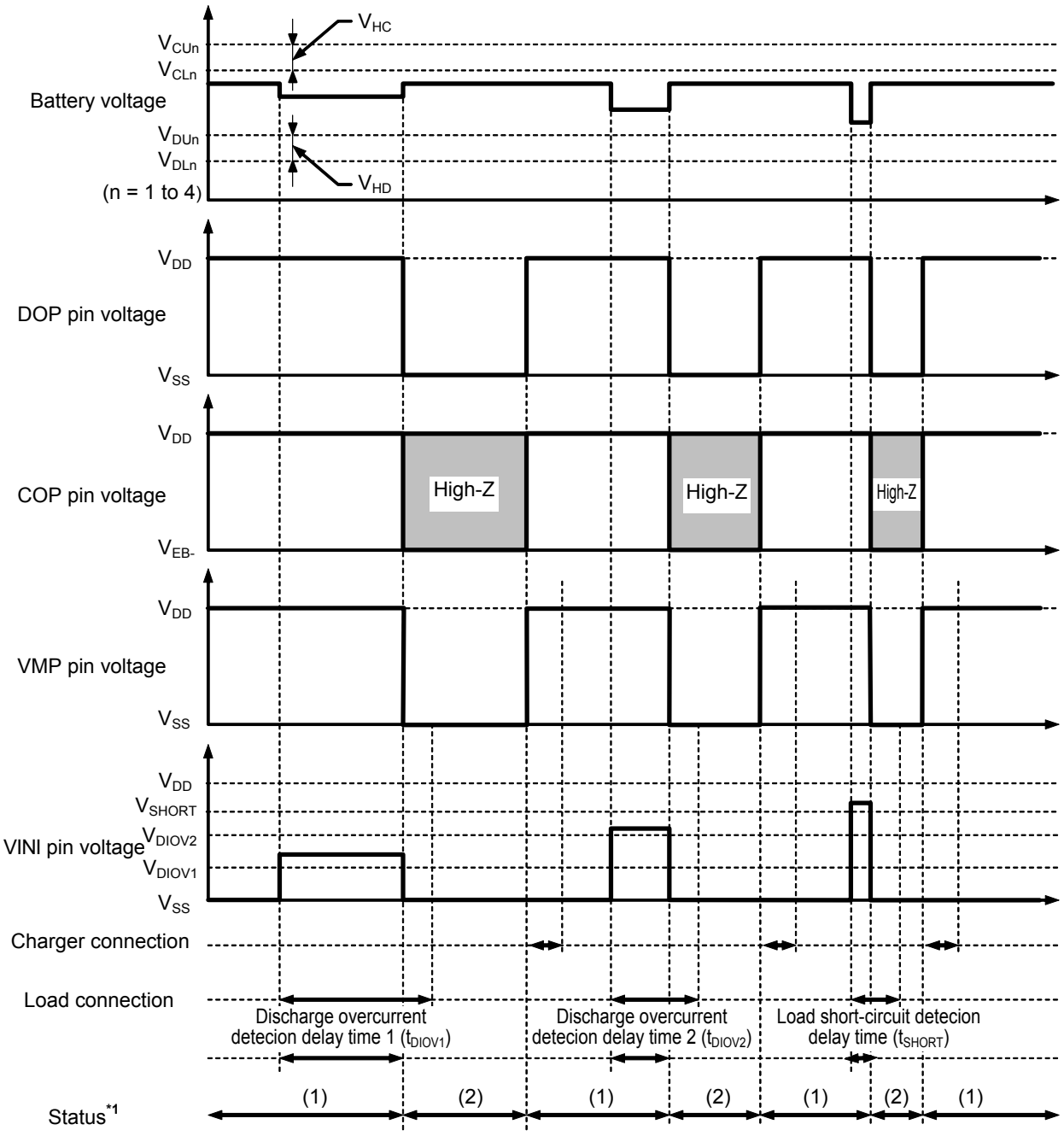



***1.** (1): Normal status
(2): Overcharge status
(3): Overdischarge status

**Remark** The charger is assumed to charge with a constant current. $V_{EB-}$ indicates the open voltage of the charger.

**Figure 9**

### 3. Discharge overcurrent detection




***1.** (1): Normal status
(2): Discharge overcurrent status

**Remark** The charger is assumed to charge with a constant current. $V_{EB-}$ indicates the open voltage of the charger.

**Figure 10**

## ■ Connection Examples of Battery Protection IC

### 1. 4-series cell (with overcurrent protection function)

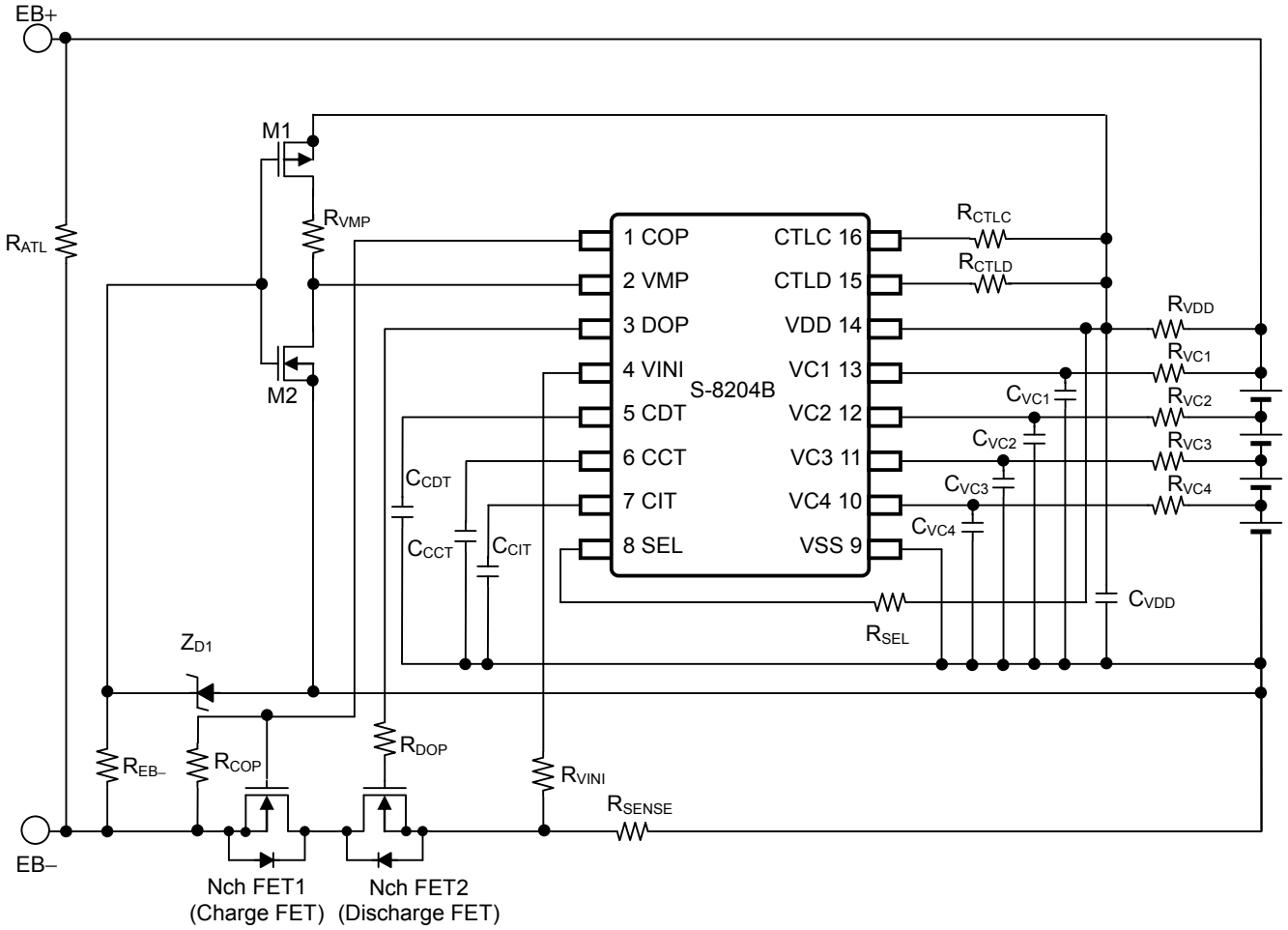



**Figure 11**

**Table 10 Constants for External Components (Circuit in Figure 11)**

| Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|
| $R_{VC1}$ *1 | 0.51 | 1 | 1 | kΩ |
| $R_{VC2}$ *1 | 0.51 | 1 | 1 | kΩ |
| $R_{VC3}$ *1 | 0.51 | 1 | 1 | kΩ |
| $R_{VC4}$ *1 | 0.51 | 1 | 1 | kΩ |
| $R_{DOP}$ | 2 | 5.1 | 10 | kΩ |
| $R_{COP}$ | 0.1 | 1 | 1 | MΩ |
| $R_{VMP}$ | 1 | 5.1 | 10 | kΩ |
| $R_{CTLC}$ | 1 | 1 | 10 | kΩ |
| $R_{CTLD}$ | 1 | 1 | 10 | kΩ |
| $R_{VINI}$ | 1 | 1 | 10 | kΩ |
| $R_{SEL}$ | 1 | 1 | 100 | kΩ |
| $R_{VDD}$ *1 | 22 | 47 | 100 | Ω |
| $C_{VC1}$ *1 | 0 | 47 | 100 | nF |
| $C_{VC2}$ *1 | 0 | 47 | 100 | nF |
| $C_{VC3}$ *1 | 0 | 47 | 100 | nF |
| $C_{VC4}$ *1 | 0 | 47 | 100 | nF |
| $C_{CCT}$ | 0.01 | 0.1 | – | μF |
| $C_{CDT}$ | 0.01 | 0.1 | – | μF |
| $C_{VDD}$ *1 | 0 | 1 | 2.2 | μF |
| $C_{CIT}$ | – | 0.1 | – | μF |
| $R_{SENSE}$ | – | – | – | – |
| M1 | – | – | – | – |
| M2 | – | – | – | – |
| $Z_{D1}$ | – | – | – | – |
| $R_{EB-}$ | – | 1 | – | MΩ |
| $R_{ATL}$ | – | 20 | – | MΩ |
| Nch FET1 | – | – | – | – |
| Nch FET2 | – | – | – | – |

***1.** Set up a filter constant to be $R_{VDD} \times C_{VDD}$ = 47 μF • Ω or more, and to be $R_{VC1} \times C_{VC1} = R_{VC2} \times C_{VC2} = R_{VC3} \times C_{VC3} = R_{VC4} \times C_{VC4} = R_{VDD} \times C_{VDD}$.

**Caution 1. The above constants may be changed without notice.**

**2. It is recommended that filter constants between the VDD pin and the VSS pin should be set to approximately 47 μF • Ω.**

**e.g., $C_{VDD} \times R_{VDD}$ = 1.0 μF × 47 Ω = 47 μF • Ω**

**Sufficient evaluation of transient power supply fluctuation and overcurrent protection function with the actual application is needed to determine the proper constants. Contact our sales office in case the constants should be set to other than 47 μF • Ω.**

**3. It has not been confirmed whether the operation is normal in circuits other than the above example of connection. In addition, the example of connection shown above and the constants do not guarantee proper operation. Perform thorough evaluation using an actual application to set the constant.**

**2. 7-series cell (cascade connection without overcurrent protection function)**

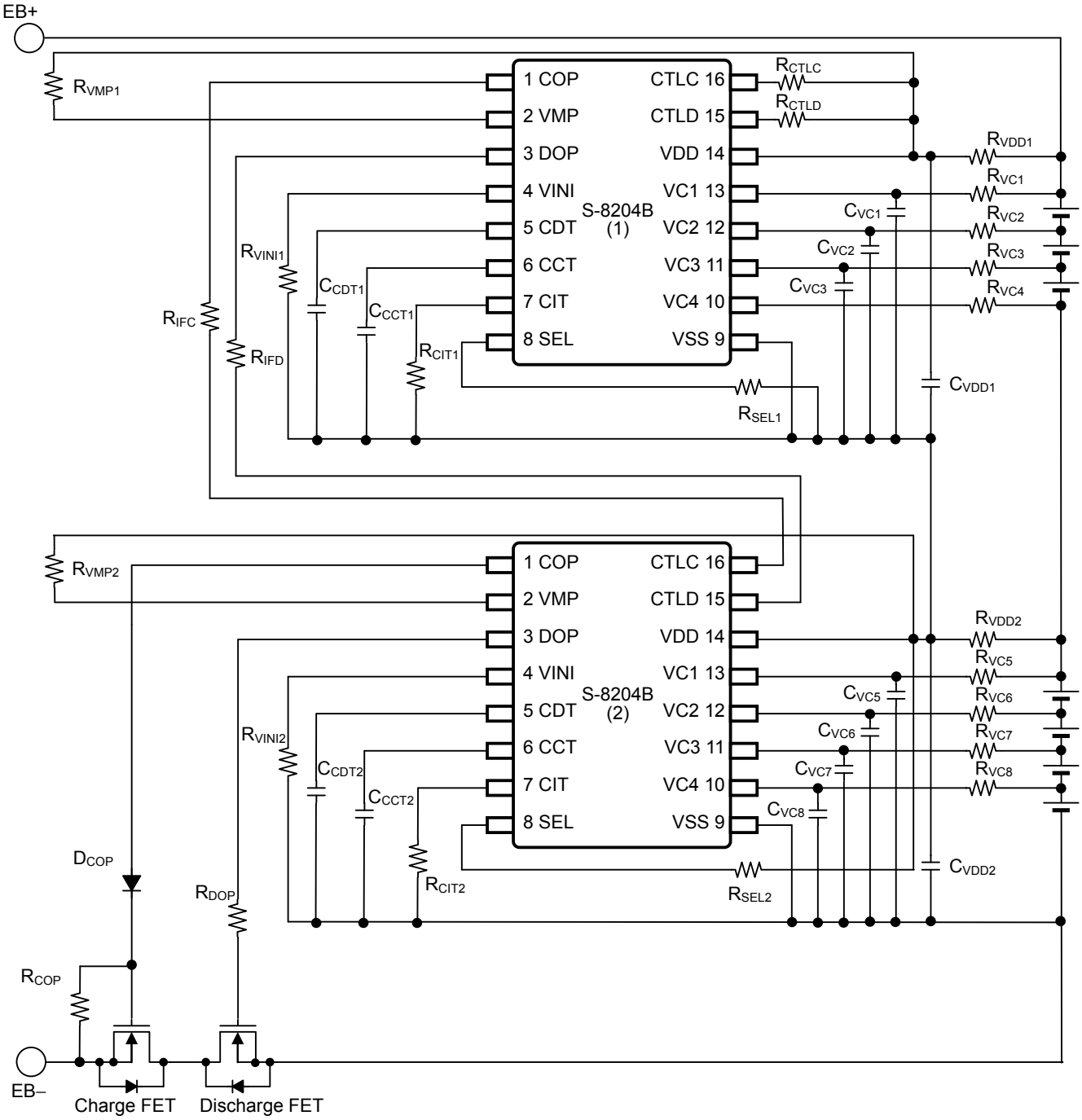



**Figure 12**

**Caution 1. It is recommended that filter constants between the VDD pin and the VSS pin should be set to approximately 47 μF • Ω.**

**e.g., $C_{VDD} \times R_{VDD}$ = 1.0 μF × 47 Ω = 47 μF • Ω**

**Sufficient evaluation of transient power supply fluctuation and overcurrent protection function with the actual application is needed to determine the proper constants. Contact our sales office in case the constants should be set to other than 47 μF • Ω.**

**2. It has not been confirmed whether the operation is normal in circuits other than the above example of connection. In addition, the example of connection shown above and the constants do not guarantee proper operation. Perform thorough evaluation using an actual application to set the constant.**

**Remark** Refer to the application note for constants of each external component.

### 3. 8-series cell (cascade connection with overcurrent protection function)

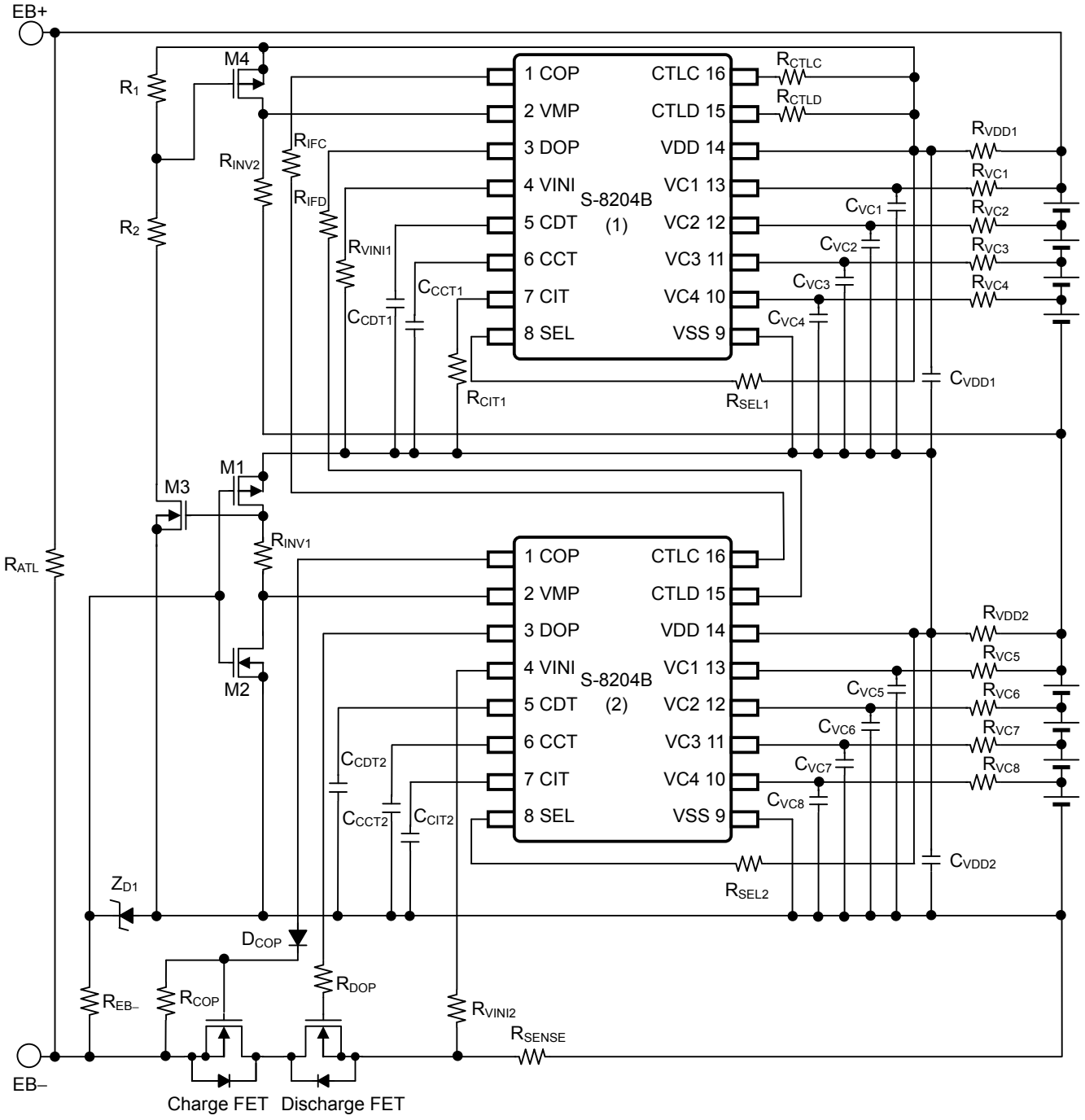



**Figure 13**

**Caution 1. It is recommended that filter constants between the VDD pin and the VSS pin should be set to approximately 47 µF • Ω.**

**e.g., $C_{VDD} \times R_{VDD}$ = 1.0 µF × 47 Ω = 47 µF • Ω**

**Sufficient evaluation of transient power supply fluctuation and overcurrent protection function with the actual application is needed to determine the proper constants. Contact our sales office in case the constants should be set to other than 47 µF • Ω.**

**2. It has not been confirmed whether the operation is normal in circuits other than the above example of connection. In addition, the example of connection shown above and the constants do not guarantee proper operation. Perform thorough evaluation using an actual application to set the constant.**

**Remark** Refer to the application note for constants of each external component.

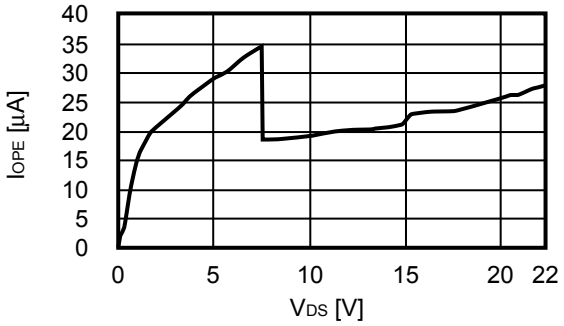
## ■ Precautions

- The application conditions for the input voltage, output voltage, and load current should not exceed the package power dissipation.
- Batteries can be connected in any order; however, there may be cases when discharging cannot be performed when a battery is connected. In such a case, short the VMP pin and the VDD pin to return the IC to the normal mode.
- If both an overcharge battery and an overdischarge battery are included among the whole batteries, the condition is set in overcharge status and overdischarge status. Therefore either charging or discharging is impossible.
- Do not apply an electrostatic discharge to this IC that exceeds the performance ratings of the built-in electrostatic protection circuit.
- SII Semiconductor Corporation claims no responsibility for any disputes arising out of or in connection with any infringement by products including this IC of patents owned by a third party.

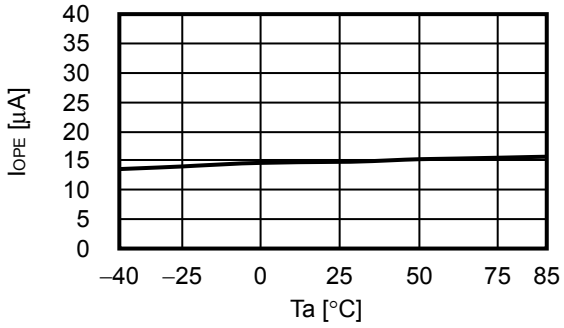
## ■ Characteristics (Typical Data)

### 1. Current consumption

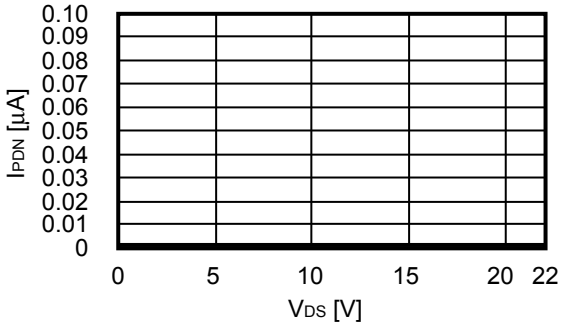
#### 1. 1 $I_{OPE}$ vs. $V_{DS}$



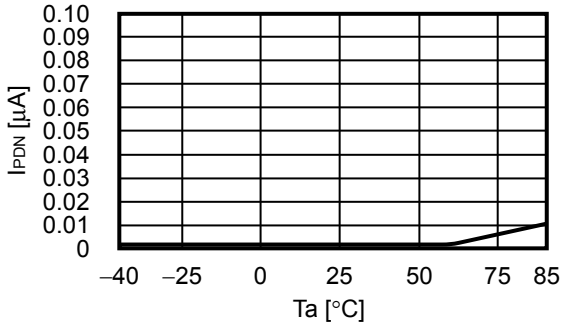

#### 1. 2 $I_{OPE}$ vs. Ta




#### 1. 3 $I_{PDN}$ vs. $V_{DS}$

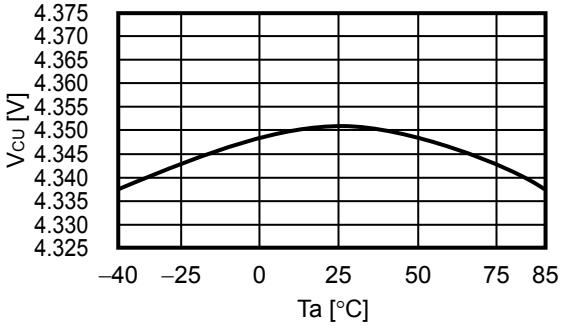



#### 1. 4 $I_{PDN}$ vs. Ta

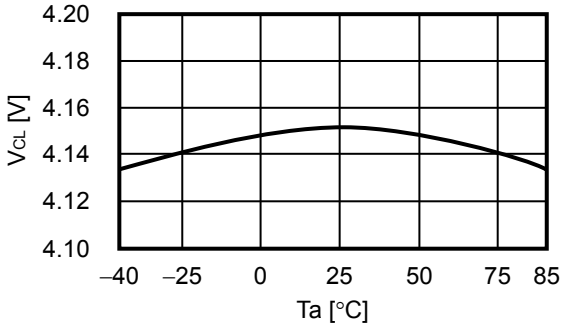



### 2. Overcharge detection / release voltage, overdischarge detection / release voltage, overcurrent detection voltage

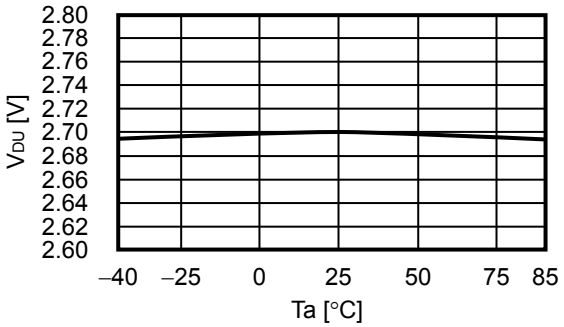
#### 2. 1 $V_{CU}$ vs. Ta



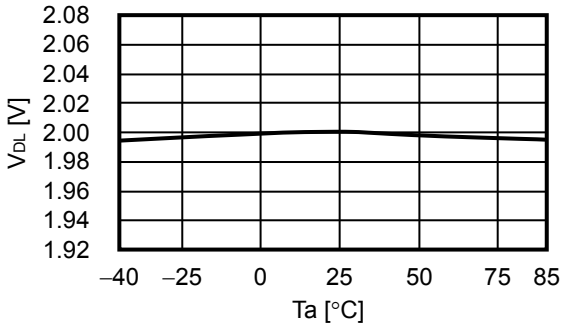

#### 2. 2 $V_{CL}$ vs. Ta



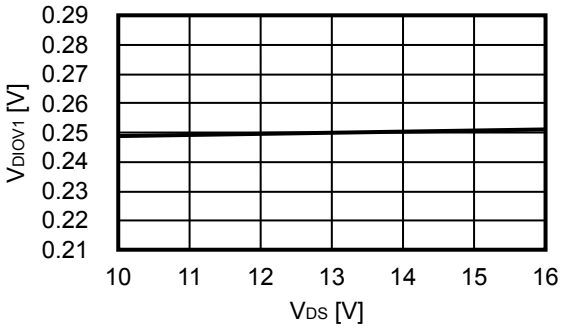

#### 2. 3 $V_{DU}$ vs. Ta



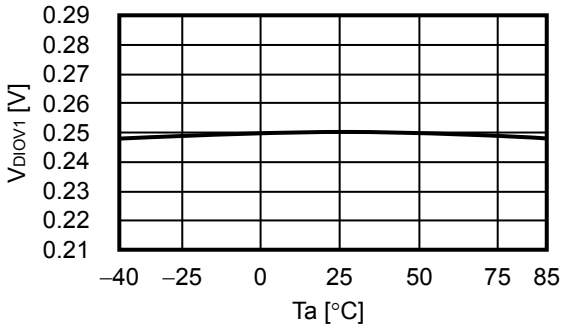

#### 2. 4 $V_{DL}$ vs. Ta



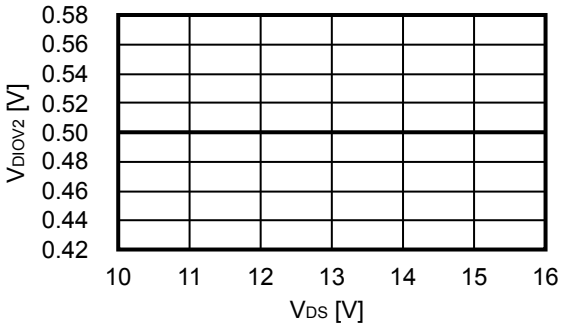
**2. 5 $V_{DIOV1}$ vs. $V_{DS}$**



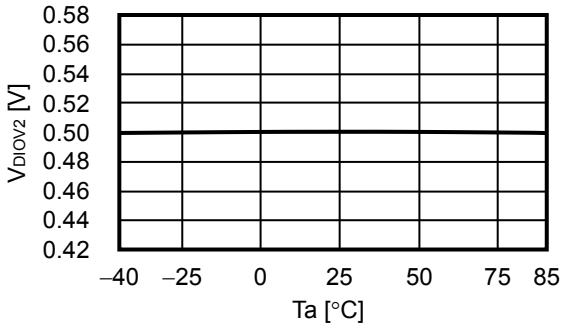

**2. 6 $V_{DIOV1}$ vs. Ta**



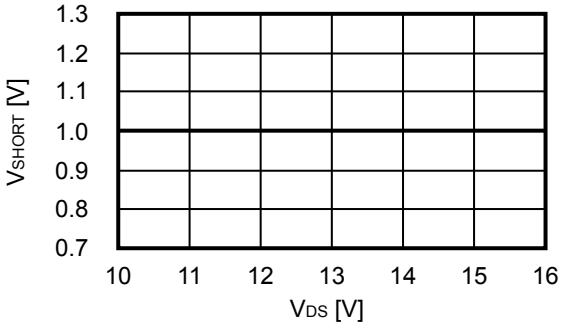

**2. 7 $V_{DIOV2}$ vs. $V_{DS}$**



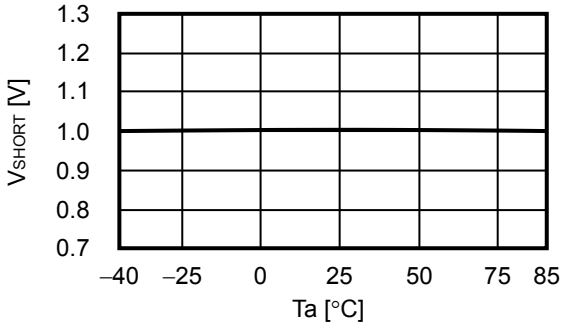

**2. 8 $V_{DIOV2}$ vs. Ta**




**2. 9 $V_{SHORT}$ vs. $V_{DS}$**

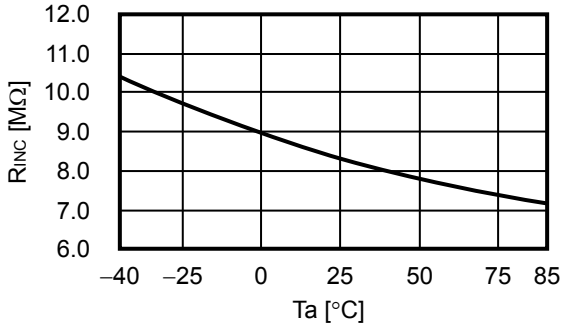



**2. 10 $V_{SHORT}$ vs. Ta**

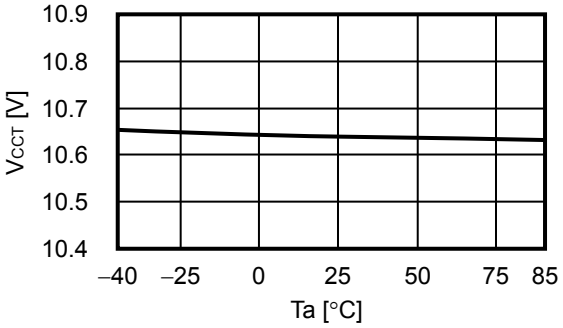


## 3. CCT pin internal resistance / detection voltage, CDT pin internal resistance / detection voltage, CIT pin internal resistance / detection voltage and load short-circuit detection delay time

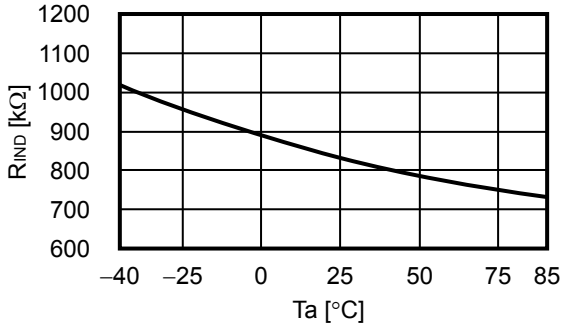
### 3. 1 $R_{INC}$ vs. Ta



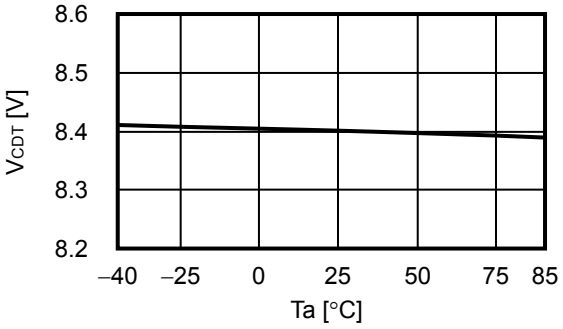

### 3. 2 $V_{CCT}$ vs. Ta ($V_{DS}$ = 15.2 V)



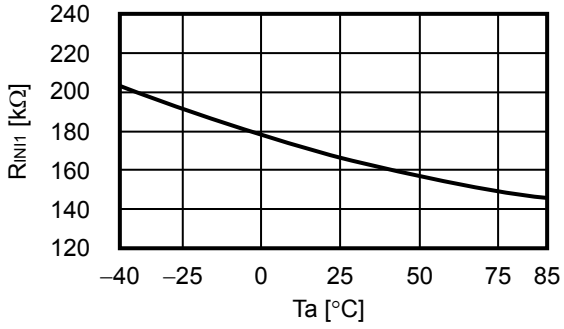

### 3. 3 $R_{IND}$ vs. Ta



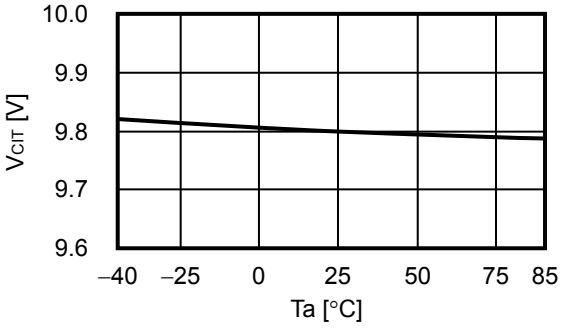

### 3. 4 $V_{CDT}$ vs. Ta ($V_{DS}$ = 12.0 V)



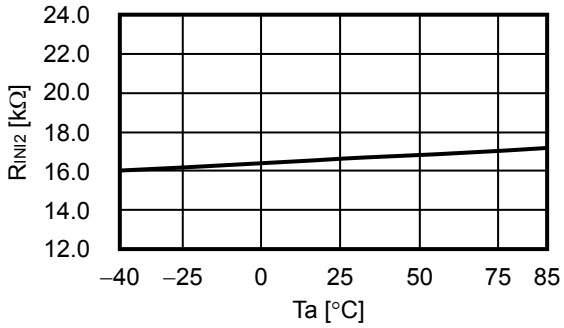

### 3. 5 $R_{INI1}$ vs. Ta



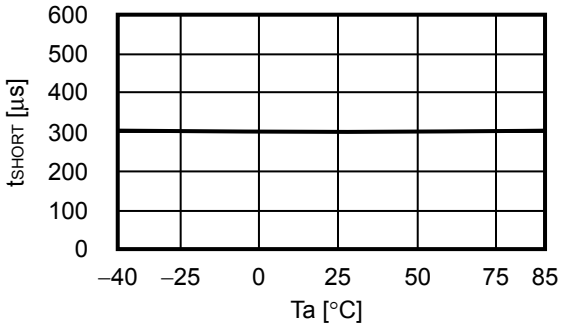

### 3. 6 $V_{CIT}$ vs. Ta ($V_{DS}$ = 14.0 V)




### 3. 7 $R_{INI2}$ vs. Ta

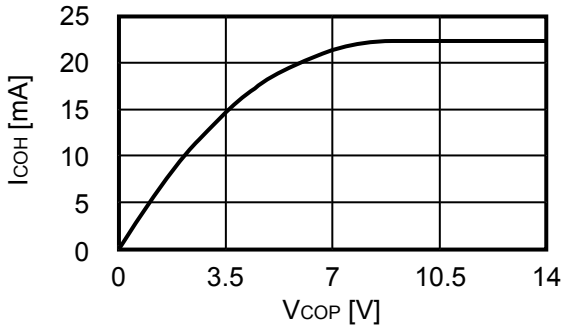



### 3. 8 $t_{SHORT}$ vs. Ta

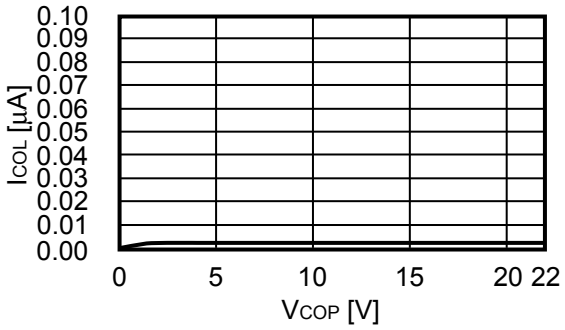


## 4. COP pin / DOP pin

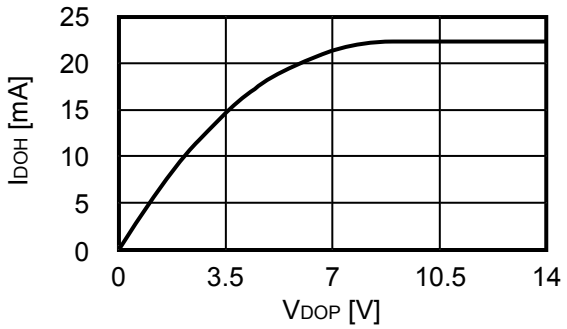
### 4. 1 $I_{COH}$ vs. $V_{COP}$



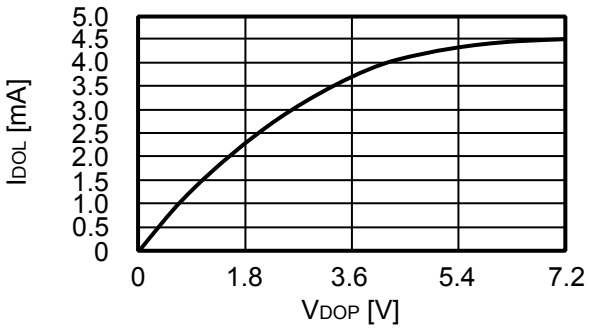

### 4. 2 $I_{COL}$ vs. $V_{COP}$

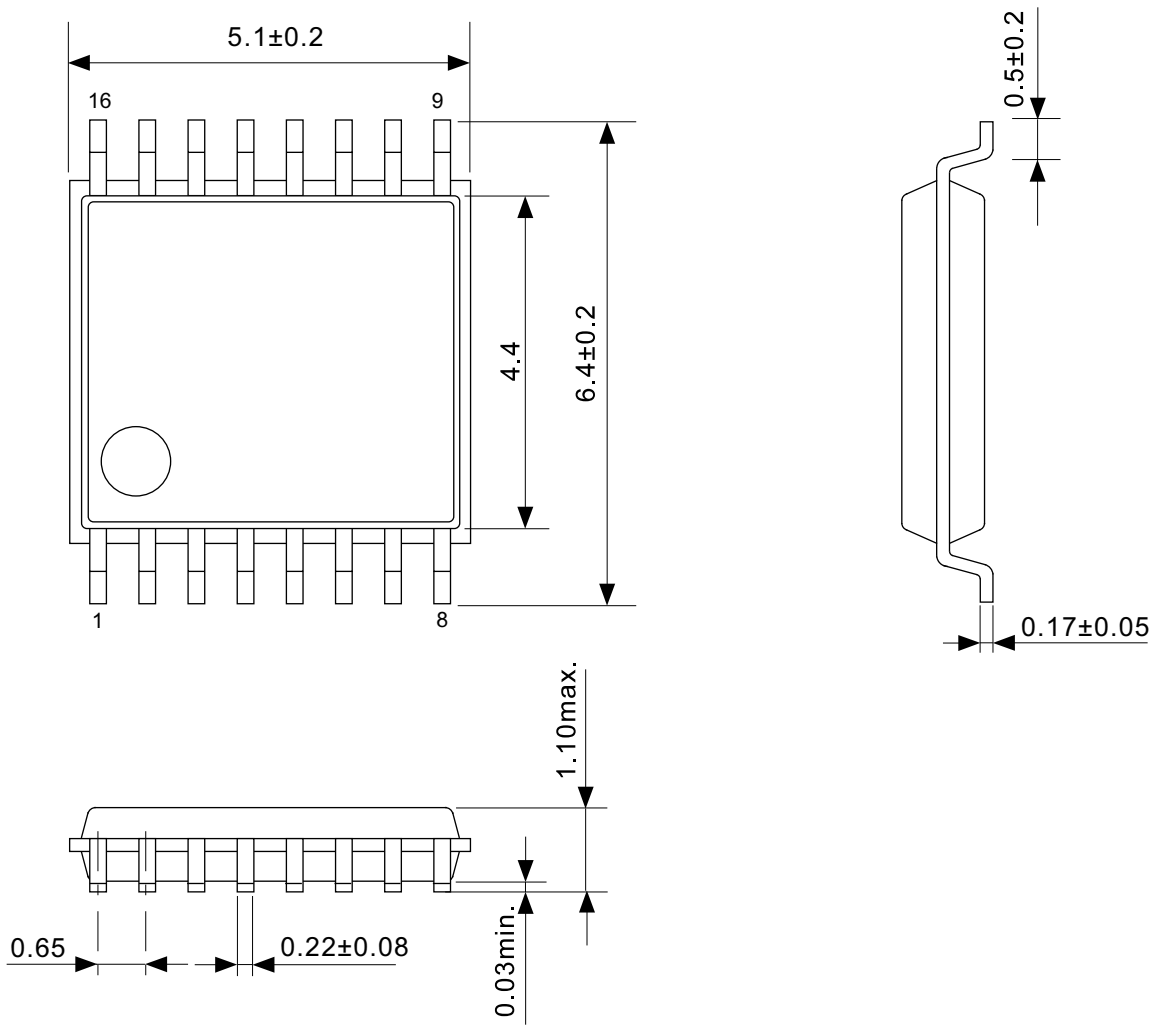



### 4. 3 $I_{DOH}$ vs. $V_{DOP}$



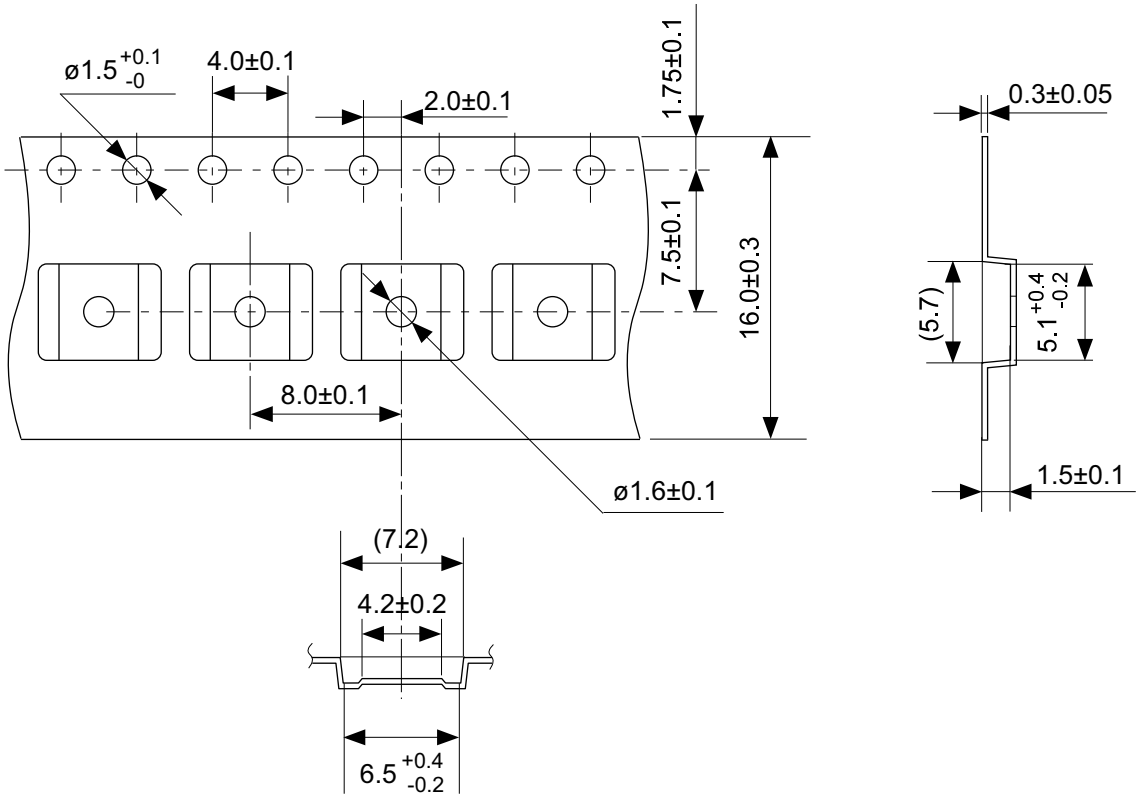

### 4. 4 $I_{DOL}$ vs. $V_{DOP}$

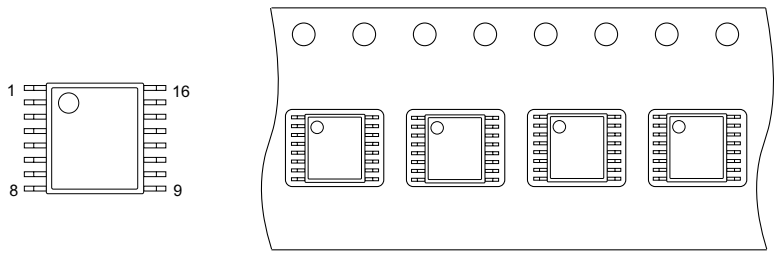





No. FT016-A-P-SD-1.2

| | |
|---|---|
| TITLE | TSSOP16-A-PKG Dimensions |
| No. | FT016-A-P-SD-1.2 |
| ANGLE | |
| UNIT | mm |
| | |
| SII Semiconductor Corporation | |




No. FT016-A-C-SD-1.1

| | |
|---|---|
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| ANGLE | |
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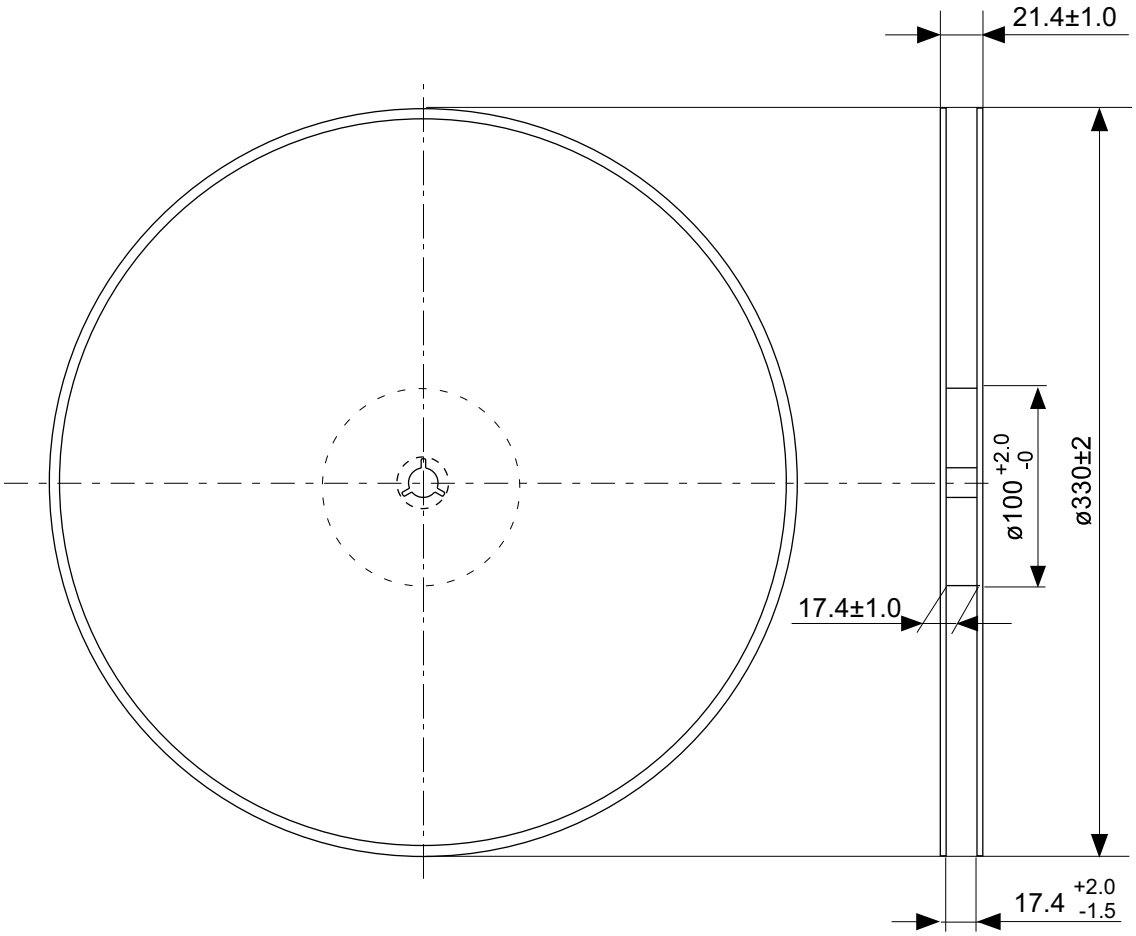
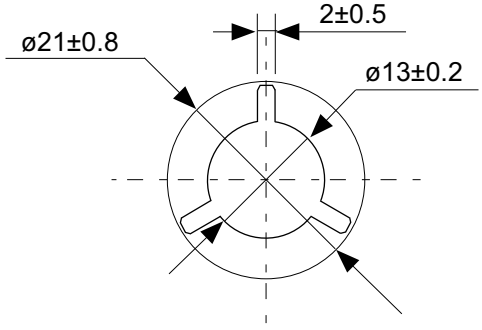
| SII Semiconductor Corporation | |




Enlarged drawing in the central part




No. FT016-A-R-SD-2.0

| | | | |
|---|---|---|---|
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| No. | FT016-A-R-SD-2.0 | | |
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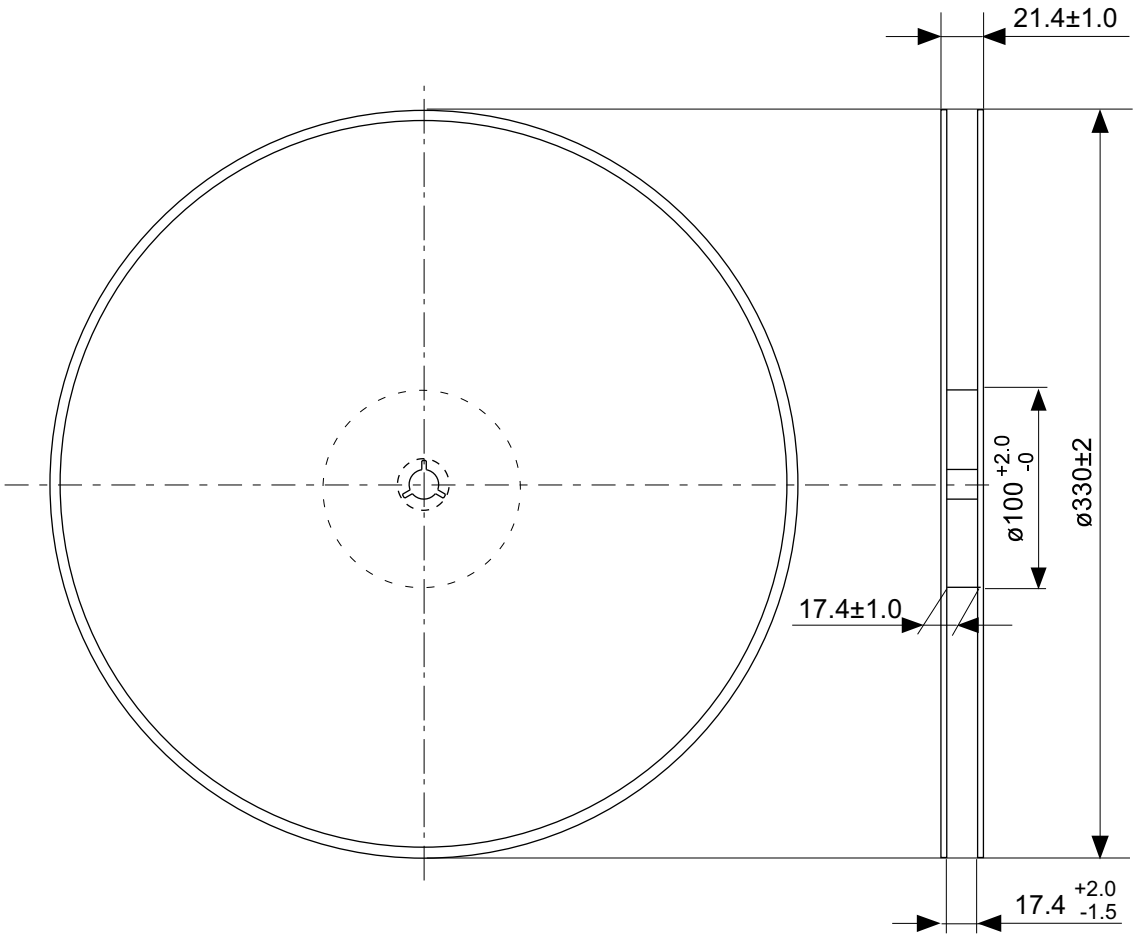
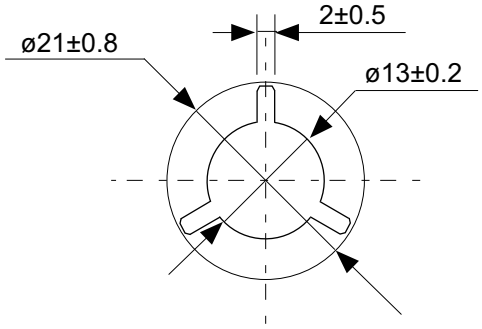
| UNIT | mm | | |
| | | | |
| SII Semiconductor Corporation | | | |




Enlarged drawing in the central part




No. FT016-A-R-S1-1.0

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| No. | FT016-A-R-S1-1.0 | | |
| ANGLE | | QTY. | 4,000 |
| UNIT | mm | | |
| | | | |
| SII Semiconductor Corporation | | | |

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