LTC5543

2.3GHz to 4GHz High Dynamic Range Downconverting Mixer

FEATURES

- **Conversion Gain: 8.4dB at 2500MHz**
- **IIP3: 24.5dBm at 2500MHz**
- **Noise Figure: 10.2dB at 2500MHz**
- **17.5dB NF Under +5dBm Blocking**
- **High Input P1dB**
- **3.3V Supply, 660mW Power Consumption**
- **Shutdown Pin**
- **50Ω Single-Ended RF and LO Inputs**
- **LO Inputs 50Ω Matched when Shutdown**
- **High Isolation LO Switch**
- 0dBm LO Drive Level
- High LO-RF and LO-IF Isolation
- Small Solution Size
- 20-Lead (5mm × 5mm) QFN package

APPLICATIONS

- Wireless Infrastructure Receivers (LTE, WiMAX, WCS)
- Point-To-Point Microwave Links
- High Dynamic Range Downmixer Applications

DESCRIPTION

The LTC®5543 is part of a family of high dynamic range, high gain passive downconverting mixers covering the 600MHz to 4GHz frequency range. **The LTC5543 is optimized for 2.3GHz to 4GHz RF applications. The LO frequency must fall within the 2.4GHz to 3.6GHz range for optimum performance.** A typical application is a LTE or WiMAX receiver with a 2.3GHz to 2.7GHz RF input and high-side LO.

The LTC5543 is designed for 3.3V operation, however; the IF amplifier can be powered by 5V for the highest P1dB. An integrated SPDT LO switch with fast switching accepts two active LO signals, while providing high isolation.

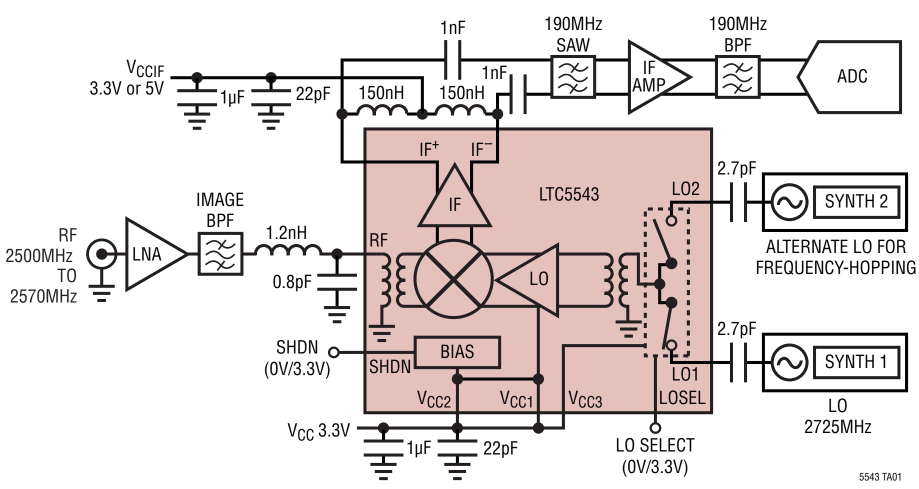
The LTC5543's high conversion gain and high dynamic range enable the use of lossy IF filters in high-selectivity receiver designs, while minimizing the total solution cost, board space and system-level variation.

High Dynamic Range Downconverting Mixer Family

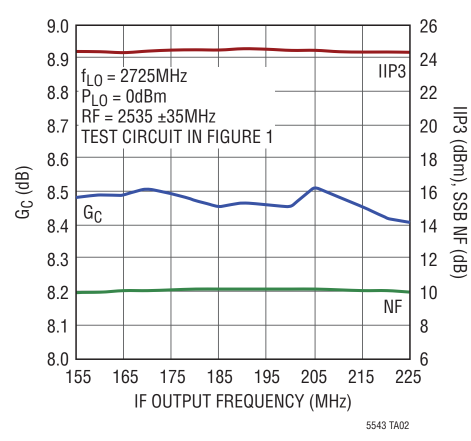
PART#	RF RANGE	LO RANGE
LTC5540	600MHz –1.3GHz	700MHz – 1.2GHz
LTC5541	1.3GHz – 2.3GHz	1.4GHz – 2.0GHz
LTC5542	1.6GHz – 2.7GHz	1.7GHz – 2.5GHz
LTC5543	**2.3GHz – 4GHz**	**2.4GHz – 3.6GHz**

TYPICAL APPLICATION

Wideband Receiver



Wideband Conversion Gain, IIP3 and NF vs IF Output Frequency



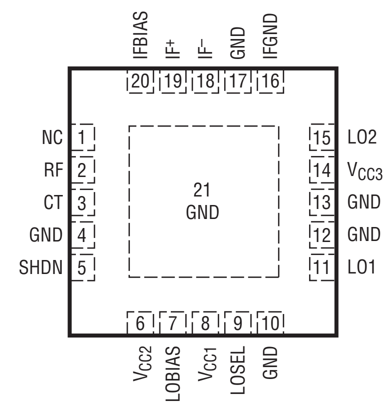
ABSOLUTE MAXIMUM RATINGS

(Note 1)

Mixer Supply Voltage (V_{CC1}, V_{CC2})..........................3.8V
LO Switch Supply Voltage (V_{CC3})............................3.8V
IF Supply Voltage (IF^+, IF^-) 5.5V
Shutdown Voltage (SHDN)................–0.3V to V_{CC} +0.3V
LO Select Voltage (LOSEL)................–0.3V to V_{CC} +0.3V
LO1, LO2 Input Power (2GHz to 4GHz) 9dBm
LO1, LO2 Input DC Voltage ....±0.5V
RF Input Power (2GHz to 4GHz)..........................15dBm
RF Input DC Voltage.. ±0.1V
Operating Temperature Range ....–40°C to 85°C
Storage Temperature Range ....–65°C to 150°C
Junction Temperature (T_J) .... 150°C

PIN CONFIGURATION

TOP VIEW



UH PACKAGE
20-LEAD (5mm × 5mm) PLASTIC QFN
T_{JMAX} = 150°C, θ_{JA} = 34°C/W, θ_{JC} = 3°C/W
EXPOSED PAD (PIN 21) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC5543IUH#PBF	LTC5543IUH#TRPBF	5543	20-Lead (5mm x 5mm) Plastic QFN	–40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

AC ELECTRICAL CHARACTERISTICS

V_{CC} = 3.3V, V_{CCIF} = 3.3V, SHDN = Low, T_A = 25°C, P_{LO} = 0dBm, unless otherwise noted. Test circuit shown in Figure 1. (Notes 2, 3, 4)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
LO Input Frequency Range			2400 to 3600		MHz
RF Input Frequency Range	Low-Side LO High-Side LO		2400 to 4000 2200 to 3200		MHz MHz
IF Output Frequency Range	Requires External Matching		5 to 600		MHz
RF Input Return Loss	Z_0 = 50Ω, 2200MHz to 3800MHz		>12		dB
LO Input Return Loss	Z_0 = 50Ω, 2400MHz to 3600MHz		>12		dB
IF Output Return Loss	Requires External Matching		>12		dB
LO Input Power	f_{LO} = 2400MHz to 3600MHz	–4	0	6	dBm
LO to RF Leakage	f_{LO} = 2400MHz to 3600MHz		<–28		dBm
LO to IF Leakage	f_{LO} = 2400MHz to 3600MHz		<–35		dBm
LO Switch Isolation	LO1 Selected, 2400MHz < f_{LO} < 3600MHz LO2 Selected, 2400MHz < f_{LO} < 3600MHz		>44 >47		dB dB
RF to LO Isolation	f_{RF} = 2200MHz to 4000MHz		>37		dB
RF to IF Isolation	f_{RF} = 2200MHz to 4000MHz		>33		dB

AC ELECTRICAL CHARACTERISTICS

V_{CC} = 3.3V, V_{CCIF} = 3.3V, SHDN = Low, T_A = 25°C, P_{LO} = 0dBm, P_{RF} = –3dBm (Δf = 2MHz for two-tone IIP3 tests),unless otherwise noted. Test circuit shown in Figure 1. (Notes 2, 3, 4)

High-Side LO Downmixer Application: RF = 2300MHz to 2700MHz, IF = 190MHz, $f_{LO} = f_{RF}+f_{IF}$

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Conversion Gain	RF = 2300MHz RF = 2500MHz RF = 2700MHz	7.0	8.9 8.4 8.2		dB
Conversion Gain Flatness	RF = 2500 ±30MHz, LO = 2690MHz, IF=190 ±30MHz		±0.1		dB
Conversion Gain vs Temperature	T_A = –40°C to +85°C, RF = 2500MHz		–0.007		dB/°C
Input 3rd Order Intercept	RF = 2300MHz RF = 2500MHz RF = 2700MHz	22.5	23.8 24.5 24.4		dBm
SSB Noise Figure	RF = 2300MHz RF = 2500MHz RF = 2700MHz		9.9 10.2 10.4	11.9	dB
SSB Noise Figure Under Blocking	f_{RF} = 2500MHz, f_{LO} = 2690MHz, f_{BLOCK} = 2300MHz, P_{BLOCK} = 5dBm		17.5		dB
2LO – 2RF Output Spurious Product ($f_{RF} = f_{LO} – f_{IF}/2$)	f_{RF} = 2595MHz at –10dBm, f_{LO} = 2690MHz, f_{IF} = 190MHz		–61		dBc
3LO – 3RF Output Spurious Product ($f_{RF} = f_{LO} – f_{IF}/3$)	f_{RF} = 2626.67MHz at –10dBm, f_{LO} = 2690MHz, f_{IF} = 190MHz		–74		dBc
Input 1dB Compression	RF = 2500MHz, V_{CCIF} = 3.3V RF = 2500MHz, V_{CCIF} = 5V		10.9 13.9		dBm

Low-Side LO Downmixer Application: RF = 2400MHz to 3800MHz, IF = 190MHz, $f_{LO} = f_{RF}–f_{IF}$

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Conversion Gain	RF = 2600MHz RF = 3300MHz RF = 3500MHz	5.3	8.9 7.1 6.7		dB
Conversion Gain Flatness	RF = 3500MHz ±30MHz, LO = 3310MHz, IF = 190 ±30MHz		±0.15		dB
Conversion Gain vs Temperature	T_A = –40°C to 85°C, RF = 3500MHz		–0.004		dB/°C
Input 3rd Order Intercept	RF = 2600MHz RF = 3300MHz RF = 3500MHz	22.5	24.7 25.6 25.1		dBm
SSB Noise Figure	RF = 2600MHz RF = 3300MHz RF = 3500MHz		9.6 11.6 11.8		dB
2RF – 2LO Output Spurious Product ($f_{RF} = f_{LO} + f_{IF/2}$)	f_{RF} = 3405MHz at –10dBm, f_{LO} = 3310MHz f_{IF} = 190MHz		–50		dBc
3RF – 3LO Output Spurious Product ($f_{RF} = f_{LO} + f_{IF/3}$)	f_{RF} = 3373.33MHz at –10dBm, f_{LO} = 3310MHz f_{IF} = 190MHz		–77		dBc
Input 1dB Compression	RF = 3500MHz, V_{CCIF} = 3.3V RF = 3500MHz, V_{CCIF} = 5V		11.3 11.8		dBm

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 3.3V, V_{CCIF} = 3.3V, SHDN = Low, T_A = 25°C, unless otherwise noted. Test circuit shown in Figure 1. (Note 2)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Power Supply Requirements (V_{CC}, V_{CCIF})					
V_{CC} Supply Voltage (Pins 6, 8 and 14)		3.1	3.3	3.5	V
V_{CCIF} Supply Voltage (Pins 18 and 19)		3.1	3.3	5.3	V
V_{CC} Supply Current (Pins 6 + 8 + 14) V_{CCIF} Supply Current (Pins 18 + 19) Total Supply Current (V_{CC} + V_{CCIF})			99 102 201	116 122 238	mA
Total Supply Current – Shutdown	SHDN = High			500	µA
Shutdown Logic Input (SHDN) Low = On, High = Off					
SHDN Input High Voltage (Off)		3			V
SHDN Input Low Voltage (On)				0.3	V
SHDN Input Current	–0.3V to V_{CC} + 0.3V	–20		30	µA
Turn On Time			1		µs
Turn Off Time			1.5		µs
LO Select Logic Input (LOSEL) Low = LO1 Selected, High = LO2 Selected					
LOSEL Input High Voltage		3			V
LOSEL Input Low Voltage				0.3	V
LOSEL Input Current	–0.3V to V_{CC} + 0.3V	–20		30	µA
LO Switching Time			50		ns

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTC5543 is guaranteed functional over the operating temperature range from –40°C to 85°C.

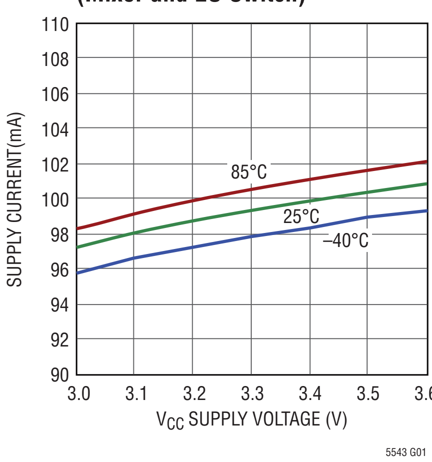
Note 3: SSB Noise Figure measurements performed with a small-signal noise source, bandpass filter and 6dB matching pad on RF input, bandpass filter and 6dB matching pad on the LO input, and no other RF signals applied.

Note 4: LO switch isolation is measured at the IF output port at the IF frequency with f_{LO1} and f_{LO2} offset by 2MHz.

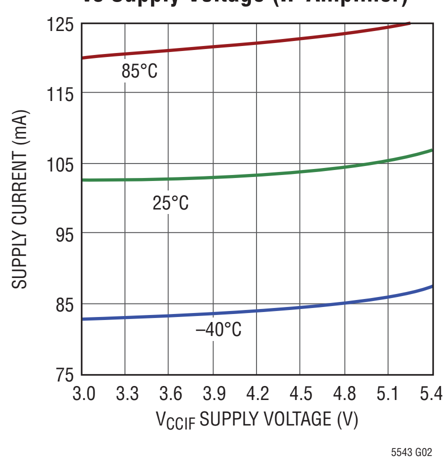
TYPICAL DC PERFORMANCE CHARACTERISTICS

SHDN = Low, Test circuit shown in Figure 1.

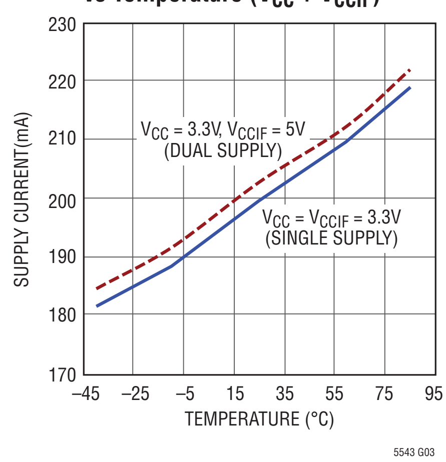
V_{CC} Supply Current vs Supply Voltage (Mixer and LO Switch)



V_{CCIF} Supply Current vs Supply Voltage (IF Amplifier)



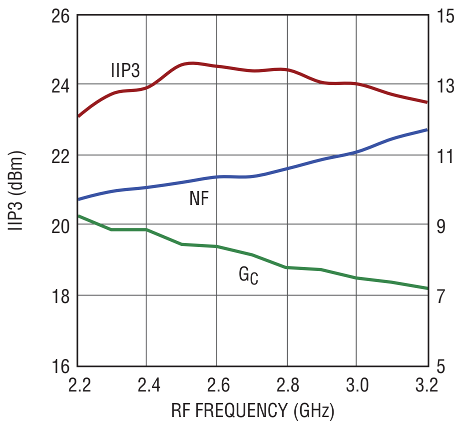
Total Supply Current vs Temperature (V_{CC} + V_{CCIF})



TYPICAL AC PERFORMANCE CHARACTERISTICS High-Side LO

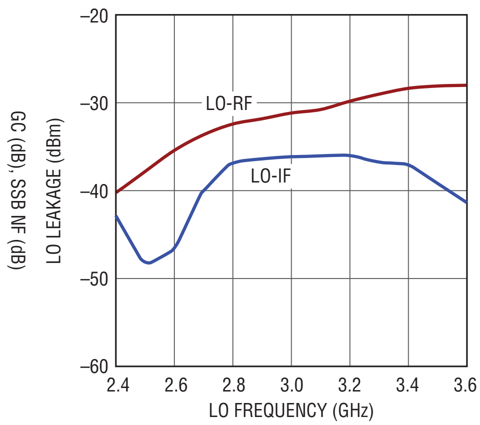
V_{CC} = 3.3V, V_{CCIF} = 3.3V, SHDN = Low, T_A = 25°C, P_{LO} = 0dBm, P_{RF} = –3dBm (–3dBm/tone for two-tone IIP3 tests, ∆f = 2MHz), IF = 190MHz, unless otherwise noted. Test circuit shown in Figure 1.

Conversion Gain, IIP3 and NF vs RF Frequency



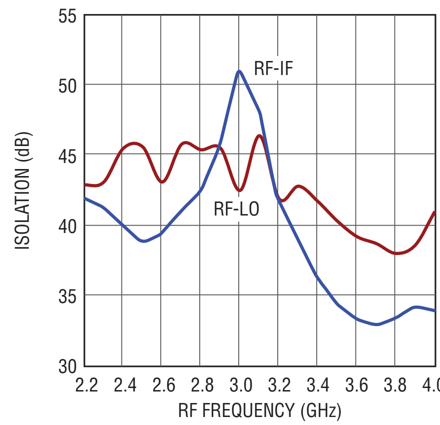
5543 G04

LO Leakage vs LO Frequency



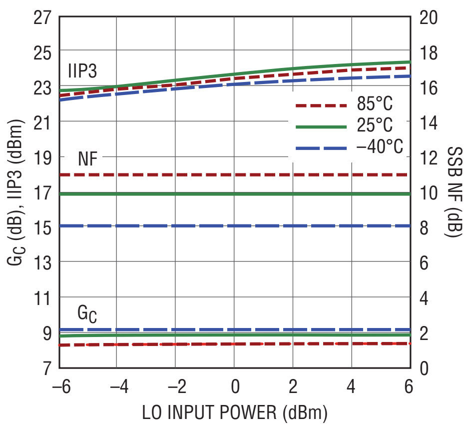
5543 G05

RF Isolation vs RF Frequency



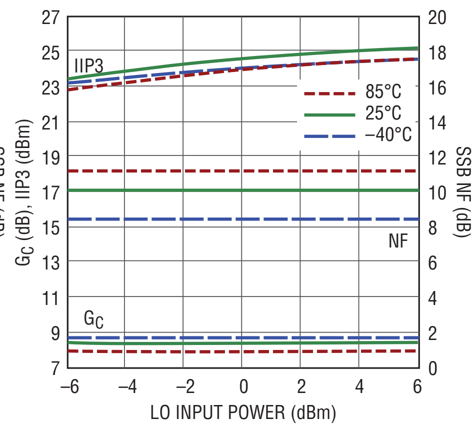
5543 G06

2300MHz Conversion Gain, IIP3 and NF vs LO Power



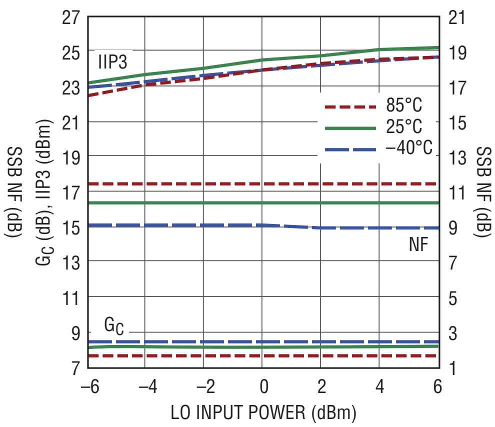
5543 G07

2500MHz Conversion Gain, IIP3 and NF vs LO Power



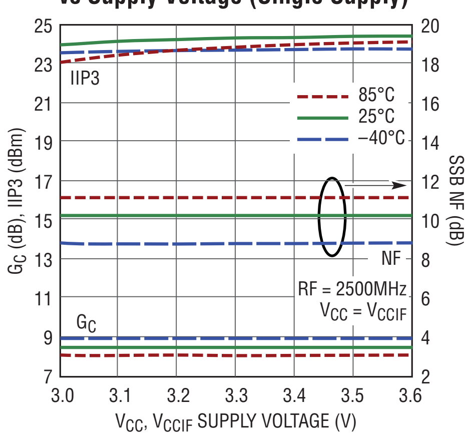
5543 G08

2700MHz Conversion Gain, IIP3 and NF vs LO Power



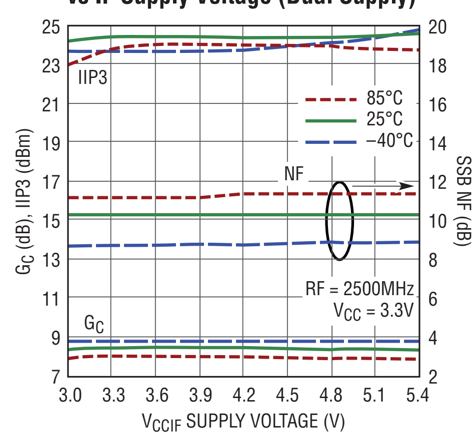
5543 G09

Conversion Gain, IIP3 and NF vs Supply Voltage (Single Supply)



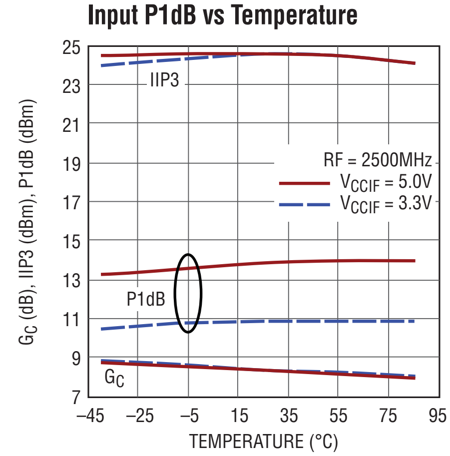
5543 G10

Conversion Gain, IIP3 and NF vs IF Supply Voltage (Dual Supply)



5543 G11

Conversion Gain, IIP3 and RF Input P1dB vs Temperature



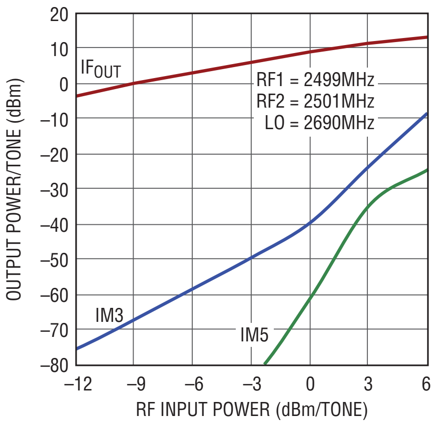
5543 G12

5543f

TYPICAL AC PERFORMANCE CHARACTERISTICS High-Side LO (continued)

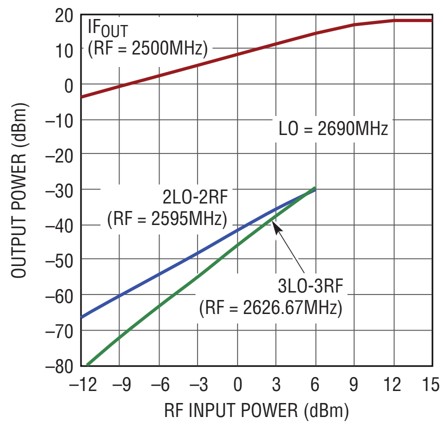
V_{CC} = 3.3V, V_{CCIF} = 3.3V, SHDN = Low, T_A = 25°C, P_{LO} = 0dBm, P_{RF} = –3dBm (–3dBm/tone for two-tone IIP3 tests, Δf = 2MHz), IF = 190MHz, unless otherwise noted. Test circuit shown in Figure 1.

2-Tone IF Output Power, IM3 and IM5 vs RF Input Power



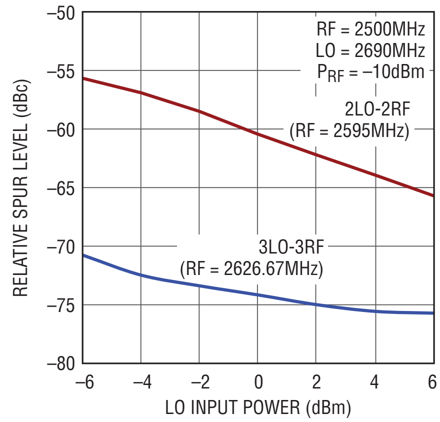
5543 G13

Single-Tone IF Output Power, 2 × 2 and 3 × 3 Spurs vs RF Input Power



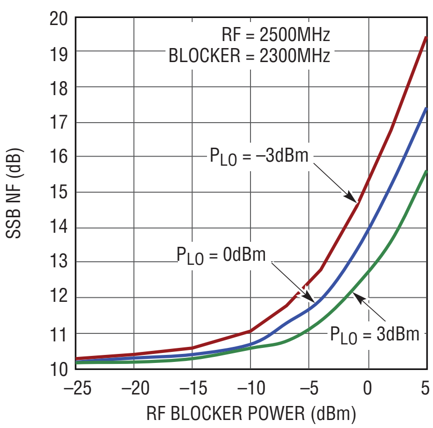
5543 G14

2 × 2 and 3 × 3 Spurs vs LO Power



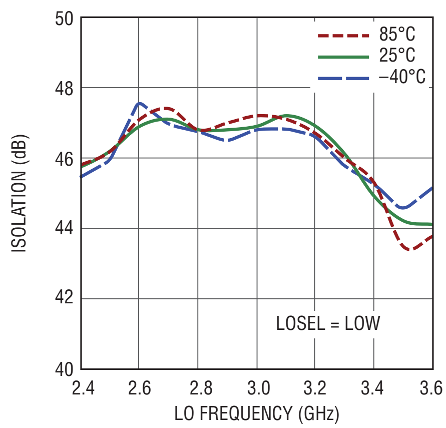
5543 G15

SSB Noise Figure vs RF Blocker Level



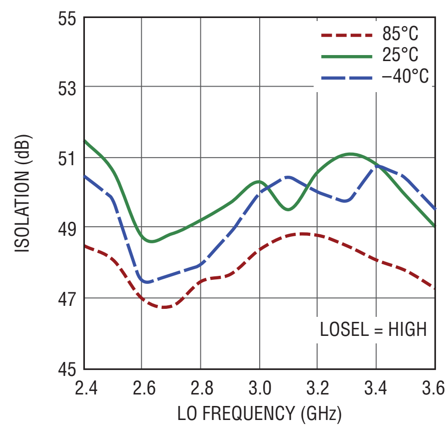
5543 G16

LO Switch Isolation vs LO Frequency–LO1 Selected



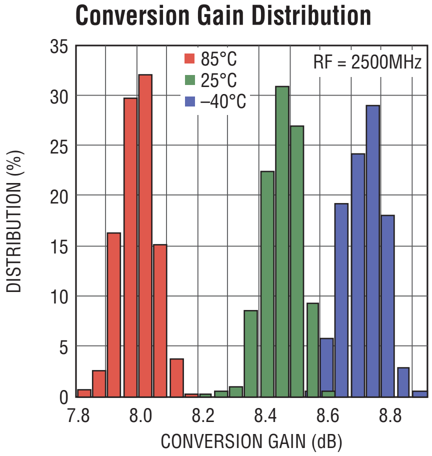
5543 G17

LO Switch Isolation vs LO Frequency–LO2 Selected



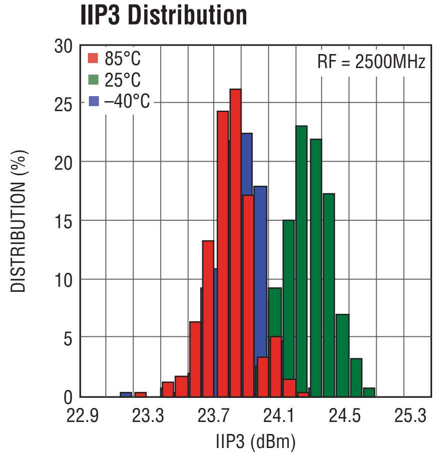
5543 G18

Conversion Gain Distribution



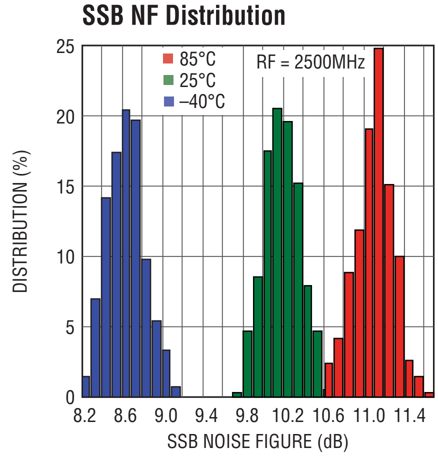
5543 G18a

IIP3 Distribution



5543 G18b

SSB NF Distribution

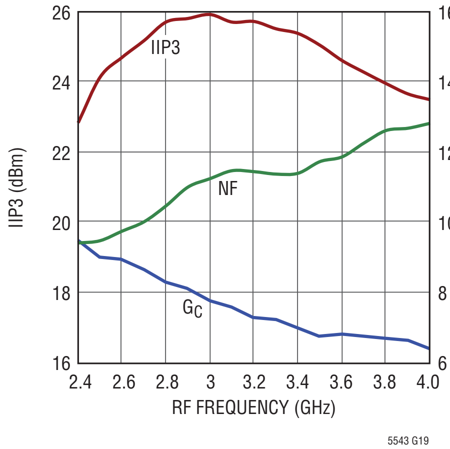


5543 G18c

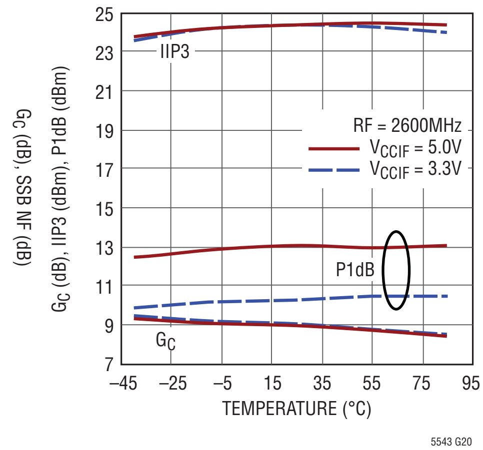
TYPICAL AC PERFORMANCE CHARACTERISTICS Low-Side LO

V_{CC} = 3.3V, V_{CCIF} = 3.3V, SHDN = Low, T_A = 25°C, P_{LO} = 0dBm, P_{RF} = –3dBm (–3dBm/tone for two-tone IIP3 tests, ∆f = 2MHz), IF = 190MHz, unless otherwise noted. Test circuit shown in Figure 1.

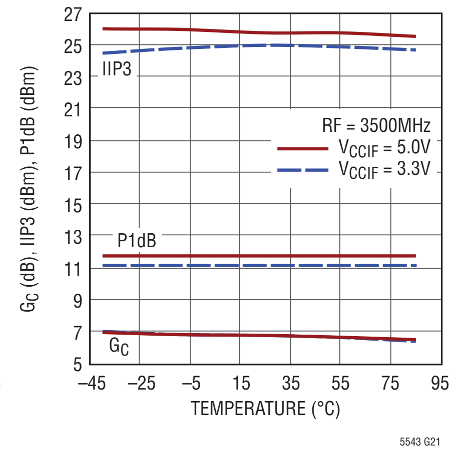
Conversion Gain, IIP3 and NF vs RF Frequency



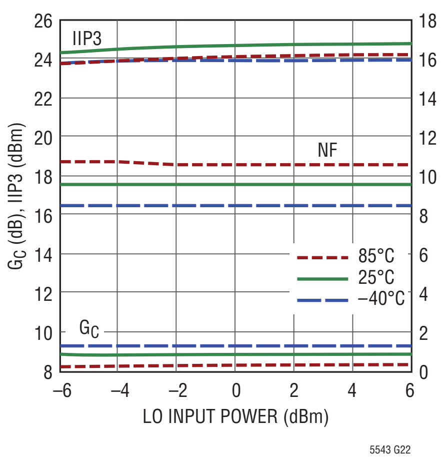
2600MHz Conversion Gain, IIP3 and RF Input P1dB vs Temperature



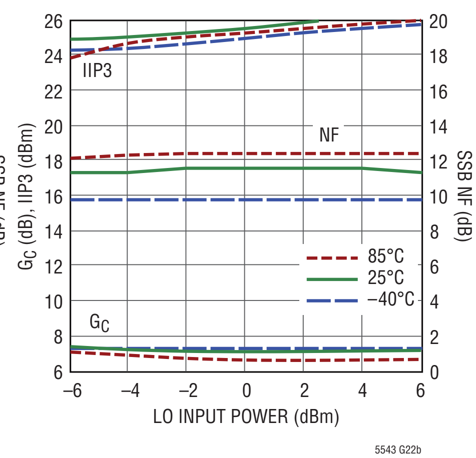
3500MHz Conversion Gain, IIP3 and RF Input P1dB vs Temperature



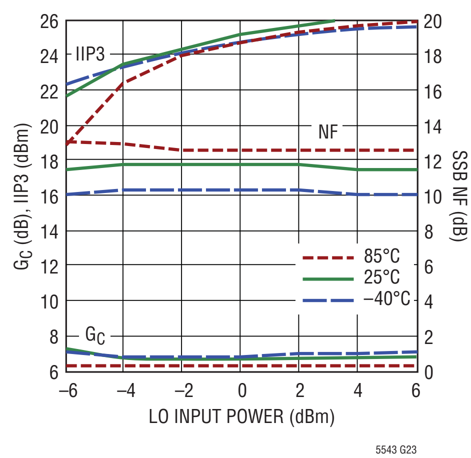
2600MHz Conversion Gain, IIP3 and NF vs LO Power



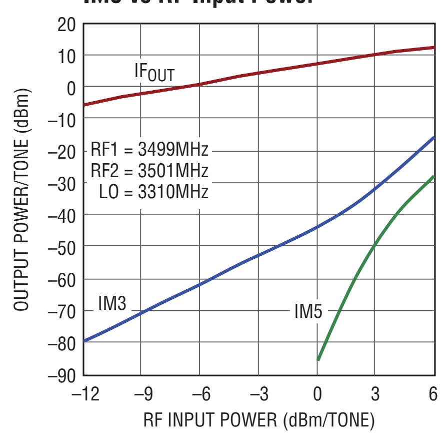
3300MHz Conversion Gain, IIP3 and NF vs LO Power



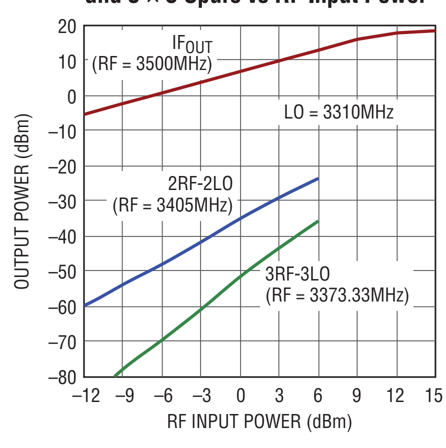
3500MHz Conversion Gain, IIP3 and NF vs LO Power



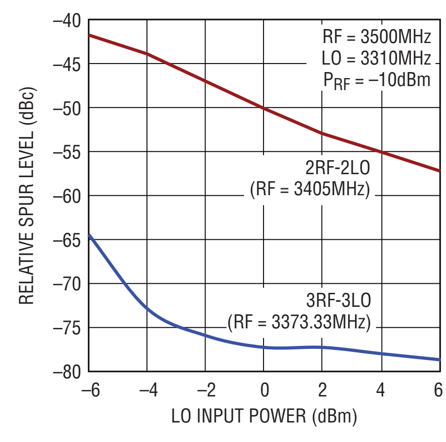
2-Tone IF Output Power, IM3 and IM5 vs RF Input Power



Single-Tone IF Output Power, 2 × 2 and 3 × 3 Spurs vs RF Input Power



2 × 2 and 3 × 3 Spur Suppression vs LO Power



PIN FUNCTIONS

NC (Pin 1): This pin is not connected internally. It can be left floating, connected to ground or to V_{CC}.

RF (Pin 2): Single-Ended Input for the RF Signal. This pin is internally connected to the primary side of the RF input transformer, which has low DC resistance to ground. **A series DC-blocking capacitor should be used to avoid damage to the integrated transformer.** The RF input is impedance matched, as long as the selected LO input is driven with a 0dBm ±6dB source between 2.4GHz and 3.6GHz.

CT (Pin 3): RF Transformer Secondary Center-Tap. This pin may require a bypass capacitor to ground. See the Applications Information section. This pin has an internally generated bias voltage of 1.2V. It must be DC-isolated from ground and V_{CC}.

GND (Pins 4, 10, 12, 13, 17, Exposed Pad Pin 21): Ground. These pins must be soldered to the RF ground plane on the circuit board. The exposed pad metal of the package provides both electrical contact to ground and good thermal contact to the printed circuit board.

SHDN (Pin 5): Shutdown Pin. When the input voltage is less than 0.3V, the internal circuits supplied through pins 6, 8, 14, 18 and 19 are enabled. When the input voltage is greater than 3V, all circuits are disabled. Typical input current is less than 10μA. This pin must not be allowed to float.

V_{CC2} (Pin 6) and V_{CC1} (Pin 8): Power Supply Pins for the LO Buffer and Bias Circuits. These pins are internally connected and must be externally connected to a regulated 3.3V supply, with bypass capacitors located close to the pin. Typical current consumption is 99mA.

LOBIAS (Pin 7): This Pin Allows Adjustment of the LO Buffer Current. Typical DC voltage is 2.2V.

LOSEL (Pin 9): LO1/LO2 Select Pin. When the input voltage is less than 0.3V, the LO1 port is selected. When the input voltage is greater than 3V, the LO2 port is selected. Typical input current is 11μA for LOSEL = 3.3V. This pin must not be allowed to float.

LO1 (Pin 11) and LO2 (Pin 15): Single-Ended Inputs for the Local Oscillators. These pins are internally biased at 0V and require external DC blocking capacitors. Both inputs are internally matched to 50Ω, even when the chip is disabled (SHDN = high).

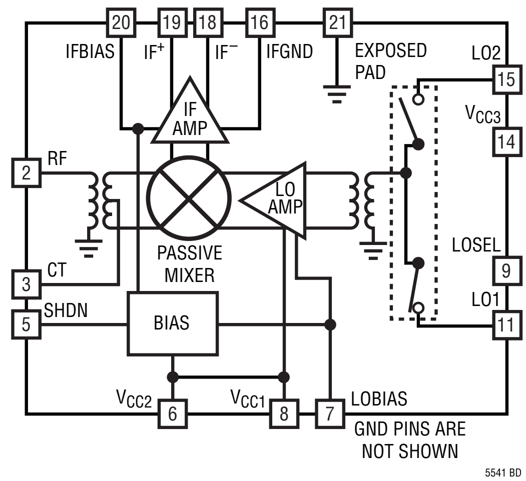
V_{CC3} (Pin 14): Power Supply Pin for the LO Switch. This pin must be connected to a regulated 3.3V supply and bypassed to ground with a capacitor near the pin. Typical DC current consumption is less than 100μA.

IFGND (Pin 16): DC Ground Return for the IF Amplifier. This pin must be connected to ground to complete the IF amplifier's DC current path. Typical DC current is 102mA.

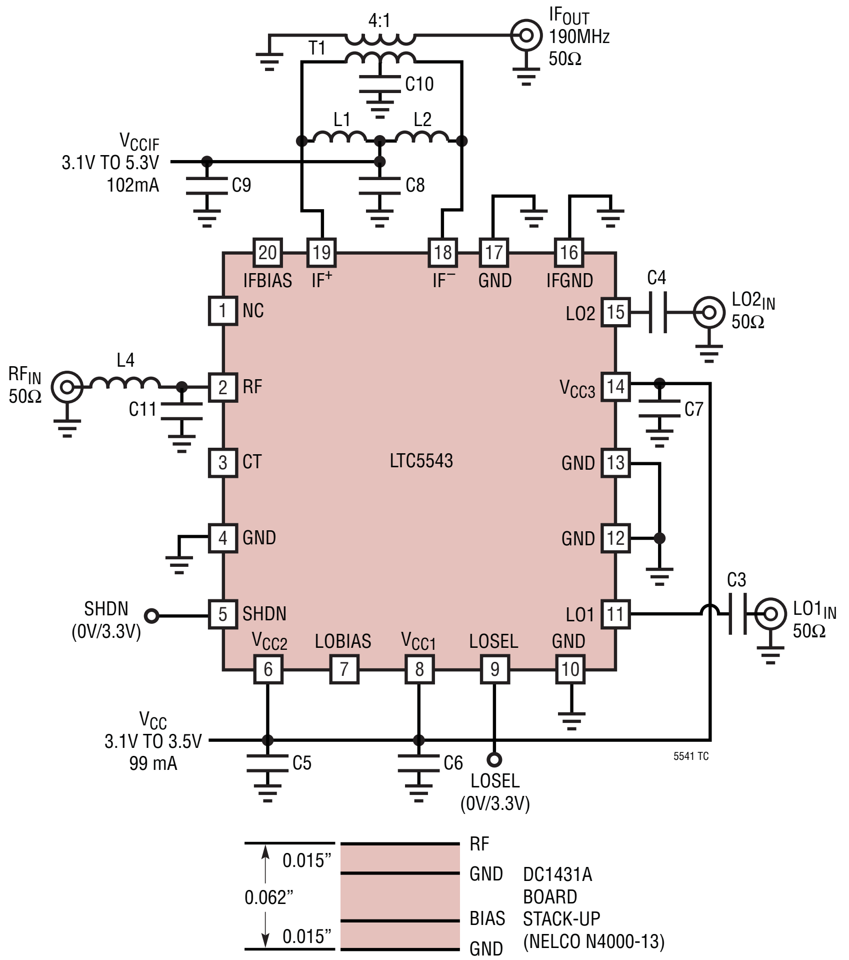
IF^- (Pin 18) and IF^+ (Pin 19): Open-Collector Differential Outputs for the IF Amplifier. These pins must be connected to a DC supply through impedance matching inductors, or a transformer center-tap. Typical DC current consumption is 51mA into each pin.

IFBIAS (Pin 20): This Pin Allows Adjustment of the IF Amplifier Current. Typical DC voltage is 2.1V.

BLOCK DIAGRAM



TEST CIRCUIT



L1, L2 vs IF Frequencies	
IF (MHz)	**L1, L2 (nH)**
140	270
190	150
240	100
305	56
380	39
456	24

REF DES	VALUE	SIZE	COMMENTS
C3, C4	2.7pF	0402	AVX
C6, C7, C8	22pF	0402	AVX
C5, C9	1µF	0603	AVX
C10	1000pF	0402	AVX
C11	0.8pF	0402	AVX
L1, L2	150nH	0603	Coilcraft 0603CS
L4	1.2nH	0402	Toko LL1005-FH
T1 (Alternate)	TC4-1W-7ALN+ (WBC4-6TLB)		Mini-Circuits (Coilcraft)

Figure 1. Standard Downmixer Test Circuit Schematic (190MHz IF)

APPLICATIONS INFORMATION

Introduction

The LTC5543 consists of a high linearity passive double-balanced mixer core, IF buffer amplifier, high speed single-pole double-throw (SPDT) LO switch, LO buffer amplifier and bias/shutdown circuits. See Block Diagram section for a description of each pin function. The RF and LO inputs are single-ended. The IF output is differential. Low-side or high-side LO injection can be used. The evaluation circuit, shown in Figure 1, utilizes bandpass IF output matching and an IF transformer to realize a 50Ω single-ended IF output. The evaluation board layout is shown in Figure 2.

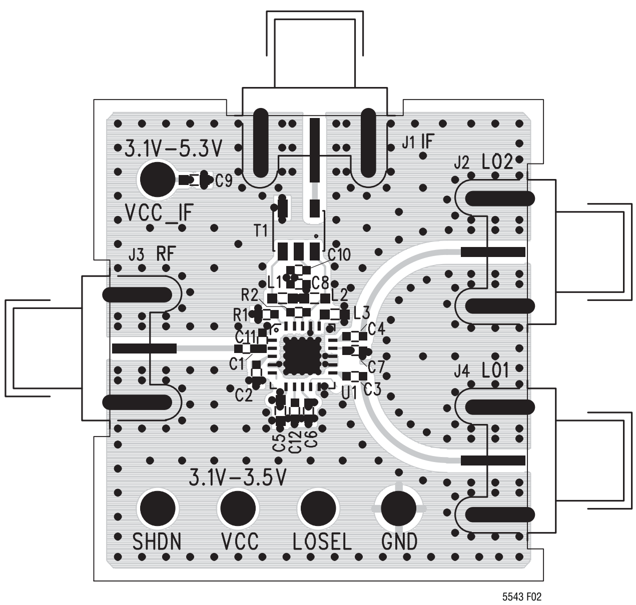


Figure 2. Evaluation Board Layout

RF Input

The mixer's RF input, shown in Figure 3, is connected to the primary winding of an integrated transformer. A 50Ω match is realized with a series inductor (L4) and a shunt capacitor (C11). The primary side of the RF transformer is DC-grounded internally and the DC resistance of the primary is approximately 3.2Ω. A DC blocking capacitor is needed if the RF source has DC voltage present.

The secondary winding of the RF transformer is internally connected to the passive mixer. The center-tap of the transformer secondary is connected to pin 3 (CT) to allow the connection of bypass capacitor, C2. The value of C2 is LO frequency-dependent and is not required for most applications. When used, C2 should be located within 2mm of pin 3 for proper high-frequency decoupling. The nominal DC voltage on the CT pin is 1.2V.

For the RF input to be matched, the selected LO input must be driven. A broadband input match is realized with L4 = 1.2nH and C11 = 0.8pF. The measured RF input return loss is shown in Figure 4 for LO frequencies of 2.6GHz, 3.0GHz and 3.4GHz. These LO frequencies correspond to the lower, middle and upper values of the LO range. As shown in Figure 4, the RF input impedance is somewhat dependent on LO frequency.

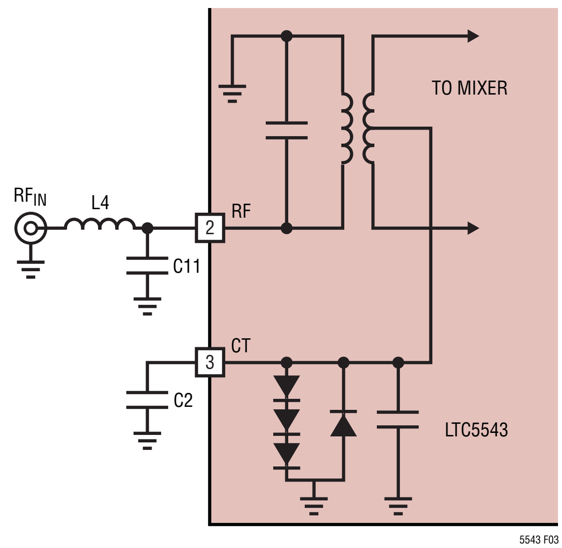


Figure 3. RF Input Schematic

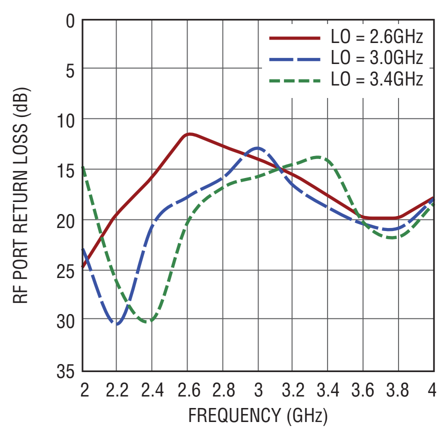


Figure 4. RF Input Return Loss

APPLICATIONS INFORMATION

The RF input impedance and input reflection coefficient, versus RF frequency, is listed in Table 1. The reference plane for this data is pin 2 of the IC, with no external matching, and the LO is driven at 2.69GHz.

Table 1. RF Input Impedance and S11 (at Pin 2, No External Matching, LO Input Driven at 2.69GHz)

FREQUENCY (GHz)	INPUT IMPEDANCE	S11	
		MAG	ANGLE
2.0	44.6 + j14.7	0.16	101.3
2.2	41.0 + j11.9	0.16	119.7
2.4	37.7 + j10.7	0.18	132.0
2.6	31.7 + j9.4	0.25	146.2
2.8	26.2 + j18.8	0.38	127.8
3.0	28.3 + j22.4	0.38	118.1
3.2	28.2 + j24.5	0.40	114.3
3.4	27.7 + j27.8	0.43	109.0
3.6	28.7 + j31.2	0.46	102.7
3.8	29.9 + j32.8	0.45	99.2
4.0	30.4 + j33.4	0.44	97.8

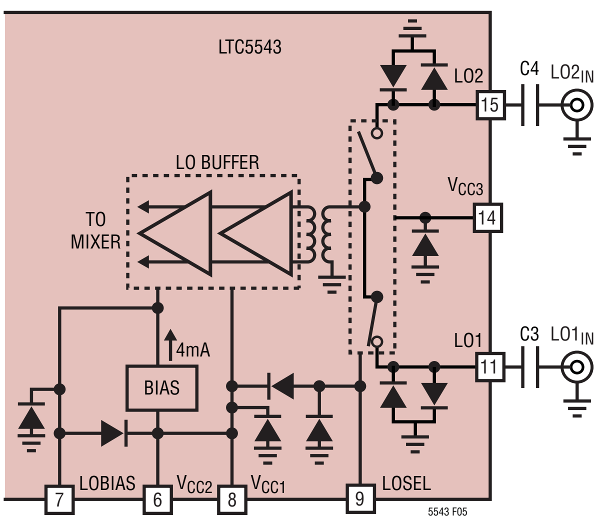


Figure 5. LO Input Schematic

LO Inputs

The mixer's LO input circuit, shown in Figure 5, consists of an integrated SPDT switch, a balun transformer, and a two-stage high-speed limiting differential amplifier to drive the mixer core. The LTC5543's LO amplifiers are optimized for the 2.4GHz to 3.6GHz LO frequency range. LO frequencies above or below this frequency range may be used with degraded performance.

The LO switch is designed for high isolation and fast (<50ns) switching. This allows the use of two active synthesizers in frequency-hopping applications. If only one synthesizer is used, then the unused LO input may be grounded. The LO switch is powered by V_{CC3} (Pin 14) and controlled by the LOSEL logic input (Pin 9). The LO1 and LO2 inputs are always 50Ω-matched when V_{CC} is applied to the chip, even when the chip is shutdown. The DC resistance of the selected LO input is approximately 20Ω and the unselected input is approximately 50Ω. A logic table for the LO switch is shown in Table 2. Measured LO input return loss is shown in Figure 6.

Table 2. LO Switch Logic Table

LOSEL	ACTIVE LO INPUT
Low	LO1
High	LO2

The LO amplifiers are powered by V_{CC1} and V_{CC2} (pin 8 and pin 6). When the chip is enabled (SHDN = low), the internal bias circuit provides a regulated 4mA current to the amplifier's bias input, which in turn causes the amplifiers to draw approximately 90mA of DC current. This 4mA reference current is also connected to LOBIAS (Pin 7) to allow modification of the amplifier's DC bias current for special applications. The recommended application circuits require no LO amplifier bias modification, so this pin should be left open-circuited.

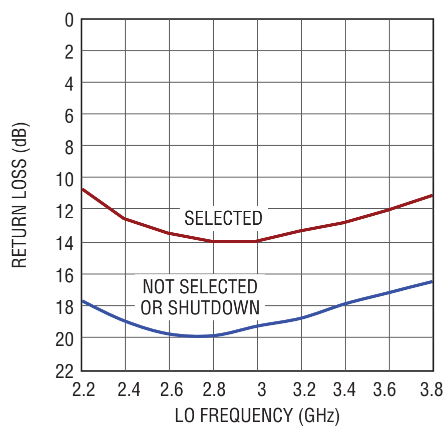


Figure 6. LO Input Return loss

APPLICATIONS INFORMATION

The nominal LO input level is 0dBm although the limiting amplifiers will deliver excellent performance over a ±6dB input power range. LO input power greater than 6dBm may cause conduction of the internal ESD diodes. Series capacitors C3 and C4 optimize the input match and provide DC blocking.

The LO1 input impedance and input reflection coefficient, versus frequency, is shown in Table 3. The LO2 port is identical due to the symmetric device layout and packaging.

Table 3. LO1 Input Impedance vs Frequency (at Pin 11, No External Matching, LOSEL = Low)

FREQUENCY (GHz)	INPUT IMPEDANCE	S11	
		MAG	ANGLE
2.0	28.9 + j3.6	0.27	167.7
2.2	30.8 + j8.7	0.26	149.5
2.4	33.4 + j11.7	0.24	136.8
2.6	34.6 + j13.7	0.24	129.1
2.8	35.3 + j16.2	0.25	121.5
3.0	36.0 + j18.8	0.27	114.3
3.2	37.2 + j22.1	0.28	105.9
3.4	38.7 + j24.6	0.30	99.2
3.6	39.4 + j26.9	0.31	94.8
3.8	39.7 + j29.1	0.33	91.5
4.0	39.6 + j32.4	0.36	87.9

IF Output

The IF amplifier, shown in Figure 7, has differential open-collector outputs (IF^+ and IF^-), a DC ground return pin (IFGND), and a pin for modifying the internal bias (IFBIAS). The IF outputs must be biased at the supply voltage (V_{CCIF}), which is applied through matching inductors L1 and L2. Alternatively, the IF outputs can be biased through the center tap of a transformer. The common node of L1 and L2 can be connected to the center tap of the transformer. Each IF output pin draws approximately 51mA of DC supply current (102mA total). IFGND (pin 16) must be grounded or the amplifier will not draw DC current. Grounding through inductor L3 may improve LO-IF and RF-IF leakage performance in some applications, but is otherwise not necessary. High DC resistance in L3 will reduce the IF amplifier supply current, which will degrade RF performance.

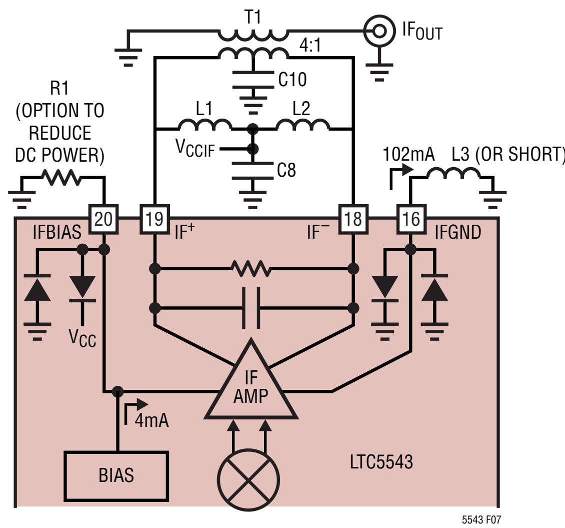


Figure 7. IF Amplifier Schematic with Transformer-Based Bandpass Match

For optimum single-ended performance, the differential IF outputs must be combined through an external IF transformer or discrete IF balun circuit. The evaluation board (see Figures 1 and 2) uses a 4:1 ratio IF transformer for impedance transformation and differential to single-ended transformation. It is also possible to eliminate the IF transformer and drive differential filters or amplifiers directly.

The IF output impedance can be modeled as 320Ω in parallel with 2.4pF at IF frequencies. An equivalent small-signal model (including bondwire inductance) is shown in Figure 8. Frequency-dependent differential IF output impedance is listed in Table 4. This data is referenced to the package pins (with no external components) and includes the effects of IC and package parasitics.

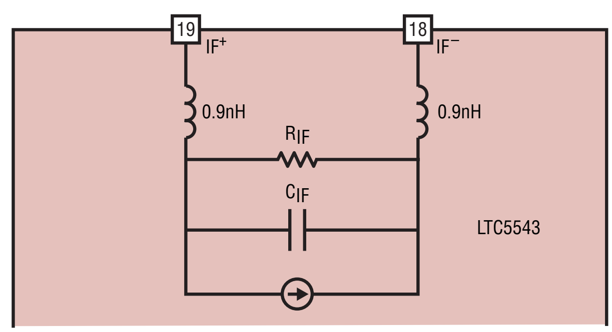


Figure 8. IF Output Small-Signal Model

APPLICATIONS INFORMATION

Transformer-Based Bandpass IF Matching

The IF output can be matched for IF frequencies as low as 90MHz or as high as 500MHz using the bandpass IF matching shown in Figure 1 and Figure 7. L1 and L2 resonate with the internal IF output capacitance at the desired IF frequency. The value of L1, L2 is calculated as follows:

$$L1, L2 = 1/[(2\ \pi\ f_{IF})^2 \bullet 2 \bullet C_{IF}]$$

where C_{IF} is the internal IF capacitance (listed in Table 4).

Values of L1 and L2 are tabulated in Figure 1 for various IF frequencies.

Table 4. IF Output Impedance vs Frequency

FREQUENCY (MHz)	DIFFERENTIAL OUTPUT IMPEDANCE (R_{IF} || X_{IF} (C_{IF}))
90	348 || –j680 (2.6pF)
140	335 || –j455 (2.5pF)
190	324 || –j349 (2.4pF)
240	320 || –j276 (2.4pF)
300	315 || –j221 (2.4pF)
380	310 || –j182 (2.3pF)
456	302 || –j145 (2.4pF)

The typical performance of the LTC5543 using transformer-based bandpass IF matching at 305MHz output frequency is shown in Figure 9. The values of L1 and L2 are 56nH as shown in Figure 1.

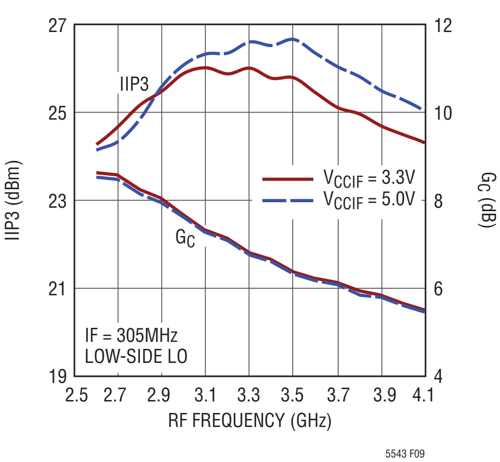


Figure 9. Conversion Gain and IIP3 vs RF Frequency Using Transformer-Based IF Matching

Discrete IF Balun Matching

For many applications, it is possible to replace the IF Transformer with the discrete IF Balun shown in Figure 10. The values of L5, L6, C13 and C14 are calculated to realize a 180° phase shift at the desired IF frequency and provide a 50Ω single-ended output, using the equations listed below. Inductor L7 is used to cancel the internal capacitance C_{IF} and supplies bias voltage to the IF pin. C15 is a DC blocking capacitor.

$$L5, L6 = \frac{\sqrt{R_{IF} \bullet R_{OUT}}}{\omega_{IF}}$$

$$C13, C14 = \frac{1}{\omega_{IF} \bullet \sqrt{R_{IF} \bullet R_{OUT}}}$$

$$L7 = \frac{|X_{IF}|}{\omega_{IF}}$$

These equations give a good starting point, but it is usually necessary to adjust the component values after building and testing the circuit. The final solution can be achieved with less iteration by considering the parasitics of L7 in the above calculation.

The typical performance of the LTC5543 using a 456MHz discrete IF Balun is shown in Figure 11. The actual component values are:

L5, L6 = 36nH, L7 = 48nH and C13, C14 = 3.3pF

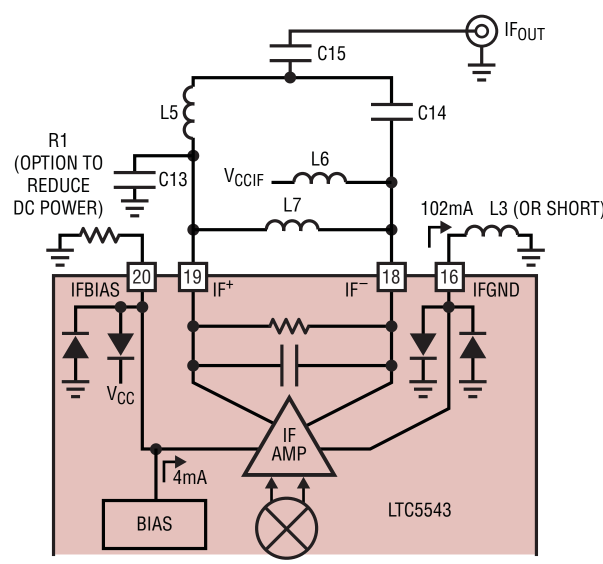


Figure 10. IF Amplifier Schematic with Discrete IF Balun

APPLICATIONS INFORMATION

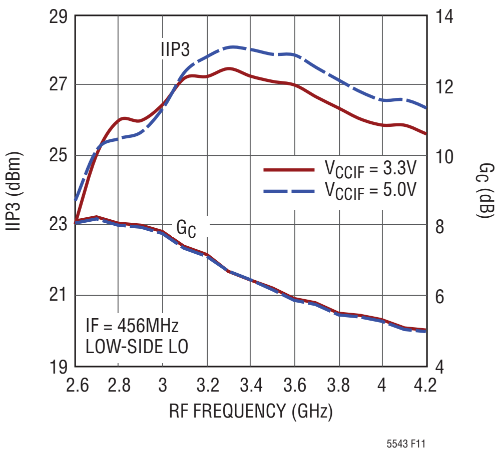


Figure 11. Conversion Gain and IIp3 vs RF Frequency Using a 456MHz Discrete IF Balun

Measured IF output return losses for transformer-based bandpass IF matching (190MHz and 305MHz IF frequency) and discrete Balun IF matching (456MHz IF frequency) are plotted in Figure 12.

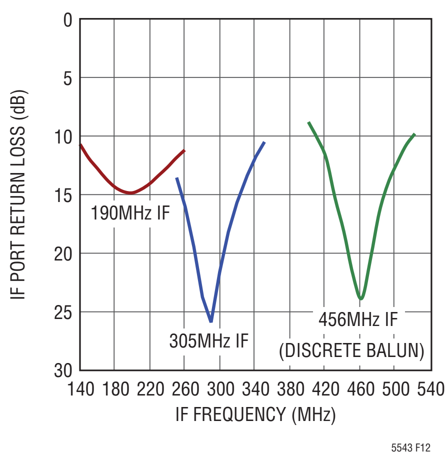


Figure 12. IF Output Return Loss

IF Amplifier Bias

The IF amplifier delivers excellent performance with V_{CCIF} = 3.3V, which allows the V_{CC} and V_{CCIF} supplies to be common. With V_{CCIF} increased to 5V, the RF input P1dB increases by more than 3dB, at the expense of higher power consumption. Mixer performance at 2500MHz is shown in Table 5 with V_{CCIF} = 3.3V and 5V. For the highest conversion gain, high-Q wire-wound chip inductors are recommended for L1 and L2, especially when using V_{CCIF} = 3.3V. Low-cost multilayer chip inductors may be substituted, with a slight degradation in performance.

Table 5. Performance Comparison with V_{CCIF} = 3.3V and 5V (RF = 2500MHz, High-Side LO, IF = 190MHz)

V_{CCIF} (V)	I_{CCIF} (mA)	G_C (dB)	P1dB (dBm)	IIP3 (dBm)	NF (dB)
3.3	102	8.4	10.9	24.5	10.2
5	105	8.4	13.9	24.5	10.3

The IFBIAS pin (pin 20) is available for reducing the DC current consumption of the IF amplifier, at the expense of reduced performance. This pin should be left open-circuited for optimum performance. The internal bias circuit produces a 4mA reference for the IF amplifier, which causes the amplifier to draw approximately 102mA. If resistor R1 is connected to pin 20 as shown in Figure 7, a portion of the reference current can be shunted to ground, resulting in reduced IF amplifier current. For example, R1 = 1kΩ will shunt away 1.5mA from pin 20 and the IF amplifier current will be reduced by 38% to approximately 62mA. The nominal, open-circuit DC voltage at pin 20 is 2.1V. Table 6 lists RF performance at 2500MHz versus IF amplifier current.

Table 6. Mixer Performance with Reduced IF Amplifier Current (RF = 2500MHz, High-Side LO, IF = 190MHz, V_{CC} = V_{CCIF} = 3.3V)

R1 (kΩ)	I_{CCIF} (mA)	G_C (dB)	IIP3 (dBm)	P1dB (dBm)	NF (dB)
OPEN	102	8.4	24.5	10.9	10.2
4.7	90	8.3	24.1	11	10.1
2.2	81	8.1	23.5	11	10.2
1	62	7.7	21.6	11	10.2
(RF = 3500MHz, Low-Side LO, IF = 190MHz, V_{CC} = V_{CCIF} = 3.3V)					
R1 (kΩ)	**I_{CCIF} (mA)**	**G_C (dB)**	**IIP3 (dBm)**	**P1dB (dBm)**	**NF (dB)**
OPEN	100	6.7	25.1	11.3	11.8
4.7	90	6.4	24.7	11.4	11.7
2.2	82	6.1	24.2	11.5	11.8
1	64	5.3	23.2	11.4	12.1

Shutdown Interface

Figure 13 shows a simplified schematic of the SHDN pin interface. To disable the chip, the SHDN voltage must be higher than 3.0V. If the shutdown function is not required, the SHDN pin should be connected directly to GND. The voltage at the SHDN pin should never exceed the power supply voltage (V_{CC}) by more than 0.3V. If this should occur, the supply current could be sourced through the ESD diode, potentially damaging the IC.

APPLICATIONS INFORMATION

The SHDN pin must be pulled high or low. If left floating, then the on/off state of the IC will be indeterminate. If a three-state condition can exist at the SHDN pin, then a pull-up or pull-down resistor must be used.

Supply Voltage Ramping

Fast ramping of the supply voltage can cause a current glitch in the internal ESD protection circuits. Depending on the supply inductance, this could result in a supply voltage transient that exceeds the maximum rating. A supply voltage ramp time of greater than 1ms is recommended.

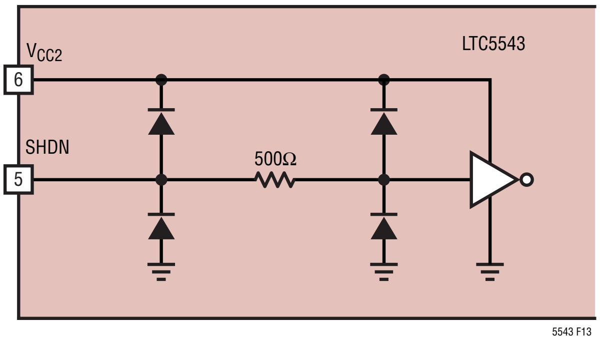
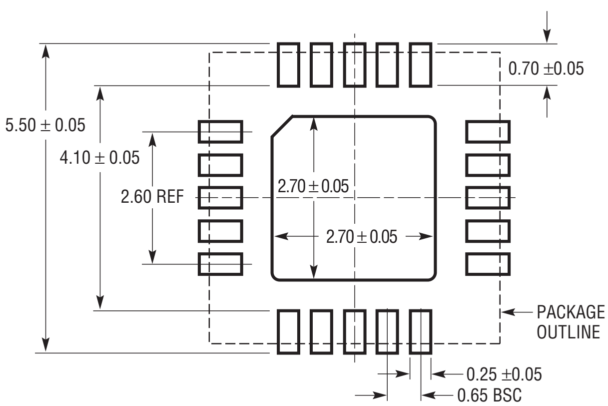


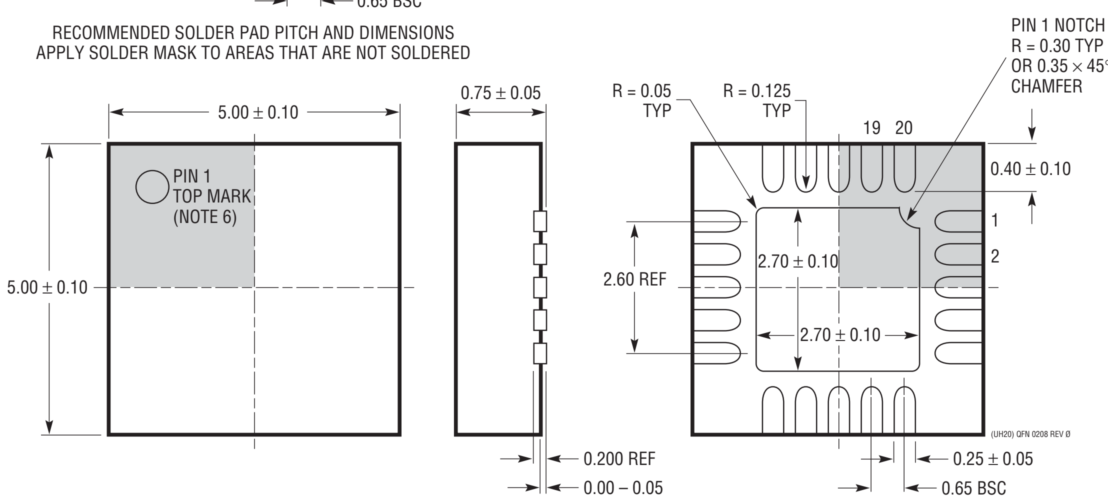
Figure 13. Shutdown Input Circuit

PACKAGE DESCRIPTION

UH Package
20-Lead Plastic QFN (5mm × 5mm)
(Reference LTC DWG # 05-08-1818 Rev Ø)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED



BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING IS NOT A JEDEC PACKAGE OUTLINE
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.20mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
Infrastructure		
LT®5514	Ultralow Distortion, IF Amplifier/ADC Driver with Digitally Controlled Gain	850MHz Bandwidth, 47dBm OIP3 at 100MHz, 10.5dB to 33dB Gain Control Range
LT5517	40MHz to 900MHz Quadrature Demodulator	21dBm IIP3, Integrated LO Quadrature Generator
LT5521	10MHz to 3700MHz High Linearity Upconverting Mixer	24.2dBm IIP3 at 1.95GHz, NF = 12.5dB, 3.15V to 5.25V Supply, Single-Ended LO Port Operation
LT5522	400MHz to 2.7GHz High Signal Level Downconverting Mixer	4.5V to 5.25V Supply, 25dBm IIP3 at 900MHz, NF = 12.5dB, 50Ω Single-Ended RF and LO Ports
LT5527	400MHz to 3.7GHz, 5V Downconverting Mixer	2.3dB Conversion Gain, 23.5dBm IIP3 and 12.5dB NF at 1900MHz, 5V/78mA Supply
LTC6400-X	300MHz Low Distortion IF Amp/ADC Driver	Fixed Gain of 8dB, 14dB, 20dB and 26dB; >36dBm OIP3 at 300MHz, Differential I/O
LTC6401-X	140MHz Low Distortion IF Amp/ADC Driver	Fixed Gain of 8dB, 14dB, 20dB and 26dB; >40dBm OIP3 at 140MHz, Differential I/O
LTC6416	2GHz 16-Bit ADC Buffer	40.25dBm OIP3 to 300MHz, Programmable Fast Recovery Output Clamping
LTC6412	31dB Linear Analog VGA	35dBm OIP3 at 240MHz, Continuous Gain Range –14dB to 17dB
LT5554	Ultralow Distort IF Digital VGA	48dBm OIP3 at 200MHz, 2dB to 18dB Gain Range, 0.125dB Gain Steps
LT5557	400MHz to 3.8GHz 3.3V Downconverting Mixer	2.9dB Conversion Gain, 24.7dBm IIP3 and 11.7dB NF at 1950MHz, 3.3V/82mA Supply
LT5560	Ultra-Low Power Active Mixer	10mA Supply Current, 10dBm IIP3, 10dB NF, Usable as Up- or Down-Converter.
LT5568	700MHz to 1050MHz High Linearity Direct Quadrature Modulator	22.9dBm OIP3 at 850MHz, –160.3dBm/Hz Noise Floor, 50Ω, 0.5V_{DC} Baseband Interface, 3-Ch CDMA2000 ACPR = –71.4dBc at 850MHz
LT5572	1.5GHz to 2.5GHz High Linearity Direct Quadrature Modulator	21.6dBm OIP3 at 2GHz, –158.6dBm/Hz Noise Floor, High-Ohmic 0.5V_{DC} Baseband Interface, 4-Ch W-CDMA ACPR = –67.7dBc at 2.14GHz
LT5575	700MHz to 2.7GHz Direct Conversion I/Q Demodulator	Integrated Baluns, 28dBm IIP3, 13dBm P1dB, 0.03dB I/Q Amplitude Match, 0.4° Phase Match
LT5578	400MHz to 2.7GHz High Linearty Upconverting Mixer	27dBm OIP3 at 900MHz, 24.2dBm at 1.95GHz, Integrated RF Transformer
LT5579	1.5GHz to 3.8GHz High Linearity Upconverting Mixer	27.3dBm OIP3 at 2.14GHz, NF = 9.9dB, 3.3V Supply, Single-Ended LO and RF Ports
LTC5598	5MHz to 1.6GHz I/Q Modulator	27.7dBm OIP3 at 140MHz, 22.9dBm at 900MHz, –161.2dBm/Hz Noise Floor
RF Power Detectors		
LTC5505	RF Power Detectors with >40dB Dynamic Range	300MHz to 3GHz, Temperature Compensated, 2.7V to 6V Supply
LTC5532	300MHz to 7GHz Precision RF Power Detector	Precision V_{OUT} Offset Control, Adjustable Gain and Offset
LT5534	50MHz to 3GHz Log RF Power Detector with 60dB Dynamic Range	±1dB Output Variation over Temperature, 38ns Response Time, Log Linear Response
LTC5536	Precision 600MHz to 7GHz RF Power Detector with Fast Comparator Output	25ns Response Time, Comparator Reference Input, Latch Enable Input, –26dBm to +12dBm Input Range
LT5537	Wide Dynamic Range Log RF/IF Detector	Low Frequency to 1GHz, 83dB Log Linear Dynamic Range
LT5570	2.7GHz Mean-Squared Detector	±0.5dB Accuracy Over Temperature and >50dB Dynamic Range, Fast 500ns Rise Time
LT5581	6GHz Low Power RMS Detector	40dB Dynamic Range, ±1dB Accuracy Over Temperature, 1.5mA Supply Current
ADCs		
LTC2208	16-Bit, 130Msps ADC	78dBFS Noise Floor, >83dB SFDR at 250MHz
LTC2262-14	14-Bit, 150Msps ADC Ultralow Power at 1.8V Supply	72.8dB SNR, 88dB SFDR, 149mW Power Consumption
LTC2242-12	12-Bit, 250Msps ADC	65.4dB SNR, 78dB SFDR, 740mW Power Consumption

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http://moschip.ru/get-element

Вы можете разместить у нас заказ для любого Вашего проекта, будь то серийное производство или разработка единичного прибора.

В нашем ассортименте представлены ведущие мировые производители активных и пассивных электронных компонентов.

Нашей специализацией является поставка электронной компонентной базы двойного назначения, продукции таких производителей как XILINX, Intel (ex.ALTERA), Vicor, Microchip, Texas Instruments, Analog Devices, Mini-Circuits, Amphenol, Glenair.

Сотрудничество с глобальными дистрибьюторами электронных компонентов, предоставляет возможность заказывать и получать с международных складов практически любой перечень компонентов в оптимальные для Вас сроки.

На всех этапах разработки и производства наши партнеры могут получить квалифицированную поддержку опытных инженеров.

Система менеджмента качества компании отвечает требованиям в соответствии с ГОСТ Р ИСО 9001, ГОСТ РВ 0015-002 и ЭС РД 009

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