

# MC74HC541A

## Octal 3-State Noninverting Buffer/Line Driver/Line Receiver

### High-Performance Silicon-Gate CMOS

The MC74HC541A is identical in pinout to the LS541. The device inputs are compatible with Standard CMOS outputs. External pull-up resistors make them compatible with LSTTL outputs.

The HC541A is an octal noninverting buffer/line driver/line receiver designed to be used with 3-state memory address drivers, clock drivers, and other bus-oriented systems. This device features inputs and outputs on opposite sides of the package and two ANDed active-low output enables.

The HC541A is similar in function to the HC540A, which has inverting outputs.

#### Features

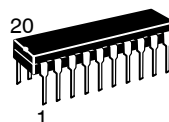
- Output Drive Capability: 15 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS and TTL
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1  $\mu$ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance With the JEDEC Standard No. 7 A Requirements
- Chip Complexity: 134 FETs or 33.5 Equivalent Gates
- These Devices are Pb-Free and are RoHS Compliant



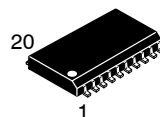
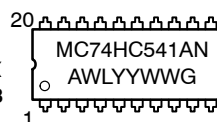
ON Semiconductor®

<http://onsemi.com>

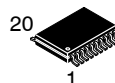
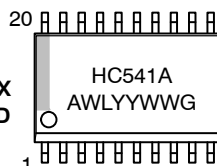
#### MARKING DIAGRAMS



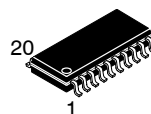
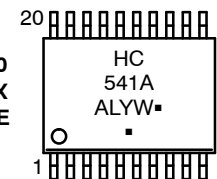
PDIP-20  
N SUFFIX  
CASE 738



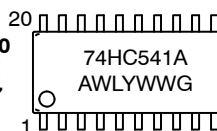
SOIC-20  
DW SUFFIX  
CASE 751D



TSSOP-20  
DT SUFFIX  
CASE 948E



SOEIAJ-20  
F SUFFIX  
CASE 967



A = Assembly Location  
WL, L = Wafer Lot  
YY, Y = Year  
WW, W = Work Week  
G or ■ = Pb-Free Package

(Note: Microdot may be in either location)

#### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

# MC74HC541A

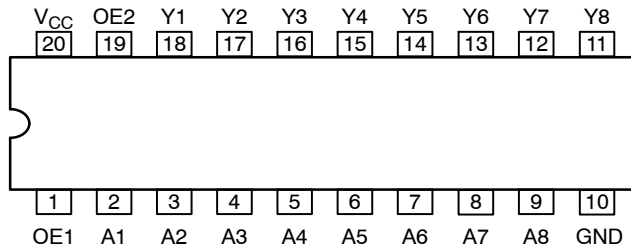


Figure 1. Pinout: 20-Lead Packages (Top View)

## FUNCTION TABLE

| Inputs |     |   | Output Y |
|--------|-----|---|----------|
| OE1    | OE2 | A |          |
| L      | L   | L | L        |
| L      | L   | H | H        |
| H      | X   | X | Z        |
| X      | H   | X | Z        |

X = Don't Care

Z = High Impedance

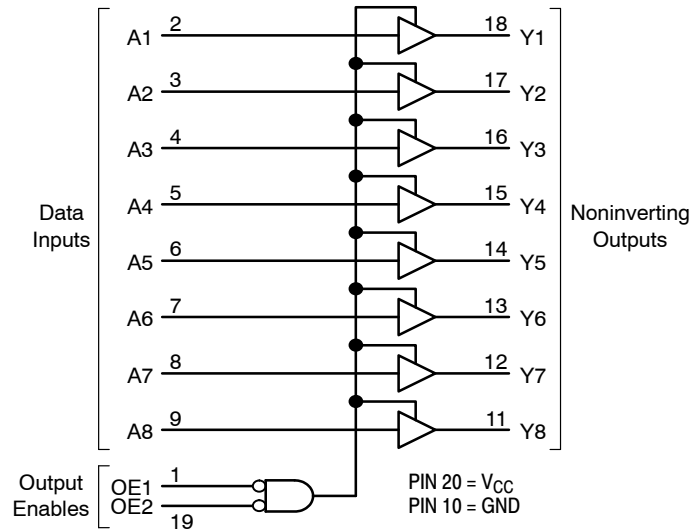


Figure 2. Logic Diagram

## ORDERING INFORMATION

| Device          | Package                   | Shipping†        |
|-----------------|---------------------------|------------------|
| MC74HC541ANG    | PDIP-20<br>(Pb-Free)      | 18 Units / Rail  |
| MC74HC541ADWG   | SOIC-20 WIDE<br>(Pb-Free) | 38 Units / Rail  |
| MC74HC541ADWR2G | SOIC-20 WIDE<br>(Pb-Free) | 1000 Tape & Reel |
| MC74HC541ADTG   | TSSOP-20*                 | 75 Units / Rail  |
| MC74HC541ADTR2G | TSSOP-20*                 | 2500 Tape & Reel |
| MC74HC541AFG    | SOEIAJ-20<br>(Pb-Free)    | 40 Units / Rail  |
| MC74HC541AFELG  | SOEIAJ-20<br>(Pb-Free)    | 2000 Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

\*This package is inherently Pb-Free.

# MC74HC541A

## MAXIMUM RATINGS

| Symbol        | Parameter                                              | Value                                                                                                             | Unit                        |
|---------------|--------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------|-----------------------------|
| $V_{CC}$      | DC Supply Voltage                                      | $-0.5$ to $+7.0$                                                                                                  | V                           |
| $V_I$         | DC Input Voltage                                       | $-0.5 \leq V_I \leq V_{CC} + 0.5$                                                                                 | V                           |
| $V_O$         | DC Output Voltage (Note 1)                             | $-0.5 \leq V_O \leq V_{CC} + 0.5$                                                                                 | V                           |
| $I_{IK}$      | DC Input Diode Current                                 | $\pm 20$                                                                                                          | mA                          |
| $I_{OK}$      | DC Output Diode Current                                | $\pm 35$                                                                                                          | mA                          |
| $I_O$         | DC Output Sink Current                                 | $\pm 35$                                                                                                          | mA                          |
| $I_{CC}$      | DC Supply Current per Supply Pin                       | $\pm 75$                                                                                                          | mA                          |
| $I_{GND}$     | DC Ground Current per Ground Pin                       | $\pm 75$                                                                                                          | mA                          |
| $T_{STG}$     | Storage Temperature Range                              | $-65$ to $+150$                                                                                                   | $^{\circ}\text{C}$          |
| $T_L$         | Lead Temperature, 1 mm from Case for 10 Seconds        | 260                                                                                                               | $^{\circ}\text{C}$          |
| $T_J$         | Junction Temperature under Bias                        | $+150$                                                                                                            | $^{\circ}\text{C}$          |
| $\theta_{JA}$ | Thermal Resistance                                     | PDIP<br>SOIC<br>TSSOP<br>67<br>96<br>128                                                                          | $^{\circ}\text{C}/\text{W}$ |
| $P_D$         | Power Dissipation in Still Air at $85^{\circ}\text{C}$ | PDIP<br>SOIC<br>TSSOP<br>750<br>500<br>450                                                                        | mW                          |
| MSL           | Moisture Sensitivity                                   | Level 1                                                                                                           |                             |
| $F_R$         | Flammability Rating                                    | Oxygen Index: 30% – 35%<br>UL 94 V-0 @ 0.125 in                                                                   |                             |
| $V_{ESD}$     | ESD Withstand Voltage                                  | Human Body Model (Note 2)<br>Machine Model (Note 3)<br>Charged Device Model (Note 4)<br>> 4000<br>> 300<br>> 1000 | V                           |
| $I_{Latchup}$ | Latchup Performance                                    | Above $V_{CC}$ and Below GND at $85^{\circ}\text{C}$ (Note 5)<br>$\pm 300$                                        | mA                          |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1.  $I_O$  absolute maximum rating must be observed.
2. Tested to EIA/JESD22-A114-A.
3. Tested to EIA/JESD22-A115-A.
4. Tested to JESD22-C101-A.
5. Tested to EIA/JESD78.

## RECOMMENDED OPERATING CONDITIONS

| Symbol            | Parameter                                            | Min                                                                                          | Max                | Unit               |
|-------------------|------------------------------------------------------|----------------------------------------------------------------------------------------------|--------------------|--------------------|
| $V_{CC}$          | DC Supply Voltage (Referenced to GND)                | 2.0                                                                                          | 6.0                | V                  |
| $V_{IN}, V_{OUT}$ | DC Input Voltage, Output Voltage (Referenced to GND) | 0                                                                                            | $V_{CC}$           | V                  |
| $T_A$             | Operating Temperature Range, All Package Types       | $-55$                                                                                        | $+125$             | $^{\circ}\text{C}$ |
| $t_r, t_f$        | Input Rise/Fall Time (Figure 3)                      | $V_{CC} = 2.0\text{ V}$<br>$V_{CC} = 4.5\text{ V}$<br>$V_{CC} = 6.0\text{ V}$<br>0<br>0<br>0 | 1000<br>500<br>400 | ns                 |

6. Unused inputs may not be left open. All inputs must be tied to a high-logic voltage level or a low-logic input voltage level.

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## DC CHARACTERISTICS (Voltages Referenced to GND)

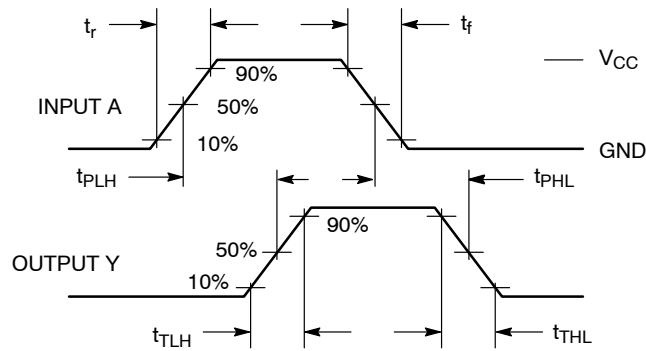
| Symbol          | Parameter                                      | Condition                                                                                                                           | V <sub>CC</sub><br>V     | Guaranteed Limit             |                              |                              | Unit |
|-----------------|------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------|--------------------------|------------------------------|------------------------------|------------------------------|------|
|                 |                                                |                                                                                                                                     |                          | –55 to<br>25°C               | ≤ 85°C                       | ≤ 125°C                      |      |
| V <sub>IH</sub> | Minimum High-Level Input Voltage               | V <sub>OUT</sub> = 0.1 V<br> I <sub>OUT</sub>   ≤ 20 μA                                                                             | 2.0<br>3.0<br>4.5<br>6.0 | 1.50<br>2.10<br>3.15<br>4.20 | 1.50<br>2.10<br>3.15<br>4.20 | 1.50<br>2.10<br>3.15<br>4.20 | V    |
| V <sub>IL</sub> | Maximum Low-Level Input Voltage                | V <sub>OUT</sub> = V <sub>CC</sub> – 0.1 V<br> I <sub>OUT</sub>   ≤ 20 μA                                                           | 2.0<br>3.0<br>4.5<br>6.0 | 0.50<br>0.90<br>1.35<br>1.80 | 0.50<br>0.90<br>1.35<br>1.80 | 0.50<br>0.90<br>1.35<br>1.80 | V    |
| V <sub>OH</sub> | Minimum High-Level Output Voltage              | V <sub>IN</sub> = V <sub>IL</sub><br> I <sub>OUT</sub>   ≤ 20 μA                                                                    | 2.0<br>4.5<br>6.0        | 1.9<br>4.4<br>5.9            | 1.9<br>4.4<br>5.9            | 1.9<br>4.4<br>5.9            | V    |
|                 |                                                | V <sub>IN</sub> = V <sub>IL</sub>  I <sub>OUT</sub>   ≤ 3.6 mA                                                                      | 3.0                      | 2.48                         | 2.34                         | 2.20                         |      |
|                 |                                                | I <sub>OUT</sub>   ≤ 6.0 mA                                                                                                         | 4.5                      | 3.98                         | 3.84                         | 3.70                         |      |
|                 |                                                | I <sub>OUT</sub>   ≤ 7.8 mA                                                                                                         | 6.0                      | 5.48                         | 5.34                         | 5.20                         |      |
| V <sub>OL</sub> | Maximum Low-Level Output Voltage               | V <sub>IN</sub> = V <sub>IH</sub><br> I <sub>OUT</sub>   ≤ 20 μA                                                                    | 2.0<br>4.5<br>6.0        | 0.1<br>0.1<br>0.1            | 0.1<br>0.1<br>0.1            | 0.1<br>0.1<br>0.1            | V    |
|                 |                                                | V <sub>IN</sub> = V <sub>IH</sub>  I <sub>OUT</sub>   ≤ 3.6 mA                                                                      | 3.0                      | 0.26                         | 0.33                         | 0.40                         |      |
|                 |                                                | I <sub>OUT</sub>   ≤ 6.0 mA                                                                                                         | 4.5                      | 0.26                         | 0.33                         | 0.40                         |      |
|                 |                                                | I <sub>OUT</sub>   ≤ 7.8 mA                                                                                                         | 6.0                      | 0.26                         | 0.33                         | 0.40                         |      |
| I <sub>IN</sub> | Maximum Input Leakage Current                  | V <sub>IN</sub> = V <sub>CC</sub> or GND                                                                                            | 6.0                      | ±0.1                         | ±1.0                         | ±1.0                         | μA   |
| I <sub>OZ</sub> | Maximum 3-State Leakage Current                | Output in High Impedance State<br>V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub><br>V <sub>OUT</sub> = V <sub>CC</sub> or GND | 6.0                      | ±0.5                         | ±5.0                         | ±10.0                        | μA   |
| I <sub>CC</sub> | Maximum Quiescent Supply Current (per Package) | V <sub>IN</sub> = V <sub>CC</sub> or GND<br>I <sub>OUT</sub> = 0 μA                                                                 | 6.0                      | 4                            | 40                           | 160                          | μA   |

## AC CHARACTERISTICS (C<sub>L</sub> = 50 pF, Input t<sub>r</sub> = t<sub>f</sub> = 6 ns)

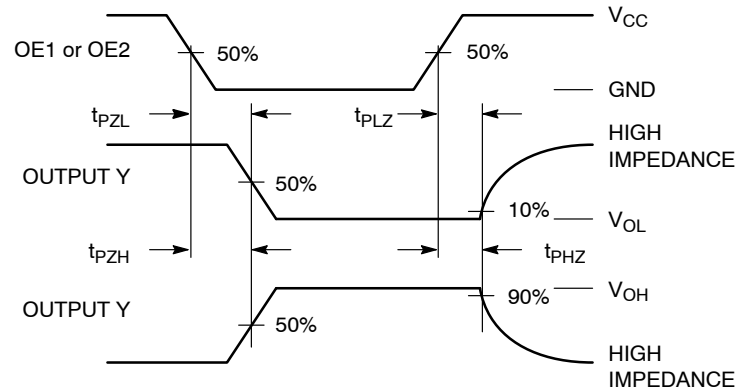
| Symbol                                 | Parameter                                                                 | V <sub>CC</sub><br>V                                           | Guaranteed Limit |        |         | Unit |
|----------------------------------------|---------------------------------------------------------------------------|----------------------------------------------------------------|------------------|--------|---------|------|
|                                        |                                                                           |                                                                | – 55 to<br>25°C  | ≤ 85°C | ≤ 125°C |      |
| t <sub>PLH</sub> ,<br>t <sub>PHL</sub> | Maximum Propagation Delay, Input A to Output Y<br>(Figures 3 and 5)       | 2.0                                                            | 80               | 100    | 120     | ns   |
|                                        |                                                                           | 3.0                                                            | 30               | 40     | 55      |      |
|                                        |                                                                           | 4.5                                                            | 18               | 23     | 28      |      |
|                                        |                                                                           | 6.0                                                            | 15               | 20     | 25      |      |
| t <sub>PLZ</sub> ,<br>t <sub>PHZ</sub> | Maximum Propagation Delay, Output Enable to Output Y<br>(Figures 4 and 6) | 2.0                                                            | 110              | 140    | 165     | ns   |
|                                        |                                                                           | 3.0                                                            | 45               | 60     | 75      |      |
|                                        |                                                                           | 4.5                                                            | 25               | 31     | 38      |      |
|                                        |                                                                           | 6.0                                                            | 21               | 26     | 31      |      |
| t <sub>PZL</sub> ,<br>t <sub>PZH</sub> | Maximum Propagation Delay, Output Enable to Output Y<br>(Figures 4 and 6) | 2.0                                                            | 110              | 140    | 165     | ns   |
|                                        |                                                                           | 3.0                                                            | 45               | 60     | 75      |      |
|                                        |                                                                           | 4.5                                                            | 25               | 31     | 38      |      |
|                                        |                                                                           | 6.0                                                            | 21               | 26     | 31      |      |
| t <sub>TLH</sub> ,<br>t <sub>THL</sub> | Maximum Output Transition Time, Any Output<br>(Figures 3 and 5)           | 2.0                                                            | 60               | 75     | 90      | ns   |
|                                        |                                                                           | 3.0                                                            | 22               | 28     | 34      |      |
|                                        |                                                                           | 4.5                                                            | 12               | 15     | 18      |      |
|                                        |                                                                           | 6.0                                                            | 10               | 13     | 15      |      |
| C <sub>IN</sub>                        | Maximum Input Capacitance                                                 |                                                                | 10               | 10     | 10      | pF   |
| C <sub>OUT</sub>                       | Maximum 3–State Output Capacitance (High Impedance State Output)          |                                                                | 15               | 15     | 15      | pF   |
| C <sub>PD</sub>                        | Power Dissipation Capacitance (Per Buffer) (Note 7)                       | Typical @ 25°C, V <sub>CC</sub> = 5.0 V, V <sub>EE</sub> = 0 V |                  |        |         | pF   |
|                                        |                                                                           | 35                                                             |                  |        |         |      |

7. Used to determine the no-load dynamic power consumption: P<sub>D</sub> = C<sub>PD</sub> V<sub>CC</sub><sup>2</sup>f + I<sub>CC</sub> V<sub>CC</sub>.

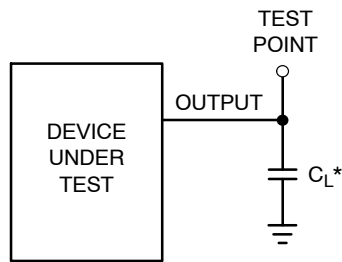
## MC74HC541A



**Figure 3. Switching Waveform**

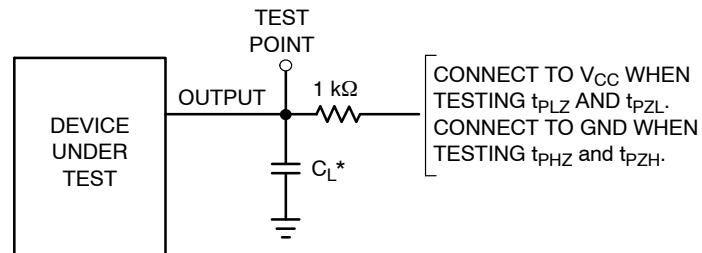


**Figure 4. Switching Waveform**



\*Includes all probe and jig capacitance

**Figure 5. Test Circuit**



\*Includes all probe and jig capacitance

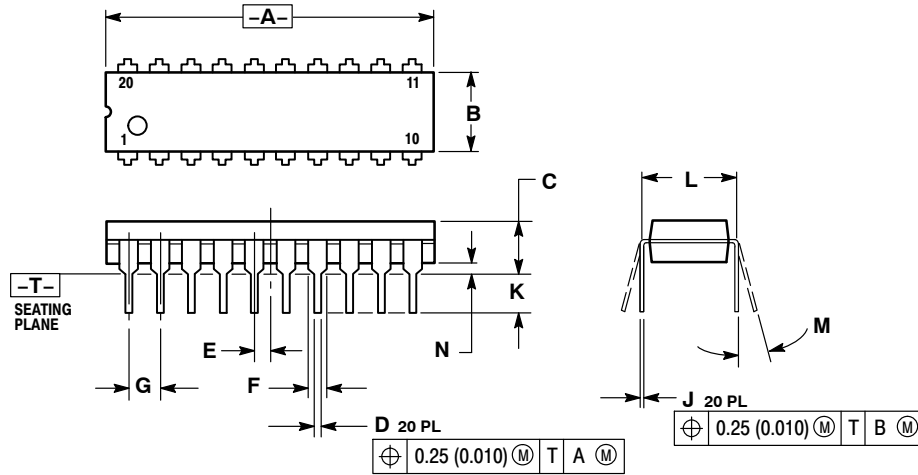
**Figure 6. Test Circuit**



# MC74HC541A

## PACKAGE DIMENSIONS

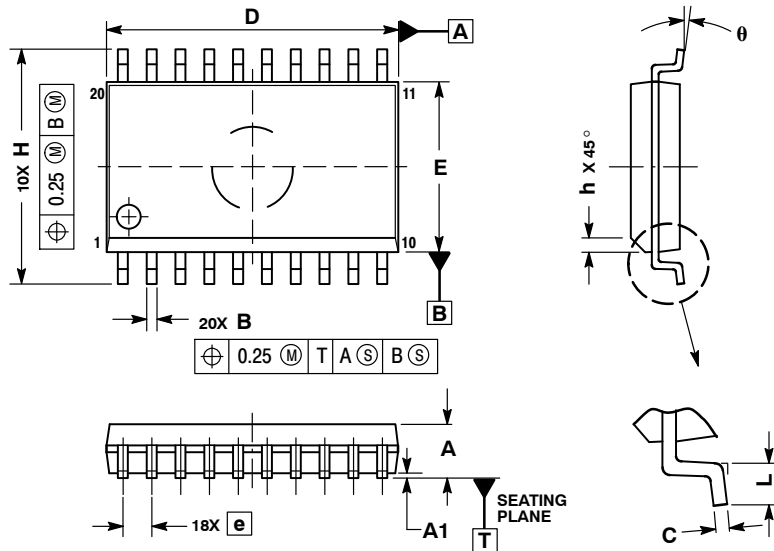
PDIP-20  
N SUFFIX  
PLASTIC DIP PACKAGE  
CASE 738-03  
ISSUE E



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: INCH.
  3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
  4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

| DIM | INCHES    |       | MILLIMETERS |       |
|-----|-----------|-------|-------------|-------|
|     | MIN       | MAX   | MIN         | MAX   |
| A   | 1.010     | 1.070 | 25.66       | 27.17 |
| B   | 0.240     | 0.260 | 6.10        | 6.60  |
| C   | 0.150     | 0.180 | 3.81        | 4.57  |
| D   | 0.015     | 0.022 | 0.39        | 0.55  |
| E   | 0.050 BSC |       | 1.27 BSC    |       |
| F   | 0.050     | 0.070 | 1.27        | 1.77  |
| G   | 0.100 BSC |       | 2.54 BSC    |       |
| J   | 0.008     | 0.015 | 0.21        | 0.38  |
| K   | 0.110     | 0.140 | 2.80        | 3.55  |
| L   | 0.300 BSC |       | 7.62 BSC    |       |
| M   | 0°        | 15°   | 0°          | 15°   |
| N   | 0.020     | 0.040 | 0.51        | 1.01  |

SOIC-20  
DW SUFFIX  
CASE 751D-05  
ISSUE G



- NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
  2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
  3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
  4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
  5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

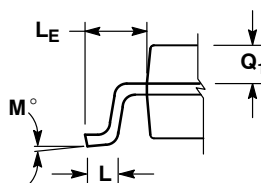
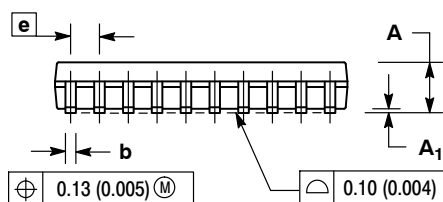
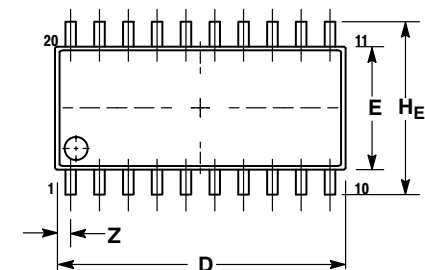
| DIM | MILLIMETERS |       |
|-----|-------------|-------|
|     | MIN         | MAX   |
| A   | 2.35        | 2.65  |
| A1  | 0.10        | 0.25  |
| B   | 0.35        | 0.49  |
| C   | 0.23        | 0.32  |
| D   | 12.65       | 12.95 |
| E   | 7.40        | 7.60  |
| e   | 1.27 BSC    |       |
| H   | 10.05       | 10.55 |
| h   | 0.25        | 0.75  |
| L   | 0.50        | 0.90  |
| θ   | 0°          | 7°    |



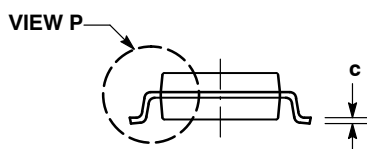
# MC74HC541A

## PACKAGE DIMENSIONS

SOEIAJ-20  
F SUFFIX  
CASE 967-01  
ISSUE A



DETAIL P



### NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

| DIM            | MILLIMETERS |       | INCHES    |       |
|----------------|-------------|-------|-----------|-------|
|                | MIN         | MAX   | MIN       | MAX   |
| A              | ---         | 2.05  | ---       | 0.081 |
| A <sub>1</sub> | 0.05        | 0.20  | 0.002     | 0.008 |
| b              | 0.35        | 0.50  | 0.014     | 0.020 |
| c              | 0.15        | 0.25  | 0.006     | 0.010 |
| D              | 12.35       | 12.80 | 0.486     | 0.504 |
| E              | 5.10        | 5.45  | 0.201     | 0.215 |
| e              | 1.27 BSC    |       | 0.050 BSC |       |
| H <sub>E</sub> | 7.40        | 8.20  | 0.291     | 0.323 |
| L              | 0.50        | 0.85  | 0.020     | 0.033 |
| L <sub>E</sub> | 1.10        | 1.50  | 0.043     | 0.059 |
| M              | 0°          | 10°   | 0°        | 10°   |
| Q <sub>1</sub> | 0.70        | 0.90  | 0.028     | 0.035 |
| Z              | ---         | 0.81  | ---       | 0.032 |

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