

## FEATURES

6-channel, current output DAC

14-bit resolution

Programmable output current ranges

Channel 0: 0 mA to 300 mA, -60 mA to +300 mA, -60 mA to 0 mA

Channel 1: 0 mA to 140 mA, 0 mA to 250 mA

Channel 2: 0 mA to 55 mA, 0 mA to 150 mA

Channel 3, Channel 4, Channel 5: 0 mA to 45 mA, 0 mA to 100 mA

All current sourcing output ranges scale back by up to 0.5x

1.25 V, on-chip voltage reference

Integrated precision reference resistor

SPI interface

Reset function

Output current monitor

Compliance voltage monitor

Die temperature monitor

Integrated thermal shutdown

49-ball, 4 mm × 4 mm WLCSP package

Operating temperature: -40°C to +105°C

## APPLICATIONS

Photonics control

LED driver programmable current source

Current mode biasing

## GENERAL DESCRIPTION

The AD5770R is a 6-channel, 14-bit resolution, low noise, programmable current output, digital-to-analog converter (DAC) for photonics control applications. The device incorporates a 1.25 V, on-chip voltage reference, a 2.5 kΩ precision resistor for reference current generation, die temperature, output monitoring functions, fault alarm, and reset functions.

The AD5770R contains five 14-bit resolution current sourcing DAC channels and one 14-bit resolution current sourcing and sinking DAC channel.

Channel 0 can be configured to sink up to 60 mA and source up to 300 mA. Channel 1 to Channel 5 have multiple programmable output current sourcing ranges set by register access.

Each DAC operates with a wide power supply rail from 0.8 V to AVDD - 0.4 V for optimizing power efficiency and thermal power dissipation.

The AD5770R operates from a 2.9 V to 5.5 V AVDD supply and is specified over the -40°C to +105°C temperature range.

## FUNCTIONAL BLOCK DIAGRAM

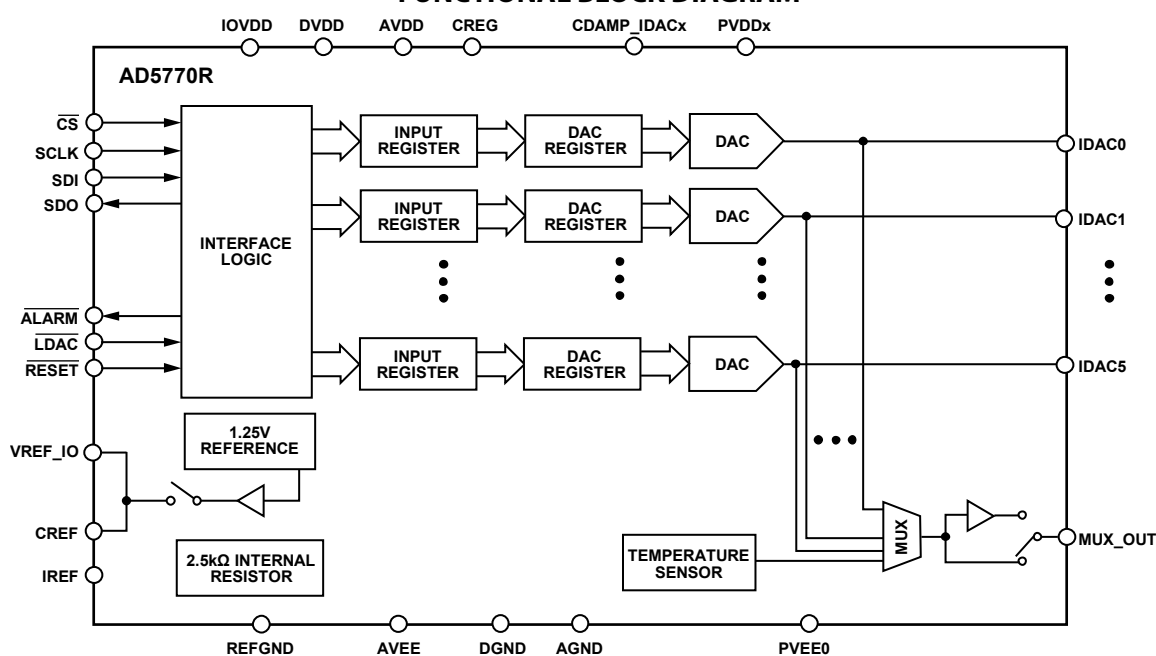


Figure 1.

16128-001

Rev. A

[Document Feedback](#)

Information furnished by Analog Devices is believed to be accurate and reliable. However, no responsibility is assumed by Analog Devices for its use, nor for any infringements of patents or other rights of third parties that may result from its use. Specifications subject to change without notice. No license is granted by implication or otherwise under any patent or patent rights of Analog Devices. Trademarks and registered trademarks are the property of their respective owners.

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.  
Tel: 781.329.4700 ©2019 Analog Devices, Inc. All rights reserved.  
[Technical Support](#) [www.analog.com](http://www.analog.com)

## TABLE OF CONTENTS

|                                                  |    |                                                   |    |
|--------------------------------------------------|----|---------------------------------------------------|----|
| Features .....                                   | 1  | Load DAC.....                                     | 28 |
| Applications.....                                | 1  | Input Page Mask Register.....                     | 28 |
| General Description .....                        | 1  | DAC Page Mask Register.....                       | 28 |
| Functional Block Diagram .....                   | 1  | Output Stages .....                               | 28 |
| Revision History .....                           | 2  | Output Filter .....                               | 30 |
| Specifications.....                              | 3  | Output Current Scaling .....                      | 30 |
| AC Performance Characteristics .....             | 6  | ALARM .....                                       | 30 |
| Timing Specifications .....                      | 7  | Applications Information.....                     | 33 |
| Timing Diagrams.....                             | 8  | Microprocessor Interfacing.....                   | 33 |
| Absolute Maximum Ratings.....                    | 9  | AD5770R to SPI Interface.....                     | 33 |
| Thermal Resistance .....                         | 9  | Thermal Considerations.....                       | 33 |
| ESD Caution.....                                 | 9  | Combining Channels to Increase Current Range..... | 33 |
| Pin Configuration and Function Descriptions..... | 10 | Layout Guidelines.....                            | 33 |
| Typical Performance Characteristics .....        | 12 | Register Summary .....                            | 35 |
| Terminology .....                                | 24 | SPI Configuration Registers.....                  | 35 |
| Theory of Operation .....                        | 25 | AD5770R Configuration Registers .....             | 35 |
| Digital to Analog Converter .....                | 25 | Register Details .....                            | 38 |
| Precision Reference Current Generation .....     | 25 | Outline Dimensions .....                          | 59 |
| Diagnostic Monitoring .....                      | 25 | Ordering Guide .....                              | 59 |
| Serial Interface .....                           | 26 |                                                   |    |
| Reset Function .....                             | 28 |                                                   |    |

## REVISION HISTORY

### 11/2019—Rev. 0 to Rev. A

|                                                                                                                                            |    |
|--------------------------------------------------------------------------------------------------------------------------------------------|----|
| Changes to AVEE Supply Current Parameter, Table 1 .....                                                                                    | 5  |
| Changes to Figure 2.....                                                                                                                   | 8  |
| Changes to Figure 41 Caption, Figure 42 Caption, Figure 43<br>Caption, Figure 44 Caption, Figure 45 Caption,<br>and Figure 46 Caption..... | 18 |
| Changes to Figure 47 Caption.....                                                                                                          | 19 |
| Changes to Output Current Scaling Section .....                                                                                            | 30 |
| Changes to Table 10.....                                                                                                                   | 31 |
| Changes to Table 11.....                                                                                                                   | 34 |

### 2/2019—Revision 0: Initial Version

## SPECIFICATIONS

AVDD = DVDD = 2.9 V to 5.5 V, PVDD = 0.8 V to AVDD – 0.4 V, AVEE = –3.0 V to 0 V,  $2.5\text{ V} \leq \text{PVDD} - \text{AVEE} \leq 5.5\text{ V}$ , IOVDD = 1.65 V to 5.5 V,  $\text{AVEE} \leq \text{PVEE0} \leq 0\text{ V}$ ,  $\text{AVDD} - \text{PVEE0} \leq 5.5\text{ V}$ , VREF = 1.25 V external voltage reference, ambient temperature ( $T_A$ ) = –40°C to +105°C, unless otherwise noted.

Table 1.

| Parameter <sup>1</sup>                   | Min  | Typ | Max  | Unit                     | Test Conditions/Comments                                                                                                               |
|------------------------------------------|------|-----|------|--------------------------|----------------------------------------------------------------------------------------------------------------------------------------|
| STATIC PERFORMANCE, EXTERNAL $R_{SET}^2$ |      |     |      |                          |                                                                                                                                        |
| Resolution                               | 14   |     |      | Bits                     | VREF = 1.25 V external voltage reference, assumes ideal 2.5 kΩ external $R_{SET}$ resistor, all channels and all output current ranges |
| Relative Accuracy (INL)                  | –6.5 |     | +6.5 | LSB                      |                                                                                                                                        |
| Differential Nonlinearity (DNL)          | –1   |     | +1   | LSB                      | $T_A = -20^\circ\text{C}$ to $+105^\circ\text{C}$ , guaranteed monotonic                                                               |
|                                          | –1   |     | +1.2 | LSB                      | Guaranteed monotonic                                                                                                                   |
| Total Unadjusted Error                   | –1.3 |     | +1.3 | % full-scale range (FSR) |                                                                                                                                        |
| Zero-Scale Error                         |      |     | +600 | μA                       | All 0s loaded into the DAC register                                                                                                    |
| Zero-Scale Error Drift                   |      | 500 |      | nA/°C                    | Channel 0, Channel 1                                                                                                                   |
|                                          |      | 300 |      | nA/°C                    | Channel 2                                                                                                                              |
|                                          |      | 170 |      | nA/°C                    | Channel 3, Channel 4, Channel 5                                                                                                        |
| Offset Error                             | –600 |     | +600 | μA                       |                                                                                                                                        |
| Offset Error Drift                       |      | 1   |      | μA/°C                    | Channel 0, Channel 1                                                                                                                   |
|                                          |      | 0.5 |      | μA/°C                    | Channel 2, Channel 3, Channel 4, Channel 5                                                                                             |
| Full-Scale Error                         | –1.3 |     | +1.3 | % FSR                    | All 1s loaded into the DAC register                                                                                                    |
| Full-Scale Error Drift                   |      | 20  |      | ppm/°C                   | Channel 0, Channel 1                                                                                                                   |
|                                          |      | 50  |      | ppm/°C                   | Channel 2, Channel 3, Channel 4, Channel 5                                                                                             |
| Gain Error                               | –1.3 |     | +1.3 | % FSR                    |                                                                                                                                        |
| Gain Temperature Coefficient             |      | 30  |      | ppm/°C                   | Channel 0, Channel 1                                                                                                                   |
|                                          |      | 80  |      | ppm/°C                   | Channel 2, Channel 3, Channel 4, Channel 5                                                                                             |
| DC Crosstalk                             |      | 2   |      | LSB                      | $T_A = 25^\circ\text{C}$ , due to full-scale change in output current on a single adjacent channel                                     |
| DC Power Supply Rejection Ratio (PSRR)   |      | 17  |      | μA/V                     | $T_A = 25^\circ\text{C}$ , DAC register loaded to full scale                                                                           |
| STATIC PERFORMANCE, INTERNAL $R_{SET}$   |      |     |      |                          |                                                                                                                                        |
| Resolution                               | 14   |     |      | Bits                     | VREF = 1.25 V internal voltage reference, all channels and all output current ranges                                                   |
| Relative Accuracy (INL)                  | –6.5 |     | +6.5 | LSB                      |                                                                                                                                        |
| Differential Nonlinearity (DNL)          | –1   |     | +1   | LSB                      | $T_A = -20^\circ\text{C}$ to $+105^\circ\text{C}$ , guaranteed monotonic                                                               |
|                                          | –1   |     | +1.2 | LSB                      | Guaranteed monotonic                                                                                                                   |
| Total Unadjusted Error (TUE)             | –1.3 |     | +1.3 | % FSR                    |                                                                                                                                        |
| Zero-Scale Error                         |      |     | +600 | μA                       | All 0s loaded into the DAC register                                                                                                    |
| Zero-Scale Error Drift                   |      | 500 |      | nA/°C                    | Channel 0, Channel 1                                                                                                                   |
|                                          |      | 300 |      | nA/°C                    | Channel 2                                                                                                                              |
|                                          |      | 170 |      | nA/°C                    | Channel 3, Channel 4, Channel 5                                                                                                        |
| Offset Error                             | –600 |     | +600 | μA                       |                                                                                                                                        |
| Offset Error Drift                       |      | 1   |      | μA/°C                    | Channel 0, Channel 1                                                                                                                   |
|                                          |      | 0.5 |      | μA/°C                    | Channel 2, Channel 3, Channel 4, Channel 5                                                                                             |
| Full-Scale Error                         | –1.3 |     | +1.3 | % FSR                    | All 1s loaded into the DAC register                                                                                                    |
| Full-Scale Error Drift                   |      | 20  |      | ppm/°C                   | Channel 0, Channel 1                                                                                                                   |
|                                          |      | 50  |      | ppm/°C                   | Channel 2, Channel 3, Channel 4, Channel 5                                                                                             |
| Gain Error                               | –1.3 |     | +1.3 | % FSR                    |                                                                                                                                        |
| Gain Temperature Coefficient             |      | 30  |      | ppm/°C                   | Channel 0, Channel 1                                                                                                                   |
|                                          |      | 80  |      | ppm/°C                   | Channel 2, Channel 3, Channel 4, Channel 5                                                                                             |

| Parameter <sup>1</sup>                     | Min         | Typ  | Max           | Unit   | Test Conditions/Comments                                                                                          |
|--------------------------------------------|-------------|------|---------------|--------|-------------------------------------------------------------------------------------------------------------------|
| DC Crosstalk                               |             | 2    |               | LSB    | T <sub>A</sub> = 25°C, due to 200 mW change in output power on a single channel                                   |
| DC PSRR                                    |             | 17   |               | μA/V   | T <sub>A</sub> = 25°C, DAC register loaded to midscale                                                            |
| <b>OUTPUT CHARACTERISTICS</b>              |             |      |               |        |                                                                                                                   |
| Output Current Ranges                      |             |      |               |        |                                                                                                                   |
| Channel 0                                  | –60         |      | 0             | mA     |                                                                                                                   |
|                                            | –60         |      | +300          | mA     |                                                                                                                   |
|                                            | 0           |      | 300           | mA     |                                                                                                                   |
| Channel 1                                  | 0           |      | 140           | mA     |                                                                                                                   |
|                                            | 0           |      | 250           | mA     |                                                                                                                   |
| Channel 2                                  | 0           |      | 55            | mA     |                                                                                                                   |
|                                            | 0           |      | 150           | mA     |                                                                                                                   |
| Channel 3, Channel 4, Channel 5            | 0           |      | 45            | mA     |                                                                                                                   |
|                                            | 0           |      | 100           | mA     |                                                                                                                   |
| Output Compliance Voltage <sup>3</sup>     |             |      |               |        |                                                                                                                   |
| Channel 0                                  | 0           |      | PVDD0 – 0.45  | V      | When sourcing in the 0 mA to 300 mA range, DAC register is loaded to full scale                                   |
|                                            | PVEE0 + 0.5 |      |               |        | When sinking current on the –60 mA to 0 mA and the –60 mA to +300 mA ranges, DAC register is loaded to zero scale |
| Channel 1                                  | 0           |      | PVDD1 – 0.275 | V      | When configured to the 140 mA range with low headroom, DAC register is loaded to full scale                       |
|                                            | 0           |      | PVDD1 – 0.45  | V      | When configured to the 250 mA range or to the 140 mA range with low noise, DAC register is loaded to full scale   |
| Channel 2, Channel 3, Channel 4, Channel 5 | 0           |      | PVDDx – 0.275 | V      | All output ranges, DAC register loaded to full scale                                                              |
| DC Output Impedance                        |             | 600  |               | kΩ     | T <sub>A</sub> = 25°C                                                                                             |
| <b>VOLTAGE REFERENCE INPUT</b>             |             |      |               |        |                                                                                                                   |
| Reference Input Impedance                  |             | 60   |               | GΩ     | T <sub>A</sub> = 25°C, external 1.25 V reference option                                                           |
|                                            |             | 115  |               | kΩ     | T <sub>A</sub> = 25°C, external 2.5 V reference option                                                            |
| Reference Input Range                      |             | 1.25 |               | V      | For specified performance, external 1.25 V reference option                                                       |
|                                            |             | 2.5  |               | V      | External 2.5 V reference option                                                                                   |
| <b>VOLTAGE REFERENCE OUTPUT</b>            |             |      |               |        |                                                                                                                   |
| Output Voltage                             | 1.245       | 1.25 | 1.255         | V      | T <sub>A</sub> = 25°C, reference output on Internal R <sub>SET</sub> resistor                                     |
| Reference Temperature Coefficient          |             | 15   |               | ppm/°C |                                                                                                                   |
| Output Impedance                           |             | 0.01 |               | Ω      |                                                                                                                   |
| Output Current Load Capability             |             | ±5   |               | mA     |                                                                                                                   |
| Maximum Capacitive Load                    |             | 10   |               | μF     |                                                                                                                   |
| Load Regulation Sourcing                   |             | 250  |               | μV/mA  |                                                                                                                   |
| Load Regulation Sinking                    |             | 250  |               | μV/mA  |                                                                                                                   |
| Output Voltage Noise                       |             | 920  |               | nV rms | T <sub>A</sub> = 25°C, 0.1 Hz to 10 Hz                                                                            |
| Output Voltage Noise Spectral Density      |             | 70   |               | nV/√Hz | T <sub>A</sub> = 25°C, 1 kHz                                                                                      |
|                                            |             | 70   |               | nV/√Hz | T <sub>A</sub> = 25°C, 10 kHz                                                                                     |
| Line Regulation                            |             | 35   |               | μV/V   | T <sub>A</sub> = 25°C, due to change in AVDD                                                                      |
| <b>INTEGRATED MULTIPLEXER</b>              |             |      |               |        |                                                                                                                   |
| Buffer Output Current                      |             | ±8   |               | mA     |                                                                                                                   |
| Buffer Output Impedance                    |             | 0.5  |               | Ω      |                                                                                                                   |
| Buffer Offset                              |             | 0.3  |               | mV     |                                                                                                                   |
| Buffer Maximum Capacitive Load             |             | 100  |               | pF     |                                                                                                                   |

| Parameter <sup>1</sup>             | Min                | Typ  | Max                | Unit           | Test Conditions/Comments                                                  |
|------------------------------------|--------------------|------|--------------------|----------------|---------------------------------------------------------------------------|
| LOGIC INPUTS                       |                    |      |                    |                | $\overline{CS}$ , $SCLK$ , $SDI$ , $LDAC$ , $\overline{RESET}$            |
| Input Current                      | –3.5               |      | +3.5               | $\mu A$        | Per pin                                                                   |
| Input Voltage                      |                    |      |                    |                |                                                                           |
| Input Low Voltage ( $V_{INL}$ )    |                    |      | $0.3 \times IOVDD$ | V              |                                                                           |
| Input High Voltage ( $V_{INH}$ )   | $0.7 \times IOVDD$ |      |                    | V              |                                                                           |
| Pin Capacitance                    |                    | 4.5  |                    | pF             | Per pin                                                                   |
| LOGIC OUTPUTS                      |                    |      |                    |                |                                                                           |
| SDO Pin                            |                    |      |                    |                |                                                                           |
| Output Low Voltage ( $V_{OL}$ )    |                    |      | 0.4                | V              |                                                                           |
| Output High Voltage ( $V_{OH}$ )   | $IOVDD - 0.4$      |      |                    | V              |                                                                           |
| Floating State Output Capacitance  |                    | 4    |                    | pF             |                                                                           |
| ALARM Pin                          |                    |      |                    |                |                                                                           |
| Output Low Voltage ( $V_{OL}$ )    |                    |      | 0.4                | V              | Open-drain enabled <sup>4</sup> , 10 k $\Omega$ pull-up resistor to IOVDD |
| Output High Voltage ( $V_{OH}$ )   | $IOVDD - 0.4$      |      |                    | V              | Open-drain enabled <sup>4</sup> , 10 k $\Omega$ pull-up resistor to IOVDD |
| TEMPERATURE MEASUREMENT DIODE      |                    |      |                    |                |                                                                           |
| Diode Output Voltage               |                    | 700  |                    | mV             | $T_A = 25^\circ C$ , internal bias current                                |
|                                    |                    | 880  |                    | mV             | $T_A = 25^\circ C$ , 100 $\mu A$ external bias current                    |
|                                    |                    | 1.04 |                    | V              | $T_A = 25^\circ C$ , 200 $\mu A$ external bias current                    |
| Temperature Coefficient            |                    | –1.8 |                    | mV/ $^\circ C$ | Internal bias current                                                     |
|                                    |                    | –1.3 |                    | mV/ $^\circ C$ | 100 $\mu A$ external bias current                                         |
|                                    |                    | –0.9 |                    | mV/ $^\circ C$ | 200 $\mu A$ external bias current                                         |
| External Bias Current <sup>5</sup> | 100                |      | 200                | $\mu A$        | Temperature diode bias current is supplied externally                     |
| THERMAL ALARMS                     |                    |      |                    |                |                                                                           |
| Overheat Warning Temperature       |                    | 125  |                    | $^\circ C$     | Junction temperature, warning flag activated                              |
| Overheat Shutdown Temperature      |                    | 150  |                    | $^\circ C$     | Junction temperature, thermal shutdown                                    |
| Overheat Warning Hysteresis        |                    | 4    |                    | $^\circ C$     |                                                                           |
| Overheat Shutdown Hysteresis       |                    | 20   |                    | $^\circ C$     |                                                                           |
| POWER REQUIREMENTS                 |                    |      |                    |                |                                                                           |
| Analog Power Supply Voltage        |                    |      |                    |                |                                                                           |
| AVDD                               | 2.9                |      | 5.5                | V              | AVDD must be equal to DVDD                                                |
| AVEE                               | –3.0               |      | 0                  | V              |                                                                           |
| PVDD0 to PVDD5                     | 0.8                |      | $AVDD - 0.4$       | V              | $2.5 V \leq PVDD - AVEE \leq 5.5 V$                                       |
| PVEE0                              | AVEE               |      | 0                  | V              | $AVDD - PVEE0 \leq 5.5 V$                                                 |
| Analog Power Supply Current        |                    |      |                    |                |                                                                           |
| AVDD Supply Current                |                    | 32   |                    | mA             | Internal voltage reference option selected                                |
| AVEE Supply Current                |                    | –16  |                    | mA             |                                                                           |
| PVDD0 to PVDD5 Supply Current      |                    | 125  |                    | $\mu A$        |                                                                           |
| Digital Power Supply Voltage       |                    |      |                    |                |                                                                           |
| DVDD                               | 2.9                |      | 5.5                | V              | AVDD must be equal to DVDD                                                |
| IOVDD                              | 1.65               |      | 5.5                | V              |                                                                           |

| Parameter <sup>1</sup>       | Min | Typ | Max | Unit | Test Conditions/Comments             |
|------------------------------|-----|-----|-----|------|--------------------------------------|
| Digital Power Supply Current |     |     |     |      |                                      |
| DVDD Supply Current          |     | 1.1 |     | mA   |                                      |
| IODVDD Supply Current        |     | 200 |     | nA   |                                      |
| Power Consumption            |     | 110 |     | mW   | All outputs at 0 A, nominal supplies |

<sup>1</sup> See the Terminology section.

<sup>2</sup> See the Precision R<sub>SET</sub> Resistor section for more information about the internal and external R<sub>SET</sub> resistors.

<sup>3</sup> When sourcing current, the output compliance voltage is the maximum voltage at the IDACx pin, for which the output current is within 0.1% of the measured full-scale range. When sinking current on Channel 0, the output compliance voltage is the minimum voltage at the IDAC0 pin, for which the output current is within 0.1% of the measured zero-scale current.

<sup>4</sup> The active low  $\overline{\text{ALARM}}$  pin can be configured as an open drain. Refer to the  $\overline{\text{ALARM}}$  section.

<sup>5</sup> The internal temperature sensing diode can be biased with an internal or external current. Refer to the Internal Die Temperature Monitoring section.

## AC PERFORMANCE CHARACTERISTICS

AVDD = DVDD = 2.9 V to 5.5 V, PVDD = 0.8 V to AVDD – 0.4 V, AVEE = –3.0 V to 0 V, 2.5 V ≤ PVDD – AVEE ≤ 5.5 V,  
IOVDD = 1.65 V to 5.5 V, AVEE ≤ PVEE0 ≤ 0 V, AVDD – PVEE0 ≤ 5.5 V, VREF = 1.25 V external voltage reference, T<sub>A</sub> = 25°C, unless  
otherwise noted.

Table 2.

| Parameter <sup>1</sup>              | Min | Typ   | Max | Unit   | Test Conditions/Comments <sup>2</sup>                                                                      |
|-------------------------------------|-----|-------|-----|--------|------------------------------------------------------------------------------------------------------------|
| DYNAMIC PERFORMANCE                 |     |       |     |        |                                                                                                            |
| Output Current Settling Time        |     | 13    |     | μs     | Zero-scale to full-scale step settling to ±4 LSB, 0 mA to 300 mA range                                     |
|                                     |     | 10    |     | μs     | Zero-scale to full-scale step settling to ±4 LSB, 0 mA to 45 mA range, Channel 3, Channel 4, and Channel 5 |
| Slew Rate                           |     | 50    |     | mA/μs  | Channel 0, 0 mA to 300 mA range                                                                            |
|                                     |     | 10    |     | mA/μs  | Channel 3, Channel 4, Channel 5, 0 mA to 45 mA range                                                       |
| Digital-to-Analog Glitch Impulse    |     | 0.057 |     | nA-sec | 1 LSB change around major carry                                                                            |
| Multiplexer Switching Glitch        |     | 14    |     | pA-sec | Switching monitored channel                                                                                |
| Digital Feedthrough                 |     | 0.03  |     | nA-sec |                                                                                                            |
| Digital Crosstalk                   |     | 0.03  |     | nA-sec |                                                                                                            |
| DAC-to-DAC Crosstalk                |     | 0.8   |     | nA-sec | Victim Channel 4, due to a 300 mA step change on Channel 0                                                 |
| Output Noise Spectral Density (NSD) |     | 35    |     | nA/√Hz | Channel 0, 0 mA to 300 mA range, at 1 kHz, DAC register loaded to midscale                                 |
|                                     |     | 18    |     | nA/√Hz | Channel 1, 0 mA to 140 mA low noise range, at 1 kHz, DAC register loaded to midscale                       |
|                                     |     | 19    |     | nA/√Hz | Channel 2, 0 mA to 150 mA range, at 1 kHz, DAC register loaded to midscale                                 |
|                                     |     | 13    |     | nA/√Hz | Channel 3, Channel 4, Channel 5, 0 mA to 100 mA range, at 1 kHz, DAC register loaded to midscale           |
|                                     |     | 16    |     | nA/√Hz | Channel 0, 0 mA to 300 mA range, at 10 kHz, DAC register loaded to midscale                                |
|                                     |     | 9     |     | nA/√Hz | Channel 1, 0 mA to 140 mA low noise range, at 10 kHz, DAC register loaded to midscale                      |
|                                     |     | 9     |     | nA/√Hz | Channel 2, 0 mA to 150 mA range, at 10 kHz, DAC register loaded to midscale                                |
|                                     |     | 6     |     | nA/√Hz | Channel 3, Channel 4, Channel 5, 0 mA to 100 mA range, at 10 kHz, DAC register loaded to midscale          |

| Parameter <sup>1</sup> | Min | Typ | Max | Unit   | Test Conditions/Comments <sup>2</sup>                                                                     |
|------------------------|-----|-----|-----|--------|-----------------------------------------------------------------------------------------------------------|
| Output Noise           |     | 900 |     | nA rms | 0.1 Hz to 10 Hz, Channel 0, 0 mA to 300 mA range, DAC register loaded to full scale                       |
|                        |     | 180 |     | nA rms | 0.1 Hz to 10 Hz, Channel 1, 0 mA to 140 mA low noise range, DAC register loaded to full scale             |
|                        |     | 400 |     | nA rms | 0.1 Hz to 10 Hz, Channel 2, 0 mA to 150 mA range, DAC register loaded to full scale                       |
|                        |     | 300 |     | nA rms | 0.1 Hz to 10 Hz, Channel 3, Channel 4, Channel 5, 0 mA to 100 mA range, DAC register loaded to full scale |
| PVDDx AC PSRR          |     | −98 |     | dB     | 100 Hz                                                                                                    |
|                        |     | −87 |     | dB     | 1 kHz                                                                                                     |
|                        |     | −67 |     | dB     | 10 kHz                                                                                                    |
|                        |     | −23 |     | dB     | 1000 kHz                                                                                                  |
|                        |     | −8  |     | dB     | 3000 kHz                                                                                                  |

<sup>1</sup> See the Terminology section.

<sup>2</sup> Temperature range is −40°C to +105°C, typically at 25°C.

## TIMING SPECIFICATIONS

Table 3.

| Parameter                   | 1.65 V ≤ IOVDD ≤ 5.5 V | Unit   | Test Conditions/Comments                                                     |
|-----------------------------|------------------------|--------|------------------------------------------------------------------------------|
| t <sub>1</sub>              | 50                     | ns min | SCLK cycle time, write operation.                                            |
|                             | 100                    | ns min | SCLK cycle time, read operation.                                             |
| t <sub>2</sub>              | 20                     | ns min | SCLK high time.                                                              |
| t <sub>3</sub>              | 20                     | ns min | SCLK low time.                                                               |
| t <sub>4</sub>              | 25                     | ns min | $\overline{\text{CS}}$ to SCLK rising edge setup time.                       |
| t <sub>5</sub>              | 10                     | ns min | Data setup time.                                                             |
| t <sub>6</sub>              | 10                     | ns min | Data hold time.                                                              |
| t <sub>7</sub>              | 0                      | ns min | SCLK rising edge to $\overline{\text{CS}}$ rising edge. LDAC idle high mode. |
| t <sub>7</sub> <sup>1</sup> | 250                    | ns min | SCLK rising edge to $\overline{\text{CS}}$ rising edge. LDAC idle low mode.  |
| t <sub>8</sub>              | 30                     | ns min | $\overline{\text{CS}}$ high time.                                            |
| t <sub>9</sub>              | 40                     | ns min | $\overline{\text{CS}}$ rising edge to SCLK rising edge.                      |
| t <sub>10</sub>             | 5                      | ns min | SCLK rising edge to $\overline{\text{CS}}$ falling edge.                     |
| t <sub>11</sub>             | 90                     | ns max | SDO data valid from SCLK falling edge.                                       |
| t <sub>12</sub>             | 40                     | ns min | $\overline{\text{CS}}$ rising edge to SDO disabled.                          |
| t <sub>13</sub>             | 100                    | ns min | $\overline{\text{LDAC}}$ pulse width low.                                    |
| t <sub>14</sub>             | 10                     | ns min | $\overline{\text{LDAC}}$ falling edge to $\overline{\text{CS}}$ rising edge. |
| t <sub>15</sub>             | 100                    | ns min | SCLK rising edge to $\overline{\text{LDAC}}$ falling edge.                   |
| t <sub>16</sub>             | 10                     | ns min | $\overline{\text{RESET}}$ minimum pulse width low.                           |
| t <sub>17</sub>             | 100                    | ns max | $\overline{\text{RESET}}$ pulse activation time.                             |

<sup>1</sup> t<sub>7</sub> ≥ 250 ns only applies to the first SCLK rising edge to  $\overline{\text{CS}}$  rising edge after  $\overline{\text{LDAC}}$  (IDLE LOW) falling edge. t<sub>7</sub> ≥ 0 ns applies for all other SCLK rising edge to  $\overline{\text{CS}}$  rising edge. Refer to Figure 3.

Table 4. LDAC Idle Low Timing

| Parameter      | 1.65 V ≤ IOVDD ≤ 5.5 V | Unit   | Test Conditions/Comments                                                                                                                                                       |
|----------------|------------------------|--------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| t <sub>1</sub> | 250                    | ns min | SCLK rising edge to $\overline{\text{CS}}$ rising edge. The first SCLK rising edge to $\overline{\text{CS}}$ rising edge after $\overline{\text{LDAC}}$ idle low falling edge. |
| t <sub>2</sub> | 0                      | ns min | SCLK rising edge to $\overline{\text{CS}}$ rising edge.                                                                                                                        |
| t <sub>3</sub> | 10                     | ns min | $\overline{\text{LDAC}}$ falling edge to $\overline{\text{CS}}$ rising edge.                                                                                                   |

TIMING DIAGRAMS

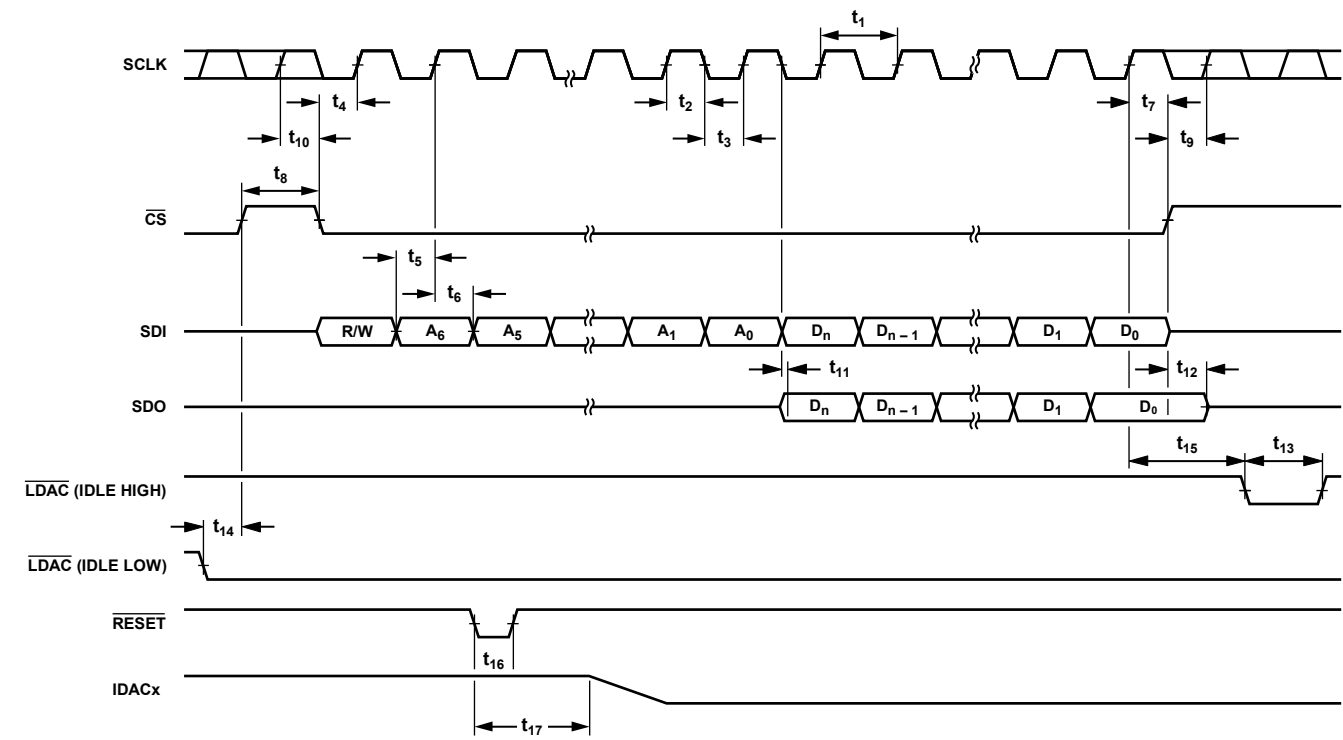


Figure 2. Timing Diagram (Not to Scale)

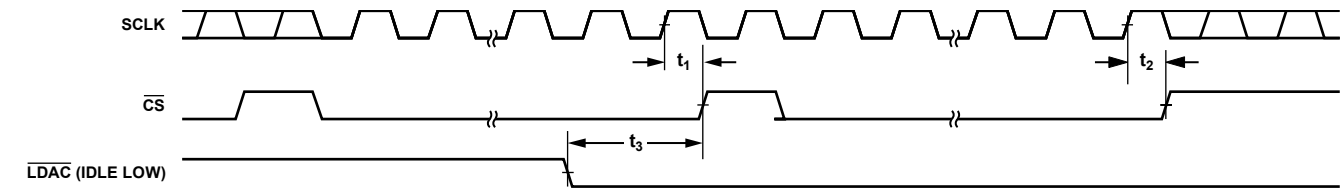


Figure 3. LDAC Idle Low Timing Diagram

## ABSOLUTE MAXIMUM RATINGS

T<sub>A</sub> = 25°C, unless otherwise noted

Table 5.

| Parameter                                       | Rating                                                |
|-------------------------------------------------|-------------------------------------------------------|
| AVDD to DVDD                                    | −0.3 V to +0.3 V                                      |
| AVDD to AGND                                    | −0.3 V to +6.5 V                                      |
| AVDD to PVDDx                                   | −0.3 V to +6.5 V                                      |
| AVDD to AVEE                                    | −0.3 V to +10 V                                       |
| AVEE to AGND                                    | +0.3 V to −3.5 V                                      |
| PVEE0 to AGND                                   | +0.3 V to −3.5 V                                      |
| AVEE to PVEE0                                   | −3.0 V to +0.3 V                                      |
| PVDDx to AGND                                   | −0.3 V to +6.5 V                                      |
| PVDDx to AVEE                                   | −0.3 V to +8.5 V                                      |
| AVDD to PVEE0                                   | −0.3 V to +6.5 V                                      |
| VREF_IO to AGND                                 | −0.3 V to AVDD + 0.3 V                                |
| IDAC0 to PVEE0                                  | −0.3 V to +6.5 V                                      |
| IDAC1 through IDAC5 to AGND                     | −0.3 V to PVDDx + 0.3 V                               |
| DVDD to DGND                                    | −0.3 V to +6.5 V                                      |
| IOVDD to DGND                                   | −0.3 V to +6.5 V                                      |
| REFGND to AGND                                  | −0.3 V to +0.3 V                                      |
| AGND to DGND                                    | −0.3 V to +0.3 V                                      |
| Digital Inputs to DGND <sup>1</sup>             | −0.3 V to IOVDD + 0.3 V                               |
| Digital Outputs to DGND <sup>2</sup>            | −0.3 V to IOVDD + 0.3 V                               |
| Operating Temperature Range                     | −40°C to +105°C                                       |
| Storage Temperature Range                       | −65°C to +150°C                                       |
| Maximum Junction Temperature, T <sub>JMAX</sub> | 150°C                                                 |
| Power Dissipation                               | (T <sub>JMAX</sub> − T <sub>A</sub> )/θ <sub>JA</sub> |
| Lead Temperature, Soldering Reflow              | 260°C, as per JEDEC J-STD-020                         |

<sup>1</sup> Digital inputs include SCLK, SDI,  $\overline{\text{RESET}}$ , and  $\overline{\text{LDAC}}$ .

<sup>2</sup> Digital outputs include SDO and  $\overline{\text{ALARM}}$

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

## THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ<sub>JA</sub> is the natural convection junction to ambient thermal resistance measured in a one cubic foot sealed enclosure.

Table 6. Thermal Resistance

| Package Type | θ <sub>JA</sub> | Unit |
|--------------|-----------------|------|
| CB-49-5      | 30 <sup>1</sup> | °C/W |

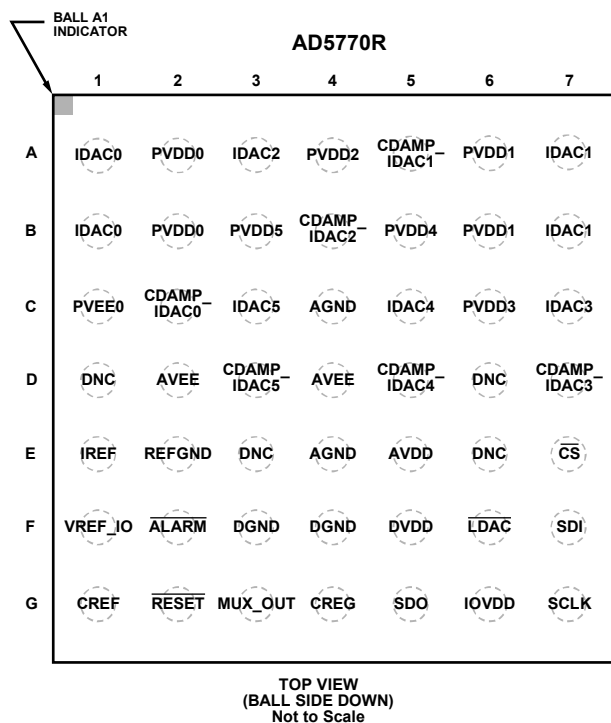
<sup>1</sup> Thermal impedance simulated values are based on JEDEC 2S2P thermal test board with 16 thermal vias. See JEDEC JESD51.

## ESD CAUTION



**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

## PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



## NOTES

1. DNC = DO NOT CONNECT. DO NOT CONNECT TO THESE PINS.

16128-004

Figure 4. Pin Configuration

Table 7. Pin Function Descriptions

| Pin No.        | Mnemonic    | Type <sup>1</sup> | Description                                                                                                                              |
|----------------|-------------|-------------------|------------------------------------------------------------------------------------------------------------------------------------------|
| A1, B1         | IDAC0       | AO                | Current Output of Channel 0 is Available on this Pin. Channel 0 sinks up to 60 mA and sources up to 300 mA.                              |
| A2, B2         | PVDD0       | S                 | Power Supply for IDAC0.                                                                                                                  |
| A3             | IDAC2       | AO                | Current Output of Channel 2 is Available on this Pin. Channel 2 sources up to 150 mA.                                                    |
| A4             | PVDD2       | S                 | Power Supply for IDAC2.                                                                                                                  |
| A5             | CDAMP_IDAC1 | AI                | Damping Capacitor for IDAC1. Connect a 10 nF capacitor between this pin and the PVDD1 supply.                                            |
| A6, B6         | PVDD1       | S                 | Power Supply for IDAC1.                                                                                                                  |
| A7, B7         | IDAC1       | AO                | Current Output of Channel 1 is Available on this Pin. Channel 1 sources up to 250 mA.                                                    |
| B3             | PVDD5       | S                 | Power Supply for IDAC5.                                                                                                                  |
| B4             | CDAMP_IDAC2 | AI                | Damping Capacitor for IDAC2. Connect a 10 nF capacitor between this pin and the PVDD2 supply.                                            |
| B5             | PVDD4       | S                 | Power Supply for IDAC4.                                                                                                                  |
| C1             | PVEE0       | S                 | Power Supply Return for IDAC0 Sink. When sinking this current on Channel 0, up to 60 mA flows out of PVEE0.                              |
| C2             | CDAMP_IDAC0 | AI                | Damping Capacitor for IDAC0. Connect a 10 nF capacitor between this pin and the PVDD0 supply.                                            |
| C3             | IDAC5       | AO                | Current Output of Channel 5 is Available on this Pin. Channel 5 sources up to 100 mA.                                                    |
| C4, E4         | AGND        | S                 | Analog Supply Ground Pin.                                                                                                                |
| C5             | IDAC4       | AO                | Current Output of Channel 4 is Available on this Pin. Channel 4 sources up to 100 mA.                                                    |
| C6             | PVDD3       | S                 | Power Supply for IDAC3.                                                                                                                  |
| C7             | IDAC3       | AO                | Current Output of Channel 3 is Available on this Pin. Channel 3 sources up to 100 mA.                                                    |
| D1, D6, E3, E6 | DNC         | DNC               | Do Not Connect. Do not connect to this pin.                                                                                              |
| D2, D4         | AVEE        | S                 | Negative Power Supply. AVEE must be between -3 V and 0 V. This pin supplies the low side voltage for biasing some analog circuit blocks. |
| D3             | CDAMP_IDAC5 | AI                | Damping Capacitor for IDAC5. Connect a 10 nF capacitor between this pin and the PVDD5 supply.                                            |
| D5             | CDAMP_IDAC4 | AI                | Damping Capacitor for IDAC4. Connect a 10 nF capacitor between this pin and the PVDD4 supply.                                            |
| D7             | CDAMP_IDAC3 | AI                | Damping Capacitor for IDAC3. Connect a 10 nF capacitor between this pin and the PVDD3 supply.                                            |

| Pin No. | Mnemonic           | Type <sup>1</sup> | Description                                                                                                                                                                                                                                                                                          |
|---------|--------------------|-------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| E1      | IREF               | AI/O              | External Resistor Pin for Reference Current Generation (Optional). When using an external $R_{SET}$ resistor, connect this pin directly to REFGND via a low drift, 2.5 k $\Omega$ external resistor.                                                                                                 |
| E2      | REFGND             | S                 | Reference Supply Ground Pin. Connect this pin with a low impedance path to AGND. If using an external resistor, the low side of the $R_{SET}$ resistor must be connected to REFGND before the connection to AGND.                                                                                    |
| E5      | AVDD               | S                 | Analog Power Supply. AVDD must be between 2.9 V and 5.5 V. This pin supplies power to the analog circuit blocks on the device. This pin must be at the same potential as DVDD.                                                                                                                       |
| E7      | $\overline{CS}$    | DI                | Active Low Control Input. $\overline{CS}$ is used to frame data during a SPI transaction. When $\overline{CS}$ is low, data is transferred on the rising edges of SCLK.                                                                                                                              |
| F1      | VREF_IO            | AI/O              | Voltage Reference Input/Output. When the internal reference is enabled, the buffered 1.25 V reference voltage can be made available on this pin. When the internal reference is disabled, an external reference must be applied to this pin. The external reference voltage must be 1.25 V or 2.5 V. |
| F2      | $\overline{ALARM}$ | DO                | Active Low Output. When $\overline{ALARM}$ goes low, this alerts the user of a change in the status register. User must read the status register to deassert this pin.                                                                                                                               |
| F3, F4  | DGND               | S                 | Digital Power Supply Ground.                                                                                                                                                                                                                                                                         |
| F5      | DVDD               | S                 | Digital Power Supply. DVDD must be between 2.9 V and 5.5 V. This pin supplies power to the digital core and internal oscillator blocks on the device. This pin must be at the same potential as AVDD.                                                                                                |
| F6      | $\overline{LDAC}$  | DI                | Logic Input. Pulsing this pin low allows any or all DAC registers to be updated if the input registers have new data, allowing any or all DAC outputs to update synchronously. Alternatively, this pin can be tied low.                                                                              |
| F7      | SDI                | DI                | Serial Data Input. Data to be written to the device is provided on this input and is clocked into the register on the rising edge of SCLK.                                                                                                                                                           |
| G1      | CREF               | AI/O              | Filter Capacitor for Voltage Reference. A 0.1 $\mu$ F capacitor connected from the CREF pin to AGND is recommended to achieve the specified performance from the AD5770R.                                                                                                                            |
| G2      | $\overline{RESET}$ | DI                | Active Low Reset Input. Tie this pin high for normal operation. Asserting this pin low resets the AD5770R to the default configuration.                                                                                                                                                              |
| G3      | MUX_OUT            | AI/O              | Analog Output. An external analog-to-digital converter (ADC) reads voltages on this pin for diagnostic purposes. Use external excitation current for the temperature sensing diode and force the current on this pin.                                                                                |
| G4      | CREG               | AI/O              | Filter Capacitor for Internal Regulator. A 1 $\mu$ F capacitor connected from the CREG pin to AGND is recommended to achieve the specified performance from the AD5770R.                                                                                                                             |
| G5      | SDO                | DO                | Serial Data Output. A read back operation provides data on this output pin as a serial data stream. Data is clocked out on the falling edge of SCLK and is valid on the rising edge of SCLK.                                                                                                         |
| G6      | IOVDD              | S                 | Logic Power Supply. IOVDD must be between 1.65 V and 5.5 V. This pin supplies power to the serial interface circuit blocks on the device.                                                                                                                                                            |
| G7      | SCLK               | DI                | Serial Clock Input. Data is clocked into the input shift register on the rising edge of the serial clock input. Data can be transferred at rates up to 20 MHz when writing to the AD5770R. This pin has a maximum speed of 10 MHz when performing a read operation from the AD5770R.                 |

<sup>1</sup> AO is analog output, S is power, AI is analog input, DNC is do not connect, AI/O is analog input and output, DI is digital input, and DO is digital output.

## TYPICAL PERFORMANCE CHARACTERISTICS

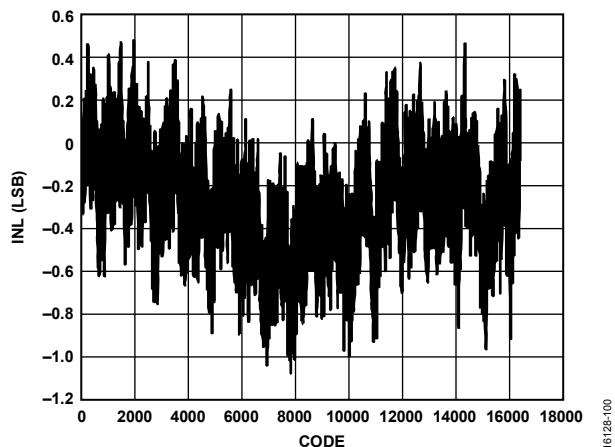


Figure 5. INL Error vs. DAC Code (Channel 0, 0 mA to 300 mA Range)

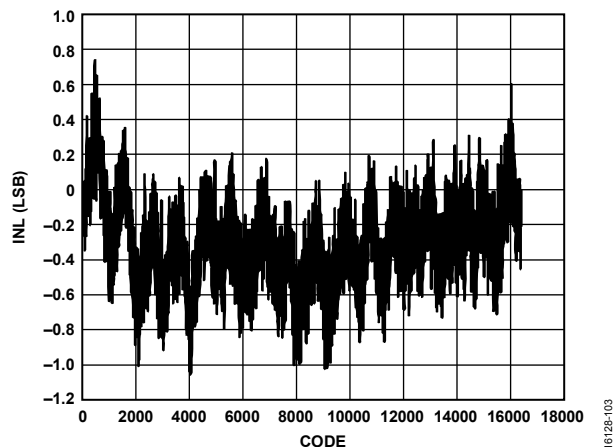


Figure 8. INL Error vs. DAC Code (Channel 3, 0 mA to 100 mA Range)

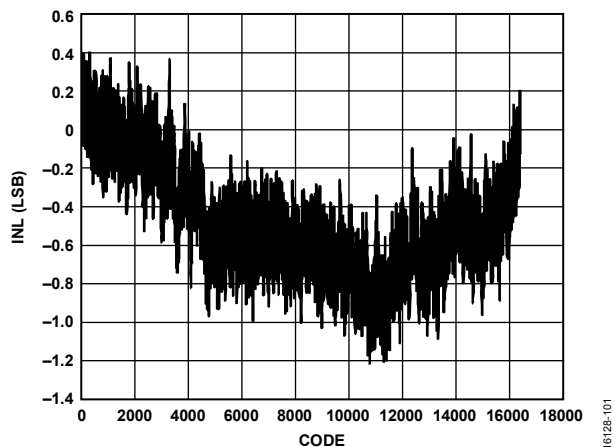


Figure 6. INL Error vs. DAC Code (Channel 1, 0 mA to 250 mA Range)

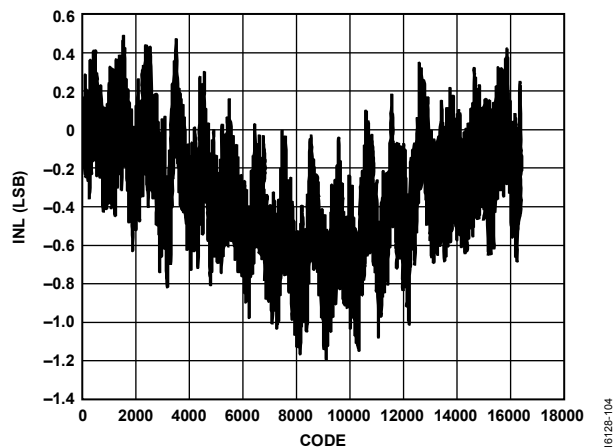


Figure 9. INL Error vs. DAC Code (Channel 4, 0 mA to 100 mA Range)

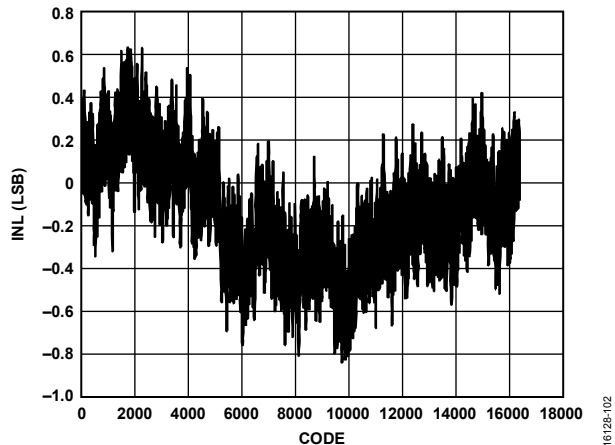


Figure 7. INL Error vs. DAC Code (Channel 2, 0 mA to 150 mA Range)

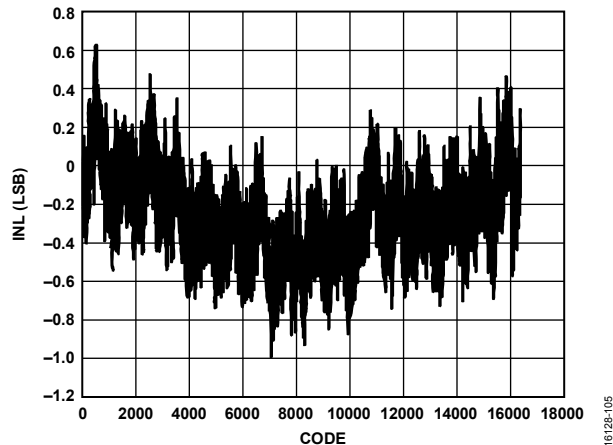


Figure 10. INL Error vs. DAC Code (Channel 5, 0 mA to 100 mA Range)

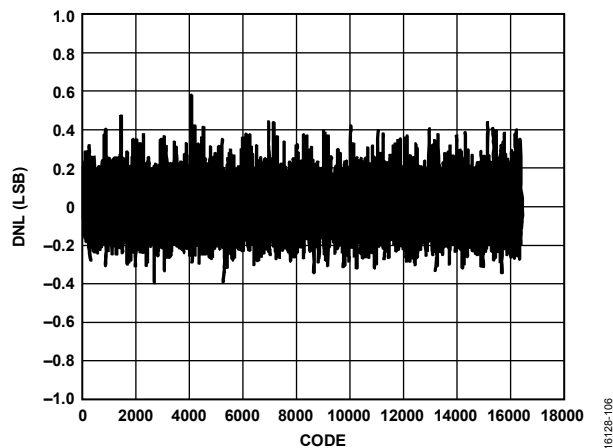


Figure 11. DNL Error vs. DAC Code (Channel 0, 0 mA to 300 mA Range)

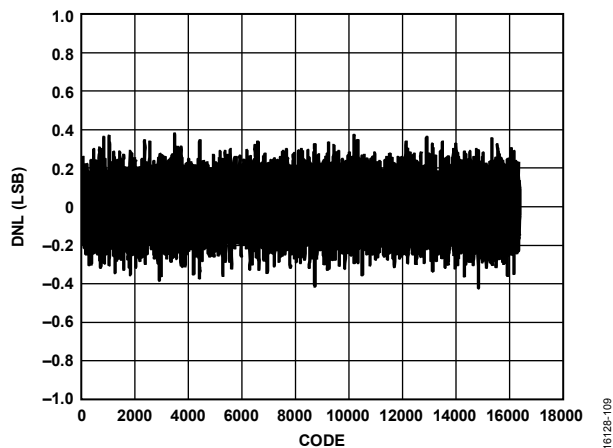


Figure 14. DNL Error vs. DAC Code (Channel 3, 0 mA to 100 mA Range)

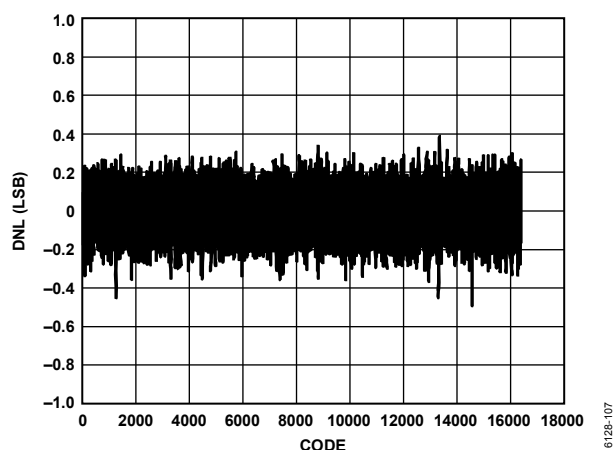


Figure 12. DNL Error vs. DAC Code (Channel 1, 0 mA to 250 mA Range)

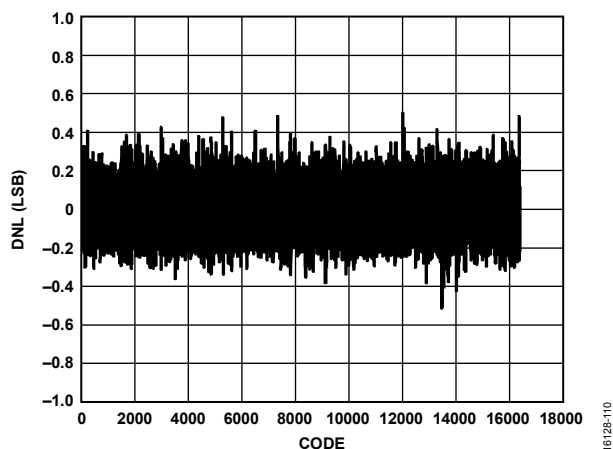


Figure 15. DNL Error vs. DAC Code (Channel 4, 0 mA to 100 mA Range)

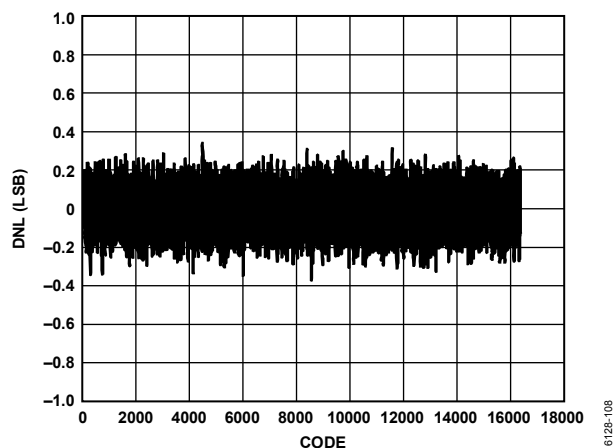


Figure 13. DNL Error vs. DAC Code (Channel 2, 0 mA to 150 mA Range)

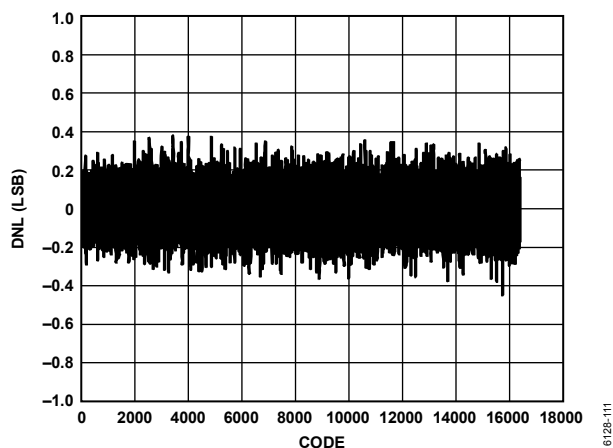


Figure 16. DNL Error vs. DAC Code (Channel 5, 0 mA to 100 mA Range)

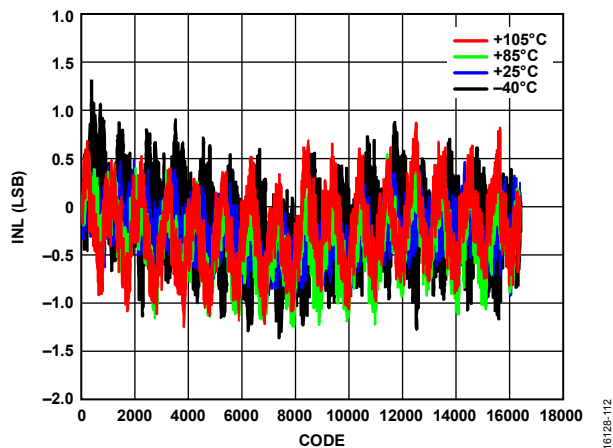


Figure 17. INL Error vs. DAC Code for Various Temperatures (Channel 0, 0 mA to 300 mA Range)

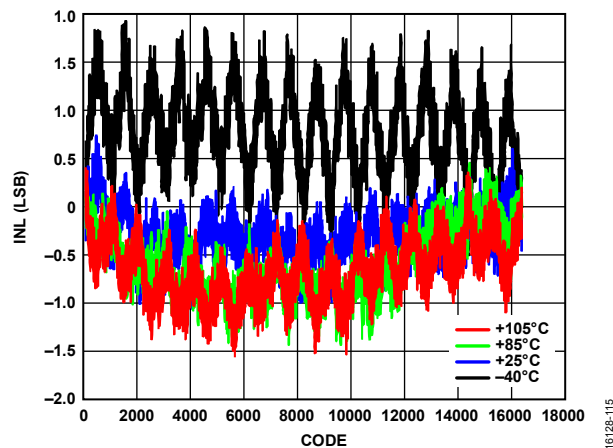


Figure 20. INL Error vs. DAC Code for Various Temperatures (Channel 3, 0 mA to 100 mA Range)

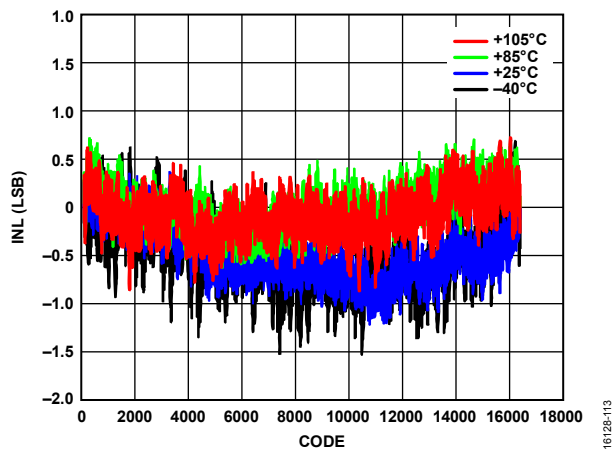


Figure 18. INL Error vs. DAC Code for Various Temperatures (Channel 1, 0 mA to 250 mA Range)

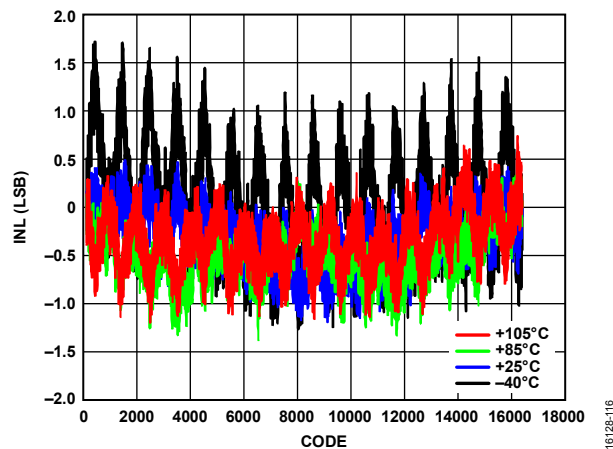


Figure 21. INL Error vs. DAC Code for Various Temperatures (Channel 4, 0 mA to 100 mA Range)

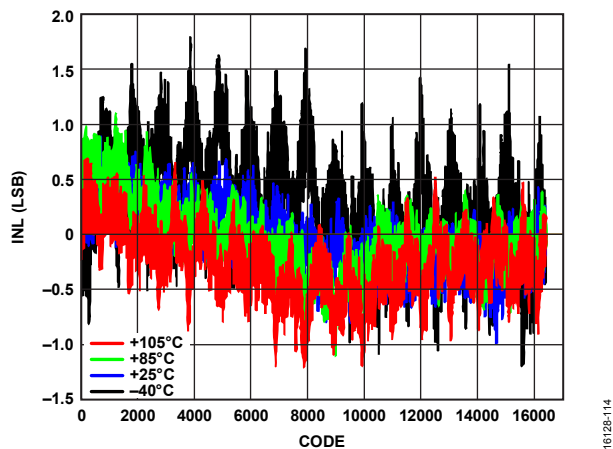


Figure 19. INL Error vs. DAC Code for Various Temperatures (Channel 2, 0 mA to 150 mA Range)

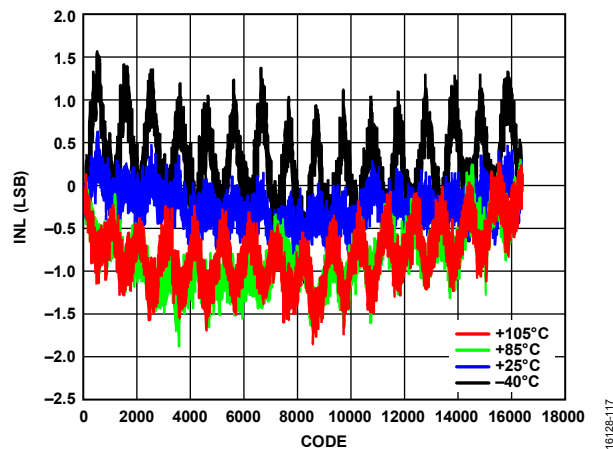


Figure 22. INL Error vs. DAC Code for Various Temperatures (Channel 5, 0 mA to 100 mA Range)

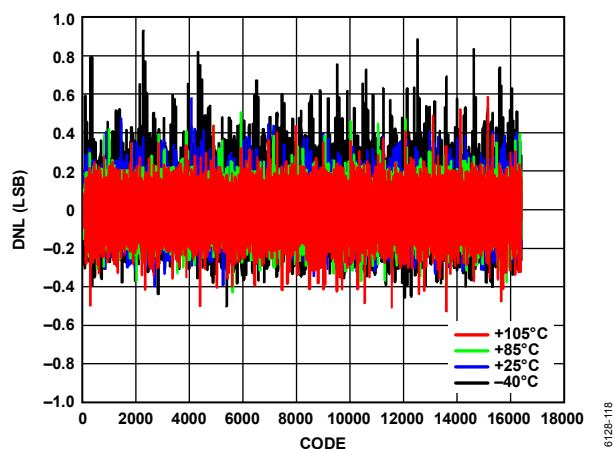


Figure 23. DNL Error vs. DAC Code for Various Temperatures (Channel 0, 0 mA to 300 mA Range)

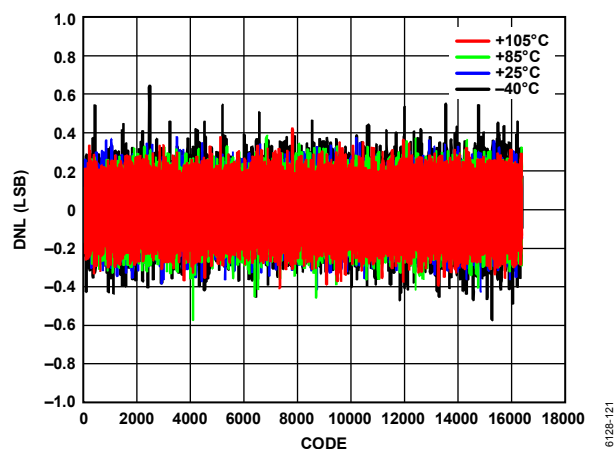


Figure 26. DNL Error vs. DAC Code for Various Temperatures (Channel 3, 0 mA to 100 mA Range)

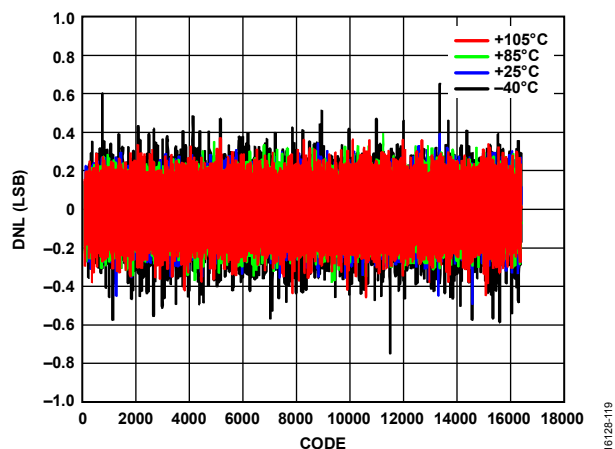


Figure 24. DNL Error vs. DAC Code for Various Temperatures (Channel 1, 0 mA to 250 mA Range)

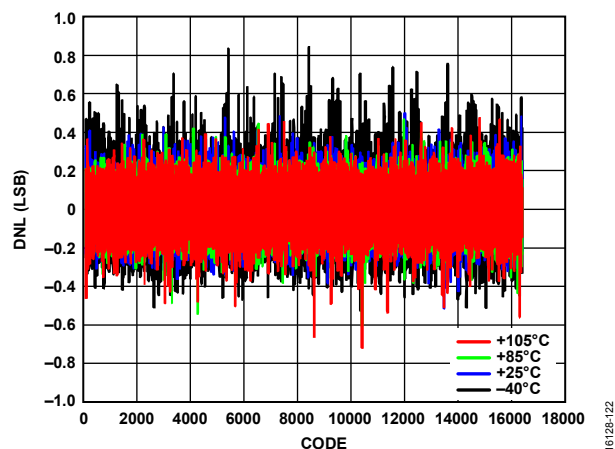


Figure 27. DNL Error vs. DAC Code for Various Temperatures (Channel 4, 0 mA to 100 mA Range)

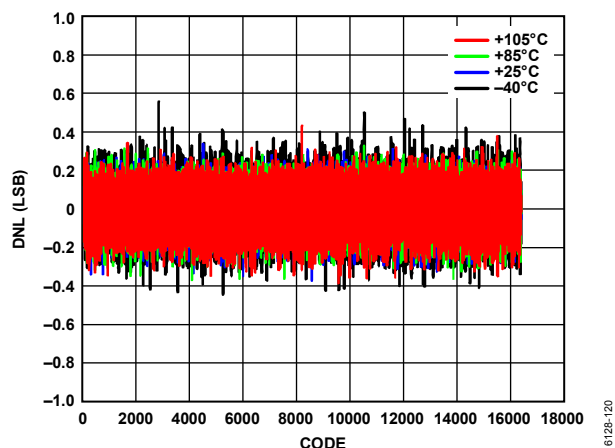


Figure 25. DNL Error vs. DAC Code for Various Temperatures (Channel 2, 0 mA to 150 mA Range)

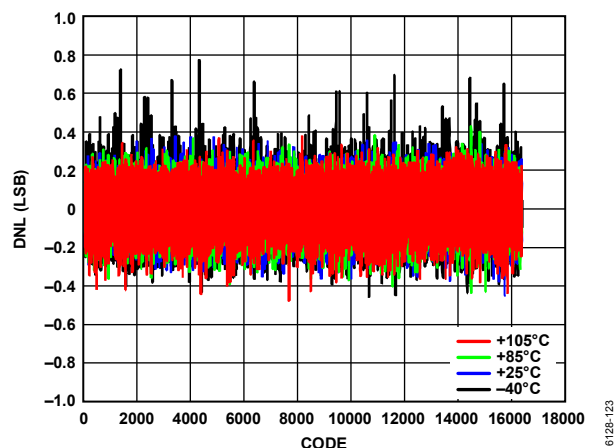
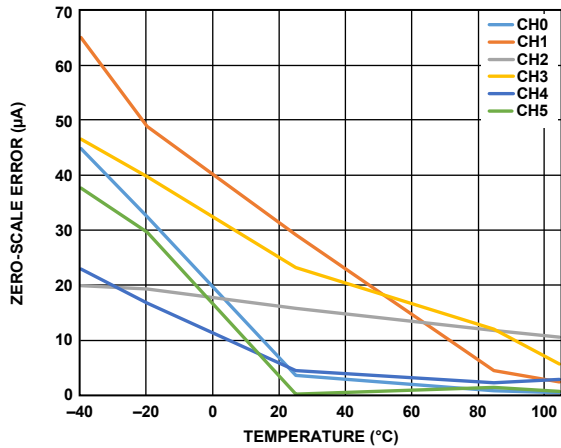
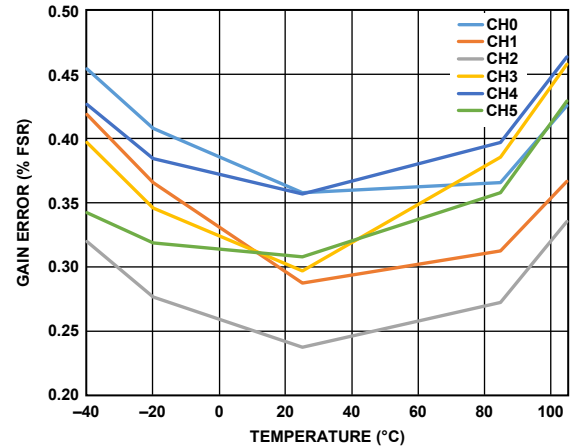


Figure 28. DNL Error vs. DAC Code for Various Temperatures (Channel 5, 0 mA to 100 mA Range)



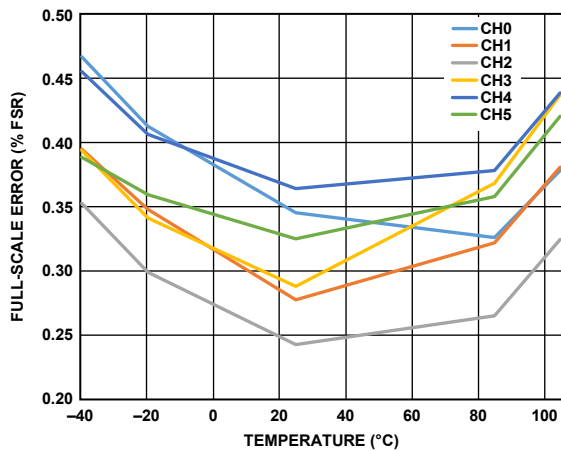
16128-124

Figure 29. Zero-Scale Error vs. Temperature



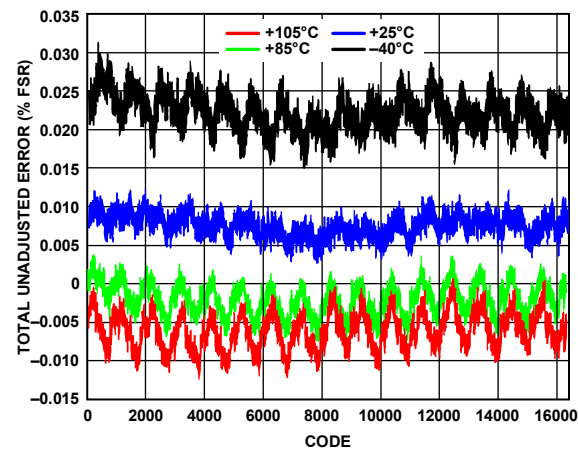
16128-127

Figure 32. Gain Error vs. Temperature



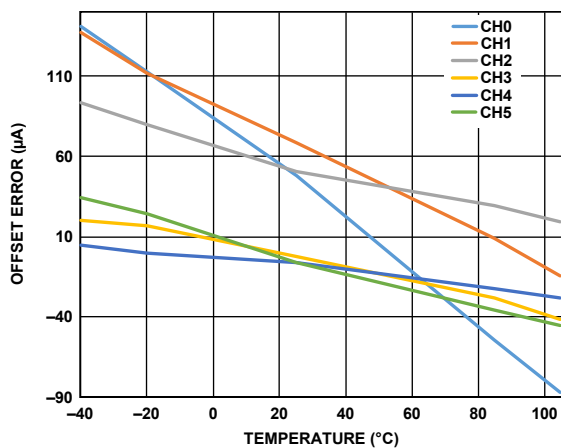
16128-125

Figure 30. Full-Scale Error vs. Temperature



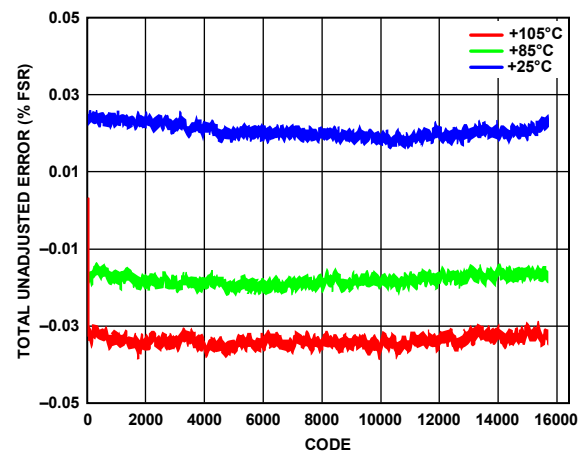
16128-148

Figure 33. Total Unadjusted Error vs. DAC Code for Various Temperatures (Channel 0, 0 mA to 300 mA Range)



16128-126

Figure 31. Offset Error vs. Temperature



16128-149

Figure 34. Total Unadjusted Error vs. DAC Code for Various Temperatures (Channel 1, 0 mA to 250 mA Range)

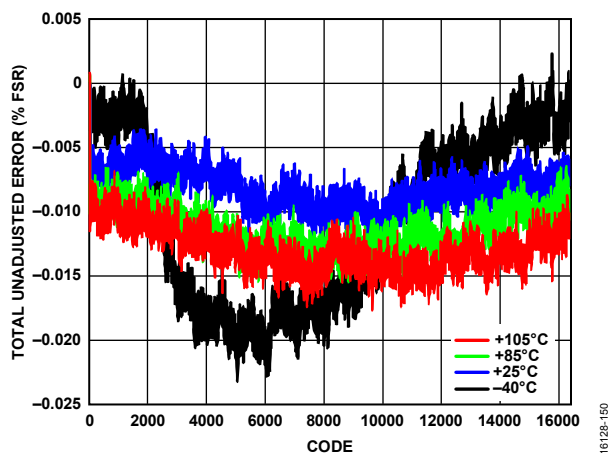


Figure 35. Total Unadjusted Error vs. DAC Code for Various Temperatures (Channel 2, 0 mA to 150 mA Range)

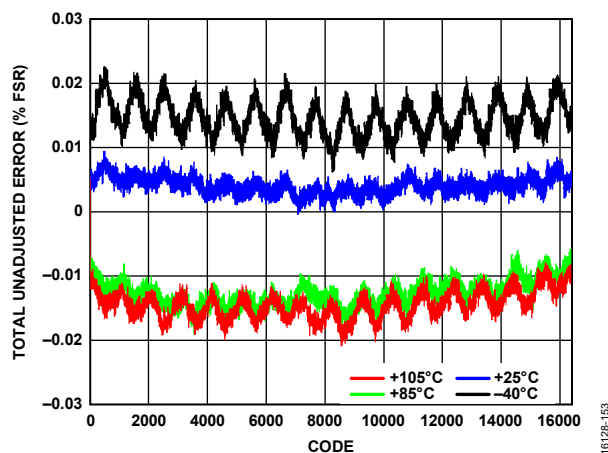


Figure 38. Total Unadjusted Error vs. DAC Code for Various Temperatures (Channel 5, 0 mA to 100 mA Range)

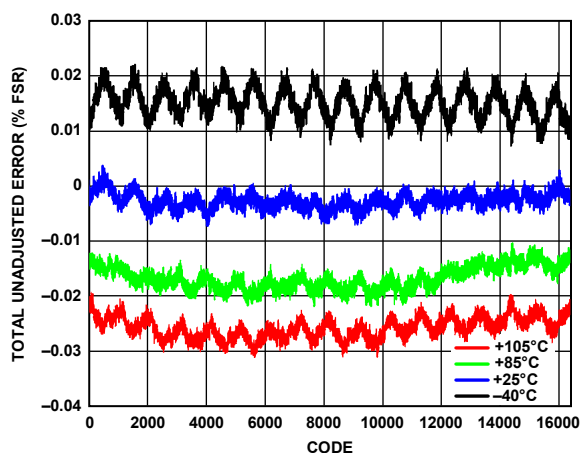


Figure 36. Total Unadjusted Error vs. DAC Code for Various Temperatures (Channel 3, 0 mA to 100 mA Range)

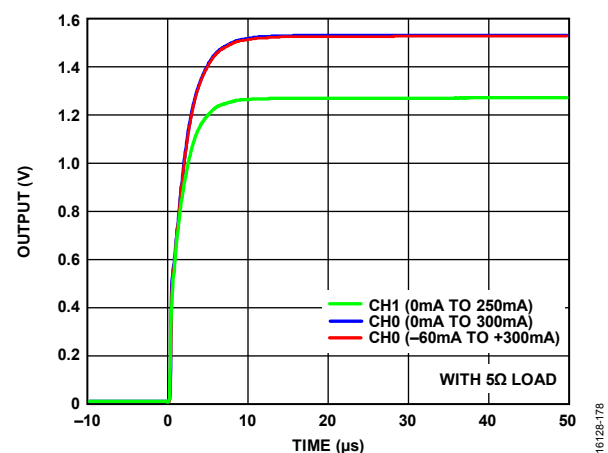


Figure 39. Full-Scale Settling Time (Rising Step)

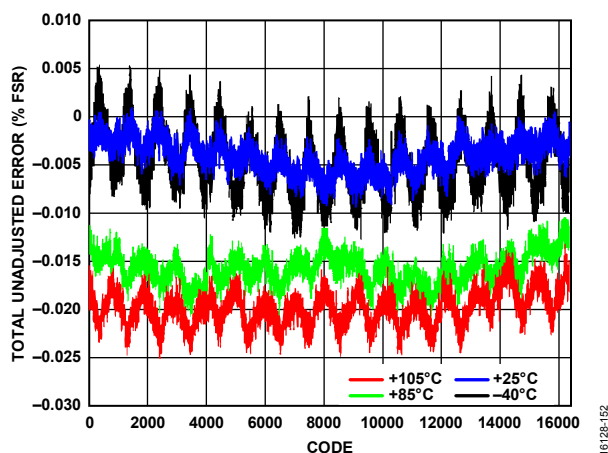


Figure 37. Total Unadjusted Error vs. DAC Code for Various Temperatures (Channel 4, 0 mA to 100 mA Range)

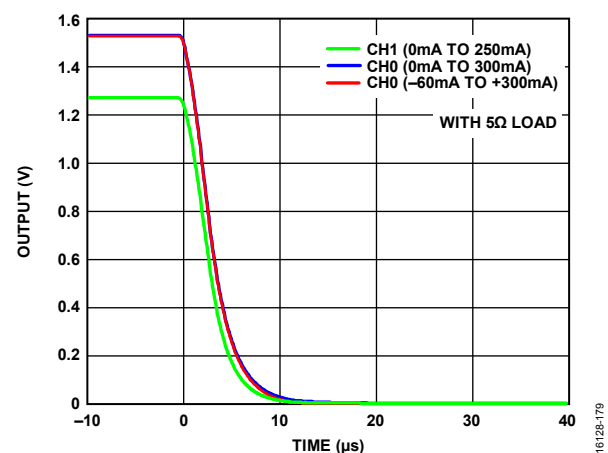


Figure 40. Full-Scale Settling Time (Falling Step)

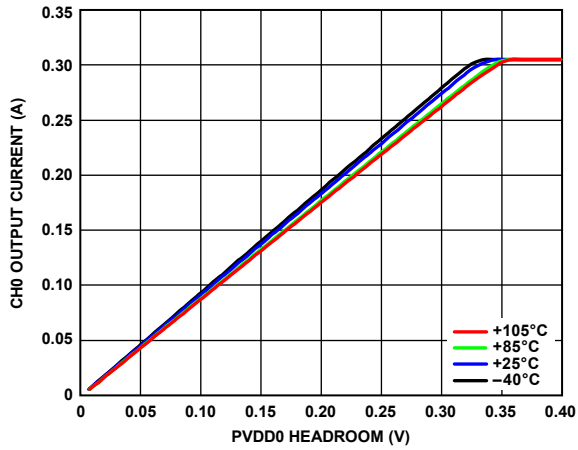


Figure 41. CH0 Output Current vs. PVDD0 Headroom for Various Temperatures

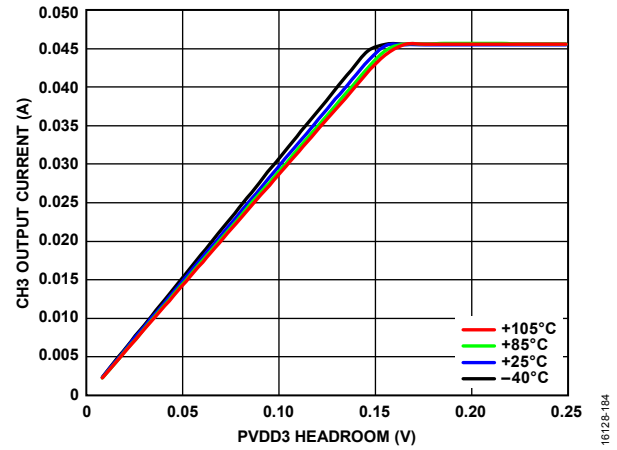


Figure 44. CH3 Output Current vs. PVDD3 Headroom for Various Temperatures

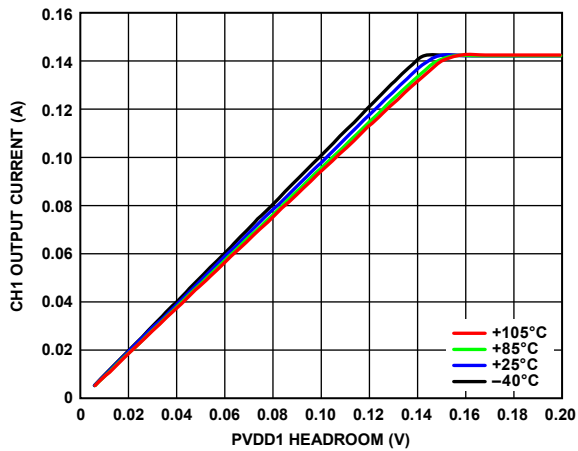


Figure 42. CH1 Output Current vs. PVDD1 Headroom for Various Temperatures

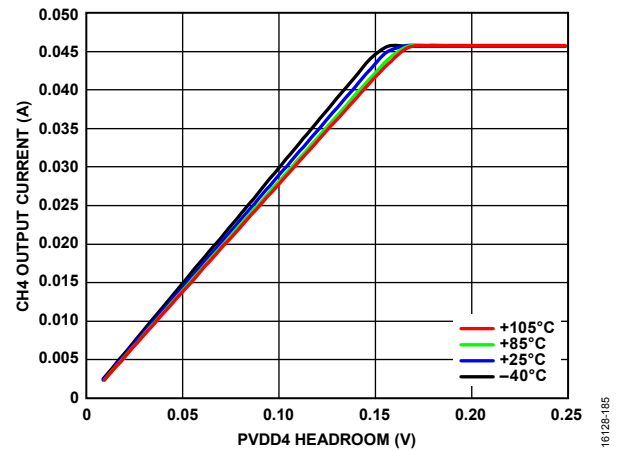


Figure 45. CH4 Output Current vs. PVDD4 Headroom for Various Temperatures

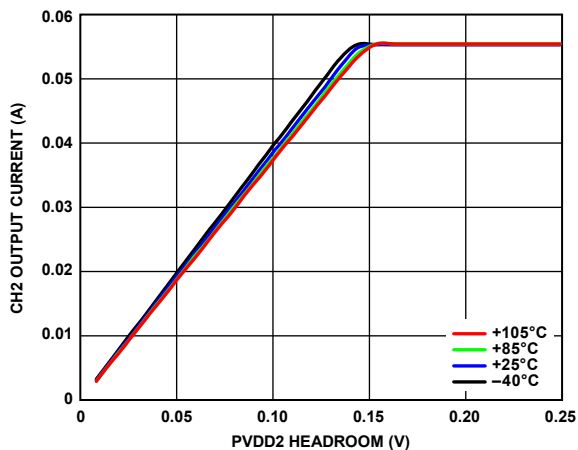


Figure 43. CH2 Output Current vs. PVDD2 Headroom for Various Temperatures

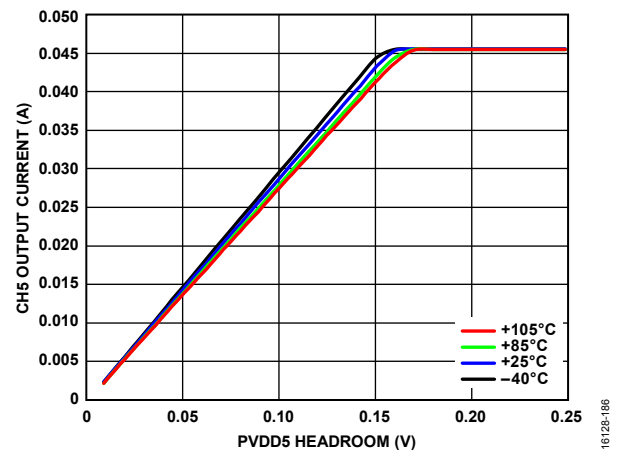


Figure 46. CH5 Output Current vs. PVDD5 Footroom for Various Temperatures

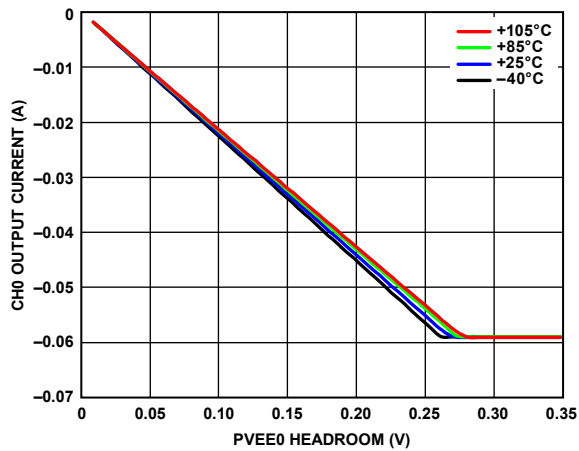


Figure 47. CH0 Output Current vs. PVEE0 Footroom for Various Temperatures

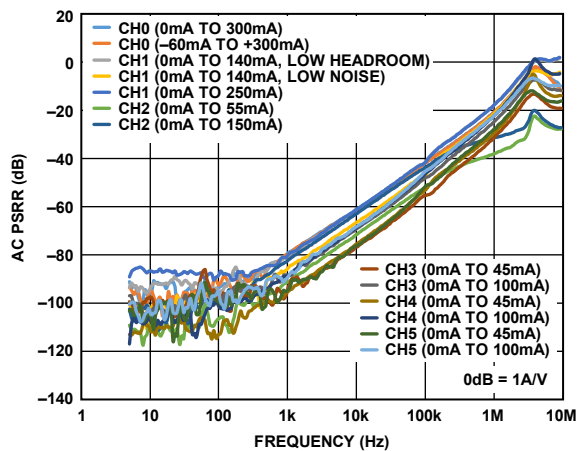


Figure 48. AC PSRR vs. Frequency (All Ranges)

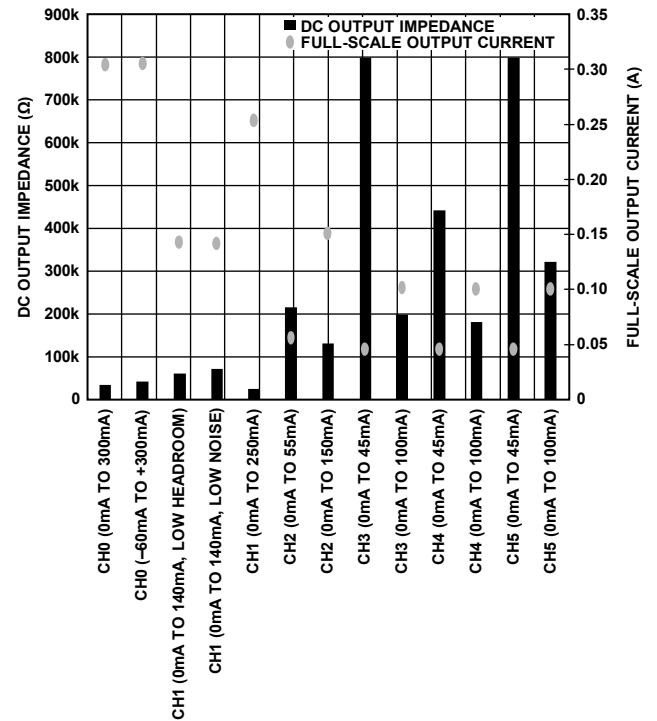


Figure 49. DC Output Impedance vs. Full-Scale Output Current (All Ranges)

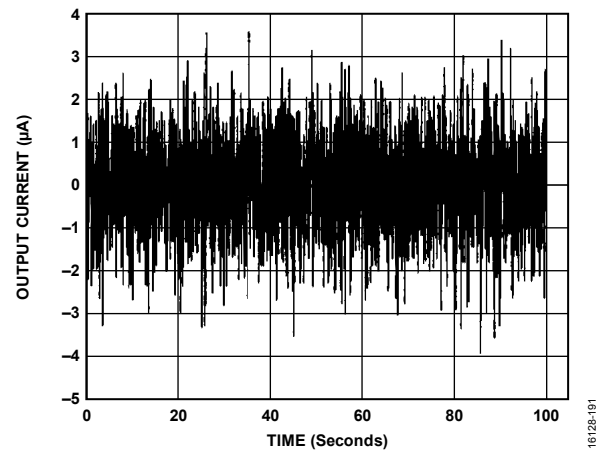


Figure 50. Peak-to-Peak Noise, 0.1 Hz to 10 Hz Bandwidth, (CH0 0mA to 300mA Range)

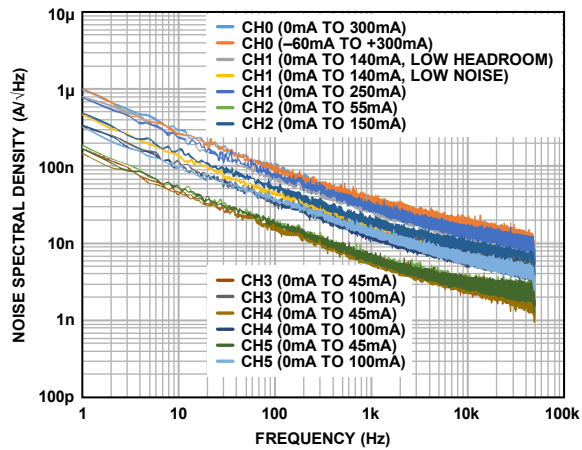


Figure 51. Output NSD vs. Frequency (All Ranges)

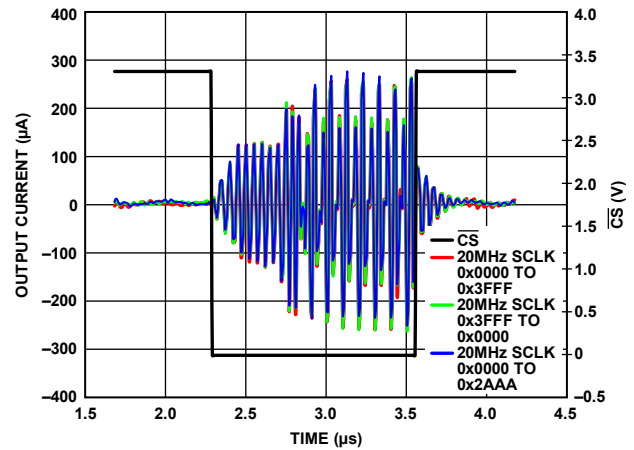


Figure 54. Digital Feedthrough

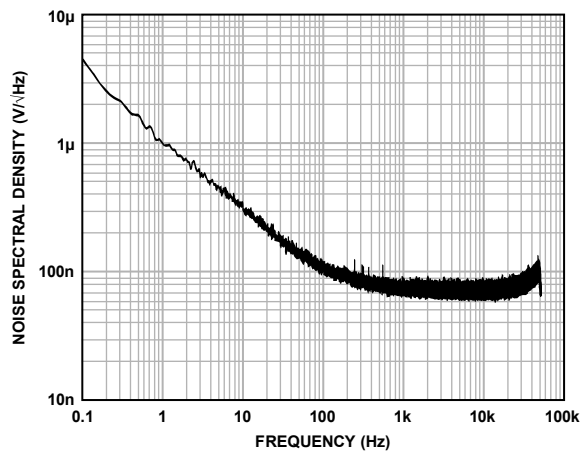


Figure 52. VREF\_IO Output NSD vs. Frequency

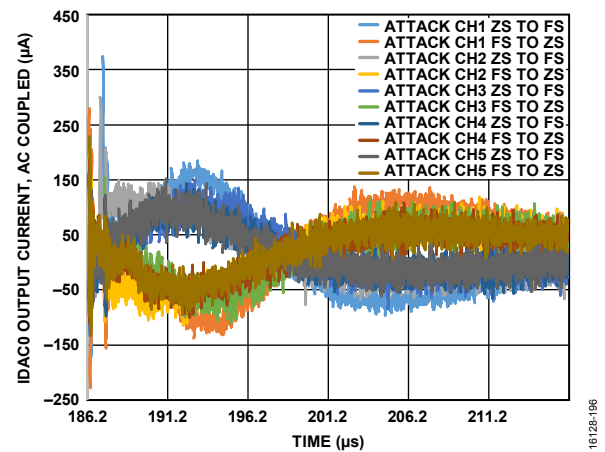


Figure 55. DAC to DAC Crosstalk (Victim Channel Zero)

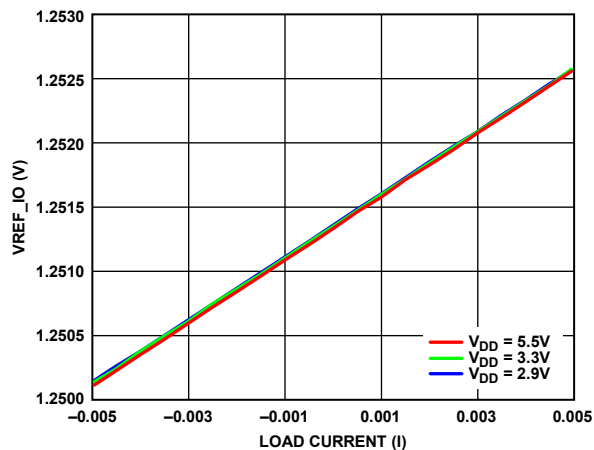


Figure 53. VREF\_IO Voltage vs. Load Current

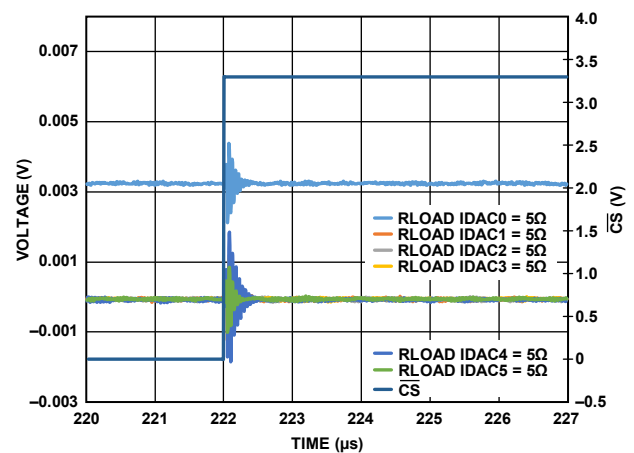


Figure 56. Analog Crosstalk

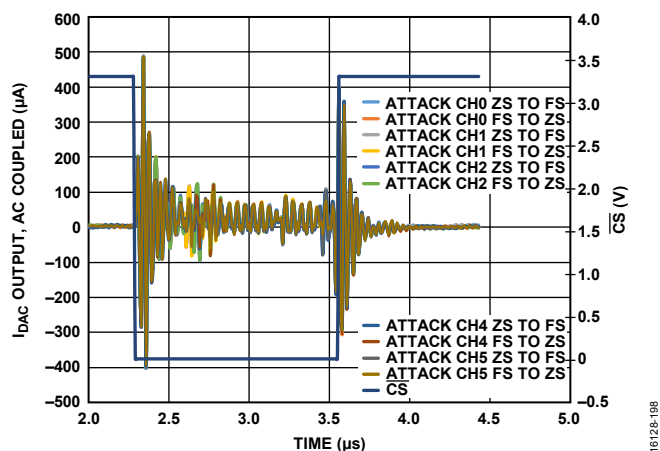


Figure 57. Digital Crosstalk

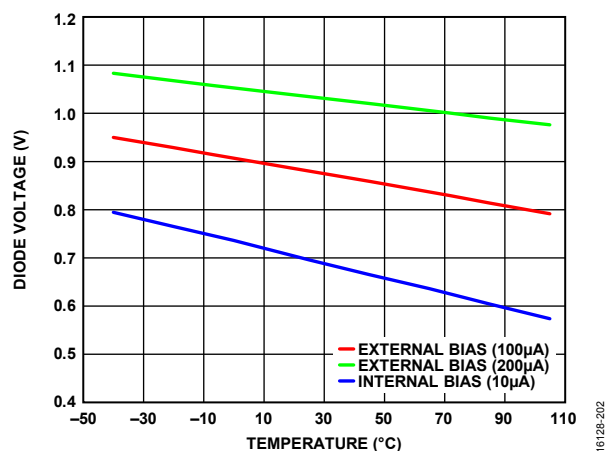


Figure 60. Diode Voltage vs. Temperature

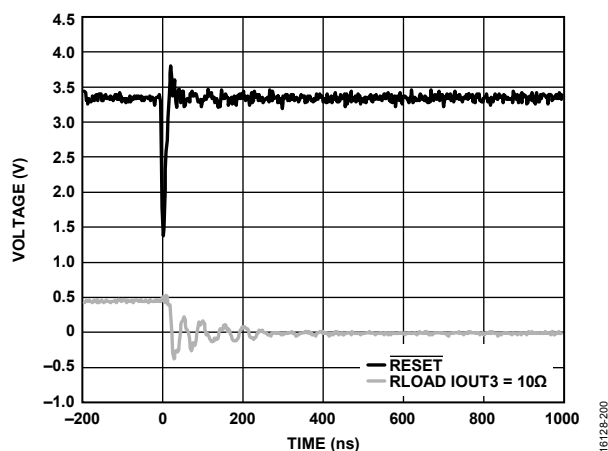


Figure 58. Reset Glitch

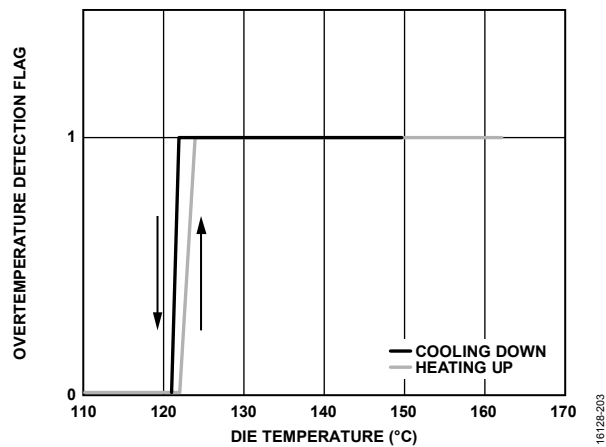


Figure 61. Overheat Warning

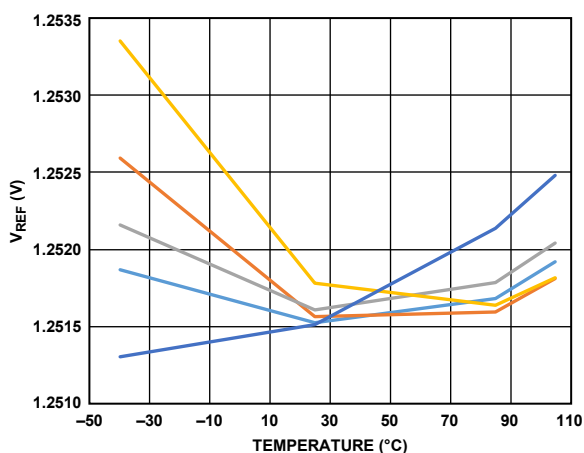
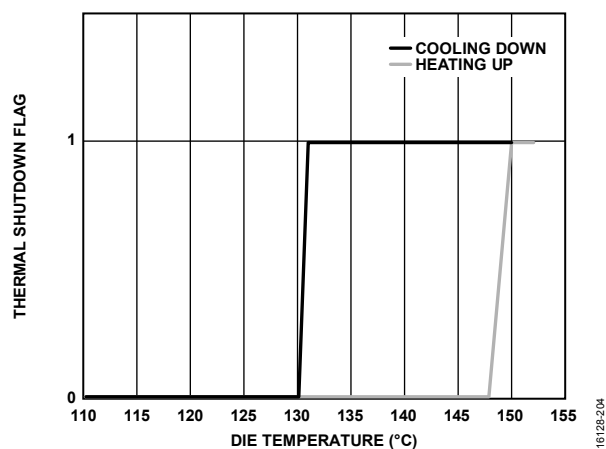
Figure 59.  $V_{REF}$  vs. Temperature for Devices for Five AD5770R Devices

Figure 62. Overheat Shutdown

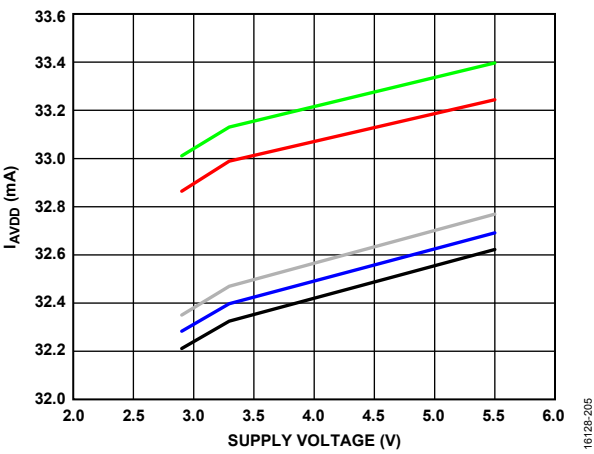


Figure 63. AVDD Supply Current ( $I_{AVDD}$ ) vs. Supply Voltage for Five AD5770R Devices

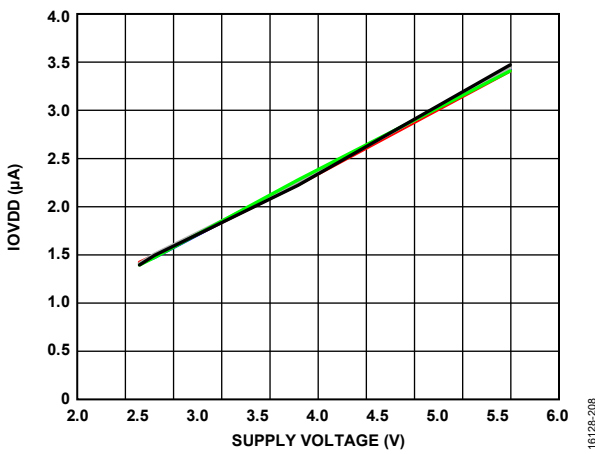


Figure 66. IOVDD Supply Current vs. IOVDD Supply Voltage for Five AD5770R Devices

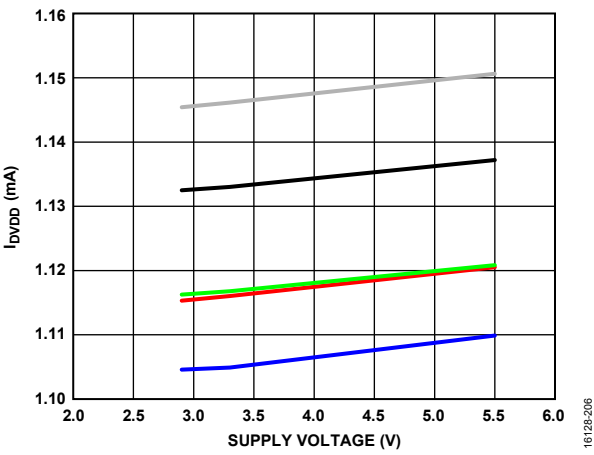


Figure 64. DVDD Supply Current ( $I_{DVDD}$ ) vs. Supply Voltage for Five AD5770R Devices

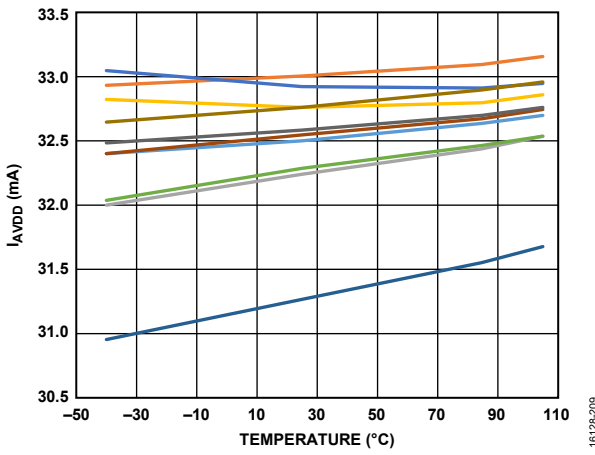


Figure 67.  $I_{AVDD}$  vs. Temperature for Ten AD5770R Devices

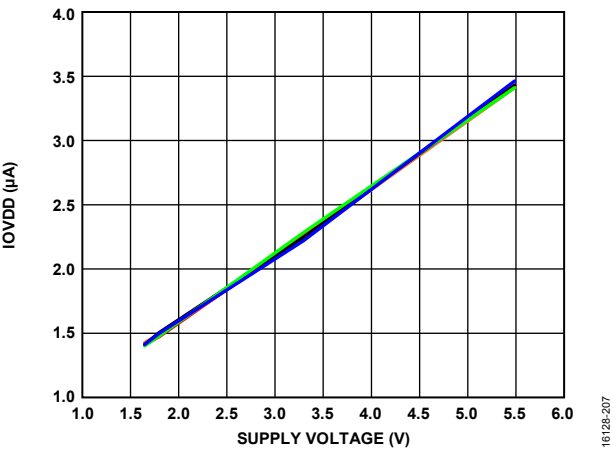


Figure 65. IOVDD Supply Current vs. IOVDD Supply Voltage for Five AD5770R Devices

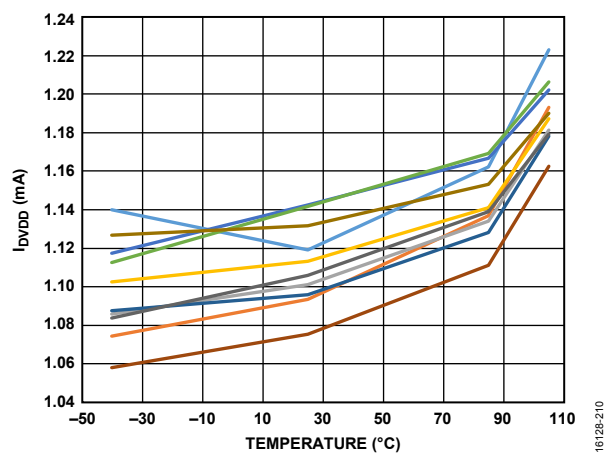


Figure 68.  $I_{DVDD}$  vs. Temperature for Ten AD5770R Devices

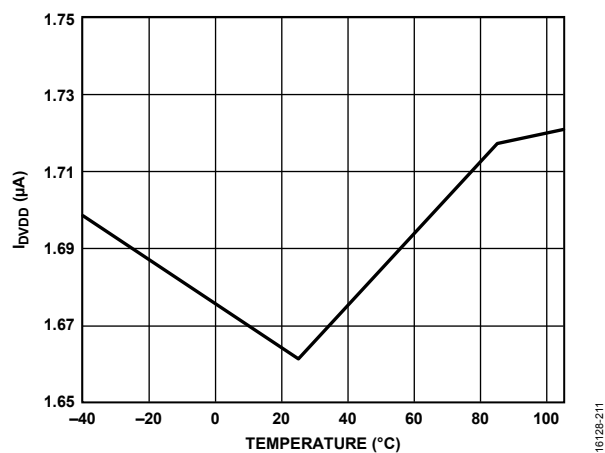


Figure 69.  $I_{DVDD}$  vs. Temperature

## TERMINOLOGY

### TUE

Total unadjusted error is a measure of the output error taking all the various errors into account, namely INL error, offset error, gain error, and output drift over supplies, temperature, and time. TUE is expressed in % FSR.

### Relative Accuracy or Integral Nonlinearity (INL)

Relative accuracy or integral nonlinearity is a measurement of the maximum deviation, in LSBs, from a straight line passing through the endpoints of the DAC transfer function. Typical INL error vs. DAC code plots are shown in Figure 5 to Figure 10.

### Differential Nonlinearity (DNL)

Differential nonlinearity is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of  $\pm 1$  LSB maximum ensures monotonicity. This DAC is guaranteed monotonic by design. Typical DNL error vs. DAC code plots are shown in Figure 11 to Figure 16.

### Zero-Scale Error

Zero-scale error is a measurement of the output error when zero code (0x0000) is loaded to the DAC register. Zero code error is expressed in  $\mu\text{A}$ .

### Zero-Scale Error Temperature Coefficient

Zero code error drift is a measure of the change in zero code error with a change in temperature. It is expressed in  $\text{nA}/^\circ\text{C}$ .

### Gain Error

Gain error is a measure of the span error of the DAC. It is the deviation in slope of the DAC transfer characteristic from the ideal expressed as % FSR.

### Gain Error Temperature Coefficient

Gain temperature coefficient is a measurement of the change in gain error with changes in temperature. It is expressed in ppm of FSR/ $^\circ\text{C}$ .

### Offset Error

Offset error is a measurement of the difference between  $I_{\text{OUTX}}$  (actual) and  $I_{\text{OUTX}}$  (ideal), expressed in  $\mu\text{A}$ , in the linear region of the transfer function. Offset error can be negative or positive.

### Offset Error Drift

Offset error drift is a measurement of the change in offset error with a change in temperature. It is expressed in  $\mu\text{A}/^\circ\text{C}$ .

### DC Power Supply Rejection Ratio (PSRR)

PSRR indicates how the output of the DAC is affected by changes in the supply voltage. PSRR is the ratio of the change in  $I_{\text{OUTX}}$  to a change in  $AV_{\text{DD}}$  for a full-scale output of the DAC. It is measured in  $\mu\text{A}/\text{V}$ .

### Output Settling Time

Output settling time is the amount of time it takes for the output of a DAC to settle to a specified level for a zero-scale to full-scale input change and is measured from the falling edge of LDAC.

### Digital-to-Analog Glitch Impulse

Digital-to-analog glitch impulse is the impulse injected into the analog output when the input code in the DAC register changes state. It is normally specified as the area of the glitch in  $\text{nA}\cdot\text{sec}$ , and is measured when the digital input code is changed by 1 LSB at the major carry transition (0x1FFF to 0x2000 for the AD5770R).

### Digital Feedthrough

Digital feedthrough is a measure of the impulse injected into the analog output of the DAC from the digital inputs of the DAC, but is measured when the DAC output is not updated. It is specified in  $\text{nA}\cdot\text{sec}$  and measured with a full-scale code change on the data bus, that is, from all 0s to all 1s and vice versa.

### DC Crosstalk

DC crosstalk is the dc change in the output level of one DAC in response to a change in the output of another DAC. It is measured with a full-scale output change on one DAC when monitoring another DAC maintained at midscale. It is expressed in  $\text{nA}\cdot\text{sec}$ .

### Digital Crosstalk

Digital crosstalk is the glitch impulse transferred to the output of one DAC at midscale in response to a full-scale code change (all 0s to all 1s and vice versa) in the input register of another DAC. It is measured in standalone mode and is expressed in  $\text{nA}\cdot\text{sec}$ .

### DAC to DAC Crosstalk

DAC to DAC crosstalk is the glitch impulse transferred to the output of one DAC due to a digital code change and subsequent analog output change of another DAC. It is measured by loading the attack channel with a full-scale code change (all 0s to all 1s and vice versa), using the write to and update commands when monitoring the output of the victim channel that is at midscale. The energy of the glitch is expressed in  $\text{nA}\cdot\text{sec}$ .

### Output Noise Spectral Density

Output noise spectral density is a measurement of the internally generated random noise. Random noise is characterized as a spectral density ( $\text{nA}/\sqrt{\text{Hz}}$ ). It is measured by loading the DAC to midscale and measuring noise at the output. It is measured in  $\text{nA}/\sqrt{\text{Hz}}$ .

### Multiplexer Switching Glitch

The multiplexer switching glitch is a measure of the impulse injected into the analog output of the DAC when the monitor mux is changed to monitor a different channel.

### AC Power Supply Rejection Ratio (AC PSRR)

AC power supply rejection ratio is a measure of the rejection of the output current to ac changes in the power supplies applied to the DAC. AC PSRR is measured for a given amplitude and frequency change in power supply voltage and is expressed in decibels.

## THEORY OF OPERATION

### DIGITAL TO ANALOG CONVERTER

The AD5770R is a 6-channel, 14-bit, serial input, current output DAC capable of multiple low noise output current ranges with high power efficiency. Each of the six DACs has a segmented current steering architecture, chosen to achieve low glitch performance when changing codes.

### PRECISION REFERENCE CURRENT GENERATION

The AD5770R requires a 500  $\mu$ A precision reference current for all four DAC cores, which is generated using a 1.25 V voltage reference and a 2.5 k $\Omega$  precision  $R_{SET}$  resistor. The AD5770R integrates an internal 1.25 V voltage reference and 2.5 k $\Omega$  internal precision  $R_{SET}$  resistor for this function. The AD5770R can also use an external voltage reference and external precision  $R_{SET}$  resistor for the reference current generation. Ensure that the voltage reference and the precision  $R_{SET}$  resistor have low noise, high accuracy, and low temperature drift to help minimize the overall IDACx gain error and gain error drift. Table 1 outlines the performance specifications of the AD5770R with both the internal reference and internal  $R_{SET}$  resistor, and an external 1.25 V reference and external precision  $R_{SET}$  resistor.

#### Voltage Reference

The AD5770R can use an external voltage reference for the precision reference current generation. The external reference voltage can be either 1.25 V or 2.5 V, configured by writing to the `REFERENCE_VOLTAGE_SEL` bits in the reference register. When the user selects the 2.5 V external voltage reference option, an internal voltage divider attenuates to achieve the 1.25 V required.

The device powers up with the external 2.5 V reference voltage option selected.

The AD5770R integrates a low noise, on-chip, 15 ppm/ $^{\circ}$ C, 1.25 V voltage reference that can be used as the voltage reference. The on-chip reference is powered down by default and is enabled when the `REFERENCE_VOLTAGE_SEL` bits in the reference register select the internal reference.

The buffered 1.25 V internal reference voltage can be made available at the `VREF_IO` pin for use as a system reference.

Regardless of the voltage reference scheme used, it is recommended that a 100 nF capacitor is placed between the `CREF` pin and AGND to achieve specified performance. A simplified diagram of the voltage reference configuration is shown in Figure 70.

When the internal 1.25 V reference is selected and made available on the `VREF_IO` pin, switch SWA1 and switch SWA2 are closed, and switch SWA3 is connected to switch SWA2.

When the internal 1.25 V reference is selected but not made available on the `VREF_IO` pin, switch SWA1 is open, switch SWA2 is closed, and switch SWA3 is connected to switch SWA2.

When the external 1.25 V reference option is selected, switch SWA1 is closed, switch SWA2 is open, and switch SWA3 is connected to switch SWA2.

When the external 2.5 V option is selected, switch SWA1 and switch SWA2 are open and switch SWA3 is connected to the resistor divider shown in Figure 70.

#### Precision $R_{SET}$ Resistor

The AD5770R integrates an on-chip 2.5 k $\Omega$  (10 ppm/ $^{\circ}$ C, 0.1%) precision  $R_{SET}$  resistor that can be used for the reference current generation. If required, an external precision  $R_{SET}$  resistor can be used for reference current generation. The user selects an internal or an external reference resistor by writing to the `REFERENCE_RESISTOR_SEL` bit in the reference register. The AD5770R powers up with the internal precision  $R_{SET}$  resistor selected.

The AD5770R integrates fault protection circuitry when using an external resistor. The AD5770R automatically switches from an external to an internal resistor if the external resistor option is selected, and if the external resistance is below the minimum specification. A simplified diagram of how the reference resistor is configured by changing switch SWB1 is shown in Figure 70.

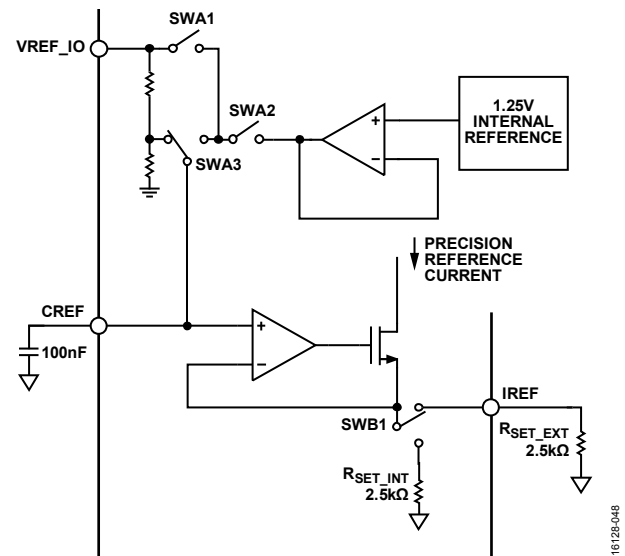


Figure 70. AD5770R Reference Options

### DIAGNOSTIC MONITORING

The AD5770R diagnostic feature allows the user to monitor output compliance voltages, output currents, and the internal die temperature of the device. The output compliance voltages, which are voltages representative of output current and internal die temperature, are multiplexed on-chip and are available on the `MUX_OUT` pin and can be measured using an external ADC.

Diagnostics monitoring is disabled on power up and can be enabled by writing to the `MON_FUNCTION` bits in the `MONITOR_SETUP` register.

The AD5770R integrates a voltage buffer on the multiplexer output to ease system design. The multiplexer buffer is disabled and bypassed on power up. The multiplexer buffer is enabled by setting the MUX\_BUFFER bit in the MONITOR\_SETUP register.

### Compliance Voltage Monitoring

When the MON\_FUNCTION bits in the MONITOR\_SETUP register are set to select output voltage monitoring, the output compliance voltage of the selected DAC channel is multiplexed onto the MUX\_OUT pin. The IDACx channel to be monitored is selected using the MON\_CH bits in the MONITOR\_SETUP register.

### Output Current Monitoring

When the MON\_FUNCTION bits in the MONITOR\_SETUP register select output current monitoring, a voltage representation of the output current of the selected DAC channel is multiplexed onto the MUX\_OUT pin. The output current can only be monitored in current sourcing mode. The IDACx channel to be monitored is selected using the MON\_CH bits in the MONITOR\_SETUP register.

The output current is calculated by

$$I_{SOURCE} = \frac{I_{FULLSCALE} \times (V_{MUX} - V_{OS})}{400 \text{ mV}} \quad (1)$$

where:

$I_{SOURCE}$  is the output current being sourced.

$I_{FULLSCALE}$  is the full-scale output current.

$V_{MUX}$  is the measured voltage at the MUX\_OUT pin.

$V_{OS}$  is the monitor offset voltage, nominally 28 mV.

Uncalibrated, the current monitoring feature is accurate to within 10% of the full-scale output range. To improve the accuracy of the current monitor feature, calibrate  $V_{OS}$  by measuring the voltage at the MUX\_OUT pin at zero scale. To calibrate the 400 mV term, measure the voltage at the MUX\_OUT pin at full scale.

For 0 mA to 140 mA low headroom mode on Channel 1, use a value of 250 mA for  $I_{FULLSCALE}$ .

### Internal Die Temperature Monitoring

When temperature monitoring is selected in the MONITOR\_SETUP register, a voltage representation of the internal die temperature is multiplexed onto the MUX\_OUT pin. To monitor the internal die temperature, a precision current is forced through a diode on the chip, and the voltage across the diode is multiplexed onto the MUX\_OUT pin. Choose to use an external bias current for the temperature monitoring function by setting the IB\_EXT\_EN bit high in the MONITOR\_SETUP register. The external bias current must be forced into the MUX\_OUT pin. The multiplexer buffer must be bypassed when using an external bias current for temperature monitoring.

Using the internal bias current with the IB\_EXT\_EN bit set low, calculate the internal die temperature as follows:

$$T = \frac{700 \text{ mV} - V_D}{1.8 \text{ mV}} + 25 \quad (2)$$

where:

$T$  is the die temperature ( $^{\circ}\text{C}$ ).

$V_D$  is the diode voltage.

Using an external bias current of 100  $\mu\text{A}$ , with the IB\_EXT\_EN bit set high, the internal die temperature can be calculated as follows:

$$T = \frac{880 \text{ mV} - V_D}{1.3 \text{ mV}} + 25 \quad (3)$$

When using an external bias current of 200  $\mu\text{A}$ , with the IB\_EXT\_EN bit set high, the die temperature can be calculated as follows:

$$T = \frac{1.04 \text{ V} - V_D}{0.9 \text{ mV}} + 25 \quad (4)$$

## SERIAL INTERFACE

The AD5770R has a 4-wire ( $\overline{\text{CS}}$ , SCLK, SDI, and SDO) interface that is compatible with SPI, QSPI, and MICROWIRE interface standards as well as most digital signal processors (DSPs).

For both read and write SPI transactions, data must be valid on the rising edge of SCLK (SCLK clock polarity = 0, SCLK clock phase = 0). For all SPI transactions, data is shifted MSB first. Communication with the device is separated into two distinct phases of operation. The first phase is the instruction phase and is used to initiate some action of the device. The second phase is the data phase where data is either passed to the device to operate on or received from the device in response to the instruction phase. Figure 71 illustrates the SPI transaction phases.

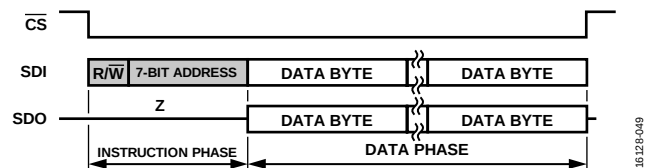


Figure 71. SPI Transaction Phases

### Instruction Phase

The instruction phase immediately follows the falling edge of  $\overline{\text{CS}}$  that initiates the SPI transaction. The instruction phase consists of a read/write bit (R/W) followed by a register address word. Setting R/W high selects a read instruction. Setting R/W low selects a write instruction. The address word is 7 bits long. The register address sent in the instruction phase is used as the starting address to start writing or reading from. Refer to Table 12 and Table 13 for a full list of registers and the associated addresses.

### Data Phase

The data phase immediately follows the instruction phase. When a write instruction is sent to the device, data is written to the register location selected. When a read instruction is sent to the device, data stored in the register location selected is shifted out on the SDO pin.

### SPI Frame Synchronization

The  $\overline{\text{CS}}$  pin is used to frame data during an SPI transaction. A falling edge on  $\overline{\text{CS}}$  initiates a SPI transaction. Deasserting  $\overline{\text{CS}}$  during a SPI transaction terminates part or all of the data transfer. If  $\overline{\text{CS}}$  is deasserted (returned high) before the instruction phase is complete, the transaction aborts and the AD5770R returns to the ready state. If  $\overline{\text{CS}}$  is deasserted before the first data word is written, the transaction aborts and the AD5770R returns to the ready state. If  $\overline{\text{CS}}$  is deasserted after one or more data words have been written, those completed data words are written or read, but any partial written data words are aborted.

### Streaming Mode

The  $\overline{\text{CS}}$  pin can be held low, and multiple data bytes can be shifted during the data phase, which reduces the amount of overhead associated with data transfer. This mode of operation is known as streaming mode. When in streaming mode, the register address sent in the instruction phase is automatically incremented or decremented after each byte of data is processed. The ADDR\_ASCENSION\_MSB bit and ADDR\_ASCENSION\_LSB bit in the INTERFACE\_CONFIG\_A register selects the address increment or decrement. The default operation is to decrement addresses when streaming data. Figure 72 illustrates a streaming mode SPI write transaction in which the six input registers are accessed using only a single instruction byte. The register address is automatically decremented after each data byte is processed. Figure 73 illustrates a streaming mode SPI read transaction in which the six DAC registers are accessed using a decrementing address.

### Single Instruction Mode

When the single instruction bit is set in the INTERFACE\_CONFIG\_B register, streaming mode is disabled, and the AD5770R is placed in single instruction mode. In single instruction mode, the internal SPI state machine resets after the data phase as if  $\overline{\text{CS}}$  was deasserted, and awaits the next instruction. Single instruction mode forces each data phase to

be preceded with a new instruction phase even though the  $\overline{\text{CS}}$  line has not been deasserted by the SPI master. Single instruction mode allows the user to access one or more registers in a single synchronization frame without having to deassert the  $\overline{\text{CS}}$  line after each data byte. The default for this bit is cleared, resulting in streaming mode being enabled.

Figure 74 illustrates an SPI transaction in single instruction mode in which the following sequence of events occur:

1. Sets the output range of Channel 1.
2. Enables the output of Channel 1.
3. Writes to the Channel 1 DAC register.
4. Reads the status register.

### Multibyte Registers

If writing to a multibyte register,  $\overline{\text{CS}}$  must be held low for the whole transaction for the write to be valid. The address used must be the address of the most significant byte. The ADDR\_ASCENSION\_MSB bit and the ADDR\_ASCENSION\_LSB bit in the INTERFACE\_CONFIG\_A register must be cleared. This applies when reading or writing to any multibyte register in both single instruction mode and streaming mode. Figure 75 illustrates a multibyte register access. The AD5770R contains 14 multibyte registers, as follows:

- Six input registers.
- Six DAC registers.
- One input page mask register.
- One DAC page mask register.

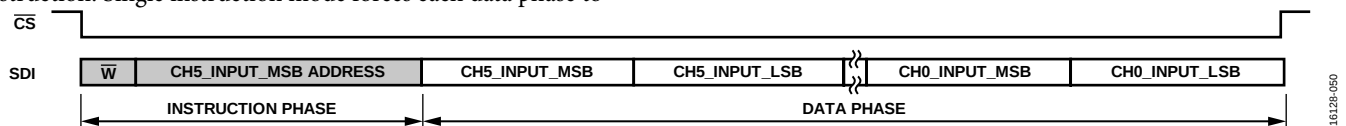


Figure 72. Streaming Mode SPI Write Transaction with Decrementing Address

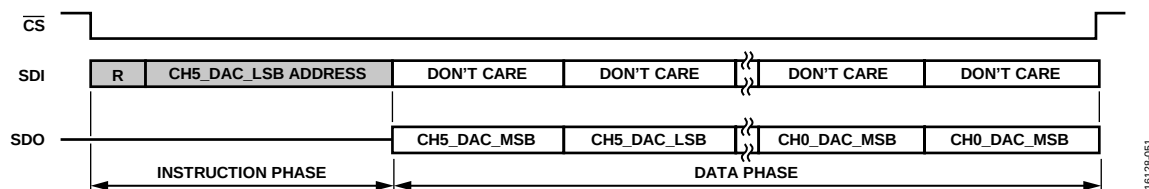


Figure 73. Streaming Mode SPI Read Transaction with Decrementing Address

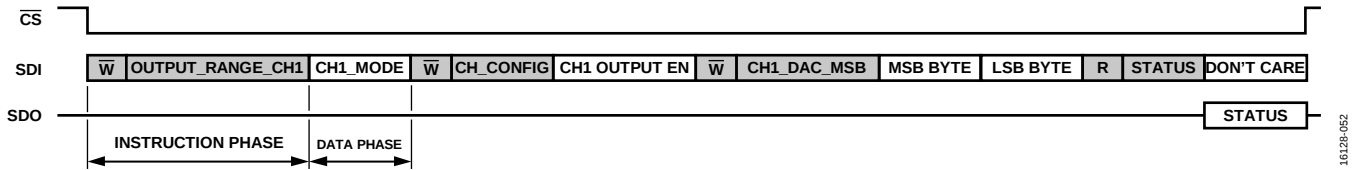


Figure 74. SPI Transaction in Single Instruction Mode

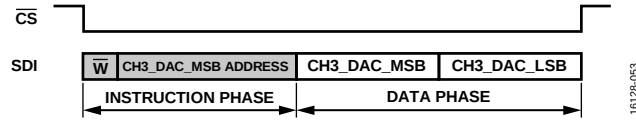


Figure 75. Multibyte Register Write

## RESET FUNCTION

The AD5770R has an asynchronous  $\overline{\text{RESET}}$  pin. For normal operation,  $\overline{\text{RESET}}$  is tied high. Asserting the  $\overline{\text{RESET}}$  pin to logic low for at least 10 ns resets all registers to their default values. The reset function takes 100 ns, maximum. Data must not be written to the device during this time.

The AD5770R has a software reset function that performs the same function as the  $\overline{\text{RESET}}$  pin, with the exception of not resetting the INTERFACE\_CONFIG\_A register. The reset function is activated by setting the SW\_RESET\_MSB and SW\_RESET\_LSB bits in the INTERFACE\_CONFIG\_A register. The SW\_RESET\_MSB and SW\_RESET\_LSB bits clear automatically during a software reset.

A reset function must not be performed when the TEMP\_WARNING bit in the status register is high. Ensure that the device reads the correct trim values from the internal memory.

## LOAD DAC

The AD5770R DAC consists of double buffered registers for the DAC code. Data for one or many channels can be written to the input register without changing the DAC outputs. A load DAC command issued to the device transfers input register content into the DAC register, updating the DAC output.

### Hardware $\overline{\text{LDAC}}$ Pin

The AD5770R has an active low  $\overline{\text{LDAC}}$  pin that can synchronize updates to the outputs of the DACs. When  $\overline{\text{LDAC}}$  is held high, DAC codes can be written to the input registers of the DAC without affecting the output. When  $\overline{\text{LDAC}}$  is taken low, the contents of the input register are transferred to the DAC register of the corresponding channel, and the output updates. The  $\overline{\text{LDAC}}$  idle high behavior is shown in Figure 2.

When the  $\overline{\text{LDAC}}$  pin is held low before the last rising edge of  $\overline{\text{CS}}$  prior to the beginning of a new SPI transaction and the input registers contents are modified, the update to the DAC output happens when the LSB of the DAC input register is written. The  $\overline{\text{LDAC}}$  idle low behavior is shown in Figure 2 and Figure 3.

The  $\overline{\text{LDAC}}$  pin functionality can be masked for any or all channels by configuring the corresponding HW\_LDAC\_MASK\_CHx bits high in the HW\_LDAC register, which is

useful in cases where only a selection of channels are required to update synchronously.

### Software $\overline{\text{LDAC}}$

It is possible to transfer data from any or all input registers to the corresponding DAC registers with a write to the SW\_LDAC register, which is useful in cases where only a selection of channels are required to update synchronously.

Setting the SW\_LDAC register for any channel updates the selected channels DAC register with the input register contents. The contents of the SW\_LDAC register clear to 0x00 after a software LDAC operation.

## INPUT PAGE MASK REGISTER

Following a write to the input page mask register, the code loaded into this register is copied into the input register of any channels selected in the CH\_SELECT register.

## DAC PAGE MASK REGISTER

Following a write to the DAC page mask register, the DAC code loaded into this register is copied into the DAC register of any channels selected in the CH\_SELECT register.

## OUTPUT STAGES

Each of the six AD5770R channels has a programmable current output stage that sets the required output current.

### Channel 0 Sink Current Generator

To sink current on Channel 0, the sink current generator must be enabled by setting the CH0\_SINK\_EN bit in the CHANNEL\_CONFIG register to one. On power-up, the sink current generator is enabled.

### Output Shutdown

On power-up, the outputs of each channel are in shutdown mode. When a DAC output is in shutdown mode, the output current is set to 0 mA. However, the bias circuitry for each IDACx channel remains powered up, and only the output is shut down. The shutdown bits for each register are located in the CHANNEL\_CONFIG register. When changing between output modes on a DAC channel, the output stage of the channel must be shut down to prevent glitches on the output.

**Channel 0**

Channel 0 of the AD5770R sinks up to 60 mA and sources up to 300 mA of current. This channel has three different modes of operation. The CH0\_MODE bits in the OUTPUT\_RANGE\_CH0 register configure the different modes. The configuration options for Channel 0 are listed in Table 8.

On power-up, Channel 0 defaults to the 0 mA to 300 mA range.

Channel 0 has a sinking only mode of –60 mA to 0 mA. In this mode, the DAC has a zero-scale output of –60 mA and a full-scale output of 0 mA. To enter this mode safely without output glitches, the output must be shut down first by setting CH0\_SHUTDOWN\_B high in the CHANNEL\_CONFIG register.

Channel 0 has a sourcing and sinking mode where the DAC has a zero-scale output of –60 mA and a full-scale output of +300 mA. To reduce glitches on the output of Channel 0, CH0\_MODE must be configured before taking the output out of shutdown.

**Channel 1**

Channel 1 can be set up to source 0 mA to 140 mA or 0 mA to 250 mA. The full-scale output range for Channel 1 must be set

by writing to the CH1\_MODE bits of the OUTPUT\_RANGE\_CH1 register. In addition to the 0 mA to 250 mA range, Channel 1 has two 0 mA to 140 mA ranges; the channel can be set up to optimize for better noise and PSRR or for reduced headroom. The configuration options for Channel 1 are listed in Table 8.

**Channel 2**

Channel 2 can be set up to source 0 mA to 55 mA or 0 mA to 150 mA. The full-scale output range for Channel 2 must be set by writing to the CH2\_MODE bits of the OUTPUT\_RANGE\_CH2 register. Table 8 lists configuration options for Channel 2.

**Channel 3 to Channel 5**

Channel 3, Channel 4, and Channel 5 of the AD5770R can be set up to source 0 mA to 45 mA or 0 mA to 100 mA. The full-scale output ranges for Channel 3, Channel 4, and Channel 5 must be set by writing to the CH3\_MODE, CH4\_MODE, and CH5\_MODE bits of the OUTPUT\_RANGE\_CH3, OUTPUT\_RANGE\_CH4, and OUTPUT\_RANGE\_CH5 registers. The configuration options for Channel 3, Channel 4, and Channel 5 are listed in Table 8.

**Table 8. Output Range Mode Register Setup**

| Channel   | Mode Bit Name | Mode | Zero-Scale Output (mA) | Full-Scale Output (mA) <sup>1</sup> | Minimum Headroom (mV) | Comments                           |
|-----------|---------------|------|------------------------|-------------------------------------|-----------------------|------------------------------------|
| Channel 0 | CH0_MODE      | 0x0  | 0                      | 300                                 | 450                   | Low headroom<br>Low noise and PSRR |
|           |               | 0x1  | –60                    | 0                                   | 0 <sup>2</sup>        |                                    |
|           |               | 0x2  | –60                    | 300                                 | 450 <sup>2</sup>      |                                    |
| Channel 1 | CH1_MODE      | 0x1  | 0                      | 140                                 | 275                   |                                    |
|           |               | 0x2  | 0                      | 140                                 | 450                   |                                    |
|           |               | 0x3  | 0                      | 250                                 | 450                   |                                    |
| Channel 2 | CH2_MODE      | 0x0  | 0                      | 55                                  | 275                   |                                    |
|           |               | 0x1  | 0                      | 150                                 | 275                   |                                    |
| Channel 3 | CH3_MODE      | 0x0  | 0                      | 45                                  | 275                   |                                    |
|           |               | 0x1  | 0                      | 100                                 | 275                   |                                    |
| Channel 4 | CH4_MODE      | 0x0  | 0                      | 45                                  | 275                   |                                    |
|           |               | 0x1  | 0                      | 100                                 | 275                   |                                    |
| Channel 5 | CH5_MODE      | 0x0  | 0                      | 45                                  | 275                   |                                    |
|           |               | 0x1  | 0                      | 100                                 | 275                   |                                    |

<sup>1</sup> Output current scaling feature disabled. See the Output Current Scaling section for more information.

<sup>2</sup> 500 mV footroom from PVEE0 supply required when sinking current.

## OUTPUT FILTER

Each channel of the AD5770R has a user programmable variable resistor in the output stage used for filtering. The output filter resistor creates a low-pass RC filter with the 10 nF external capacitor connected to the CDAMP\_IDACx pin. The value loaded into the OUTPUT\_FILTER\_CH0x register configures the value of the variable resistor. Table 9 shows the cutoff frequency of each resistor setting.

**Table 9. IDACx Filter Bandwidth Control Settings**

| OUTPUT_FILTER_CHx Setting | Resistor Value | Cutoff Frequency |
|---------------------------|----------------|------------------|
| 0x0                       | 60 Ω           | 262 kHz          |
| 0x5                       | 5.6 kΩ         | 2.8 kHz          |
| 0x6                       | 11.2 kΩ        | 1.4 kHz          |
| 0x7                       | 22.2 kΩ        | 715 Hz           |
| 0x8                       | 44.4 kΩ        | 357 Hz           |
| 0x9                       | 104 kΩ         | 153 Hz           |

## OUTPUT CURRENT SCALING

When in current sourcing mode only, the full-scale output current of each channel of the AD5770R can be scaled by up to ½ of the nominal full-scale current and maintain 14-bit monotonicity.

The full-scale output current of any channel can be scaled by writing to the CHx\_OUTPUT\_SCALING bits of the OUTPUT\_RANGE\_CHx register. The value loaded into the CHx\_OUTPUT\_SCALING bits determines the multiplier, which scales the full-scale current. The adjusted full-scale current of an IDACx channel is calculated by,

$$I_{ADJ} = I_{NOM} \times \left(1 - \frac{x}{128}\right) \quad (5)$$

where:

$I_{ADJ}$  is the adjusted full-scale output current.

$I_{NOM}$  is the nominal full-scale output current.

$x$  is the code loaded into output scaling register,  $0 \leq x \leq 63$ .

For the range scaling feature to take effect on the output current for a particular channel, write to the DAC register for that channel after writing to the OUTPUT\_RANGE\_CHx register.

Refer to Table 10 for a list of output current ranges achievable using the scaling feature.

## ALARM

The AD5770R provides a number of fault alerts that are signaled via the ALARM pin and the status register. The active low ALARM pin can be configured as an open-drain output by setting the OPEN\_DRAIN\_EN bit in the ALARM\_CONFIG register, allowing several devices to be connected together to one pull-up resistor for global fault detection. Open drain mode on the ALARM pin is disabled on power up.

## Background CRC Failure

The AD5770R periodically performs a background cyclic redundancy check (CRC) on the status of the on-chip registers to ensure that the memory bits are not corrupted. In the unlikely event that the background CRC fails, the ALARM pin activates and the BACKGROUND\_CRC\_STATUS bit in the status register is set high. Reading the status register deasserts the ALARM pin. A hardware or software reset is required to clear the BACKGROUND\_CRC\_STATUS bit. The ALARM pin can be set to ignore background CRC failures by setting the BACKGROUND\_CRC\_ALARM\_MASK bit of the ALARM\_CONFIG register.

## Overtemperature Warning and Shutdown

To protect the device from damage from overtemperature occurrences during operation, the AD5770R has an overtemperature warning alert and an overtemperature shutdown alert.

When the internal die temperature reaches approximately 125°C, the ALARM pin activates, and the TEMP\_WARNING bit in the status register is set high. The user must read the status register to deassert the ALARM pin.

When the internal die temperature reaches approximately 145°C, the ALARM pin activates (if not already activated) and the OVER\_TEMP bit in the status register is set. The user must read the status register to deassert the ALARM pin.

If the THERMAL\_SHUTDOWN\_EN bit in the ALARM\_CONFIG register is set to high, the device shuts down the output stages to protect from over temperature, and the outputs remain shut down until the user initiates a software or hardware reset to the device.

The TEMP\_WARNING and OVER\_TEMP flags in the status register clear when the device temperature returns below approximately 120°C. To guarantee proper data downloads from the internal memory, a reset function must not be performed when the TEMP\_WARNING bit in the status register is high.

The ALARM pin can be set to ignore over temperature faults and over temperature warnings by setting the OVER\_TEMP\_ALARM\_MASK and TEMP\_WARNING\_ALARM\_MASK bits of the ALARM\_CONFIG register.

## Negative Compliance Voltage

The compliance voltage on IDAC0 pin of the AD5770R can be a negative value when sinking current. The AD5770R has a negative compliance voltage alert feature to protect an external unipolar ADC connected to the MUX\_OUT pin.

The following sequence of events occurs if the user enables voltage monitoring of Channel 0 when the voltage on IDAC0 is negative:

1. The ALARM pin activates.
2. The MUX\_OUT pin is disabled.
3. The NEGATIVE\_CHANNEL0 bit in the status register is set.

The status register must be read to deassert the ALARM pin.

The following sequence of events occurs if the voltage on IDAC0 goes negative after the user enables voltage monitoring of Channel 0:

1. The ALARM pin activates.
2. The MUX\_OUT pin is set to the same voltage as PVDD0.
3. The NEGATIVE\_CHANNEL0 bit in the status register is set.

The status register must be read to deassert the ALARM pin.

The ALARM pin can be set to ignore the negative compliance voltage warning by setting the NEGATIVE\_CHANNEL0\_ALARM\_MASK bit of the ALARM\_CONFIG register.

#### IREF Fault

When the external  $R_{SET}$  resistor option is selected, it is important that the value of this external  $R_{SET}$  resistor cannot create a reference

current that is too high and can damage the device. The AD5770R incorporates an internal protection circuit that protects the device if the reference current is too high.

When the protection circuit detects a reference current that is too high, the following events occur:

1. This circuit switches to the internal  $R_{SET}$  resistor.
2. The ALARM pin activates.
3. The IREF\_FAULT bit in the status register is set.

The user must then read the status register to deassert the ALARM pin. The ALARM pin can be set to ignore IREF faults by setting the IREF\_FAULT\_ALARM\_MASK bit of the ALARM\_CONFIG register.

**Table 10. Full-Scale Output Current Per Channels, for All Scaling Code Values**

| Scaling Code | Channel 0, 0 mA to 300 mA Range (mA) | Channel 1, 0 mA to 140 mA Range (mA) | Channel 1, 0 mA to 250 mA Range (mA) | Channel 2, 0 mA to 55 mA Range (mA) | Channel 2, 0 mA to 150 mA Range (mA) | Channel 3 to Channel 5, 0 mA to 45 mA Range (mA) | Channel 3 to Channel 5, 0 mA to 100 mA Range (mA) |
|--------------|--------------------------------------|--------------------------------------|--------------------------------------|-------------------------------------|--------------------------------------|--------------------------------------------------|---------------------------------------------------|
| 0 (Default)  | 300                                  | 140                                  | 250                                  | 55                                  | 150                                  | 45                                               | 100                                               |
| 1            | 298                                  | 139                                  | 248                                  | 55                                  | 149                                  | 45                                               | 99                                                |
| 2            | 295                                  | 138                                  | 246                                  | 54                                  | 148                                  | 44                                               | 98                                                |
| 3            | 293                                  | 137                                  | 244                                  | 54                                  | 146                                  | 44                                               | 98                                                |
| 4            | 291                                  | 136                                  | 242                                  | 53                                  | 145                                  | 44                                               | 97                                                |
| 5            | 288                                  | 135                                  | 240                                  | 53                                  | 144                                  | 43                                               | 96                                                |
| 6            | 286                                  | 133                                  | 238                                  | 52                                  | 143                                  | 43                                               | 95                                                |
| 7            | 284                                  | 132                                  | 236                                  | 52                                  | 142                                  | 43                                               | 95                                                |
| 8            | 281                                  | 131                                  | 234                                  | 52                                  | 141                                  | 42                                               | 94                                                |
| 9            | 279                                  | 130                                  | 232                                  | 51                                  | 139                                  | 42                                               | 93                                                |
| 10           | 277                                  | 129                                  | 230                                  | 51                                  | 138                                  | 41                                               | 92                                                |
| 11           | 274                                  | 128                                  | 229                                  | 50                                  | 137                                  | 41                                               | 91                                                |
| 12           | 272                                  | 127                                  | 227                                  | 50                                  | 136                                  | 41                                               | 91                                                |
| 13           | 270                                  | 126                                  | 225                                  | 49                                  | 135                                  | 40                                               | 90                                                |
| 14           | 267                                  | 125                                  | 223                                  | 49                                  | 134                                  | 40                                               | 89                                                |
| 15           | 265                                  | 124                                  | 221                                  | 49                                  | 132                                  | 40                                               | 88                                                |
| 16           | 263                                  | 123                                  | 219                                  | 48                                  | 131                                  | 39                                               | 88                                                |
| 17           | 260                                  | 121                                  | 217                                  | 48                                  | 130                                  | 39                                               | 87                                                |
| 18           | 258                                  | 120                                  | 215                                  | 47                                  | 129                                  | 39                                               | 86                                                |
| 19           | 255                                  | 119                                  | 213                                  | 47                                  | 128                                  | 38                                               | 85                                                |
| 20           | 253                                  | 118                                  | 211                                  | 46                                  | 127                                  | 38                                               | 84                                                |
| 21           | 251                                  | 117                                  | 209                                  | 46                                  | 125                                  | 38                                               | 84                                                |
| 22           | 248                                  | 116                                  | 207                                  | 46                                  | 124                                  | 37                                               | 83                                                |
| 23           | 246                                  | 115                                  | 205                                  | 45                                  | 123                                  | 37                                               | 82                                                |
| 24           | 244                                  | 114                                  | 203                                  | 45                                  | 122                                  | 37                                               | 81                                                |
| 25           | 241                                  | 113                                  | 201                                  | 44                                  | 121                                  | 36                                               | 80                                                |
| 26           | 239                                  | 112                                  | 199                                  | 44                                  | 120                                  | 36                                               | 80                                                |
| 27           | 237                                  | 110                                  | 197                                  | 43                                  | 118                                  | 36                                               | 79                                                |
| 28           | 234                                  | 109                                  | 195                                  | 43                                  | 117                                  | 35                                               | 78                                                |
| 29           | 232                                  | 108                                  | 193                                  | 43                                  | 116                                  | 35                                               | 77                                                |
| 30           | 230                                  | 107                                  | 191                                  | 42                                  | 115                                  | 34                                               | 77                                                |
| 31           | 227                                  | 106                                  | 189                                  | 42                                  | 114                                  | 34                                               | 76                                                |

| Scaling Code | Channel 0, 0 mA to 300 mA Range (mA) | Channel 1, 0 mA to 140 mA Range (mA) | Channel 1, 0 mA to 250 mA Range (mA) | Channel 2, 0 mA to 55 mA Range (mA) | Channel 2, 0 mA to 150 mA Range (mA) | Channel 3 to Channel 5, 0 mA to 45 mA Range (mA) | Channel 3 to Channel 5, 0 mA to 100 mA Range (mA) |
|--------------|--------------------------------------|--------------------------------------|--------------------------------------|-------------------------------------|--------------------------------------|--------------------------------------------------|---------------------------------------------------|
| 32           | 225                                  | 105                                  | 188                                  | 41                                  | 113                                  | 34                                               | 75                                                |
| 33           | 223                                  | 104                                  | 186                                  | 41                                  | 111                                  | 33                                               | 74                                                |
| 34           | 220                                  | 103                                  | 184                                  | 40                                  | 110                                  | 33                                               | 73                                                |
| 35           | 218                                  | 102                                  | 182                                  | 40                                  | 109                                  | 33                                               | 73                                                |
| 36           | 216                                  | 101                                  | 180                                  | 40                                  | 108                                  | 32                                               | 72                                                |
| 37           | 213                                  | 100                                  | 178                                  | 39                                  | 107                                  | 32                                               | 71                                                |
| 38           | 211                                  | 98                                   | 176                                  | 39                                  | 105                                  | 32                                               | 70                                                |
| 39           | 209                                  | 97                                   | 174                                  | 38                                  | 104                                  | 31                                               | 70                                                |
| 40           | 206                                  | 96                                   | 172                                  | 38                                  | 103                                  | 31                                               | 69                                                |
| 41           | 204                                  | 95                                   | 170                                  | 37                                  | 102                                  | 31                                               | 68                                                |
| 42           | 202                                  | 94                                   | 168                                  | 37                                  | 101                                  | 30                                               | 67                                                |
| 43           | 199                                  | 93                                   | 166                                  | 37                                  | 100                                  | 30                                               | 66                                                |
| 44           | 197                                  | 92                                   | 164                                  | 36                                  | 98                                   | 30                                               | 66                                                |
| 45           | 195                                  | 91                                   | 162                                  | 36                                  | 97                                   | 29                                               | 65                                                |
| 46           | 192                                  | 90                                   | 160                                  | 35                                  | 96                                   | 29                                               | 64                                                |
| 47           | 190                                  | 89                                   | 158                                  | 35                                  | 95                                   | 28                                               | 63                                                |
| 48           | 188                                  | 88                                   | 156                                  | 34                                  | 94                                   | 28                                               | 63                                                |
| 49           | 185                                  | 86                                   | 154                                  | 34                                  | 93                                   | 28                                               | 62                                                |
| 50           | 183                                  | 85                                   | 152                                  | 34                                  | 91                                   | 27                                               | 61                                                |
| 51           | 180                                  | 84                                   | 150                                  | 33                                  | 90                                   | 27                                               | 60                                                |
| 52           | 178                                  | 83                                   | 148                                  | 33                                  | 89                                   | 27                                               | 59                                                |
| 53           | 176                                  | 82                                   | 146                                  | 32                                  | 88                                   | 26                                               | 59                                                |
| 54           | 173                                  | 81                                   | 145                                  | 32                                  | 87                                   | 26                                               | 58                                                |
| 55           | 171                                  | 80                                   | 143                                  | 31                                  | 86                                   | 26                                               | 57                                                |
| 56           | 169                                  | 79                                   | 141                                  | 31                                  | 84                                   | 25                                               | 56                                                |
| 57           | 166                                  | 78                                   | 139                                  | 31                                  | 83                                   | 25                                               | 55                                                |
| 58           | 164                                  | 77                                   | 137                                  | 30                                  | 82                                   | 25                                               | 55                                                |
| 59           | 162                                  | 75                                   | 135                                  | 30                                  | 81                                   | 24                                               | 54                                                |
| 60           | 159                                  | 74                                   | 133                                  | 29                                  | 80                                   | 24                                               | 53                                                |
| 61           | 157                                  | 73                                   | 131                                  | 29                                  | 79                                   | 24                                               | 52                                                |
| 62           | 155                                  | 72                                   | 129                                  | 28                                  | 77                                   | 23                                               | 52                                                |
| 63           | 152                                  | 71                                   | 127                                  | 28                                  | 76                                   | 23                                               | 51                                                |

## APPLICATIONS INFORMATION

### MICROPROCESSOR INTERFACING

Microprocessor interfacing to the AD5770R is via a serial bus that uses a standard protocol compatible with DSPs and microcontrollers. The communications channel requires a 4-wire serial interface consisting of a clock signal, a data input signal, a data output signal, and a synchronization signal.

### AD5770R TO SPI INTERFACE

The SPI interface of the AD5770R is designed to be easily connected to industry-standard DSPs and microcontrollers. Figure 76 shows the AD5770R connected to the ADuCM320. The ADuCM320 has an integrated SPI port that can be connected directly to the SPI pins of the AD5770R.

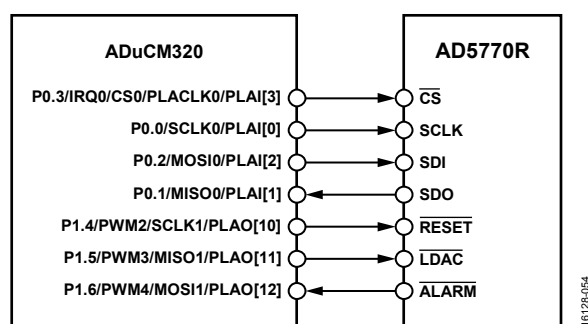


Figure 76. ADuCM320 SPI Interface

### THERMAL CONSIDERATIONS

The AD5770R has a maximum junction temperature of 150°C (see Table 5). To ensure reliable and specified operation over the lifetime of the device, it is important that the AD5770R is not operated under conditions that cause the junction temperature to exceed 150°C. The junction temperature is directly affected by the power dissipated across the AD5770R and the ambient temperature.

Table 1 specifies the output current ranges for each AD5770R channel and the maximum power supply voltages. Therefore, it is important to understand the effects of power dissipation on the package and the effects the package has on the junction temperature. The AD5770R is packaged in a 49-ball, 4 mm × 4 mm, wafer level chip scale packaging (WLCSP) package. The thermal impedance,  $\theta_{JA}$ , is specified in Table 6.

Table 11 provides examples of the maximum allowed power dissipation and the maximum allowed ambient temperature under certain conditions.

### COMBINING CHANNELS TO INCREASE CURRENT RANGE

The maximum current that can be sourced from IDAC0 is 300 mA. It is possible to increase the current source capability by connecting two channels directly together. Figure 77 shows IDAC1 combined with IDAC2 to create a full-scale output current of 400 mA. When channels are combined, care must be taken to ensure the following:

- The output compliance voltage stays within the range specified in Table 1.
- The output voltage stays within the absolute maximum ratings specified in Table 5.

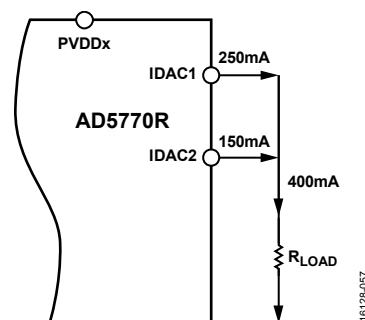


Figure 77. Increasing the Current Range by Summing Channels

### LAYOUT GUIDELINES

Take careful consideration of the power supply and ground return layout in order to ensure the rated performance. Design the PCB on which the AD5770R is mounted so that the AD5770R lies on the analog plane.

The AD5770R must have an ample supply bypassing of 10  $\mu$ F in parallel with 0.1  $\mu$ F on each supply, located as close to the package as possible (ideally directly against the device). The 10  $\mu$ F capacitors are the tantalum bead type. The 0.1  $\mu$ F capacitor must have low effective series resistance (ESR) and low effective series inductance (ESI). Common ceramic capacitors provide a low impedance path to ground at high frequencies to handle transient currents, due to internal logic switching.

Ensure that the power supply line has as large a trace as possible to provide a low impedance path and reduce glitch effects on the supply line. Shield clocks and other fast switching digital signals from other parts of the board by using a digital ground. Avoid crossover of digital and analog signals if possible. When traces cross on opposite sides of the board, ensure that they run at right angles to each other to reduce feedthrough effects through the board. The best board layout technique is the microstrip technique, where the component side of the board is dedicated to the ground plane only, and the signal traces are placed on the solder side. However, this technique is not always possible with a 2-layer board.

Because the AD5770R can dissipate a large amount of power, it is recommended to provide some heat sinking capability to allow power to dissipate easily.

For the WLCSP package, heat is transferred through the solder balls to the PCB board.  $\theta_{JA}$  thermal impedance is dependent on board construction. More copper layers enable heat to be removed more effectively.

If using an external  $R_{SET}$  resistor, the low side of the  $R_{SET}$  resistor must be connected to REFGND before the connection to AGND. Ensure that the width of the trace connecting  $R_{SET}$  to the IREF pin is as wide as possible to reduce the resistance and the temperature coefficient of the trace.

**Table 11. Thermal Considerations for 49-Ball WLCSP Package**

| Parameter                                  | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
|--------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Maximum Power Dissipation <sup>1</sup>     | Maximum allowed AD5770R power dissipation ( $P_{DISS}$ ) when operating at an ambient temperature of 105°C,<br>$\frac{T_{JMAX} - T_A}{\theta_{JA}} = \frac{150^\circ\text{C} - 105^\circ\text{C}}{30^\circ\text{C} / \text{W}} = 1.5 \text{ W}$                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| Recommended Power Dissipation <sup>1</sup> | Maximum recommended AD5770R $P_{DISS}$ when operating at an ambient temperature of 85°C and a junction temperature of 115°C,<br>$\frac{T_J - T_A}{\theta_{JA}} = \frac{115^\circ\text{C} - 85^\circ\text{C}}{30^\circ\text{C} / \text{W}} = 1 \text{ W}$                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
| Ambient Temperature <sup>1</sup>           | Maximum recommended ambient temperature when dissipating 980.4 mW across the AD5770R while maintaining a junction temperature of 115°C.<br>$T_J - P_{DISS} \times \theta_{JA} = 115^\circ\text{C} - (980.4\text{mW} \times 30^\circ\text{C}/\text{W}) = 85.58^\circ\text{C}$<br>Power dissipation calculation example:<br>AVDD = DVDD = IOVDD = 3.3 V, PVDDx = 2.5 V<br>AVEE = PVEE0 = 0 V, $R_{LOAD} = 6 \Omega$ per channel, AD5770R quiescent power dissipation = 110 mW<br>IDAC0 = 300 mA, power dissipation = 210 mW<br>IDAC1 = 150 mA, power dissipation = 240 mW<br>IDAC2 = 55 mA, power dissipation = 119.35 mW<br>IDAC3, IDAC4, IDAC5 = 45 mA, power dissipation = 301.05 mW<br>Total power dissipation = 110 mW + 870.4 mW = 980.4 W |

<sup>1</sup>  $T_{JMAX}$  in Table 5 is the junction temperature that the AD5770R can tolerate, but not operate at. It is recommended that the junction temperature does not exceed 115°C.

# REGISTER SUMMARY

## SPI CONFIGURATION REGISTERS

Table 12. AD5770R SPI Configuration Register Summary

| Reg  | Name               | Bits  | Bit 7               | Bit 6    | Bit 5                  | Bit 4          | Bit 3             | Bit 2              | Bit 1    | Bit 0        | Reset | R/W |
|------|--------------------|-------|---------------------|----------|------------------------|----------------|-------------------|--------------------|----------|--------------|-------|-----|
| 0x00 | INTERFACE_CONFIG_A | [7:0] | SW_RESET_MSB        | Reserved | ADDR_ASCENSION_MSB     | SDO_ACTIVE_MSB | SDO_ACTIVE_LSB    | ADDR_ASCENSION_LSB | Reserved | SW_RESET_LSB | 0x18  | R/W |
| 0x01 | INTERFACE_CONFIG_B | [7:0] | SINGLE_INST         | Reserved |                        |                | SHORT_INSTRUCTION | Reserved           |          |              | 0x08  | R/W |
| 0x03 | CHIP_TYPE          | [7:0] | Reserved            |          |                        |                | CHIP_TYPE         |                    |          |              | 0x08  | R   |
| 0x04 | PRODUCT_ID_L       | [7:0] | PRODUCT_ID[7:0]     |          |                        |                |                   |                    |          |              | 0x04  | R   |
| 0x05 | PRODUCT_ID_H       | [7:0] | PRODUCT_ID[15:8]    |          |                        |                |                   |                    |          |              | 0x40  | R   |
| 0x06 | CHIP_GRADE         | [7:0] | GRADE               |          |                        |                | DEVICE_REVISION   |                    |          |              | 0x00  | R   |
| 0x0A | SCRATCH_PAD        | [7:0] | VALUE               |          |                        |                |                   |                    |          |              | 0x00  | R/W |
| 0x0B | SPI_REVISION       | [7:0] | VERSION             |          |                        |                |                   |                    |          |              | 0x82  | R   |
| 0x0C | VENDOR_L           | [7:0] | VID[7:0]            |          |                        |                |                   |                    |          |              | 0x56  | R   |
| 0x0D | VENDOR_H           | [7:0] | VID[15:8]           |          |                        |                |                   |                    |          |              | 0x04  | R   |
| 0x0E | STREAM_MODE        | [7:0] | LENGTH              |          |                        |                |                   |                    |          |              | 0x00  | R/W |
| 0x10 | INTERFACE_CONFIG_C | [7:0] | Reserved            |          | STRICT_REGISTER_ACCESS | Reserved       |                   |                    |          |              | 0x20  | R   |
| 0x11 | INTERFACE_STATUS_A | [7:0] | INTERFACE_NOT_READY | Reserved |                        |                |                   |                    |          |              | 0x00  | R   |

## AD5770R CONFIGURATION REGISTERS

Table 13. AD5770R Configuration Register Summary

| Reg  | Name              | Bits  | Bit 7                     | Bit 6                 | Bit 5                        | Bit 4                | Bit 3                   | Bit 2                  | Bit 1                 | Bit 0          | Reset | R/W  |     |
|------|-------------------|-------|---------------------------|-----------------------|------------------------------|----------------------|-------------------------|------------------------|-----------------------|----------------|-------|------|-----|
| 0x14 | CHANNEL_CONFIG    | [7:0] | CH0_SINK_EN               | Reserved              | CH5_SHUTDOWN_B               | CH4_SHUTDOWN_B       | CH3_SHUTDOWN_B          | CH2_SHUTDOWN_B         | CH1_SHUTDOWN_B        | CH0_SHUTDOWN_B | 0x80  | R/W  |     |
| 0x15 | OUTPUT_RANGE_CH0  | [7:0] | CH0_OUTPUT_SCALING        |                       |                              |                      |                         |                        | CH0_MODE              |                | 0x00  | R/W  |     |
| 0x16 | OUTPUT_RANGE_CH1  | [7:0] | CH1_OUTPUT_SCALING        |                       |                              |                      |                         |                        | CH1_MODE              |                | 0x02  | R/W  |     |
| 0x17 | OUTPUT_RANGE_CH2  | [7:0] | CH2_OUTPUT_SCALING        |                       |                              |                      |                         |                        | Reserved              | CH2_MODE       | 0x00  | R/W  |     |
| 0x18 | OUTPUT_RANGE_CH3  | [7:0] | CH3_OUTPUT_SCALING        |                       |                              |                      |                         |                        | Reserved              | CH3_MODE       | 0x00  | R/W  |     |
| 0x19 | OUTPUT_RANGE_CH4  | [7:0] | CH4_OUTPUT_SCALING        |                       |                              |                      |                         |                        | Reserved              | CH4_MODE       | 0x00  | R/W  |     |
| 0x1A | OUTPUT_RANGE_CH5  | [7:0] | CH5_OUTPUT_SCALING        |                       |                              |                      |                         |                        | Reserved              | CH5_MODE       | 0x00  | R/W  |     |
| 0x1B | REFERENCE         | [7:0] | Reserved                  |                       |                              |                      |                         | REFERENCE_RESISTOR_SEL | REFERENCE_VOLTAGE_SEL |                | 0x00  | R/W  |     |
| 0x1C | ALARM_CONFIG      | [7:0] | BACKGROUND_CRC_ALARM_MASK | IREF_FAULT_ALARM_MASK | NEGATIVE_CHANNEL0_ALARM_MASK | OVER_TEMP_ALARM_MASK | TEMP_WARNING_ALARM_MASK | BACKGROUND_CRC_EN      | THERMAL_SHUTDOWN_EN   | OPEN_DRAIN_EN  | 0x06  | R/W  |     |
| 0x1D | OUTPUT_FILTER_CH0 | [7:0] | Reserved                  |                       |                              |                      | OUTPUT_FILTER_RESISTOR0 |                        |                       |                |       | 0x00 | R/W |
| 0x1E | OUTPUT_FILTER_CH1 | [7:0] | Reserved                  |                       |                              |                      | OUTPUT_FILTER_RESISTOR1 |                        |                       |                |       | 0x00 | R/W |
| 0x1F | OUTPUT_FILTER_CH2 | [7:0] | Reserved                  |                       |                              |                      | OUTPUT_FILTER_RESISTOR2 |                        |                       |                |       | 0x00 | R/W |
| 0x20 | OUTPUT_FILTER_CH3 | [7:0] | Reserved                  |                       |                              |                      | OUTPUT_FILTER_RESISTOR3 |                        |                       |                |       | 0x00 | R/W |

| Reg  | Name                | Bits  | Bit 7                 | Bit 6    | Bit 5            | Bit 4            | Bit 3                   | Bit 2             | Bit 1            | Bit 0            | Reset | R/W |
|------|---------------------|-------|-----------------------|----------|------------------|------------------|-------------------------|-------------------|------------------|------------------|-------|-----|
| 0x21 | OUTPUT_FILTER_CH4   | [7:0] | Reserved              |          |                  |                  | OUTPUT_FILTER_RESISTOR4 |                   |                  |                  | 0x00  | R/W |
| 0x22 | OUTPUT_FILTER_CH5   | [7:0] | Reserved              |          |                  |                  | OUTPUT_FILTER_RESISTOR5 |                   |                  |                  | 0x00  | R/W |
| 0x23 | MONITOR_SETUP       | [7:0] | MON_FUNCTION          |          | MUX_BUFFER       | IB_EXT_EN        | MON_CH                  |                   |                  |                  | 0x00  | R/W |
| 0x24 | STATUS              | [7:0] | BACKGROUND_CRC_STATUS | Reserved |                  |                  | IREF_FAULT              | NEGATIVE_CHANNEL0 | OVER_TEMP        | TEMP_WARNING     | 0x00  | R   |
| 0x25 | HW_LDAC             | [7:0] | Reserved              |          | HW_LDAC_MASK_CH5 | HW_LDAC_MASK_CH4 | HW_LDAC_MASK_CH3        | HW_LDAC_MASK_CH2  | HW_LDAC_MASK_CH1 | HW_LDAC_MASK_CH0 | 0x00  | R/W |
| 0x26 | CH0_DAC_LSB         | [7:0] | DAC_DATA0[5:0]        |          |                  |                  |                         |                   | Reserved         |                  | 0x00  | R/W |
| 0x27 | CH0_DAC_MSB         | [7:0] | DAC_DATA0[13:6]       |          |                  |                  |                         |                   |                  |                  | 0x00  | R/W |
| 0x28 | CH1_DAC_LSB         | [7:0] | DAC_DATA1[5:0]        |          |                  |                  |                         |                   | Reserved         |                  | 0x00  | R/W |
| 0x29 | CH1_DAC_MSB         | [7:0] | DAC_DATA1[13:6]       |          |                  |                  |                         |                   |                  |                  | 0x00  | R/W |
| 0x2A | CH2_DAC_LSB         | [7:0] | DAC_DATA2[5:0]        |          |                  |                  |                         |                   | Reserved         |                  | 0x00  | R/W |
| 0x2B | CH2_DAC_MSB         | [7:0] | DAC_DATA2[13:6]       |          |                  |                  |                         |                   |                  |                  | 0x00  | R/W |
| 0x2C | CH3_DAC_LSB         | [7:0] | DAC_DATA3[5:0]        |          |                  |                  |                         |                   | Reserved         |                  | 0x00  | R/W |
| 0x2D | CH3_DAC_MSB         | [7:0] | DAC_DATA3[13:6]       |          |                  |                  |                         |                   |                  |                  | 0x00  | R/W |
| 0x2E | CH4_DAC_LSB         | [7:0] | DAC_DATA4[5:0]        |          |                  |                  |                         |                   | Reserved         |                  | 0x00  | R/W |
| 0x2F | CH4_DAC_MSB         | [7:0] | DAC_DATA4[13:6]       |          |                  |                  |                         |                   |                  |                  | 0x00  | R/W |
| 0x30 | CH5_DAC_LSB         | [7:0] | DAC_DATA5[5:0]        |          |                  |                  |                         |                   | Reserved         |                  | 0x00  | R/W |
| 0x31 | CH5_DAC_MSB         | [7:0] | DAC_DATA5[13:6]       |          |                  |                  |                         |                   |                  |                  | 0x00  | R/W |
| 0x32 | DAC_PAGE_MASK_LSB   | [7:0] | DAC_PAGE_MASK[5:0]    |          |                  |                  |                         |                   | Reserved         |                  | 0x00  | R/W |
| 0x33 | DAC_PAGE_MASK_MSB   | [7:0] | DAC_PAGE_MASK[13:6]   |          |                  |                  |                         |                   |                  |                  | 0x00  | R/W |
| 0x34 | CH_SELECT           | [7:0] | Reserved              |          | SEL_CH5          | SEL_CH4          | SEL_CH3                 | SEL_CH2           | SEL_CH1          | SEL_CH0          | 0x00  | R/W |
| 0x35 | INPUT_PAGE_MASK_LSB | [7:0] | INPUT_PAGE_MASK[5:0]  |          |                  |                  |                         |                   | Reserved         |                  | 0x00  | R/W |
| 0x36 | INPUT_PAGE_MASK_MSB | [7:0] | INPUT_PAGE_MASK[13:6] |          |                  |                  |                         |                   |                  |                  | 0x00  | R/W |
| 0x37 | SW_LDAC             | [7:0] | Reserved              |          | SW_LDAC_CH5      | SW_LDAC_CH4      | SW_LDAC_CH3             | SW_LDAC_CH2       | SW_LDAC_CH1      | SW_LDAC_CH0      | 0x00  | W   |
| 0x38 | CH0_INPUT_LSB       | [7:0] | INPUT_DATA0[5:0]      |          |                  |                  |                         |                   | Reserved         |                  | 0x00  | R/W |
| 0x39 | CH0_INPUT_MSB       | [7:0] | INPUT_DATA0[13:6]     |          |                  |                  |                         |                   |                  |                  | 0x00  | R/W |
| 0x3A | CH1_INPUT_LSB       | [7:0] | INPUT_DATA1[5:0]      |          |                  |                  |                         |                   | Reserved         |                  | 0x00  | R/W |
| 0x3B | CH1_INPUT_MSB       | [7:0] | INPUT_DATA1[13:6]     |          |                  |                  |                         |                   |                  |                  | 0x00  | R/W |
| 0x3C | CH2_INPUT_LSB       | [7:0] | INPUT_DATA2[5:0]      |          |                  |                  |                         |                   | Reserved         |                  | 0x00  | R/W |
| 0x3D | CH2_INPUT_MSB       | [7:0] | INPUT_DATA2[13:6]     |          |                  |                  |                         |                   |                  |                  | 0x00  | R/W |
| 0x3E | CH3_INPUT_LSB       | [7:0] | INPUT_DATA3[5:0]      |          |                  |                  |                         |                   | Reserved         |                  | 0x00  | R/W |
| 0x3F | CH3_INPUT_MSB       | [7:0] | INPUT_DATA3[13:6]     |          |                  |                  |                         |                   |                  |                  | 0x00  | R/W |
| 0x40 | CH4_INPUT_LSB       | [7:0] | INPUT_DATA4[5:0]      |          |                  |                  |                         |                   | Reserved         |                  | 0x00  | R/W |

| Reg  | Name          | Bits  | Bit 7             | Bit 6 | Bit 5     | Bit 4 | Bit 3 | Bit 2 | Bit 1    | Bit 0 | Reset | R/W |
|------|---------------|-------|-------------------|-------|-----------|-------|-------|-------|----------|-------|-------|-----|
| 0x41 | CH4_INPUT_MSB | [7:0] | INPUT_DATA4[13:6] |       |           |       |       |       |          |       | 0x00  | R/W |
| 0x42 | CH5_INPUT_LSB | [7:0] | INPUT_DATA5[5:0]  |       |           |       |       |       | Reserved |       | 0x00  | R/W |
| 0x43 | CH5_INPUT_MSB | [7:0] | INPUT_DATA5[13:6] |       |           |       |       |       |          |       | 0x00  | R/W |
| 0x44 | RESERVED      | [7:0] | RESERVED0         |       | RESERVED1 |       |       |       |          |       | 0x3F  | R   |

## REGISTER DETAILS

Address: 0x00, Reset: 0x18, Name: INTERFACE\_CONFIG\_A

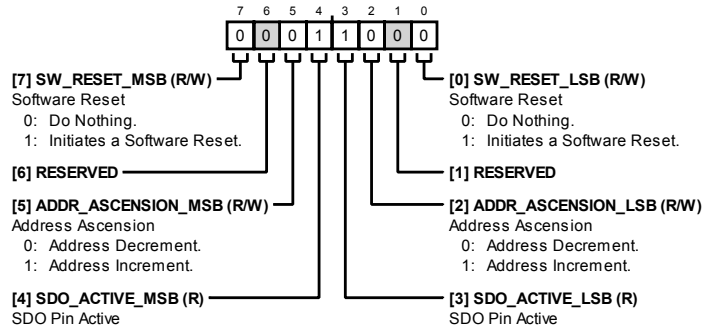


Table 14. Bit Descriptions for INTERFACE\_CONFIG\_A

| Bits | Bit Name           | Description                                                                                                                                                                                                                                          | Reset | Access |
|------|--------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------|--------|
| 7    | SW_RESET_MSB       | Software Reset. Setting both software reset bits in a single SPI write performs a software reset on the device, returning all registers except INTERFACE_CONFIG_A to the default power-up state.<br>0: do nothing.<br>1: initiates a software reset. | 0x0   | R/W    |
| 6    | Reserved           | Reserved.                                                                                                                                                                                                                                            | 0x0   | R      |
| 5    | ADDR_ASCENSION_MSB | Address Ascension. When set, this bit causes incrementing streaming addresses; otherwise, decrementing addresses are generated. This must be a mirror of ADDR_ASCENSION_LSB.<br>0: address decrement.<br>1: address increment.                       | 0x0   | R/W    |
| 4    | SDO_ACTIVE_MSB     | SDO Pin Active. SDO pin enabled. This bit is always set.                                                                                                                                                                                             | 0x1   | R      |
| 3    | SDO_ACTIVE_LSB     | SDO Pin Active. SDO pin enabled. This bit is always set.                                                                                                                                                                                             | 0x1   | R      |
| 2    | ADDR_ASCENSION_LSB | Address Ascension. When set, this bit causes incrementing streaming addresses; otherwise, decrementing addresses are generated. This must be a mirror of ADDR_ASCENSION_MSB.<br>0: address decrement.<br>1: address increment.                       | 0x0   | R/W    |
| 1    | Reserved           | Reserved.                                                                                                                                                                                                                                            | 0x0   | R      |
| 0    | SW_RESET_LSB       | Software Reset. Setting both software reset bits in a single SPI write performs a software reset on the device, returning all registers except INTERFACE_CONFIG_A to the default power up state.<br>0: do nothing.<br>1: initiates a software reset. | 0x0   | R/W    |

Address: 0x01, Reset: 0x08, Name: INTERFACE\_CONFIG\_B

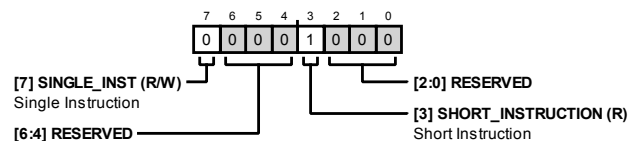


Table 15. Bit Descriptions for INTERFACE\_CONFIG\_B

| Bits  | Bit Name          | Description                                                                                                                                                                                             | Reset | Access |
|-------|-------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------|--------|
| 7     | SINGLE_INST       | Single Instruction. When this bit is set, streaming mode is disable, and each SPI transaction must specify the register address to access.<br>0: streaming mode enabled.<br>1: streaming mode disabled. | 0x0   | R/W    |
| [6:4] | Reserved          | Reserved.                                                                                                                                                                                               | 0x0   | R      |
| 3     | SHORT_INSTRUCTION | Short Instruction. When this bit is set, the address word must be 7 bits long.                                                                                                                          | 0x01  | R      |
| [2:0] | Reserved          | Reserved.                                                                                                                                                                                               | 0x0   | R      |

Address: 0x03, Reset: 0x08, Name: CHIP\_TYPE

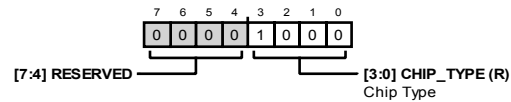


Table 16. Bit Descriptions for CHIP\_TYPE

| Bits  | Bit Name  | Description                                | Reset | Access |
|-------|-----------|--------------------------------------------|-------|--------|
| [7:4] | Reserved  | Reserved.                                  | 0x0   | R      |
| [3:0] | CHIP_TYPE | Chip Type. Precision DAC chip type = 0x08. | 0x8   | R      |

Address: 0x04, Reset: 0x04, Name: PRODUCT\_ID\_L

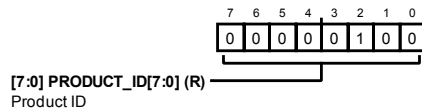


Table 17. Bit Descriptions for PRODUCT\_ID\_L

| Bits  | Bit Name        | Description                              | Reset | Access |
|-------|-----------------|------------------------------------------|-------|--------|
| [7:0] | PRODUCT_ID[7:0] | Product ID. AD5770R product ID = 0x4004. | 0x4   | R      |

Address: 0x05, Reset: 0x40, Name: PRODUCT\_ID\_H

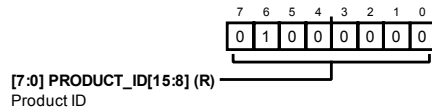


Table 18. Bit Descriptions for PRODUCT\_ID\_H

| Bits  | Bit Name         | Description                              | Reset | Access |
|-------|------------------|------------------------------------------|-------|--------|
| [7:0] | PRODUCT_ID[15:8] | Product ID. AD5770R product ID = 0x4004. | 0x40  | R      |

Address: 0x06, Reset: 0x00, Name: CHIP\_GRADE

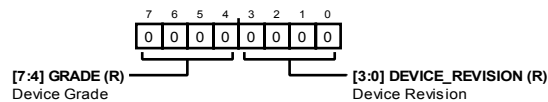


Table 19. Bit Descriptions for CHIP\_GRADE

| Bits  | Bit Name        | Description     | Reset | Access |
|-------|-----------------|-----------------|-------|--------|
| [7:4] | Grade           | Device Grade    | 0x0   | R      |
| [3:0] | DEVICE_REVISION | Device Revision | 0x0   | R      |

Address: 0x0A, Reset: 0x00, Name: SCRATCH\_PAD

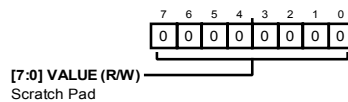


Table 20. Bit Descriptions for SCRATCH\_PAD

| Bits  | Bit Name | Description                                                              | Reset | Access |
|-------|----------|--------------------------------------------------------------------------|-------|--------|
| [7:0] | Value    | Scratch Pad. Use this is register to test communication with the device. | 0x0   | R/W    |

Address: 0x0B, Reset: 0x82, Name: SPI\_REVISION

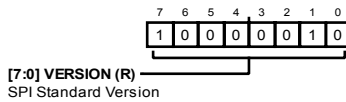


Table 21. Bit Descriptions for SPI\_REVISION

| Bits  | Bit Name | Description                                             | Reset | Access |
|-------|----------|---------------------------------------------------------|-------|--------|
| [7:0] | Version  | SPI Standard Version. Analog Devices SPI standard used. | 0x82  | R      |

Address: 0x0C, Reset: 0x56, Name: VENDOR\_L

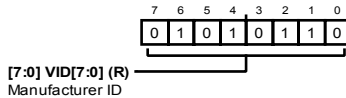


Table 22. Bit Descriptions for VENDOR\_L

| Bits  | Bit Name | Description                                  | Reset | Access |
|-------|----------|----------------------------------------------|-------|--------|
| [7:0] | VID[7:0] | Manufacturer ID. Analog Devices ID = 0x0456. | 0x56  | R      |

Address: 0x0D, Reset: 0x04, Name: VENDOR\_H

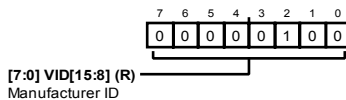


Table 23. Bit Descriptions for VENDOR\_H

| Bits  | Bit Name  | Description                                  | Reset | Access |
|-------|-----------|----------------------------------------------|-------|--------|
| [7:0] | VID[15:8] | Manufacturer ID. Analog Devices ID = 0x0456. | 0x4   | R      |

Address: 0x0E, Reset: 0x00, Name: STREAM\_MODE

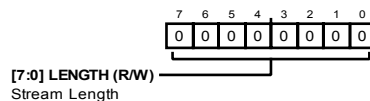


Table 24. Bit Descriptions for STREAM\_MODE

| Bits  | Bit Name | Description                                                                                                                                                                                                                                                                                                                                                                                                      | Reset | Access |
|-------|----------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------|--------|
| [7:0] | LENGTH   | Stream Length. These bits set the length of registers addresses to increment/decrement when streaming multiple bytes of data before looping back to the first register address. When the contents of this register are cleared, register addresses increment/decrement when in streaming mode until the end of the address space before looping to the last/first address and continuing to increment/decrement. | 0x0   | R/W    |

Address: 0x10, Reset: 0x20, Name: INTERFACE\_CONFIG\_C

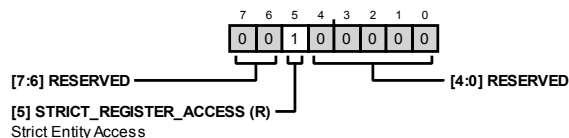


Table 25. Bit Descriptions for INTERFACE\_CONFIG\_C

| Bits  | Bit Name               | Description                                                                                                                                                                                                                                                                                      | Reset | Access |
|-------|------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------|--------|
| [7:6] | Reserved               | Reserved.                                                                                                                                                                                                                                                                                        | 0x0   | R      |
| 5     | STRICT_REGISTER_ACCESS | Strict Register Access. When this bit is set, all multibyte registers must be written to in a single SPI transaction. The address used must be the address of the most significant byte when address ascension is off or the address of the least significant byte when address ascension is on. | 0x1   | R      |
| [4:0] | Reserved               | Reserved.                                                                                                                                                                                                                                                                                        | 0x0   | R      |

Address: 0x11, Reset: 0x00, Name: INTERFACE\_STATUS\_A

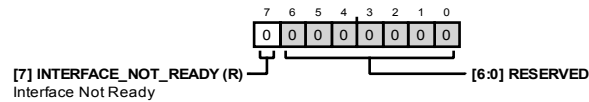


Table 26. Bit Descriptions for INTERFACE\_STATUS\_A

| Bits  | Bit Name            | Description                                                                                        | Reset | Access |
|-------|---------------------|----------------------------------------------------------------------------------------------------|-------|--------|
| 7     | INTERFACE_NOT_READY | Interface Not Ready. When this bit is set, the device is not ready to receive data on the SPI bus. | 0x0   | R      |
| [6:0] | Reserved            | Reserved.                                                                                          | 0x0   | R      |

Address: 0x14, Reset: 0x80, Name: CHANNEL\_CONFIG

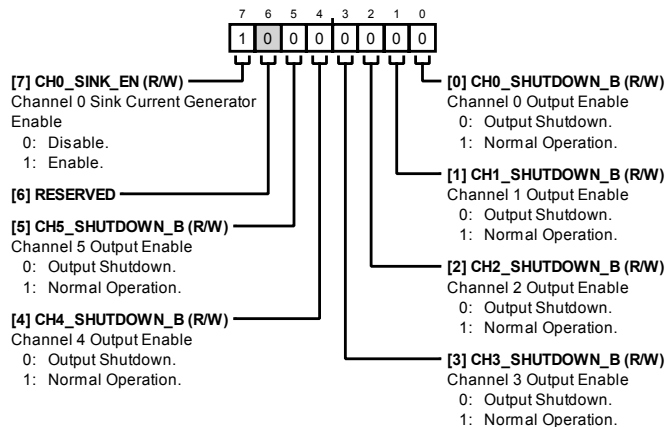


Table 27. Bit Descriptions for CHANNEL\_CONFIG

| Bits | Bit Name       | Description                                                                                                                                      | Reset | Access |
|------|----------------|--------------------------------------------------------------------------------------------------------------------------------------------------|-------|--------|
| 7    | CH0_SINK_EN    | Channel 0 Sink Current Generator Enable. When this bit is set, Channel 0 sink current is enabled.<br>0: disable.<br>1: enable.                   | 0x1   | R/W    |
| 6    | Reserved       | Reserved.                                                                                                                                        | 0x0   | R      |
| 5    | CH5_SHUTDOWN_B | Channel 5 Output Enable. This active low enable bit shuts down the output of IDAC5 when asserted.<br>0: output shutdown.<br>1: normal operation. | 0x0   | R/W    |
| 4    | CH4_SHUTDOWN_B | Channel 4 Output Enable. This active low enable bit shuts down the output of IDAC4 when asserted.<br>0: output shutdown.<br>1: normal operation. | 0x0   | R/W    |
| 3    | CH3_SHUTDOWN_B | Channel 3 Output Enable. This active low enable bit shuts down the output of IDAC3 when asserted.<br>0: output shutdown.<br>1: normal operation. | 0x0   | R/W    |
| 2    | CH2_SHUTDOWN_B | Channel 2 Output Enable. This active low enable bit shuts down the output of IDAC2 when asserted.<br>0: output shutdown.<br>1: normal operation. | 0x0   | R/W    |
| 1    | CH1_SHUTDOWN_B | Channel 1 Output Enable. This active low enable bit shuts down the output of IDAC1 when asserted.<br>0: output shutdown.<br>1: normal operation. | 0x0   | R/W    |

| Bits | Bit Name       | Description                                                                                                                                      | Reset | Access |
|------|----------------|--------------------------------------------------------------------------------------------------------------------------------------------------|-------|--------|
| 0    | CH0_SHUTDOWN_B | Channel 0 Output Enable. This active low enable bit shuts down the output of IDAC0 when asserted.<br>0: output shutdown.<br>1: normal operation. | 0x0   | R/W    |

Address: 0x15, Reset: 0x00, Name: OUTPUT\_RANGE\_CH0

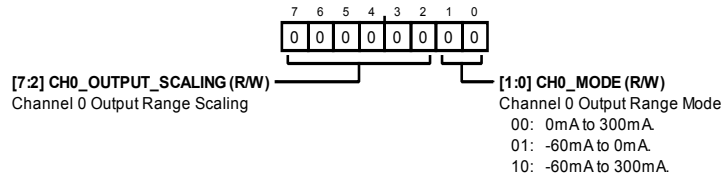


Table 28. Bit Descriptions for OUTPUT\_RANGE\_CH0

| Bits  | Bit Name           | Description                                                                                                                                                     | Reset | Access |
|-------|--------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------|-------|--------|
| [7:2] | CH0_OUTPUT_SCALING | Channel 0 Output Range Scaling. These bits set the output range scaling factor for Channel 0. Output scaling must only be used when in a sourcing current mode. | 0x0   | R/W    |
| [1:0] | CH0_MODE           | Channel 0 Output Range Mode. These bits select the output range mode for Channel 0.<br>00: 0 mA to 300 mA.<br>01: -60 mA to 0 mA.<br>10: -60 mA to +300 mA.     | 0x0   | R/W    |

Address: 0x16, Reset: 0x02, Name: OUTPUT\_RANGE\_CH1

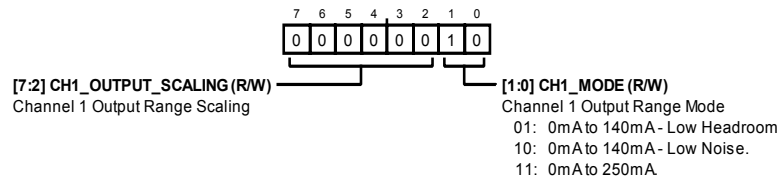


Table 29. Bit Descriptions for OUTPUT\_RANGE\_CH1

| Bits  | Bit Name           | Description                                                                                                                                                                     | Reset | Access |
|-------|--------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------|--------|
| [7:2] | CH1_OUTPUT_SCALING | Channel 1 Output Range Scaling. These bits set the output range scaling factor for Channel 1.                                                                                   | 0x0   | R/W    |
| [1:0] | CH1_MODE           | Channel 1 Output Range Mode. These bits select the output range mode for Channel 1.<br>01: 0 mA to 140 mA low headroom.<br>10: 0 mA to 140 mA low noise.<br>11: 0 mA to 250 mA. | 0x2   | R/W    |

Address: 0x17, Reset: 0x00, Name: OUTPUT\_RANGE\_CH2

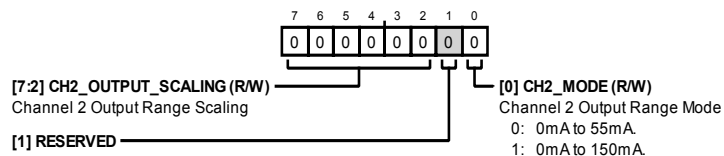


Table 30. Bit Descriptions for OUTPUT\_RANGE\_CH2

| Bits  | Bit Name           | Description                                                                                                                   | Reset | Access |
|-------|--------------------|-------------------------------------------------------------------------------------------------------------------------------|-------|--------|
| [7:2] | CH2_OUTPUT_SCALING | Channel 2 Output Range Scaling. These bits set the output range scaling factor for Channel 2.                                 | 0x0   | R/W    |
| 1     | Reserved           | Reserved.                                                                                                                     | 0x0   | R      |
| 0     | CH2_MODE           | Channel 2 Output Range Mode. This bit selects the output range mode for Channel 2.<br>0: 0 mA to 55 mA.<br>1: 0 mA to 150 mA. | 0x0   | R/W    |

Address: 0x18, Reset: 0x00, Name: OUTPUT\_RANGE\_CH3

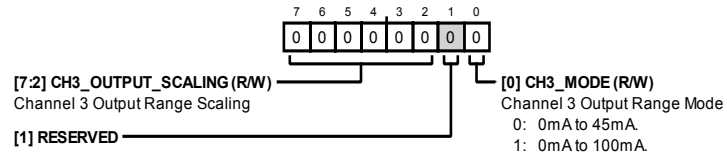


Table 31. Bit Descriptions for OUTPUT\_RANGE\_CH3

| Bits  | Bit Name           | Description                                                                                                                   | Reset | Access |
|-------|--------------------|-------------------------------------------------------------------------------------------------------------------------------|-------|--------|
| [7:2] | CH3_OUTPUT_SCALING | Channel 3 Output Range Scaling. These bits set the output range scaling factor for Channel 3.                                 | 0x0   | R/W    |
| 1     | Reserved           | Reserved.                                                                                                                     | 0x0   | R      |
| 0     | CH3_MODE           | Channel 3 Output Range Mode. This bit selects the output range mode for Channel 3.<br>0: 0 mA to 45 mA.<br>1: 0 mA to 100 mA. | 0x0   | R/W    |

Address: 0x19, Reset: 0x00, Name: OUTPUT\_RANGE\_CH4

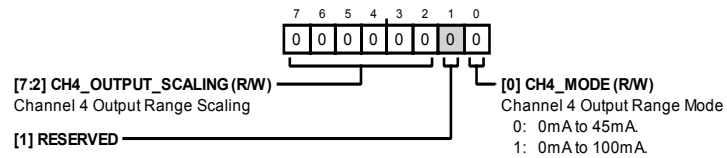


Table 32. Bit Descriptions for OUTPUT\_RANGE\_CH4

| Bits  | Bit Name           | Description                                                                                                                   | Reset | Access |
|-------|--------------------|-------------------------------------------------------------------------------------------------------------------------------|-------|--------|
| [7:2] | CH4_OUTPUT_SCALING | Channel 4 Output Range Scaling. These bits set the output range scaling factor for Channel 4.                                 | 0x0   | R/W    |
| 1     | Reserved           | Reserved.                                                                                                                     | 0x0   | R      |
| 0     | CH4_MODE           | Channel 4 Output Range Mode. This bit selects the output range mode for Channel 4.<br>0: 0 mA to 45 mA.<br>1: 0 mA to 100 mA. | 0x0   | R/W    |

Address: 0x1A, Reset: 0x00, Name: OUTPUT\_RANGE\_CH5

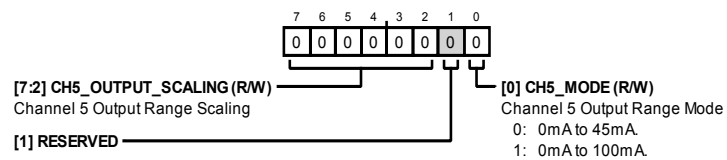


Table 33. Bit Descriptions for OUTPUT\_RANGE\_CH5

| Bits  | Bit Name           | Description                                                                                                                   | Reset | Access |
|-------|--------------------|-------------------------------------------------------------------------------------------------------------------------------|-------|--------|
| [7:2] | CH5_OUTPUT_SCALING | Channel 5 Output Range Scaling. These bits set the output range scaling factor for Channel 5.                                 | 0x0   | R/W    |
| 1     | Reserved           | Reserved.                                                                                                                     | 0x0   | R      |
| 0     | CH5_MODE           | Channel 5 Output Range Mode. This bit selects the output range mode for Channel 5.<br>0: 0 mA to 45 mA.<br>1: 0 mA to 100 mA. | 0x0   | R/W    |

Address: 0x1B, Reset: 0x00, Name: REFERENCE

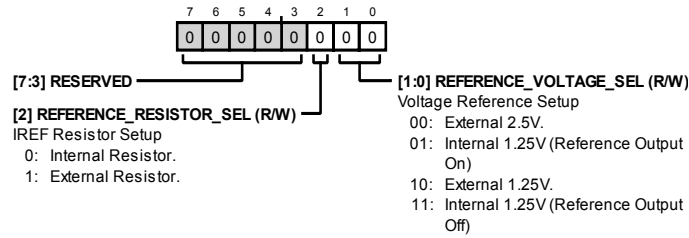


Table 34. Bit Descriptions for REFERENCE

| Bits  | Bit Name               | Description                                                                                                                                                                                                                                                | Reset | Access |
|-------|------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------|--------|
| [7:3] | Reserved               | Reserved.                                                                                                                                                                                                                                                  | 0x0   | R      |
| 2     | REFERENCE_RESISTOR_SEL | IREF Resistor Setup. This bit selects whether an internal or external resistor is used for reference current generation.<br>0: internal resistor.<br>1: external resistor.                                                                                 | 0x0   | R/W    |
| [1:0] | REFERENCE_VOLTAGE_SEL  | Voltage Reference Setup. These bits select the voltage reference scheme used for reference current generation.<br>00: external 2.5 V.<br>01: internal 1.25 V (reference output on).<br>10: external 1.25 V.<br>11: internal 1.25 V (reference output off). | 0x0   | R/W    |

Address: 0x1C, Reset: 0x06, Name: ALARM\_CONFIG

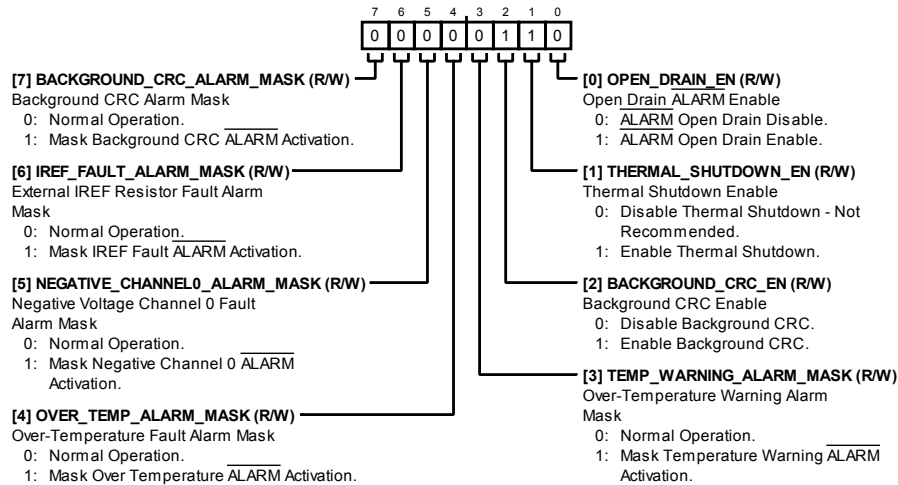


Table 35. Bit Descriptions for ALARM\_CONFIG

| Bits | Bit Name                  | Description                                                                                                                                                                                                               | Reset | Access |
|------|---------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------|--------|
| 7    | BACKGROUND_CRC_ALARM_MASK | Background CRC Alarm Mask. When this bit is set, the ALARM pin does not activate for background CRC errors.<br>0: normal operation.<br>1: mask background CRC ALARM activation.                                           | 0x0   | R/W    |
| 6    | IREF_FAULT_ALARM_MASK     | External IREF Resistor Fault Alarm Mask. When this bit is set, the ALARM pin does not activate for external reference current generation resistor faults.<br>0: normal operation.<br>1: mask IREF fault ALARM activation. | 0x0   | R/W    |

| Bits | Bit Name                     | Description                                                                                                                                                                                                                                                       | Reset | Access |
|------|------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------|--------|
| 5    | NEGATIVE_CHANNEL0_ALARM_MASK | Negative Voltage Channel 0 Fault Alarm Mask. When this bit is set, the ALARM pin does not activate when a negative voltage is multiplexed to the MUX_OUT pin due to monitoring Channel 0.<br>0: normal operation.<br>1: mask negative Channel 0 ALARM activation. | 0x0   | R/W    |
| 4    | OVER_TEMP_ALARM_MASK         | Overtemperature Fault Alarm Mask. When this bit is set, the ALARM pin does not activate for an overtemperature fault occurrence.<br>0: normal operation.<br>1: mask overtemperature ALARM activation.                                                             | 0x0   | R/W    |
| 3    | TEMP_WARNING_ALARM_MASK      | Overtemperature Warning Alarm Mask. When this bit is set, the ALARM pin does not activate for an overtemperature warning occurrence.<br>0: normal operation.<br>1: mask temperature warning ALARM activation.                                                     | 0x0   | R/W    |
| 2    | BACKGROUND_CRC_EN            | Background CRC Enable. When this bit is set, a CRC of the memory map contents is periodically computed by the device.<br>0: disable background CRC.<br>1: enable background CRC.                                                                                  | 0x1   | R/W    |
| 1    | THERMAL_SHUTDOWN_EN          | Thermal Shutdown Enable. When this bit is set, the AD5770R goes into thermal shutdown in the event of an overtemperature fault.<br>0: disable thermal shutdown (not recommended).<br>1: enable thermal shutdown.                                                  | 0x1   | R/W    |
| 0    | OPEN_DRAIN_EN                | Open-Drain ALARM Enable. When this bit is set, the ALARM pin is configured as an open-drain output.<br>0: ALARM open-drain disable.<br>1: ALARM open-drain enable.                                                                                                | 0x0   | R/W    |

Address: 0x1D, Reset: 0x00, Name: OUTPUT\_FILTER\_CH0

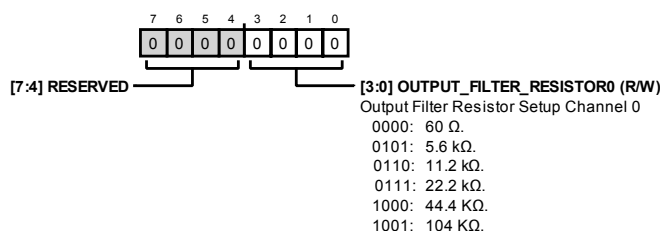


Table 36. Bit Descriptions for OUTPUT\_FILTER\_CH0

| Bits  | Bit Name                | Description                                                                                                                                                                                                                                                                                                                                                                 | Reset | Access |
|-------|-------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------|--------|
| [7:4] | Reserved                | Reserved.                                                                                                                                                                                                                                                                                                                                                                   | 0x0   | R      |
| [3:0] | OUTPUT_FILTER_RESISTOR0 | Output Filter Resistor Setup Channel 0. These bits select the internal variable resistor to be used for the output filter on Channel 0. The output filter resistor creates a resistor capacitor filter with the external capacitor connected to the CDAMP_IDAC0 pin.<br>0000: 60 Ω.<br>0101: 5.6 kΩ.<br>0110: 11.2 kΩ.<br>0111: 22.2 kΩ.<br>1000: 44.4 kΩ.<br>1001: 104 kΩ. | 0x0   | R/W    |

Address: 0x1E, Reset: 0x00, Name: OUTPUT\_FILTER\_CH1

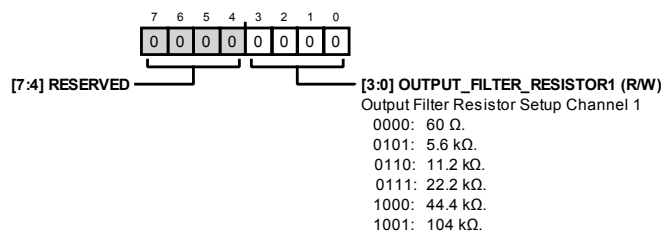


Table 37. Bit Descriptions for OUTPUT\_FILTER\_CH1

| Bits  | Bit Name                | Description                                                                                                                                                                                                                                                                                                                                                                                                                          | Reset | Access |
|-------|-------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------|--------|
| [7:4] | Reserved                | Reserved.                                                                                                                                                                                                                                                                                                                                                                                                                            | 0x0   | R      |
| [3:0] | OUTPUT_FILTER_RESISTOR1 | Output Filter Resistor Setup Channel 1. These bits select the internal variable resistor to be used for the output filter on Channel 1. The output filter resistor creates a resistor capacitor filter with the external capacitor connected to the CDAMP_IDAC1 pin.<br><br>0000: 60 $\Omega$ .<br>0101: 5.6 k $\Omega$ .<br>0110: 11.2 k $\Omega$ .<br>0111: 22.2 k $\Omega$ .<br>1000: 44.4 k $\Omega$ .<br>1001: 104 k $\Omega$ . | 0x0   | R/W    |

Address: 0x1F, Reset: 0x00, Name: OUTPUT\_FILTER\_CH2

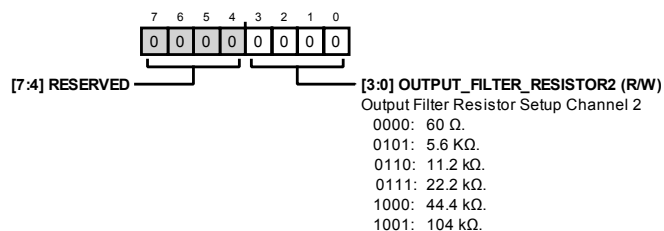


Table 38. Bit Descriptions for OUTPUT\_FILTER\_CH2

| Bits  | Bit Name                | Description                                                                                                                                                                                                                                                                                                                                                                                                                          | Reset | Access |
|-------|-------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------|--------|
| [7:4] | Reserved                | Reserved.                                                                                                                                                                                                                                                                                                                                                                                                                            | 0x0   | R      |
| [3:0] | OUTPUT_FILTER_RESISTOR2 | Output Filter Resistor Setup Channel 2. These bits select the internal variable resistor to be used for the output filter on Channel 2. The output filter resistor creates a resistor capacitor filter with the external capacitor connected to the CDAMP_IDAC2 pin.<br><br>0000: 60 $\Omega$ .<br>0101: 5.6 k $\Omega$ .<br>0110: 11.2 k $\Omega$ .<br>0111: 22.2 k $\Omega$ .<br>1000: 44.4 k $\Omega$ .<br>1001: 104 k $\Omega$ . | 0x0   | R/W    |

Address: 0x20, Reset: 0x00, Name: OUTPUT\_FILTER\_CH3

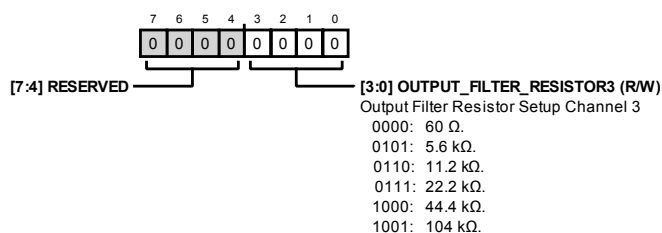


Table 39. Bit Descriptions for OUTPUT\_FILTER\_CH3

| Bits  | Bit Name                | Description                                                                                                                                                                                                                                                                                                                                                                                                                          | Reset | Access |
|-------|-------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------|--------|
| [7:4] | Reserved                | Reserved.                                                                                                                                                                                                                                                                                                                                                                                                                            | 0x0   | R      |
| [3:0] | OUTPUT_FILTER_RESISTOR3 | Output Filter Resistor Setup Channel 3. These bits select the internal variable resistor to be used for the output filter on Channel 3. The output filter resistor creates a resistor capacitor filter with the external capacitor connected to the CDAMP_IDAC3 pin.<br><br>0000: 60 $\Omega$ .<br>0101: 5.6 k $\Omega$ .<br>0110: 11.2 k $\Omega$ .<br>0111: 22.2 k $\Omega$ .<br>1000: 44.4 k $\Omega$ .<br>1001: 104 k $\Omega$ . | 0x0   | R/W    |

Address: 0x21, Reset: 0x00, Name: OUTPUT\_FILTER\_CH4

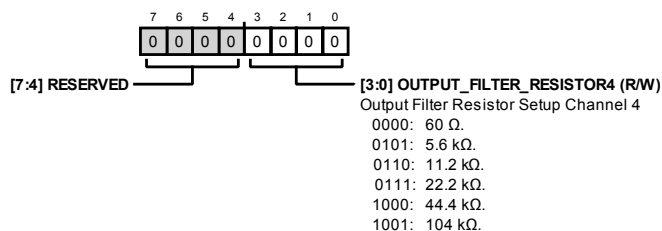


Table 40. Bit Descriptions for OUTPUT\_FILTER\_CH4

| Bits  | Bit Name                | Description                                                                                                                                                                                                                                                                                                                                                                                                                          | Reset | Access |
|-------|-------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------|--------|
| [7:4] | Reserved                | Reserved.                                                                                                                                                                                                                                                                                                                                                                                                                            | 0x0   | R      |
| [3:0] | OUTPUT_FILTER_RESISTOR4 | Output Filter Resistor Setup Channel 4. These bits select the internal variable resistor to be used for the output filter on Channel 4. The output filter resistor creates a resistor capacitor filter with the external capacitor connected to the CDAMP_IDAC4 pin.<br><br>0000: 60 $\Omega$ .<br>0101: 5.6 k $\Omega$ .<br>0110: 11.2 k $\Omega$ .<br>0111: 22.2 k $\Omega$ .<br>1000: 44.4 k $\Omega$ .<br>1001: 104 k $\Omega$ . | 0x0   | R/W    |

Address: 0x22, Reset: 0x00, Name: OUTPUT\_FILTER\_CH5

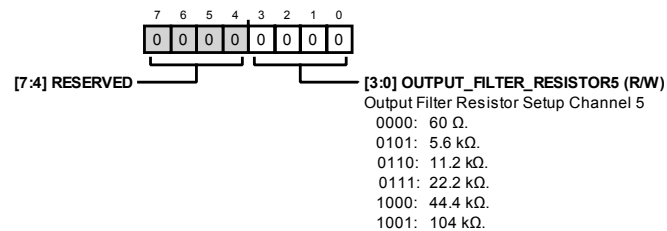


Table 41. Bit Descriptions for OUTPUT\_FILTER\_CH5

| Bits  | Bit Name                | Description                                                                                                                                                                                                                                                                                                                                                                     | Reset | Access |
|-------|-------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------|--------|
| [7:4] | Reserved                | Reserved.                                                                                                                                                                                                                                                                                                                                                                       | 0x0   | R      |
| [3:0] | OUTPUT_FILTER_RESISTOR5 | Output Filter Resistor Setup Channel 5. These bits select the internal variable resistor to be used for the output filter on Channel 5. The output filter resistor creates a resistor capacitor filter with the external capacitor connected to the CDAMP_IDAC5 pin.<br><br>0000: 60 Ω.<br>0101: 5.6 kΩ.<br>0110: 11.2 kΩ.<br>0111: 22.2 kΩ.<br>1000: 44.4 kΩ.<br>1001: 104 kΩ. | 0x0   | R/W    |

Address: 0x23, Reset: 0x00, Name: MONITOR\_SETUP

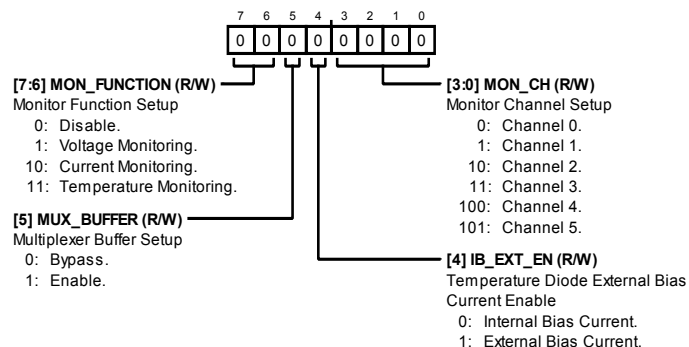


Table 42. Bit Descriptions for MONITOR\_SETUP

| Bits  | Bit Name     | Description                                                                                                                                                                                                                                                    | Reset | Access |
|-------|--------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------|--------|
| [7:6] | MON_FUNCTION | Monitor Function Setup. These bits configure which on-chip diagnostic function is selected.<br>0: disable.<br>1: voltage monitoring.<br>10: current monitoring.<br>11: temperature monitoring.                                                                 | 0x0   | R/W    |
| 5     | MUX_BUFFER   | Multiplexer Buffer Setup. When this bit is set, the multiplexer buffer is enabled and used to buffer the multiplexer output. Clearing this bit disables the buffer and bypasses it.<br>0: bypass.<br>1: enable.                                                | 0x0   | R/W    |
| 4     | IB_EXT_EN    | Temperature Diode External Bias Current Enable. When this bit is set, an internal bias current for the temperature monitoring diode is shut off. This bias current must then be supplied externally.<br>0: internal bias current.<br>1: external bias current. | 0x0   | R/W    |

| Bits  | Bit Name | Description                                                                                                                                                                                                                                     | Reset | Access |
|-------|----------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------|--------|
| [3:0] | MON_CH   | Monitor Channel Setup. These bits select the channel to be monitored when output voltage or output current diagnostics are enabled.<br>0: Channel 0.<br>1: Channel 1.<br>10: Channel 2.<br>11: Channel 3.<br>100: Channel 4.<br>101: Channel 5. | 0x0   | R/W    |

Address: 0x24, Reset: 0x00, Name: STATUS

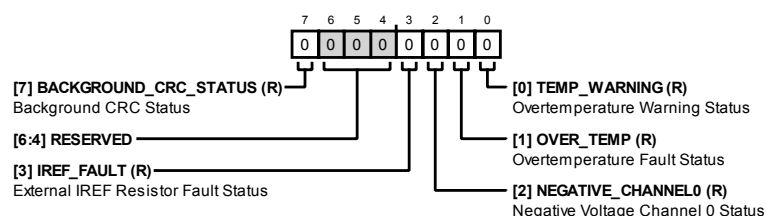


Table 43. Bit Descriptions for STATUS

| Bits  | Bit Name              | Description                                                                                                                                                                                                                                                                                                                                                                       | Reset | Access |
|-------|-----------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------|--------|
| 7     | BACKGROUND_CRC_STATUS | Background CRC Status. Read Only Status Bit. When this bit is high, this signifies that a background CRC of the memory map has failed and a memory bit may have inadvertently flipped.<br>0: normal.<br>1: background CRC error activated.                                                                                                                                        | 0x0   | R      |
| [6:4] | Reserved              | Reserved.                                                                                                                                                                                                                                                                                                                                                                         | 0x0   | R      |
| 3     | IREF_FAULT            | External IREF Resistor Fault Status. Read only status bit. When this bit is set, a fault has been detected with the external reference current generation resistor, and the internal resistor has been switched to avoid damage to the device.<br>0: normal.<br>1: IREF fault activated.                                                                                          | 0x0   | R      |
| 2     | NEGATIVE_CHANNEL0     | Negative Voltage Channel 0 Status. Read only status bit. When this bit is set, a fault has been detected due to a negative voltage being multiplexed to the MUX_OUT pin when monitoring Channel 0.<br>0: normal.<br>1: negative Channel 0 activated.                                                                                                                              | 0x0   | R      |
| 1     | OVER_TEMP             | Overtemperature Fault Status. Read only status bit. When this bit is set, an overtemperature fault occurrence has been detected. An overtemperature fault occurs when the internal die temperature reaches approximately 145°C. A reset command must be issued to the device to clear this bit.<br>0: normal.<br>1: overtemperature activated.                                    | 0x0   | R      |
| 0     | TEMP_WARNING          | Overtemperature Warning Status. Read only status bit. When this bit is set, an overtemperature warning occurrence has been detected. An overtemperature warning occurs when the internal die temperature reaches approximately 125°C. This bit is automatically cleared when the internal die temperature returns below 120°C.<br>0: normal.<br>1: temperature warning activated. | 0x0   | R      |

Address: 0x25, Reset: 0x00, Name: HW\_LDAC

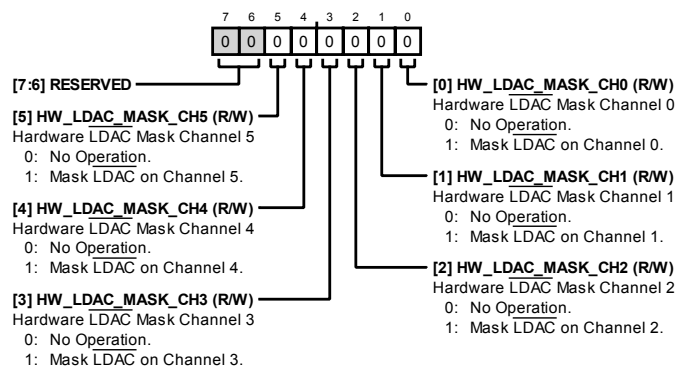


Table 44. Bit Descriptions for HW\_LDAC

| Bits  | Bit Name         | Description                                                                                                                                              | Reset | Access |
|-------|------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------|-------|--------|
| [7:6] | RESERVED         | Reserved.                                                                                                                                                | 0x0   | R      |
| 5     | HW_LDAC_MASK_CH5 | Hardware LDAC Mask Channel 5. When this bit is set, activity on the LDAC pin is ignored for Channel 5.<br>0: no operation.<br>1: mask LDAC on Channel 5. | 0x0   | R/W    |
| 4     | HW_LDAC_MASK_CH4 | Hardware LDAC Mask Channel 4. When this bit is set, activity on the LDAC pin is ignored for Channel 4.<br>0: no operation.<br>1: mask LDAC on Channel 4. | 0x0   | R/W    |
| 3     | HW_LDAC_MASK_CH3 | Hardware LDAC Mask Channel 3. When this bit is set, activity on the LDAC pin is ignored for Channel 3.<br>0: no operation.<br>1: mask LDAC on Channel 3. | 0x0   | R/W    |
| 2     | HW_LDAC_MASK_CH2 | Hardware LDAC Mask Channel 2. When this bit is set, activity on the LDAC pin is ignored for Channel 2.<br>0: no operation.<br>1: mask LDAC on Channel 2. | 0x0   | R/W    |
| 1     | HW_LDAC_MASK_CH1 | Hardware LDAC Mask Channel 1. When this bit is set, activity on the LDAC pin is ignored for Channel 1.<br>0: no operation.<br>1: mask LDAC on Channel 1. | 0x0   | R/W    |
| 0     | HW_LDAC_MASK_CH0 | Hardware LDAC Mask Channel 0. When this bit is set, activity on the LDAC pin is ignored for Channel 0.<br>0: no operation.<br>1: mask LDAC on Channel 0. | 0x0   | R/W    |

Address: 0x26, Reset: 0x00, Name: CH0\_DAC\_LSB

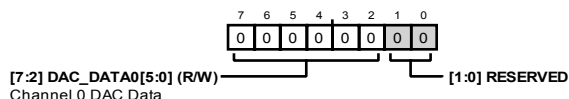


Table 45. Bit Descriptions for CH0\_DAC\_LSB

| Bits  | Bit Name       | Description                                                                             | Reset | Access |
|-------|----------------|-----------------------------------------------------------------------------------------|-------|--------|
| [7:2] | DAC_DATA0[5:0] | Channel 0 DAC Data. These bits are the DAC code loaded into the DAC register for IDAC0. | 0x0   | R/W    |
| [1:0] | RESERVED       | Reserved.                                                                               | 0x0   | R      |

Address: 0x27, Reset: 0x00, Name: CH0\_DAC\_MSB

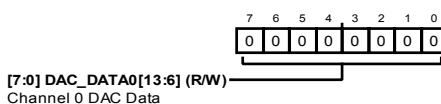


Table 46. Bit Descriptions for CH0\_DAC\_MSB

| Bits  | Bit Name        | Description                                                                             | Reset | Access |
|-------|-----------------|-----------------------------------------------------------------------------------------|-------|--------|
| [7:0] | DAC_DATA0[13:6] | Channel 0 DAC Data. These bits are the DAC code loaded into the DAC register for IDAC0. | 0x0   | R/W    |

Address: 0x28, Reset: 0x00, Name: CH1\_DAC\_LSB

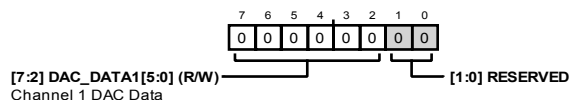


Table 47. Bit Descriptions for CH1\_DAC\_LSB

| Bits  | Bit Name       | Description                                                                             | Reset | Access |
|-------|----------------|-----------------------------------------------------------------------------------------|-------|--------|
| [7:2] | DAC_DATA1[5:0] | Channel 1 DAC Data. These bits are the DAC code loaded into the DAC register for IDAC1. | 0x0   | R/W    |
| [1:0] | Reserved       | Reserved.                                                                               | 0x0   | R      |

Address: 0x29, Reset: 0x00, Name: CH1\_DAC\_MSB

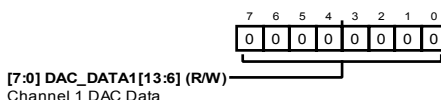


Table 48. Bit Descriptions for CH1\_DAC\_MSB

| Bits  | Bit Name        | Description                                                                             | Reset | Access |
|-------|-----------------|-----------------------------------------------------------------------------------------|-------|--------|
| [7:0] | DAC_DATA1[13:6] | Channel 1 DAC Data. These bits are the DAC code loaded into the DAC register for IDAC1. | 0x0   | R/W    |

Address: 0x2A, Reset: 0x00, Name: CH2\_DAC\_LSB

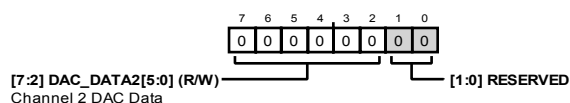


Table 49. Bit Descriptions for CH2\_DAC\_LSB

| Bits  | Bit Name       | Description                                                                             | Reset | Access |
|-------|----------------|-----------------------------------------------------------------------------------------|-------|--------|
| [7:2] | DAC_DATA2[5:0] | Channel 2 DAC Data. These bits are the DAC code loaded into the DAC register for IDAC2. | 0x0   | R/W    |
| [1:0] | Reserved       | Reserved.                                                                               | 0x0   | R      |

Address: 0x2B, Reset: 0x00, Name: CH2\_DAC\_MSB

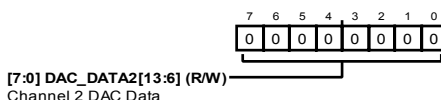


Table 50. Bit Descriptions for CH2\_DAC\_MSB

| Bits  | Bit Name        | Description                                                                             | Reset | Access |
|-------|-----------------|-----------------------------------------------------------------------------------------|-------|--------|
| [7:0] | DAC_DATA2[13:6] | Channel 2 DAC Data. These bits are the DAC code loaded into the DAC register for IDAC2. | 0x0   | R/W    |

Address: 0x2C, Reset: 0x00, Name: CH3\_DAC\_LSB

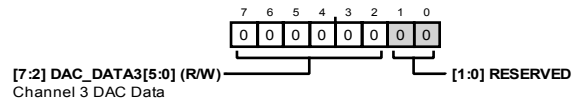


Table 51. Bit Descriptions for CH3\_DAC\_LSB

| Bits  | Bit Name       | Description                                                                             | Reset | Access |
|-------|----------------|-----------------------------------------------------------------------------------------|-------|--------|
| [7:2] | DAC_DATA3[5:0] | Channel 3 DAC Data. These bits are the DAC code loaded into the DAC register for IDAC3. | 0x0   | R/W    |
| [1:0] | Reserved       | Reserved.                                                                               | 0x0   | R      |

Address: 0x2D, Reset: 0x00, Name: CH3\_DAC\_MSB

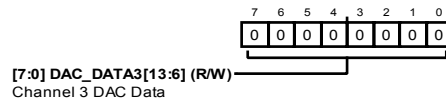


Table 52. Bit Descriptions for CH3\_DAC\_MSB

| Bits  | Bit Name        | Description                                                                             | Reset | Access |
|-------|-----------------|-----------------------------------------------------------------------------------------|-------|--------|
| [7:0] | DAC_DATA3[13:6] | Channel 3 DAC Data. These bits are the DAC code loaded into the DAC register for IDAC3. | 0x0   | R/W    |

Address: 0x2E, Reset: 0x00, Name: CH4\_DAC\_LSB

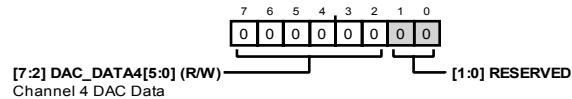


Table 53. Bit Descriptions for CH4\_DAC\_LSB

| Bits  | Bit Name       | Description                                                                             | Reset | Access |
|-------|----------------|-----------------------------------------------------------------------------------------|-------|--------|
| [7:2] | DAC_DATA4[5:0] | Channel 4 DAC Data. These bits are the DAC code loaded into the DAC register for IDAC4. | 0x0   | R/W    |
| [1:0] | Reserved       | Reserved.                                                                               | 0x0   | R      |

Address: 0x2F, Reset: 0x00, Name: CH4\_DAC\_MSB

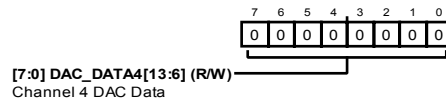


Table 54. Bit Descriptions for CH4\_DAC\_MSB

| Bits  | Bit Name        | Description                                                                             | Reset | Access |
|-------|-----------------|-----------------------------------------------------------------------------------------|-------|--------|
| [7:0] | DAC_DATA4[13:6] | Channel 4 DAC Data. These bits are the DAC code loaded into the DAC register for IDAC4. | 0x0   | R/W    |

Address: 0x30, Reset: 0x00, Name: CH5\_DAC\_LSB

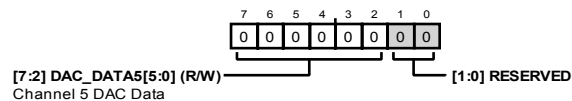


Table 55. Bit Descriptions for CH5\_DAC\_LSB

| Bits  | Bit Name       | Description                                                                             | Reset | Access |
|-------|----------------|-----------------------------------------------------------------------------------------|-------|--------|
| [7:2] | DAC_DATA5[5:0] | Channel 5 DAC Data. These bits are the DAC code loaded into the DAC register for IDAC5. | 0x0   | R/W    |
| [1:0] | Reserved       | Reserved.                                                                               | 0x0   | R      |

Address: 0x31, Reset: 0x00, Name: CH5\_DAC\_MSB

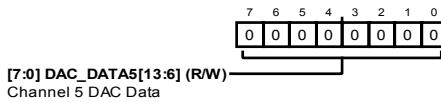


Table 56. Bit Descriptions for CH5\_DAC\_MSB

| Bits  | Bit Name        | Description                                                                             | Reset | Access |
|-------|-----------------|-----------------------------------------------------------------------------------------|-------|--------|
| [7:0] | DAC_DATA5[13:6] | Channel 5 DAC Data. These bits are the DAC code loaded into the DAC register for IDAC5. | 0x0   | R/W    |

Address: 0x32, Reset: 0x00, Name: DAC\_PAGE\_MASK\_LSB

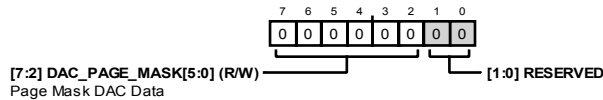


Table 57. Bit Descriptions for DAC\_PAGE\_MASK\_LSB

| Bits  | Bit Name           | Description                                                                                                                                                                        | Reset | Access |
|-------|--------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------|--------|
| [7:2] | DAC_PAGE_MASK[5:0] | Page Mask DAC Data. Following a write to this register, the DAC code loaded into this register is copied into the DAC register of any channels selected in the CH_SELECT register. | 0x0   | R/W    |
| [1:0] | Reserved           | Reserved.                                                                                                                                                                          | 0x0   | R      |

Address: 0x33, Reset: 0x00, Name: DAC\_PAGE\_MASK\_MSB

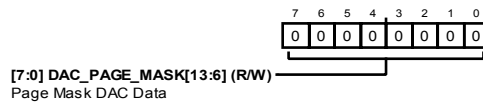


Table 58. Bit Descriptions for DAC\_PAGE\_MASK\_MSB

| Bits  | Bit Name            | Description                                                                                                                                                                        | Reset | Access |
|-------|---------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------|--------|
| [7:0] | DAC_PAGE_MASK[13:6] | Page Mask DAC Data. Following a write to this register, the DAC code loaded into this register is copied into the DAC register of any channels selected in the CH_SELECT register. | 0x0   | R/W    |

Address: 0x34, Reset: 0x00, Name: CH\_SELECT

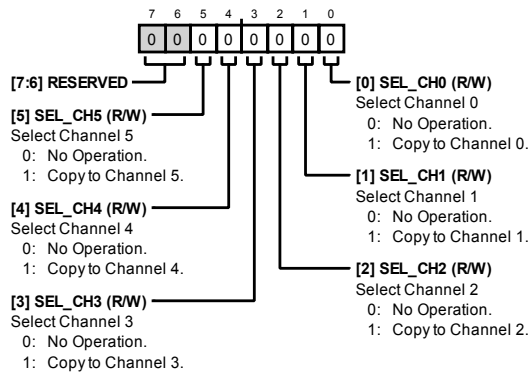


Table 59. Bit Descriptions for CH\_SELECT

| Bits  | Bit Name | Description                                                                                                                                                                                                                                         | Reset | Access |
|-------|----------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------|--------|
| [7:6] | Reserved | Reserved.                                                                                                                                                                                                                                           | 0x0   | R      |
| 5     | SEL_CH5  | Select Channel 5. When this bit is set, data written to the INPUT_PAGE_MASK register is copied to the INPUT_DATA5 bits and data written to the DAC_PAGE_MASK register is copied to the DAC_DATA5 bits.<br>0: no operation.<br>1: copy to Channel 5. | 0x0   | R/W    |
| 4     | SEL_CH4  | Select Channel 4. When this bit is set, data written to the INPUT_PAGE_MASK register is copied to the INPUT_DATA4 bits and data written to the DAC_PAGE_MASK register is copied to the DAC_DATA4 bits.<br>0: no operation.<br>1: copy to Channel 4. | 0x0   | R/W    |

| Bits | Bit Name | Description                                                                                                                                                                                                                                         | Reset | Access |
|------|----------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------|--------|
| 3    | SEL_CH3  | Select Channel 3. When this bit is set, data written to the INPUT_PAGE_MASK register is copied to the INPUT_DATA3 bits and data written to the DAC_PAGE_MASK register is copied to the DAC_DATA3 bits.<br>0: no operation.<br>1: copy to Channel 3. | 0x0   | R/W    |
| 2    | SEL_CH2  | Select Channel 2. When this bit is set, data written to the INPUT_PAGE_MASK register is copied to the INPUT_DATA2 bits and data written to the DAC_PAGE_MASK register is copied to the DAC_DATA2 bits.<br>0: no operation.<br>1: copy to Channel 2. | 0x0   | R/W    |
| 1    | SEL_CH1  | Select Channel 1. When this bit is set, data written to the INPUT_PAGE_MASK register is copied to the INPUT_DATA1 bits and data written to the DAC_PAGE_MASK register is copied to the DAC_DATA1 bits.<br>0: no operation.<br>1: copy to Channel 1. | 0x0   | R/W    |
| 0    | SEL_CH0  | Select Channel 0. When this bit is set, data written to the INPUT_PAGE_MASK register is copied to the INPUT_DATA0 bits and data written to the DAC_PAGE_MASK register is copied to the DAC_DATA0 bits.<br>0: no operation.<br>1: copy to Channel 0. | 0x0   | R/W    |

Address: 0x35, Reset: 0x00, Name: INPUT\_PAGE\_MASK\_LSB

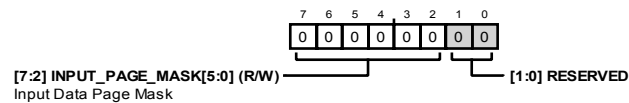


Table 60. Bit Descriptions for INPUT\_PAGE\_MASK\_LSB

| Bits  | Bit Name             | Description                                                                                                                                                                            | Reset | Access |
|-------|----------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------|--------|
| [7:2] | INPUT_PAGE_MASK[5:0] | Input Data Page Mask. Following a write to this register, the DAC code loaded into this register is copied into the input register of any channels selected in the CH_SELECT register. | 0x0   | R/W    |
| [1:0] | Reserved             | Reserved.                                                                                                                                                                              | 0x0   | R      |

Address: 0x36, Reset: 0x00, Name: INPUT\_PAGE\_MASK\_MSB

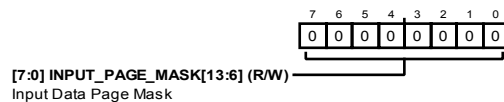


Table 61. Bit Descriptions for INPUT\_PAGE\_MASK\_MSB

| Bits  | Bit Name              | Description                                                                                                                                                                            | Reset | Access |
|-------|-----------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------|--------|
| [7:0] | INPUT_PAGE_MASK[13:6] | Input Data Page Mask. Following a write to this register, the DAC code loaded into this register is copied into the input register of any channels selected in the CH_SELECT register. | 0x0   | R/W    |

Address: 0x37, Reset: 0x00, Name: SW\_LDAC

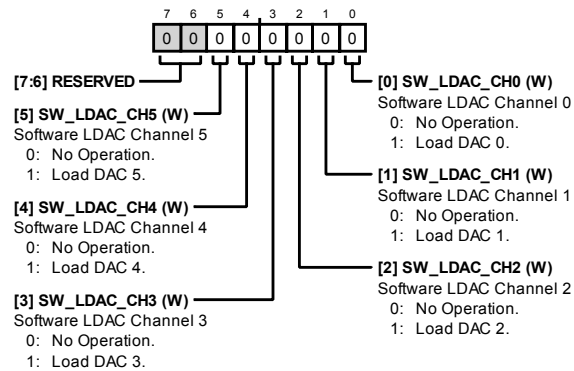


Table 62. Bit Descriptions for SW\_LDAC

| Bits  | Bit Name    | Description                                                                                                                                                                                                                 | Reset | Access |
|-------|-------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------|--------|
| [7:6] | Reserved    | Reserved.                                                                                                                                                                                                                   | 0x0   | R      |
| 5     | SW_LDAC_CH5 | Software LDAC Channel 5. Setting this bit transfers content from the INPUT_DATA5 bits to the DAC_DATA5 bits. This bit automatically resets after a write to the SW_LDAC register.<br>0: no operation.<br>1: load DAC_DATA5. | 0x0   | W      |
| 4     | SW_LDAC_CH4 | Software LDAC Channel 4. Setting this bit transfers content from the INPUT_DATA4 bits to the DAC_DATA4 bits. This bit automatically resets after a write to the SW_LDAC register.<br>0: no operation.<br>1: load DAC_DATA4. | 0x0   | W      |
| 3     | SW_LDAC_CH3 | Software LDAC Channel 3. Setting this bit transfers content from the INPUT_DATA3 bits to the DAC_DATA3 bits. This bit automatically resets after a write to the SW_LDAC register.<br>0: no operation.<br>1: load DAC_DATA3. | 0x0   | W      |
| 2     | SW_LDAC_CH2 | Software LDAC Channel 2. Setting this bit transfers content from the INPUT_DATA2 bits to the DAC_DATA2 bits. This bit automatically resets after a write to the SW_LDAC register.<br>0: no operation.<br>1: load DAC_DATA2. | 0x0   | W      |
| 1     | SW_LDAC_CH1 | Software LDAC Channel 1. Setting this bit transfers content from the INPUT_DATA1 bits to the DAC_DATA1 bits. This bit automatically resets after a write to the SW_LDAC register.<br>0: no operation.<br>1: load DAC_DATA1. | 0x0   | W      |
| 0     | SW_LDAC_CH0 | Software LDAC Channel 0. Setting this bit transfers content from the INPUT_DATA0 bits to the DAC_DATA0 bits. This bit automatically resets after a write to the SW_LDAC register.<br>0: no operation.<br>1: load DAC_DATA0. | 0x0   | W      |

Address: 0x38, Reset: 0x00, Name: CH0\_INPUT\_LSB

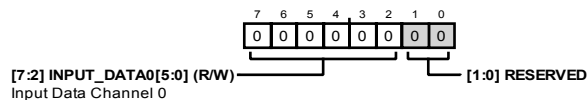


Table 63. Bit Descriptions for CH0\_INPUT\_LSB

| Bits  | Bit Name         | Description                                                                                 | Reset | Access |
|-------|------------------|---------------------------------------------------------------------------------------------|-------|--------|
| [7:2] | INPUT_DATA0[5:0] | Input Data Channel 0. These bits are the DAC code loaded into the input register for IDAC0. | 0x0   | R/W    |
| [1:0] | Reserved         | Reserved.                                                                                   | 0x0   | R      |

Address: 0x39, Reset: 0x00, Name: CH0\_INPUT\_MSB

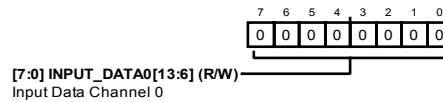


Table 64. Bit Descriptions for CH0\_INPUT\_MSB

| Bits  | Bit Name          | Description                                                                                 | Reset | Access |
|-------|-------------------|---------------------------------------------------------------------------------------------|-------|--------|
| [7:0] | INPUT_DATA0[13:6] | Input Data Channel 0. These bits are the DAC code loaded into the input register for IDAC0. | 0x0   | R/W    |

Address: 0x3A, Reset: 0x00, Name: CH1\_INPUT\_LSB

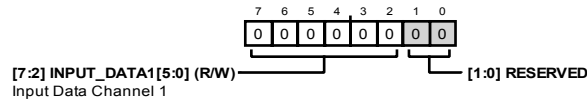


Table 65. Bit Descriptions for CH1\_INPUT\_LSB

| Bits  | Bit Name         | Description                                                                                 | Reset | Access |
|-------|------------------|---------------------------------------------------------------------------------------------|-------|--------|
| [7:2] | INPUT_DATA1[5:0] | Input Data Channel 1. These bits are the DAC code loaded into the input register for IDAC1. | 0x0   | R/W    |
| [1:0] | Reserved         | Reserved.                                                                                   | 0x0   | R      |

Address: 0x3B, Reset: 0x00, Name: CH1\_INPUT\_MSB

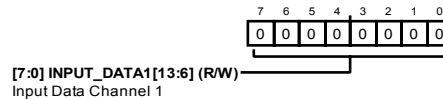


Table 66. Bit Descriptions for CH1\_INPUT\_MSB

| Bits  | Bit Name          | Description                                                                                 | Reset | Access |
|-------|-------------------|---------------------------------------------------------------------------------------------|-------|--------|
| [7:0] | INPUT_DATA1[13:6] | Input Data Channel 1. These bits are the DAC code loaded into the input register for IDAC1. | 0x0   | R/W    |

Address: 0x3C, Reset: 0x00, Name: CH2\_INPUT\_LSB

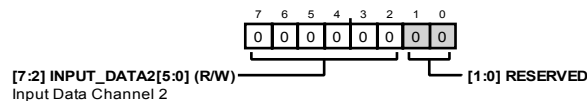


Table 67. Bit Descriptions for CH2\_INPUT\_LSB

| Bits  | Bit Name         | Description                                                                                 | Reset | Access |
|-------|------------------|---------------------------------------------------------------------------------------------|-------|--------|
| [7:2] | INPUT_DATA2[5:0] | Input Data Channel 2. These bits are the DAC code loaded into the input register for IDAC2. | 0x0   | R/W    |
| [1:0] | Reserved         | Reserved.                                                                                   | 0x0   | R      |

Address: 0x3D, Reset: 0x00, Name: CH2\_INPUT\_MSB

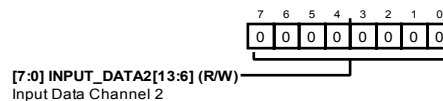


Table 68. Bit Descriptions for CH2\_INPUT\_MSB

| Bits  | Bit Name          | Description                                                                                 | Reset | Access |
|-------|-------------------|---------------------------------------------------------------------------------------------|-------|--------|
| [7:0] | INPUT_DATA2[13:6] | Input Data Channel 2. These bits are the DAC code loaded into the input register for IDAC2. | 0x0   | R/W    |

Address: 0x3E, Reset: 0x00, Name: CH3\_INPUT\_LSB

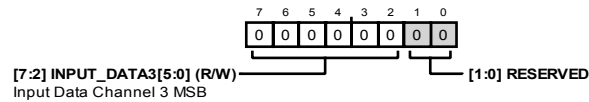


Table 69. Bit Descriptions for CH3\_INPUT\_LSB

| Bits  | Bit Name         | Description                                                                                 | Reset | Access |
|-------|------------------|---------------------------------------------------------------------------------------------|-------|--------|
| [7:2] | INPUT_DATA3[5:0] | Input Data Channel 3. These bits are the DAC code loaded into the input register for IDAC3. | 0x0   | R/W    |
| [1:0] | Reserved         | Reserved.                                                                                   | 0x0   | R      |

Address: 0x3F, Reset: 0x00, Name: CH3\_INPUT\_MSB

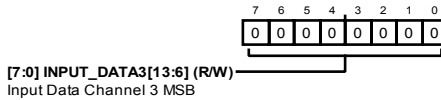


Table 70. Bit Descriptions for CH3\_INPUT\_MSB

| Bits  | Bit Name          | Description                                                                                 | Reset | Access |
|-------|-------------------|---------------------------------------------------------------------------------------------|-------|--------|
| [7:0] | INPUT_DATA3[13:6] | Input Data Channel 3. These bits are the DAC code loaded into the input register for IDAC3. | 0x0   | R/W    |

Address: 0x40, Reset: 0x00, Name: CH4\_INPUT\_LSB

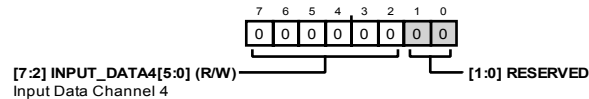


Table 71. Bit Descriptions for CH4\_INPUT\_LSB

| Bits  | Bit Name         | Description                                                                                 | Reset | Access |
|-------|------------------|---------------------------------------------------------------------------------------------|-------|--------|
| [7:2] | INPUT_DATA4[5:0] | Input Data Channel 4. These bits are the DAC code loaded into the input register for IDAC4. | 0x0   | R/W    |
| [1:0] | Reserved         | Reserved.                                                                                   | 0x0   | R      |

Address: 0x41, Reset: 0x00, Name: CH4\_INPUT\_MSB

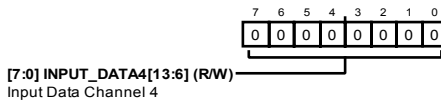


Table 72. Bit Descriptions for CH4\_INPUT\_MSB

| Bits  | Bit Name          | Description                                                                                 | Reset | Access |
|-------|-------------------|---------------------------------------------------------------------------------------------|-------|--------|
| [7:0] | INPUT_DATA4[13:6] | Input Data Channel 4. These bits are the DAC code loaded into the input register for IDAC4. | 0x0   | R/W    |

Address: 0x42, Reset: 0x00, Name: CH5\_INPUT\_LSB

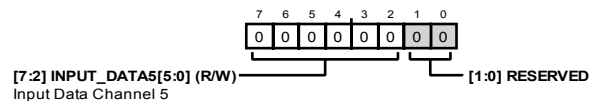


Table 73. Bit Descriptions for CH5\_INPUT\_LSB

| Bits  | Bit Name         | Description                                                                                 | Reset | Access |
|-------|------------------|---------------------------------------------------------------------------------------------|-------|--------|
| [7:2] | INPUT_DATA5[5:0] | Input Data Channel 5. These bits are the DAC code loaded into the input register for IDAC5. | 0x0   | R/W    |
| [1:0] | Reserved         | Reserved.                                                                                   | 0x0   | R      |

Address: 0x43, Reset: 0x00, Name: CH5\_INPUT\_MSB

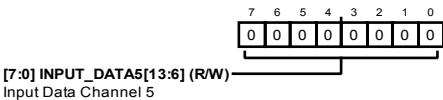


Table 74. Bit Descriptions for CH5\_INPUT\_MSB

| Bits  | Bit Name          | Description                                                                                 | Reset | Access |
|-------|-------------------|---------------------------------------------------------------------------------------------|-------|--------|
| [7:0] | INPUT_DATA5[13:6] | Input Data Channel 5. These bits are the DAC code loaded into the input register for IDAC5. | 0x0   | R/W    |

Address: 0x44, Reset: 0x3F, Name: RESERVED

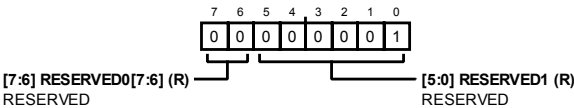


Table 75. Bit Descriptions for RESERVED

| Bits  | Bit Name  | Description | Reset | Access |
|-------|-----------|-------------|-------|--------|
| [7:6] | RESERVED0 | Reserved    | 0x0   | R      |
| [0:5] | RESERVED1 | Reserved    | 0x1   | R      |

## OUTLINE DIMENSIONS

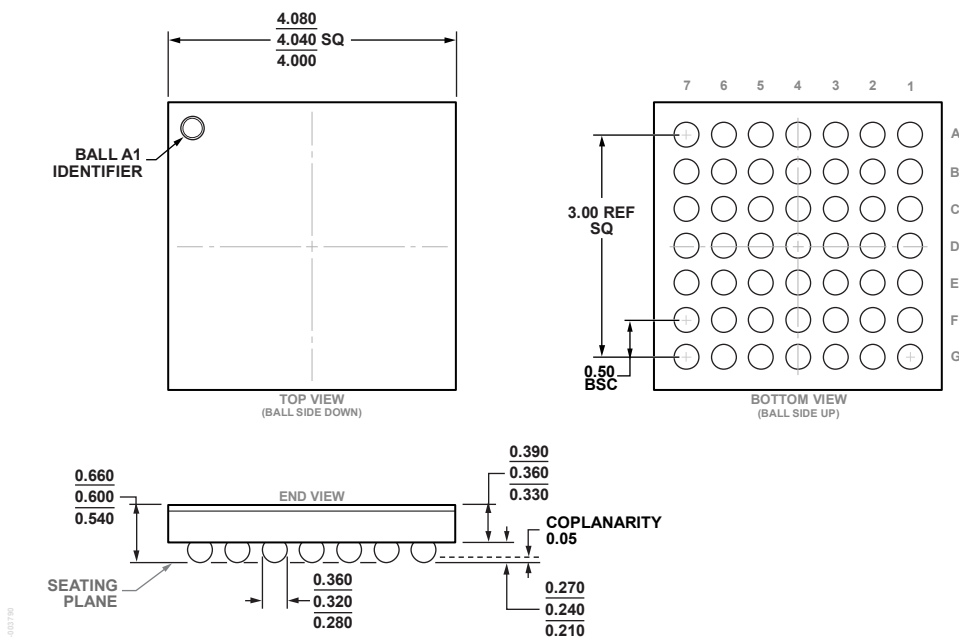


Figure 78. 49-Ball Wafer Level Chip Scale Package [WLCSP]  
(CB-49-5)

Dimensions shown in millimeters

## ORDERING GUIDE

| Model <sup>1</sup> | Temperature Range | Package Description                              | Package Option |
|--------------------|-------------------|--------------------------------------------------|----------------|
| AD5770RBCBZ-RL7    | −40°C to +105°C   | 49-Ball Wafer Level Chip Scale Packaging [WLCSP] | CB-49-5        |
| EVAL-AD5770RSDZ    |                   | Evaluation Board                                 |                |

<sup>1</sup> Z = RoHS Compliant Part.

## Данный компонент на территории Российской Федерации

**Вы можете приобрести в компании MosChip.**

Для оперативного оформления запроса Вам необходимо перейти по данной ссылке:

<http://moschip.ru/get-element>

Вы можете разместить у нас заказ для любого Вашего проекта, будь то серийное производство или разработка единичного прибора.

В нашем ассортименте представлены ведущие мировые производители активных и пассивных электронных компонентов.

Нашей специализацией является поставка электронной компонентной базы двойного назначения, продукции таких производителей как XILINX, Intel (ex.ALTERA), Vicor, Microchip, Texas Instruments, Analog Devices, Mini-Circuits, Amphenol, Glenair.

Сотрудничество с глобальными дистрибьюторами электронных компонентов, предоставляет возможность заказывать и получать с международных складов практически любой перечень компонентов в оптимальные для Вас сроки.

На всех этапах разработки и производства наши партнеры могут получить квалифицированную поддержку опытных инженеров.

Система менеджмента качества компании отвечает требованиям в соответствии с ГОСТ Р ИСО 9001, ГОСТ РВ 0015-002 и ЭС РД 009

### Офис по работе с юридическими лицами:

105318, г.Москва, ул.Щербаковская д.3, офис 1107, 1118, ДЦ «Щербаковский»

Телефон: +7 495 668-12-70 (многоканальный)

Факс: +7 495 668-12-70 (доб.304)

E-mail: [info@moschip.ru](mailto:info@moschip.ru)

Skype отдела продаж:

moschip.ru

moschip.ru\_4

moschip.ru\_6

moschip.ru\_9