

8-Port T1/E1/J1 Transceiver

General Description

The DS26518 is an 8-port framer and line interface unit (LIU) combination for T1, E1, J1 applications. Each port is independently configurable, supporting both long-haul and short-haul lines. The DS26518 Single-Chip Transceiver (SCT) is software and pinout compatible with the 4-port DS26514. It is nearly software compatible with the DS26528 and its derivatives.

Applications

Routers
 Channel Service Units (CSUs)
 Data Service Units (DSUs)
 Muxes
 Switches
 Channel Banks
 T1/E1 Test Equipment

Functional Diagram



Ordering Information

| PART | TEMP RANGE | PIN-PACKAGE |
|------------|----------------|--------------|
| DS26518GN | -40°C to +85°C | 256 TE-CSBGA |
| DS26518GN+ | -40°C to +85°C | 256 TE-CSBGA |

+ Denotes a lead-free/RoHS compliant device.

Features

- Eight Complete T1, E1, or J1 Long-Haul/ Short-Haul Transceivers (LIU Plus Framer)
- Independent T1, E1, or J1 Selections for Each Transceiver
- Fully Internal Impedance Match, No External Resistor
- Software-Selectable Transmit- and Receive-Side Termination for 100Ω T1 Twisted Pair, 110Ω J1 Twisted Pair, 120Ω E1 Twisted Pair, and 75Ω E1 Coaxial Applications
- Hitless Protection Switching
- Crystal-Less Jitter Attenuators Can Be Selected for Transmit or Receive Path; Jitter Attenuator Meets ETS CTR 12/13, ITU-T G.736, G.742, G.823, and AT&T Pub 62411
- External Master Clock Can Be Multiple of 2.048MHz or 1.544MHz for T1/J1 or E1 Operation; This Clock is Internally Adapted for T1 or E1 Usage in the Host Mode
- Receive-Signal Level Indication from -2.5dB to -36dB in T1 Mode and -2.5dB to -44dB in E1 Mode in Approximate 2.5dB Increments
- Transmit Open- and Short-Circuit Detection
- LIU LOS in Accordance with G.775, ETS 300 233, and T1.231
- Transmit Synchronizer
- Flexible Signaling Extraction and Insertion Using Either the System Interface or Microprocessor Port
- Alarm Detection and Insertion
- T1 Framing Formats of D4, SLC-96, and ESF
- J1 Support
- E1 G.704 and CRC-4 Multiframe
- T1-to-E1 Conversion

Features continued in Section 2.

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1. DETAILED DESCRIPTION

The DS26518 is an 8-port monolithic device featuring independent transceivers that can be software configured for T1, E1, or J1 operation. Each transceiver is composed of a line interface unit, framer, two HDLC controllers, elastic store, and a TDM backplane interface. The DS26518 is controlled via an 8-bit parallel port or the SPI port. Internal impedance matching and termination is provided for both transmit and receive paths, reducing external component count.

Each LIU is composed of a transmit interface, receive interface, and a jitter attenuator. The transmit interface is responsible for generating the necessary waveshapes for driving the network and providing the correct source impedance depending on the type of media used. T1 waveform generation includes DSX-1 line build-outs as well as CSU line build-outs of 0dB, -7.5dB, -15dB, and -22.5dB. E1 waveform generation includes G.703 waveshapes for both 75 Ω coax and 120 Ω twisted cables. The receive interface provides network termination and recovers clock and data from the network. The receive sensitivity adjusts automatically to the incoming signal level and can be programmed for 0dB to -43dB or 0dB to -12dB for E1 applications and 0dB to -12dB or 0dB to -36dB for T1 applications. The jitter attenuator removes phase jitter from the transmitted or received signal. The crystal-less jitter attenuator requires only a T1 or E1 clock rate, or multiple thereof, for both E1 and T1 applications, and can be placed in either transmit or receive data paths.

On the transmit side, clock, data, and frame-sync signals are provided to the framer by the backplane interface section. The framer inserts the appropriate synchronization framing patterns, alarm information, calculates and inserts the CRC codes, and provides the B8ZS/HDB3 (zero code suppression) and AMI line coding. The receive-side framer decodes AMI, B8ZS, and HDB3 line coding, synchronizes to the data stream, reports alarm information, counts framing/coding/CRC errors, and provides clock, data, and frame-sync signals to the backplane interface section.

There are two HDLC controllers per transceiver. Both transmit and receive paths have access to the two HDLC controllers. One of the HDLC controllers can be assigned to some or all time slots of the T1/E1 frame. This controller has a FIFO depth of 256 bytes. The second controller is smaller and can be assigned to at most one time slot or a portion of a time slot, or to the FDL (T1) or Sa bits (E1). This controller has a 64-byte FIFO.

The backplane interface provides a versatile method of sending and receiving data from the host system. Elastic stores provide a method for interfacing to asynchronous systems, converting from a T1/E1 network to a 2.048MHz, 4.096MHz, 8.192MHz, 16.384MHz, or N x 64kHz system backplane. The elastic stores also manage slip conditions (asynchronous interface). An interleave bus option (IBO) is provided to allow up to eight transceivers (single DS26518) to share a high-speed backplane. The DS26518 also contains an internal clock adapter useful for the creation of a synchronous, high-frequency backplane timing source.

The microprocessor port provides access for configuration and status of all the DS26518's features. Diagnostic capabilities include loopbacks, PRBS pattern generation/detection, and 16-bit loop-up and loop-down code generation and detection.

2. FEATURE HIGHLIGHTS

2.1 General

- 17mm x 17mm, 256-pin TE-CSBGA (1.00mm pitch)
- 3.3V supply with 5V tolerant inputs and outputs
- IEEE 1149.1 JTAG boundary scan
- Development support includes evaluation kit, driver source code, and reference designs

2.2 Line Interface

- Requires a single master clock (MCLK) for both E1 and T1 operation. Master clock can be 1.544MHz, 2.048MHz, 3.088MHz, 4.096MHz, 6.176MHz, 8.192MHz, 12.352MHz, or 16.384MHz.
- Fully software configurable
- Short- and long-haul applications
- Ranges include 0dB to -43dB, 0dB to -30dB, 0dB to 20dB, and 0dB to -12dB for E1; 0dB to -36dB, 0dB to 30dB, 0dB to 20dB, and 0dB to -12dB for T1
- Receiver signal level indication from -2.5dB to -36dB in T1 mode and -2.5dB to -44dB in E1 mode in 2.5dB increments
- Software-selectable receive termination for 75 Ω , 100 Ω , 110 Ω , and 120 Ω lines
- Hitless protection switching
- Monitor application gain settings of 14dB, 20dB, 26dB, and 32dB
- G.703 receive synchronization signal mode
- Flexible transmit waveform generation
- T1 DSX-1 line build-outs
- T1 CSU line build-outs of 0dB, -7.5dB, -15dB, and -22.5dB
- E1 waveforms include G.703 waveshapes for both 75 Ω coax and 120 Ω twisted cables
- Analog loss-of-signal detection
- AIS generation independent of loopbacks
- Alternating ones and zeros generation
- Receiver power-down
- Transmitter power-down
- Transmit outputs and receive inputs present a high impedance to the line when no power is applied, supporting redundancy applications
- Transmitter short-circuit limiter with current-limit-exceeded indication
- Transmit open-circuit-detected indication

2.3 Clock Synthesizers

- Backplane clocks output frequencies include 2.048MHz, 4.096MHz, 8.192MHz, and 16.384MHz
 - Derived from user-selected recovered receive clock or REFCLKIO
- CLKO output clock selectable from a wide range of frequencies referenced to MCLK

2.4 Jitter Attenuator

- 32-bit or 128-bit crystal-less jitter attenuator
- Requires only a 1.544MHz or 2.048MHz master clock or multiple thereof, for both E1 and T1 operation
- Can be placed in either the receive or transmit path or disabled
- Limit trip indication

2.5 Framer/Formatter

- Fully independent transmit and receive functionality
- Full receive and transmit path transparency
- T1 framing formats D4 and ESF per T1.403 and expanded SLC-96 support (TR-TSY-008)
- E1 FAS framing and CRC-4 multiframe per G.704/G.706, and G.732 CAS multiframe
- Transmit-side synchronizer
- Transmit midpath CRC recalculate (E1)
- Detailed alarm and status reporting with optional interrupt support
- Large path and line error counters
 - T1: BPV, CV, CRC-6, and framing bit errors
 - E1: BPV, CV, CRC-4, E-bit, and frame alignment errors
 - Timed or manual update modes
- DS1 Idle Code Generation on a per-channel basis in both transmit and receive paths
 - User defined
 - Digital Milliwatt
- ANSI T1.403-1999 support
- G.965 V5.2 link detect
- Ability to monitor one DS0 channel in both the transmit and receive paths
- In-band repeating pattern generators and detectors
 - Three independent generators and detectors
 - Patterns from 1 to 8 bits or 16 bits in length
- Bit oriented code (BOC) support
- Flexible signaling support
 - Software or hardware based
 - Interrupt generated on change of signaling data
 - Optional receive signaling freeze on loss of frame, loss of signal, or frame slip
 - Hardware pins provided to indicate loss of frame (LOF), loss of signal (LOS), loss of transmit clock (LOTC), or signaling freeze condition
- Automatic RAI generation to ETS 300 011 specifications
- RAI-CI and AIS-CI support
- Expanded access to Sa and Si bits
- Option to extend carrier loss criteria to a 1ms period as per ETS 300 233
- Japanese J1 support
- Ability to calculate and check CRC-6 according to the Japanese standard
- Ability to generate Yellow Alarm according to the Japanese standard
- T1-to-E1 conversion

2.6 System Interface

- Independent two-frame receive and transmit elastic stores
- Independent control and clocking
- Controlled slip capability with status
- Minimum delay mode supported
- Flexible TDM backplane supports bus rates from 1.544MHz to 16.384MHz
- Supports T1 to CEPT (E1) conversion
- Programmable output clocks for fractional T1, E1, H0, and H12 applications
- Interleaving PCM bus operation
- Hardware signaling capability
- Receive signaling reinsertion to a backplane multiframe sync
- Availability of signaling in a separate PCM data stream

- Signaling freezing
- Ability to pass the T1 F-bit position through the elastic stores in the 2.048MHz backplane mode
- User-selectable synthesized clock output

2.7 HDLC Controllers

- Two HDLC controller engines for each T1/E1 port
- HDLC-64: Independent 64-byte Rx and Tx buffers with interrupt support
- HDLC-256: Independent 256-byte Rx and Tx buffers with interrupt support
- HDLC-64: Access FDL, Sa, or single DS0 channel
- HDLC-256: Access up to the full T1/E1 frame
- Compatible with polled or interrupt driven environments

2.8 Test and Diagnostics

- IEEE 1149.1 support
- Per-channel programmable on-chip bit error-rate testing (BERT)
- Pseudorandom patterns including QRSS
- User-defined repetitive patterns
- Daly pattern
- Error insertion single and continuous
- Total-bit and errored-bit counts
- Payload error insertion
- Error insertion in the payload portion of the T1 frame in the transmit path
- Errors can be inserted over the entire frame or selected channels
- Insertion options include continuous and absolute number with selectable insertion rates
- F-bit corruption for line testing
- Loopbacks (remote, local, analog, and per-channel loopback)

2.9 Microcontroller Parallel Port

- 8-bit parallel control port
- Intel or Motorola nonmultiplexed support
- Flexible status registers support polled, interrupt, or hybrid program environments
- Software reset supported
- Hardware reset pin
- Software access to device ID and silicon revision

2.10 Slave Serial Peripheral Interface (SPI) Features

- Software access to device ID and silicon revision
- Three-wire synchronous serial data link operating in full-duplex slave mode up to 5Mbps
- Glueless connection and fully compliant to Motorola popular communication processors such as MPC8260 and microcontrollers such as M68HC11
- Software provision ability for active phase of the serial clock (i.e., rising edge vs. falling edge), bit ordering of the serial data (most significant first vs. least significant bit first)
- Flexible status registers support polled, interrupt, or hybrid program environments

3. APPLICATIONS

The DS26518 is useful in applications such as:

- Routers
- Channel Service Units (CSUs)
- Data Service Units (DSUs)
- Muxes
- Switches
- Channel Banks
- T1/E1 Test Equipment

4. SPECIFICATIONS COMPLIANCE

The DS26518 meets all the latest relevant telecommunications specifications. [Table 4-1](#) provides the T1 specifications and [Table 4-2](#) provides the E1 specifications and relevant sections that are applicable to the DS26518.

Table 4-1. T1-Related Telecommunications Specifications

| |
|--|
| ANSI T1.102: Digital Hierarchy Electrical Interface |
| AMI Coding |
| B8ZS Substitution Definition |
| DS1 Electrical Interface. Line rate ± 32 ppm; Pulse Amplitude between 2.4V to 3.6V peak; power level between 12.6dBm to 17.9dBm. The T1 pulse mask is provided that we comply. DSX-1 for cross connects the return loss is greater than -26dB. The DSX-1 cable is restricted up to 655 feet. |
| This specification also provides cable characteristics of DSX-Cross Connect cable—22 AVG cables of 1000 feet. |
| ANSI T1.231: Digital Hierarchy—Layer 1 in Service Performance Monitoring |
| BPV Error Definition; Excessive Zero Definition; LOS description; AIS definition. |
| ANSI T1.403: Network and Customer Installation Interface—DS1 Electrical Interface |
| Description of the Measurement of the T1 Characteristics—100 Ω . Pulse shape and template compliance according to T1.102; power level 12.4dBm to 19.7dBm when all ones are transmitted. |
| LBO for the Customer Interface (CI) is specified as 0dB, -7.5dB, and -15dB. Line rate is ± 32 ppm. Pulse Amplitude is 2.4V to 3.6V. |
| AIS generation as unframed all ones is defined. |
| The total cable attenuation is defined as 22dB. The DS26518 functions with up to -36dB cable loss. |
| Note that the pulse template defined by T1.403 and T1.102 are different, specifically at Times 0.61, -0.27, -34, and 0.77. The DS26518 is compliant to both templates. |
| Pub 62411 |
| This specification has tighter jitter tolerance and transfer characteristics than other specifications. The jitter transfer characteristics are tighter than G.736 and jitter tolerance is tighter the G.823. |
| (ANSI) “Digital Hierarchy—Electrical Interfaces” |
| (ANSI) “Digital Hierarchy—Formats Specification” |
| (ANSI) “Digital Hierarchy—Layer 1 In-Service Digital Transmission Performance Monitoring” |
| (ANSI) “Network and Customer Installation Interfaces—DS1 Electrical Interface” |
| (AT&T) “Requirements for Interfacing Digital Terminal Equipment to Services Employing the Extended Super Frame Format” |
| (AT&T) “High Capacity Digital Service Channel Interface Specification” |
| (TTC) “Frame Structures on Primary and Secondary Hierarchical Digital Interfaces” |
| (TTC) “ISDN Primary Rate User-Network Interface Layer 1 Specification” |

Table 4-2. E1-Related Telecommunications Specifications

| |
|--|
| ITU-T G.703 Physical/Electrical Characteristics of G.703 Hierarchical Digital Interfaces |
| Defines the 2048kbps bit rate— 2048 ± 50 ppm; the transmission media are 75Ω coax or 120Ω twisted pair; peak-to-peak space voltage is ± 0.237 V; nominal pulse width is 244ns. |
| Return loss 51Hz to 102Hz is 6dB, 102Hz to 3072Hz is 8dB, 2048Hz to 3072Hz is 14dB. |
| Nominal peak voltage is 2.37V for coax and 3V for twisted pair. |
| The pulse template for E1 is defined in G.703. |
| ITU-T G.736 Characteristics of Synchronous Digital Multiplex Equipment Operating at 2048kbps |
| The peak-to-peak jitter at 2048kbps must be less than $0.05U_I$ at 20Hz to 100Hz. |
| Jitter transfer between 2.048 synchronization signal and 2.048 transmission signal is provided. |
| ITU-T G.742 Second-Order Digital Multiplex Equipment Operating at 8448kbps |
| The DS26518 jitter attenuator is complaint with jitter transfer curve for sinusoidal jitter input. |
| ITU-T G.772 |
| This specification provides the method for using receiver for transceiver 0 as a monitor for the remaining seven transmitter/receiver combinations. |
| ITU-T G.775 |
| An LOS detection criterion is defined. |
| ITU-T G.823 The control of jitter and wander within digital networks that are based on 2.048kbps hierarchy. |
| G.823 Provides the jitter amplitude tolerance at different frequencies, specifically 20Hz, 2.4kHz, 18kHz, and 100kHz. |
| ETS 300 233 |
| This specification provides LOS and AIS signal criteria for E1 mode. |
| Pub 62411 |
| This specification has tighter jitter tolerance and transfer characteristics than other specifications. The jitter transfer characteristics are tighter than G.736 and jitter tolerance is tighter than G.823. |
| (ITU-T) "Synchronous Frame Structures used at 1544, 6312, 2048, 8488, and 44736kbps Hierarchical Levels" |
| (ITU-T) "Frame Alignment and Cyclic Redundancy Check (CRC) Procedures Relating to Basic Frame Structures Defined in Recommendation G.704" |
| (ITU-T) "Characteristics of Primary PCM Multiplex Equipment Operating at 2048kbps" |
| (ITU-T) Characteristics of a Synchronous Digital Multiplex Equipment Operating at 2048kbps" |
| (ITU-T) "Loss of Signal (LOS) and Alarm Indication Signal (AIS) Defect Detection and Clearance Criteria" |
| (ITU-T) "The Control of Jitter and Wander Within Digital Networks Which are Based on the 2048kbps Hierarchy" |
| (ITU-T) "Primary Rate User-Network Interface—Layer 1 Specification" |
| (ITU-T) "Error Performance Measuring Equipment Operating at the Primary Rate and Above" |
| (ITU-T) "In-Service Code Violation Monitors for Digital Systems" |
| (ETS) "Integrated Services Digital Network (ISDN); Primary Rate User-Network Interface (UNI); Part 1/Layer 1 Specification" |
| (ETS) "Transmission and Multiplexing; Physical/Electrical Characteristics of Hierarchical Digital Interfaces for Equipment Using the 2048kbps-Based Plesiochronous or Synchronous Digital Hierarchies" |
| (ETS) "Integrated Services Digital Network (ISDN); Access Digital Section for ISDN Primary Rate" |
| (ETS) "Integrated Services Digital Network (ISDN); Attachment Requirements for Terminal Equipment to Connect to an ISDN Using ISDN Primary Rate Access" |
| (ETS) "Business Telecommunications (BT); Open Network Provision (ONP) Technical Requirements; 2048kbps Digital Unstructured Leased Lines (D2048U) Attachment Requirements for Terminal Equipment Interface" |
| (ETS) "Business Telecommunications (BTC); 2048kbps Digital Structured Leased Lines (D2048S); Attachment Requirements for Terminal Equipment Interface" |
| (ITU-T) "Synchronous Frame Structures Used at 1544, 6312, 2048, 8488, and 44736kbps Hierarchical Levels" |
| (ITU-T) "Frame Alignment and Cyclic Redundancy Check (CRC) Procedures Relating to Basic Frame Structures Defined in Recommendation G.704" |

5. ACRONYMS AND GLOSSARY

This data sheet assumes a particular nomenclature of the T1 and E1 operating environment. In each 125 μ s T1 frame, there are 24 8-bit channels plus a framing bit. It is assumed that the framing bit is sent first followed by channel 1. For T1 and E1 each channel is made up of 8 bits, which are numbered 1 to 8. Bit 1, the MSB, is transmitted first. Bit 8, the LSB, is transmitted last.

Locked refers to two clock signals that are phase- or frequency-locked or derived from a common clock (i.e., a 1.544MHz clock can be locked to a 2.048MHz clock if they share the same 8kHz component).

Table 5-1. Time Slot Numbering Schemes

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------------------|---|---|---|---|---|---|---|---|---|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| TS | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | 25 | 26 | 27 | 28 | 29 | 30 | 31 |
| Channel | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | 25 | 26 | 27 | 28 | 29 | 30 | 31 | 32 |
| Phone Channel | | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | 25 | 26 | 27 | 28 | 29 | 30 |

6. MAJOR OPERATING MODES

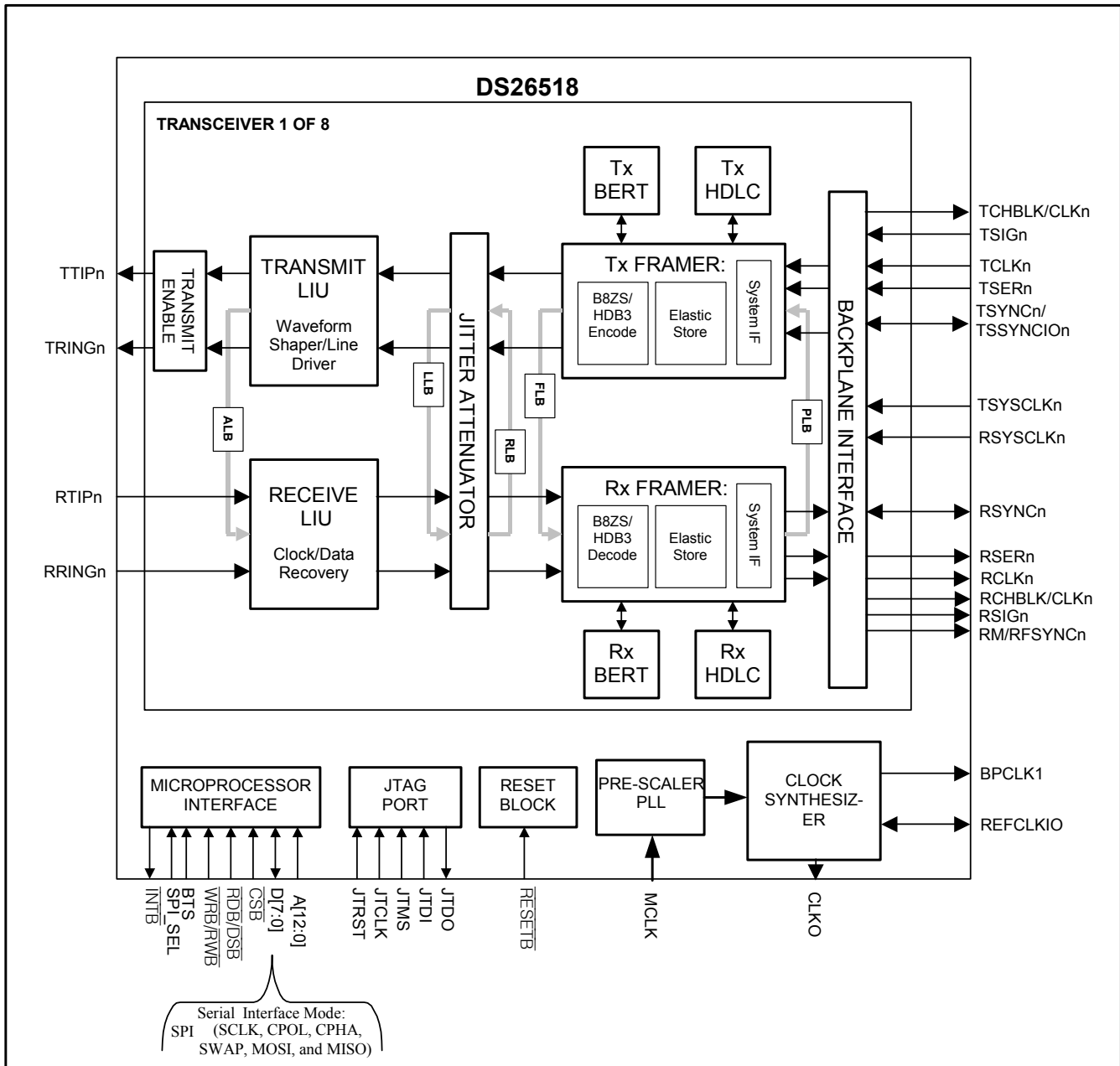
The DS26518 has two major modes of operation: T1 mode and E1 mode. The mode of operation for each LIU is configured in the [LTRCR](#) register. The mode of operation for each framer is configured in the [TMMR](#) register. J1 operation is a special case of T1 operating mode.

7. BLOCK DIAGRAMS

Figure 7-1. Block Diagram



Figure 7-2. Detailed Block Diagram



8. PIN DESCRIPTIONS

8.1 Pin Functional Description

Table 8-1. Detailed Pin Descriptions

| NAME | PIN | TYPE | FUNCTION |
|------------------------|----------|-------------------------------|--|
| ANALOG TRANSMIT | | | |
| TTIP1 | A1, A2 | Analog Output, High Impedance | <p>Transmit Bipolar Tip for Transceiver 1 to 8. These pins are differential line driver tip outputs. These pins can be high impedance if:</p> <p>If TXENABLE is low, TTIPn/TRINGn will be high impedance. Note that if TXENABLE is low, the register settings for control of TTIPn/TRINGn are ignored and output is high impedance.</p> <p>The differential outputs of TTIPn and TRINGn can provide internal matched impedance for E1 75Ω, E1 120Ω, T1 100Ω, or J1 110Ω. The user can turn off internal termination.</p> <p>Note: The two pins shown for each transmit bipolar tip (e.g., pins A1 and A2 for TTIP1) should be tied together.</p> |
| TTIP2 | H1, H2 | | |
| TTIP3 | J1 J2 | | |
| TTIP4 | T1, T2 | | |
| TTIP5 | T15, T16 | | |
| TTIP6 | J15, J16 | | |
| TTIP7 | H15, H16 | | |
| TTIP8 | A15, A16 | | |
| TRING1 | A3, B3 | Analog Output, High Impedance | <p>Transmit Bipolar Ring for Transceiver 1 to 8. These pins are differential line driver ring outputs. These pins can be high impedance if:</p> <p>If TXENABLE is low, TTIPn/TRINGn will be high impedance. Note that if TXENABLE is low, the register settings for control of TTIPn/TRINGn are ignored and output is high impedance.</p> <p>The differential outputs of TTIPn and TRINGn can provide internal matched impedance for E1 75Ω, E1 120Ω, T1 100Ω, or J1 110Ω. The user can turn off internal termination.</p> <p>Note: The two pins shown for each transmit bipolar ring (e.g., pins A3 and B3 for TRING1) should be tied together.</p> |
| TRING2 | G3, H3 | | |
| TRING3 | J3, K3 | | |
| TRING4 | R3, T3 | | |
| TRING5 | R14, T14 | | |
| TRING6 | J14, K14 | | |
| TRING7 | G14, H14 | | |
| TRING8 | A14, B14 | | |
| TXENABLE/ SCAN_EN | L13 | Input | <p>Transmit Enable. If this pin is pulled low, all transmitter outputs (TTIPn and TRINGn) are high impedance. The register settings for tri-state control of TTIPn/TRINGn are ignored if TXENABLE is low. If TXENABLE is high, the particular driver can be tri-stated by the register settings.</p> <p>Scan Enable. When low, device is in normal operation. Scan enable is selected by the SCANMODE pin. Note: User should not select scan enable—test mode only.</p> |
| ANALOG RECEIVE | | | |
| RTIP1 | C1 | Analog Input | <p>Receive Bipolar Tip for Transceiver 1 to 8. The differential inputs of RTIPn and RRINGn can provide internal matched impedance for E1 75Ω, E1 120Ω, T1 100Ω, or J1 110Ω. The user can turn off internal termination via the LIU Receive Impedance and Sensitivity Monitor register (LRISMR).</p> |
| RTIP2 | F1 | | |
| RTIP3 | L1 | | |
| RTIP4 | P1 | | |
| RTIP5 | P16 | | |
| RTIP6 | L16 | | |
| RTIP7 | F16 | | |
| RTIP8 | C16 | | |
| RRING1 | C2 | Analog Input | <p>Receive Bipolar Ring for Transceiver 1 to 8. The differential inputs of RTIPn and RRINGn can provide internal matched impedance for E1 75Ω, E1 120Ω, T1 100Ω, or J1 110Ω. The user has the option of turning off internal termination via the LIU Receive Impedance and Sensitivity Monitor register (LRISMR).</p> |
| RRING2 | F2 | | |
| RRING3 | L2 | | |
| RRING4 | P2 | | |
| RRING5 | P15 | | |
| RRING6 | L15 | | |
| RRING7 | F15 | | |
| RRING8 | C15 | | |
| RESREF | J5 | Input | <p>Resistor Reference. This pin is used to calibrate the internal impedance match resistors of the receive LIUs. This pin should be tied to V_{SS} through a 10kΩ ±1% resistor.</p> |

| NAME | PIN | TYPE | FUNCTION |
|-----------------------------|-----|---|---|
| TRANSMIT FRAMER | | | |
| TSER1 | F6 | Input | Transmit NRZ Serial Data 1 to 8. These pins are sampled on the falling edge of TCLKn when the transmit-side elastic store is disabled. These pins are sampled on the falling edge of TSYCLKn when the transmit-side elastic store is enabled. In IBO mode, data for multiple framers can be used in high-speed multiplexed scheme. This is described in Section 9.8.2 . The table there presents the combination of framer data for each of the streams. TSYCLKn is used as a reference when IBO is invoked. See Table 9-8 . |
| TSER2 | E7 | | |
| TSER3 | R4 | | |
| TSER4 | N7 | | |
| TSER5 | M10 | | |
| TSER6 | L11 | | |
| TSER7 | F10 | | |
| TSER8 | D12 | | |
| TCLK1 | C5 | Input | Transmit Clock 1 to 8. A 1.544MHz or a 2.048MHz primary clock. Used to clock data through the transmit side of the transceiver. TSErn data is sampled on the falling edge of TCLKn. TCLKn is used to sample TSErn when the elastic store is not enabled or IBO is not used. When the elastic store is enabled, TCLKn is used as the internal transmit clock for the framer side or the elastic store including the transmit framer and LIU. With the elastic store enabled, TCLKn can be either synchronous or asynchronous to TSYCLKn which either prevents or allows for slips. When IBO mode is enabled, TCLKn must be synchronous to TSYCLKn which prevents slips in the elastic store. Note: This clock must be provided for proper device operation. The only exception is when the TCR3 register is configured to source TCLK internally from RCLK. |
| TCLK2 | D7 | | |
| TCLK3 | P5 | | |
| TCLK4 | L8 | | |
| TCLK5 | L10 | | |
| TCLK6 | N11 | | |
| TCLK7 | E10 | | |
| TCLK8 | B13 | | |
| TSYSCLK1 | P13 | Input | Transmit System Clock 1. 1.544MHz, 2.048MHz, 4.096MHz, 8.192MHz, or 16.384MHz clock. Only used when the transmit-side elastic store function is enabled. Should be tied low in applications that do not use the transmit-side elastic store. The clock can be 4.096MHz, 8.912MHz, or 16.384MHz when IBO mode is used. TSYCLK1 does not have an internal pulldown resistor. Note: If the GTCR1.528MD bit is set, TSYCLK1 becomes the master TSYCLK for all framers. |
| TSYSCLK2/ AL/RSIGF/FLOS2 | F3 | Input with internal pulldown/ Output | Transmit System Clock 2 to 8. 1.544MHz, 2.048MHz, 4.096MHz, 8.192MHz, or 16.384MHz clock. Only used when the transmit-side elastic store function is enabled. Should be tied low in applications that do not use the transmit-side elastic store. The clock can be 4.096MHz, 8.912MHz, or 16.384MHz when IBO mode is used. TSYCLK1 does not have an internal pulldown resistor. Note: If the GTCR1.528MD bit is set, TSYCLK1 becomes the master TSYCLK for all framers. Analog Loss/Receive-Signaling Freeze/Framer LOS. Analog LOS reflects the LOS (loss of signal) detected by the LIU front-end and framer LOS is LOS detection by the corresponding framer; the same pins can reflect receive-signaling freeze indications. This selection can be made by settings in the Global Transceiver Clock Control Register 1 (GTCCR1). AL/RSIGF/FLOS[8:2] is available only by setting the GTCR1.528MD bit to 1. |
| TSYSCLK3/ AL/RSIGF/FLOS3 | L3 | | |
| TSYSCLK4/ AL/RSIGF/FLOS4 | P3 | | |
| TSYSCLK5/ AL/RSIGF/FLOS5 | P14 | | |
| TSYSCLK6/ AL/RSIGF/FLOS6 | L14 | | |
| TSYSCLK7/ AL/RSIGF/FLOS7 | F14 | | |
| TSYSCLK8/ AL/RSIGF/FLOS8 | C14 | | |
| TSYNC1/ TSSYNClO1 | B4 | | |
| TSYNC2/ TSSYNClO2 | F7 | | |
| TSYNC3/ TSSYNClO3 | M6 | | |
| TSYNC4/ TSSYNClO4 | M7 | | |
| TSYNC5/ TSSYNClO5 | N10 | | |
| TSYNC6/ TSSYNClO6 | T12 | | |
| TSYNC7/ TSSYNClO7 | B11 | | |

| NAME | PIN | TYPE | FUNCTION |
|----------------------|-----|------------------|---|
| TSYNC8/ TSSYNClO8 | A13 | | be generated. This pulse in combination with BPCLK1 can be used as an IBO master. TSSYNClOn can be used as a source to RSYNCn and TSSYNClOn of another DS26518 or RSYNC and TSSYNC of other Maxim parts. Note: <i>TSSYNClO[8:1] are not used when GTCR1.528MD is set. When GTCR1.528MD is set, the TSSYNClO pin (N13) is used.</i> |
| TSSYNClO | N13 | Input/ Output | <p>Note: <i>In default operation, this pin is not used. When GTCR1.528MD is set, this pin is active. If pin is not used, tie low through a resistor.</i></p> <p>Transmit System Synchronization In. This pin is selected when the transmit-side elastic store is enabled. A pulse at this pin establishes either frame or multiframe boundaries for the transmit side. Note that if the elastic store is enabled, frame or multiframe boundary will be established for all transmitters. Should be tied low in applications that do not use the transmit-side elastic store. The operation of this signal is synchronous with TSYSClKn.</p> <p>Transmit System Synchronization Out. If configured as an output and the transmit-side elastic store is enabled, an 8kHz pulse synchronous to BPCLK1 will be generated. This pulse in combination with BPCLK1 can be used as an IBO master. TSSYNClO can be used as a source to RSYNCn and TSSYNClO of another DS26518 or RSYNC and TSSYNC of other Maxim parts.</p> |
| TSIG1 | D5 | Input | <p>Transmit Signaling 1 to 8. When enabled, this input samples signaling bits for insertion into outgoing PCM data stream. Sampled on the falling edge of TClKn when the transmit-side elastic store is disabled. Sampled on the falling edge of TSYSClKn when the transmit-side elastic store is enabled. In IBO mode, the TSIGn streams can run up to 16.384MHz. See Table 9-9.</p> |
| TSIG2 | A6 | | |
| TSIG3 | T4 | | |
| TSIG4 | R6 | | |
| TSIG5 | T10 | | |
| TSIG6 | R12 | | |
| TSIG7 | A11 | | |
| TSIG8 | C13 | | |
| TCHBLK1/ TCHCLK1 | A5 | Output | <p>Transmit Channel Block/Transmit Channel Block Clock. A dual function pin.</p> <p>TCHBLK[1:8]. TCHBLKn is a user-programmable output that can be forced high or low during any of the channels. It is synchronous with TClKn when the transmit-side elastic store is disabled. It is synchronous with TSYSClKn when the transmit-side elastic store is enabled. It is useful for blocking clocks to a serial UART or LAPD controller in applications where not all channels are used such as Fractional T1, Fractional E1, 384kbps (H0), 768kbps, or ISDN-PRI. Also useful for locating individual channels in drop-and-insert applications, for external per-channel loopback, and for per-channel conditioning.</p> <p>TCHCLK[1:8]. TCHCLKn is a 192kHz (T1) or 256kHz (E1) clock that pulses high during the LSB of each channel. It can also be programmed to output a gated transmit bit clock controlled by TCHBLKn. It is synchronous with TClKn when the transmit-side elastic store is disabled. It is synchronous with TSYSClKn when the transmit-side elastic store is enabled. Useful for parallel-to-serial conversion of channel data.</p> |
| TCHBLK2/ TCHCLK2 | C7 | | |
| TCHBLK3/ TCHCLK3 | L7 | | |
| TCHBLK4/ TCHCLK4 | P7 | | |
| TCHBLK5/ TCHCLK5 | P9 | | |
| TCHBLK6/ TCHCLK6 | P11 | | |
| TCHBLK7/ TCHCLK7 | D10 | | |
| TCHBLK8/ TCHCLK8 | E11 | | |

| NAME | PIN | TYPE | FUNCTION |
|-----------------------|-----|---|---|
| RECEIVE FRAMER | | | |
| RSER1 | E5 | Output | <p>Received Serial Data 1 to 8. Received NRZ serial data. Updated on rising edges of RCLKn when the receive-side elastic store is disabled. Updated on the rising edges of RSYSCLKn when the receive-side elastic store is enabled.</p> <p>When IBO mode is used, the RSERn pins can output data for multiple framers. The RSERn data is synchronous to RSYSCLKn. See Section 9.8.2 and Table 9-6.</p> |
| RSER2 | D6 | | |
| RSER3 | N4 | | |
| RSER4 | N6 | | |
| RSER5 | M11 | | |
| RSER6 | M12 | | |
| RSER7 | B12 | | |
| RSER8 | F11 | | |
| RCLK1 | F4 | Output | <p>Receive Clock 1 to 8. A 1.544MHz (T1) or 2.048MHz (E1) clock that is used to clock data through the receive-side framer. This clock is recovered from the signal at RTIPn and RRINGn. RSERn data is output on the rising edge of RCLKn. RCLKn is used to output RSERn when the elastic store is not enabled or IBO is not used. When the elastic store is enabled or IBO is used, the RSERn is clocked by RSYSCLKn.</p> |
| RCLK2 | G4 | | |
| RCLK3 | L4 | | |
| RCLK4 | M4 | | |
| RCLK5 | K13 | | |
| RCLK6 | J13 | | |
| RCLK7 | F13 | | |
| RCLK8 | E13 | | |
| RSYSCLK1 | L12 | Input | <p>Receive System Clock 1. 1.544MHz, 2.048MHz, 4.096MHz, 8.192MHz, or 16.384MHz receive backplane clock. Only used when the receive-side elastic store function is enabled. Should be tied low in applications that do not use the receive-side elastic store. Multiple of 2.048MHz is expected when the IBO mode is used. Note: If the GTCR1.528MD bit is set, RSYSCLK1 becomes the master RSYSCLK for all framers.</p> |
| RSYSCLK2/ RLF/LTC2 | E3 | Input with internal pulldown/ Output | <p>Receive System Clock 2 to 8. 1.544MHz, 2.048MHz, 4.096MHz, 8.192MHz, or 16.384MHz receive backplane clock. Only used when the receive-side elastic store function is enabled. Should be tied low in applications that do not use the receive-side elastic store. Multiple of 2.048MHz is expected when the IBO Mode is used.</p> <p>Receive Loss of Frame/Loss of Transmit Clock. This pin can also be programmed to either toggle high when the synchronizer is searching for the frame and multiframe or to toggle high if the TCLKn pin has not been toggled for approximately three clock periods.</p> <p>RLF/LTC[8:2] are available when GTCR1.528MD = 1.</p> <p>Note: If the GTCR1.528MD bit is set, RSYSCLK1 becomes the master RSYSCLK for all framers.</p> |
| RSYSCLK3/ RLF/LTC3 | M3 | | |
| RSYSCLK4/ RLF/LTC4 | N3 | | |
| RSYSCLK5/ RLF/LTC5 | N14 | | |
| RSYSCLK6/ RLF/LTC6 | M14 | | |
| RSYSCLK7/ RLF/LTC7 | E14 | | |
| RSYSCLK8/ RLF/LTC8 | D14 | | |
| RSYNC1 | A4 | | |
| RSYNC2 | B6 | | |
| RSYNC2 | N5 | | |
| RSYNC2 | T6 | | |
| RSYNC5 | R10 | | |
| RSYNC6 | P12 | | |
| RSYNC7 | C11 | | |
| RSYNC8 | D13 | | |

| NAME | PIN | TYPE | FUNCTION |
|---------------------|-----|--------|---|
| RMSYNC1/ RFSYNC1 | C4 | Output | Receive Multiframe/Frame Synchronization 1 to 8. A dual function pin to indicate frame or multiframe synchronization. RFSYNcn is an extracted 8kHz pulse, one RCLKn wide that identifies frame boundaries. RMSYNcn is an extracted pulse, one RCLKn wide (elastic store disabled) or one RSYCLKn wide (elastic store enabled), that identifies multiframe boundaries. When the receive elastic store is enabled, the RMSYNcn signal indicates the multiframe sync on the system (backplane) side of the elastic store. In E1 mode, this pin can indicate either the CRC-4 or CAS multiframe as determined by the RSMS2 control bit in the Receive I/O Configuration register (RIOCR.1). |
| RMSYNC2/ RFSYNC2 | C6 | | |
| RMSYNC3/ RFSYNC3 | P4 | | |
| RMSYNC4/ RFSYNC4 | P6 | | |
| RMSYNC5/ RFSYNC5 | P10 | | |
| RMSYNC6/ RFSYNC6 | N12 | | |
| RMSYNC7/ RFSYNC7 | D11 | | |
| RMSYNC8/ RFSYNC8 | E12 | | |
| RSIG1 | D4 | Output | Receive Signaling 1 to 8. Outputs signaling bits in a PCM format. Updated on rising edges of RCLKn when the receive-side elastic store is disabled. Updated on the rising edges of RSYCLKn when the receive-side elastic store is enabled. See Table 9-7 . |
| RSIG2 | E6 | | |
| RSIG3 | M5 | | |
| RSIG4 | R5 | | |
| RSIG5 | R11 | | |
| RSIG6 | R13 | | |
| RSIG7 | A12 | | |
| RSIG8 | F12 | | |
| RCHBLK1/ RCHCLK1 | E4 | Output | Receive Channel Block/Receive Channel Block Clock. This pin can be configured to output either RCHBLK or RCHCLK. RCHBLK[1:8]. RCHBLKn is a user-programmable output that can be forced high or low during any of the 24 T1 or 32 E1 channels. It is synchronous with RCLKn when the receive-side elastic store is disabled. It is synchronous with RSYCLKn when the receive-side elastic store is enabled. This pin is useful for blocking clocks to a serial UART or LAPD controller in applications where not all channels are used such as fractional service, 384kbps service, 768kbps, or ISDN-PRI. Also useful for locating individual channels in drop-and-insert applications, for external per-channel loopback, and for per-channel conditioning. RCHCLK[1:8]. RCHCLKn is a 192kHz (T1) or 256kHz (E1) clock that pulses high during the LSB of each channel. It is synchronous with RCLKn when the receive-side elastic store is disabled. It is synchronous with RSYCLKn when the receive-side elastic store is enabled. It is useful for parallel-to-serial conversion of channel data. |
| RCHBLK2/ RCHCLK2 | B5 | | |
| RCHBLK3/ RCHCLK3 | L6 | | |
| RCHBLK4/ RCHCLK4 | T5 | | |
| RCHBLK5/ RCHCLK5 | T11 | | |
| RCHBLK6/ RCHCLK6 | T13 | | |
| RCHBLK7/ RCHCLK7 | C12 | | |
| RCHBLK8/ RCHCLK8 | G13 | | |
| BPCLK1 | E8 | Output | Backplane Clock 1. Programmable clock output that can be set to 2.048MHz, 4.096MHz, 8.192MHz, or 16.384MHz. The reference for this clock can be RCLK[8:1], a 1.544MHz or 2.048MHz clock frequency derived from MCLK, or an external reference clock (REFCLKIO). This allows system clocks to be referenced from external sources, the T1J1E1 recovered clocks, or the MCLK oscillator. |
| CLKO/ RLF/LTC1 | D3 | Output | Clock Out. Clock output pin that can be programmed to output numerous frequencies referenced to MCLK. Frequencies available: 1.544MHz, 2.048MHz, 4.096MHz, 8.192MHz, 12.288MHz, 16.384MHz, 256kHz, and 64kHz. GTCCR3 .CLKOSEL[2:0] selects the frequency. Receive Loss of Frame/Loss of Transmit Clock. This pin can also be programmed to either toggle high when the synchronizer is searching for the frame and multiframe, or to toggle high if the TCLKn pin has not been toggled for approximately three clock periods. RLF/LTC1 is available on the DS26518 when GTCCR1 .528MD = 1. |

| NAME | PIN | TYPE | FUNCTION |
|---------------------------------------|-----|------------------|---|
| MICROPROCESSOR INTERFACE | | | |
| A12 | C8 | Input | Address [12:0]. This bus selects a specific register in the DS26518 during read/write access. A12 is the MSB and A0 is the LSB. |
| A11 | A8 | | |
| A10 | B8 | | |
| A9 | F8 | | |
| A8 | B9 | | |
| A7 | A9 | | |
| A6 | C9 | | |
| A5 | D9 | | |
| A4 | E9 | | |
| A3 | F9 | | |
| A2 | B10 | | |
| A1 | A10 | | |
| A0 | C10 | | |
| D7/SPI_CPOL | T9 | Input/ Output | Data 7/SPI Interface Clock Polarity D7: Bit 7 of the 8-bit data bus used to input data during register writes and data outputs during register reads. Not driven when $\overline{CSB} = 1$. SPI_CPOL: This signal selects the clock polarity when SPI_SEL = 1. See Section 9.1.2 for detailed timing and functionality information. Default setting is low. |
| D6/SPI_CPHA | N9 | Input/ Output | Data 6/SPI Interface Clock Phase D6: Bit 6 of the 8-bit data bus used to input data during register writes and data outputs during register reads. Not driven when $\overline{CSB} = 1$. SPI_CPHA: This signal selects the clock phase when SPI_SEL = 1. See Section 9.1.2 for detailed timing and functionality information. Default setting is low. |
| D5/SPI_SWAP | M9 | Input/ Output | Data 5/SPI Bit Order Swap D5: Bit 5 of the 8-bit data bus used to input data during register writes and data outputs during register reads. Not driven when $\overline{CSB} = 1$. SPI_SWAP: This signal is active when SPI_SEL = 1. The address and data bit order is swapped when SPI_SWAP is high. The R/W and B bit positions are never changed in the control word. 0 = LSB is transmitted and received first. 1 = MSB is transmitted and received first. |
| D4 | R8 | Input/ Output | Data 4. Bit 4 of the 8-bit data bus used to input data during register writes and data outputs during register reads. Not driven when $\overline{CSB} = 1$. |
| D3 | T8 | Input/ Output | Data 3. Bit 3 of the 8-bit data bus used to input data during register writes and data outputs during register reads. Not driven when $\overline{CSB} = 1$. |
| D2/SPI_SCLK | P8 | Input/ Output | Data 2/SPI Serial Interface Clock D2: Bit 2 of the 8-bit data bus used to input data during register writes and data outputs during register reads. Not driven when $\overline{CSB} = 1$. SPI_SCLK: SPI Serial Clock Input when SPI_SEL = 1. |
| D1/SPI_MOSI | L9 | Input/ Output | Data 1/SPI Serial Interface Data Master Out-Slave In D1: Bit 1 of the 8-bit data bus used to input data during register writes, and data outputs during register reads. Not driven when $\overline{CSB} = 1$. SPI_MOSI: SPI Serial Data Input (Master Out-Slave In) when SPI_SEL = 1. |
| D0/SPI_MISO | N8 | Input/ Output | Data 0/SPI Serial Interface Data Master In-Slave Out D0: Bit 0 of the 8-bit data bus used to input data during register writes and data outputs during register reads. Not driven when $\overline{CSB} = 1$. SPI_MISO: SPI Serial Data Output (Master In-Slave Out) when SPI_SEL = 1. |
| \overline{CSB} | T7 | Input | Chip-Select Bar. This active-low signal is used to qualify register read/write accesses. The RDB/DSB and WRB/RWB signals are qualified with \overline{CSB} . |
| $\overline{RDB}/$ \overline{DSB} | M8 | Input | Read Bar/Data-Strobe Bar. This active-low signal along with \overline{CSB} qualifies read access to one of the DS26518 registers. The DS26518 drives the data bus with the contents of the addressed register, in Intel bus mode, while RDB and \overline{CSB} are low or, in Motorola bus mode, while DSB and \overline{CSB} are low and RWB is high. |

| NAME | PIN | TYPE | FUNCTION |
|---|-----|---|--|
| $\overline{\text{WRB}}/\overline{\text{RWB}}$ | R7 | Input | Write Bar/Read-Write Bar. This active-low signal along with $\overline{\text{CSB}}$ qualifies write access to one of the DS26518 registers. Data at D[7:0] is written into the addressed register, in Intel bus mode, at the rising edge of $\overline{\text{WRB}}$ while $\overline{\text{CSB}}$ is low or, in Motorola bus mode, at the rising edge of $\overline{\text{DSB}}$ while $\overline{\text{RWB}}$ and $\overline{\text{CSB}}$ are low. |
| $\overline{\text{INTB}}$ | R9 | Output, Tri-Stateable | Interrupt Bar. This active-low output is asserted when an unmasked interrupt event is detected. $\overline{\text{INTB}}$ will be deasserted (and tri-stated) when all interrupts have been acknowledged and serviced. Extensive mask bits are provided at the global level, framer, LIU, and BERT level. |
| SPI_SEL/ AL/RSIGF/FLOS1 | C3 | Input with internal pulldown/ Output | SPI Serial Bus Mode Select/Analog Loss/Receive Signaling Freeze/Framer LOS SPI_SEL: 0 = Parallel Bus Mode, 1 = SPI Serial Bus Mode AL/RSIGF/FLOS1: Analog LOS reflects the loss of signal detected by the LIU front-end; framer LOS is LOS detection by the corresponding framer. The same pins can reflect receive-signaling freeze indications. This selection can be made by settings in Global Transceiver Control Register (GTCR1). AL/RSIGF/FLOS1 are available by setting the GTCR1.528MD bit to 1. |
| BTS | M13 | Input | Bus Type Select. Set high to select Motorola bus timing, low to select Intel bus timing. This pin controls the function of the $\overline{\text{RDB}}/\overline{\text{DSB}}$ and $\overline{\text{WRB}}$ pins. Note: If SPI mode is selected by the SPI_SEL pin, this pin must be tied low. |
| SYSTEM INTERFACE | | | |
| MCLK | B7 | Input | Master Clock. This is an independent free-running clock whose input can be a multiple of 2.048MHz ± 50 ppm or 1.544MHz ± 50 ppm. The clock selection is available by bits MPS0 and MPS1 and FREQSEL. Multiple of 2.048MHz can be internally adapted to 1.544MHz. Multiple of 1.544MHz can be adapted to 2.048MHz. Note that TCLKn must be 2.048MHz for E1 and 1.544MHz for T1/J1 operation. See Table 10-14 . |
| $\overline{\text{RESETB}}$ | J12 | Input | Reset Bar. Active-low reset. This input forces the complete DS26518 reset. This includes reset of the registers, framers, and LIUs. |
| REFCLKIO | A7 | Input/ Output | Reference Clock Input/Output <i>Input:</i> A 2.048MHz or 1.544MHz clock input. This clock can be used to generate the backplane clock. This allows for the users to synchronize the system backplane with the reference clock. The other options for the backplane clock reference are LIU-received clocks or MCLK. <i>Output:</i> This signal can also be used to output a 1.544MHz or 2.048MHz reference clock. This allows for multiple DS26518s to share the same reference for generation of the backplane clock. Hence, in a system consisting of multiple DS26518s, one can be a master and others a slave using the same reference clock. |
| TEST | | | |
| DIGIOEN | D8 | Input, Pullup | Digital Enable. When this pin and $\overline{\text{JTRST}}$ are pulled low, all digital I/O pins are placed in a high-impedance state. If this pin is high the digital I/O pins operate normally. This pin must be connected to V_{DD} for normal operation. |
| $\overline{\text{JTRST}}$ | L5 | Input, Pullup | JTAG Reset. $\overline{\text{JTRST}}$ is used to asynchronously reset the test access port controller. After power-up, $\overline{\text{JTRST}}$ must be toggled from low to high. This action sets the device into the JTAG DEVICE ID mode. Pulling $\overline{\text{JTRST}}$ low restores normal device operation. $\overline{\text{JTRST}}$ is pulled high internally via a 10k Ω resistor operation. If boundary scan is not used, this pin should be held low. |
| JTMS | K4 | Input, Pullup | JTAG Mode Select. This pin is sampled on the rising edge of JTCLK and is used to place the test access port into the various defined IEEE 1149.1 states. This pin has a 10k Ω pullup resistor. |
| JTCLK | F5 | Input | JTAG Clock. This signal is used to shift data into JTDI on the rising edge and out of JTDO on the falling edge. |
| JTDI | H4 | Input, Pullup | JTAG Data In. Test instructions and data are clocked into this pin on the rising edge of JTCLK. This pin has a 10k Ω pullup resistor. |
| JTDO | J4 | Output, High Impedance | JTAG Data Out. Test instructions and data are clocked out of this pin on the falling edge of JTCLK. If not used, this pin should be left unconnected. |

| NAME | PIN | TYPE | FUNCTION |
|-----------------------|--|-------|---|
| SCANMODE | H13 | Input | Scan Mode. When low, normal operational clocks are used to clock the flip flops. User should tie low. |
| POWER SUPPLIES | | | |
| ATVDD | B1, B16, G1, G16, K1, K16, R1, R16 | — | 3.3V ±5% Analog Transmit Power Supply. These V_{DD} inputs are used for the transmit LIU sections of the DS26518. |
| ATVSS | B2, B15, G2, G15, K2, K15, R2, R15 | — | Analog Transmit V_{SS}. These pins are used for transmit analog V_{SS} . |
| ARVDD | D1, D16, E1, E16, M1, M16, N1, N16 | — | 3.3V ±5% Analog Receive Power Supply. These V_{DD} inputs are used for the receive LIU sections of the DS26518. |
| ARVSS | D2, D15, E2, E15, M2, M15, N2, N15 | — | Analog Receive V_{SS}. These pins are used for analog V_{SS} for the receivers. |
| ACVDD | H7 | — | 1.8V ±5% Analog Clock Conversion V_{DD}. This V_{DD} input is used for the clock conversion unit (CLAD) of the DS26518. |
| ACVSS | J7 | — | Analog Clock V_{SS}. This pin is used for clock converter analog V_{SS} . |
| DVDD33 | G5, G6, G11, G12, H5, H6, H8, H9, H10, H11 | — | 3.3V ±5% Power Supply for I/Os |
| DVDD18 | G7–G10 | — | 1.8V ±5% Power Supply for Internal V_{DD} |
| DVSS | H12, J6, J8–J11, K5–K12 | — | Digital Ground |

9. FUNCTIONAL DESCRIPTION

9.1 Processor Interface

Microprocessor control of the DS26518 is accomplished through the 28 hardware pins of the microprocessor port. The 8-bit parallel data bus can be configured for Intel or Motorola modes of operation with the bus type select (BTS) pin. When the BTS pin is a logic 0, bus timing is in Intel mode, as shown in [Figure 13-2](#) and [Figure 13-3](#). When the BTS pin is a logic 1, bus timing is in Motorola mode, as shown in [Figure 13-4](#) and [Figure 13-5](#). The address space is mapped through the use of 13 address lines, A[12:0]. Multiplexed mode is not supported on the processor interface.

The chip-select bar ($\overline{\text{CSB}}$) pin must be brought to a logic-low level to gain read and write access to the microprocessor port. With Intel timing selected, the read-data bar ($\overline{\text{RDB}}$) and write-read bar ($\overline{\text{WRB}}$) pins are used to indicate read and write operations and latch data through the interface. With Motorola timing selected, the read-write bar ($\overline{\text{RWB}}$) pin is used to indicate read and write operations while the data-strobe bar ($\overline{\text{DSB}}$) pin is used to latch data through the interface.

The interrupt output pin ($\overline{\text{INTB}}$) is an open-drain output that asserts a logic-low level upon a number of software maskable interrupt conditions. This pin is normally connected to the microprocessor interrupt input.

9.1.1 SPI Serial Port Mode

The external processor bus can be configured to operate in SPI serial bus mode. See Section [9.1.2](#) for detailed timing diagrams.

When SPI_SEL = 1, SPI bus mode is implemented using four signals: clock (SPI_SCLK), master out-slave in data (SPI_MOSI), master in-slave out data (SPI_MISO), and chip select ($\overline{\text{CSB}}$). Clock polarity and phase can be set by the D7/SPI_CPOL and D6/SPI_CPHA pins.

The order of the address and data bits in the serial stream is selectable using the D5/SPI_SWAP pin. The R/W bit is always first and B bit is always last in the initial control word and are not effected by the D5/SPI_SWAP pin setting.

SPI mode is not recommended for HDLC operations because of the bandwidth constraints of SPI.

9.1.2 SPI Functional Timing Diagrams

Note: The transmit and receive order of the address and data bits are selected by the D5/SPI_SWAP pin. The R/W (read/write) MSB bit and B (burst) LSB bit position is not affected by the D5/SPI_SWAP pin setting.

9.1.2.1 SPI Transmission Format and CPHA Polarity

When SPI_CPHA = 0, $\overline{\text{CSB}}$ may be deasserted between accesses. An access is defined as one or two control bytes followed by a data byte. $\overline{\text{CSB}}$ cannot be deasserted between the control bytes, or between the last control byte and the data byte. When SPI_CPHA = 0, $\overline{\text{CSB}}$ may also remain asserted between accesses. If it remains asserted and the BURST bit is set, no additional control bytes are expected after the first control byte(s) and data are transferred. If the BURST bit is set, the address will be incremented for each additional byte of data transferred until $\overline{\text{CSB}}$ is deasserted. If $\overline{\text{CSB}}$ remains asserted and the BURST bit is not set, a control byte(s) is expected following the data byte, and the address for the next access will be received from that. Anytime $\overline{\text{CSB}}$ is deasserted, the BURST access is terminated.

When SPI_CPHA = 1, $\overline{\text{CSB}}$ may remain asserted for more than one access without being toggled high and then low again between accesses. If the BURST bit is set, the address should increment and no additional control bytes are expected. If the BURST bit is not set, each data byte will be followed by the control byte(s) for the next access. Additionally, $\overline{\text{CSB}}$ may also be deasserted between accesses when SPI_CPHA = 1. In the case, any BURST access is terminated and the next byte received when $\overline{\text{CSB}}$ is reasserted will be a control byte.

The following diagrams describe the functionality of the SPI port for the four combinations of SPI_CPOL and SPI_CPHA. They indicate the clock edge that samples the data and the level of the clock during no-transfer events (high or low). Since the SPI port of the DS26518 acts as a slave device, the master device provides the clock. The

user must configure the SPI_CPOL and SPI_CPHA pins to describe which type of clock that the master device is providing.

Figure 9-1. SPI Serial Port Access for Read Mode, SPI_CPOL = 0, SPI_CPHA = 0

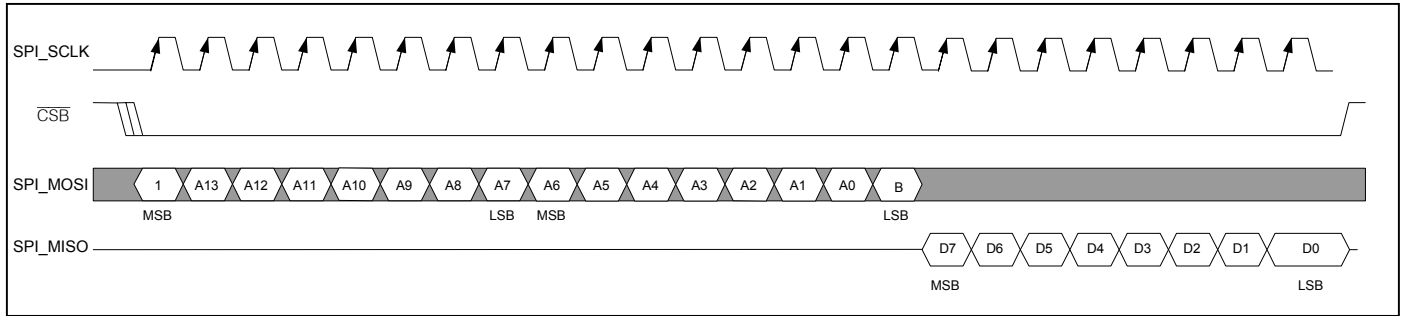


Figure 9-2. SPI Serial Port Access for Read Mode, SPI_CPOL = 1, SPI_CPHA = 0

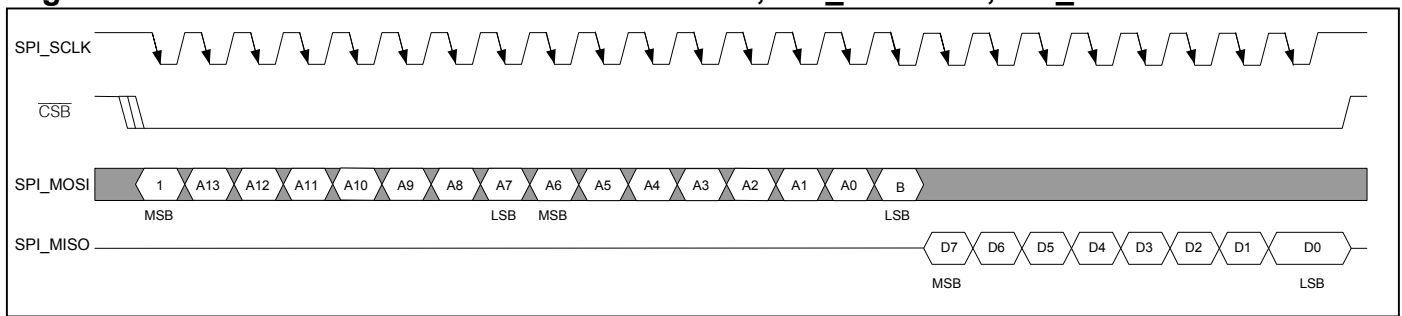


Figure 9-3. SPI Serial Port Access for Read Mode, SPI_CPOL = 0, SPI_CPHA = 1

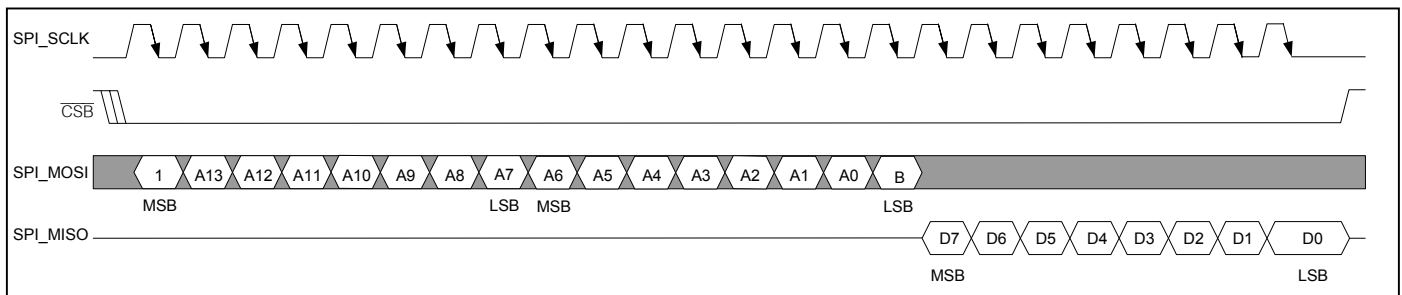


Figure 9-4. SPI Serial Port Access for Read Mode, SPI_CPOL = 1, SPI_CPHA = 1

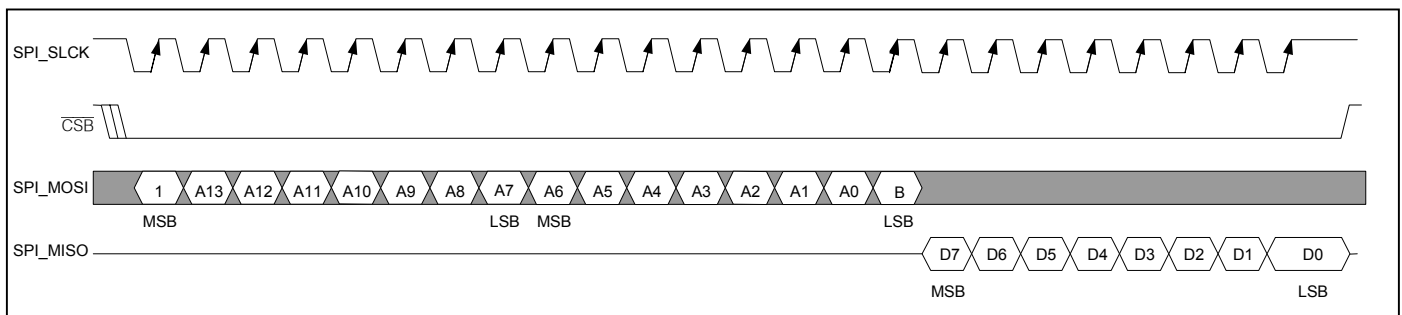


Figure 9-5. SPI Serial Port Access for Write Mode, SPI_CPOL = 0, SPI_CPHA = 0

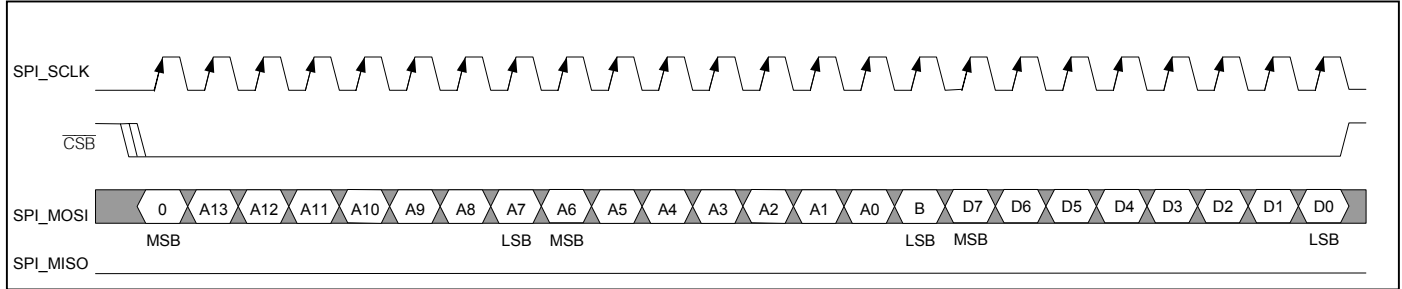


Figure 9-6. SPI Serial Port Access for Write Mode, SPI_CPOL = 1, SPI_CPHA = 0

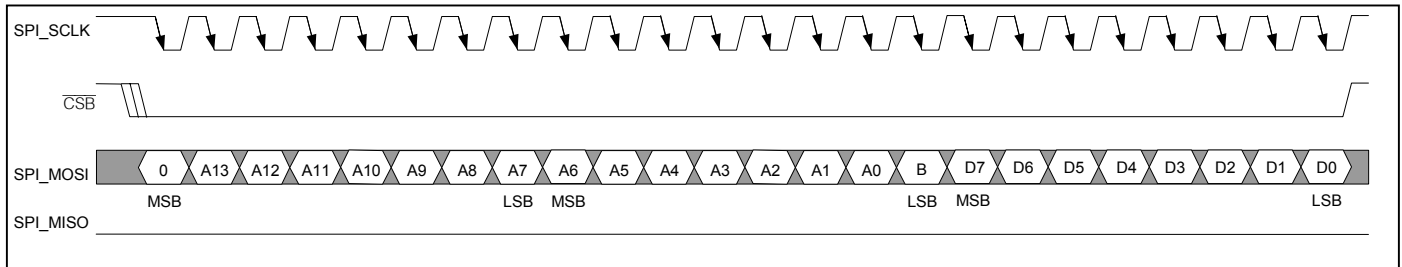


Figure 9-7. SPI Serial Port Access for Write Mode, SPI_CPOL = 0, SPI_CPHA = 1

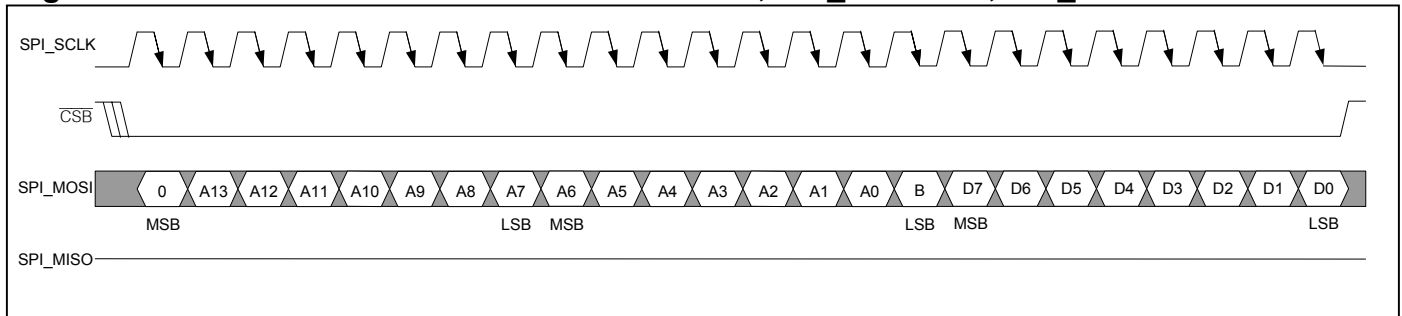
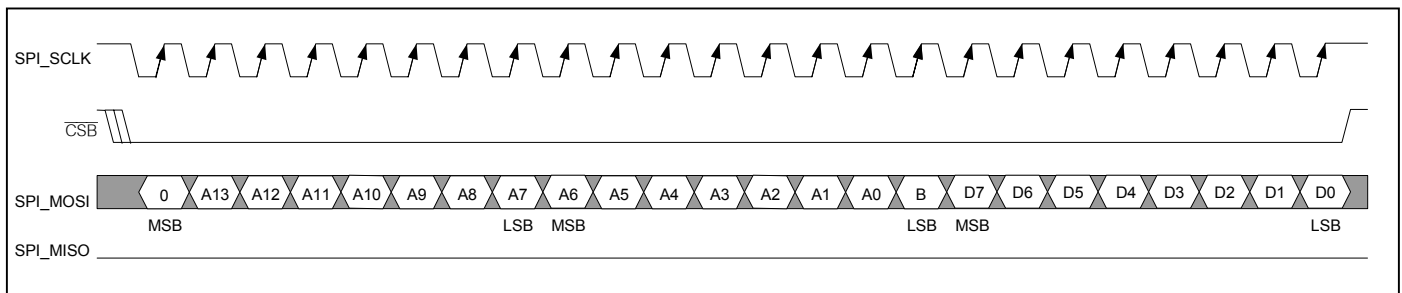


Figure 9-8. SPI Serial Port Access for Write Mode, SPI_CPOL = 1, SPI_CPHA = 1



9.2 Clock Structure

The user should provide a system clock to the MCLK input of 2.048MHz, 1.544MHz, or a multiple of up to 8x the T1 and E1 frequencies. To meet many specifications, the MCLK source should have ± 50 ppm accuracy.

9.2.1 Backplane Clock Generation

The DS26518 provides facility for provision of BPCLK1 at 2.048MHz, 4.096MHz, 8.192MHz, 16.384MHz (see [Figure 9-9](#)). The Global Transceiver Clock Control Register 1 ([GTCCR1](#)) is used to control the backplane clock generation. This register is also used to program REFCLKIO as an input or output. REFCLKIO can be an output sourcing MCLKT1 or MCLKE1 as shown in [Figure 9-9](#).

This backplane clock and frame pulse (TSSYNClOn) can be used by the DS26518 and other IBO-equipped devices as an “IBO Bus Master.” Hence, the DS26518 provides the 8kHz sync pulse and 4MHz, 8MHz, and 16MHz clock. This can be used by the link layer devices and frames connected to the IBO bus.

Figure 9-9. Backplane Clock Generation



The reference clock for the backplane clock generator can be as follows:

- External Master Clock. A prescaler can be used to generate T1 or E1 frequency.
- External Reference Clock REFCLKIO. This allows for multiple DS26518s to use the backplane clock from a common reference.
- Internal LIU recovered RCLKs 1 to 8.
- The clock generator can be used to generate BPCLK1 of 2.048MHz, 4.096MHz, 8.192MHz, or 16.384MHz for the IBO.
- If MCLK or RCLKn is used as a reference, REFCLKIO can be used to provide a 2.048MHz or 1.544MHz clock for external use.

9.2.2 CLKO Output Clock Generation

This clock output is derived from MCLK based upon the setting of the CLKOSSEL[2:0] bits in the [GTCCR3](#) register. The reference for the PLL is not the input clock on MCLK, but the scaled version of MCLK (1.544MHz or 2.048MHz). The [LTRCR.T1J1E1S](#) bit also selects the proper PLL for use in generating the appropriate frequency. This clock output pin is provided as an additional feature to eliminate the need for another board oscillator.

Table 9-1. CLKO Frequency Selection

| CLKOSSEL[3:0] | CLKO (kHz) |
|---------------|------------|
| 0000 | 2048 |
| 0001 | 4096 |
| 0010 | 8192 |
| 0011 | 16384 |
| 0100 | 1544 |
| 0101 | 3088 |
| 0110 | 6176 |
| 0111 | 12352 |
| 1000 | 1536 |
| 1001 | 3072 |
| 1010 | 6144 |
| 1011 | 12288 |
| 1100 | 32 |
| 1101 | 64 |
| 1110 | 128 |
| 1111 | 256 |

9.3 Resets and Power-Down Modes

A hardware reset is issued by forcing the $\overline{\text{RESETB}}$ pin to logic low. The $\overline{\text{RESETB}}$ input pin resets all framers, LIUs, and BERTs. Note that not all registers are cleared to 00h on a reset condition. **The register space must be reinitialized to appropriate values after a hardware or software reset has occurred.** This includes writing reserved locations to 00h.

Table 9-2. Reset Functions

| RESET FUNCTION | LOCATION | COMMENTS |
|---------------------------------|--|---|
| Hardware Device Reset | $\overline{\text{RESETB}}$ Pin | Transition to a logic 0 level resets the DS26518. |
| Hardware JTAG Reset | $\overline{\text{JTRST}}$ Pin | Resets the JTAG test port. |
| Global Software Reset | GSRR1 | Writing to this register resets the framers, LIUs and BERTs (transmit and receive). |
| Framer Receive Reset | RMMR.1 | Writing to this bit resets the receive framer. |
| Framer Transmit Reset | TMMR.1 | Writing to this bit resets the transmit framer. |
| HDLC Receive Reset | RHC.6 | Writing to this bit resets the receive HDLC controller. |
| HDLC Transmit Reset | THC1.5 | Writing to this bit resets the transmit HDLC controller. |
| Elastic Store Receive Reset | RESCR.2 | Writing to this bit resets the receive elastic store. |
| Elastic Store Transmit Reset | TESCR.2 | Writing to this bit resets the transmit elastic store. |
| Bit Oriented Code Receive Reset | T1RBOCC.7 | Writing to this bit resets the receive BOC controller. |
| Loop Code Integration Reset | T1RDNCD1 , T1RUPCD1 | Writing to these registers resets the programmable in-band code integration period. |
| Spare Code Integration Reset | T1RSCD1 | Writing to this register resets the programmable in-band code integration period. |

The DS26518 has several features included to reduce power consumption. The individual LIU transmitters can be powered down by setting the TPDE bit in the LIU Maintenance Control Register ([LMCR](#)). Note that powering down the transmit LIU results in a high-impedance state for the corresponding TTIPn and TRINGn pins and reduced operating current. The RPDE in the [LMCR](#) register can be used to power down the LIU receiver.

The TE (transmit enable) bit in the [LMCR](#) register can be used to disable the TTIPn and TRINGn outputs and place them in a high-impedance mode, while keeping the LIU in an active state (powered up). This is useful for equipment protection-switching applications.

9.4 Initialization and Configuration

9.4.1 Example Device Initialization and Sequence

STEP 1: Reset the device by pulling the $\overline{\text{RESETB}}$ pin low, applying power to the device, or by using the software reset bits outlined in Section [9.3](#). Clear all reset bits. Allow time for the reset recovery.

STEP 2: Check the Device ID in the [IDR](#) register.

STEP 3: Write the [GTCCR1](#) register to correctly configure the system clocks. If supplying a 1.544MHz MCLK follows this write with at least a 300ns delay in order to allow the clock system to properly adjust.

STEP 4: Write the entire remainder of the register space for each port with 00h, including reserved register locations.

STEP 5: Write value 71h to address 1307h. This increases the frequency of the internally generated clock that is supplied to the framers.

STEP 6: Choose T1/J1 or E1 operation for the framers by configuring the T1/E1 bit in the [TMMR](#) and [RMMR](#) registers for each framer. Set the FRM_EN bit to 1 in the [TMMR](#) and [RMMR](#) registers. If using software transmit signaling in E1 mode, program the [E1TAF](#) and [E1TNAF](#) registers as required. Configure the framer Transmit Control Registers ([TCR1–TCR4](#)). Configure the framer Receive Control Registers ([RCR1–RCR3](#)). Configure other framer features as appropriate.

STEP 7: Choose T1/J1 or E1 operation for the LIUs by configuring the T1J1E1S bit in the [LTRCR](#) register. Configure the line build-out for each LIU. Configure other LIU features as appropriate. Set the TE (transmit enable) bit to turn on the TTIPn and TRINGn outputs.

STEP 8: Configure the elastic stores, HDLC controller, and BERT as needed.

STEP 9: Set the INIT_DONE bit in the [TMMR](#) and [RMMR](#) registers for each framer.

9.5 Global Resources

All eight framers share a common microprocessor port and a common MCLK. There is a common software configurable BPCLK1 output. A set of global registers includes global resets, global interrupt status, interrupt masking, clock configuration, and the device ID register. See the global register bit map in [Table 10-7](#). A common JTAG controller is used for all ports.

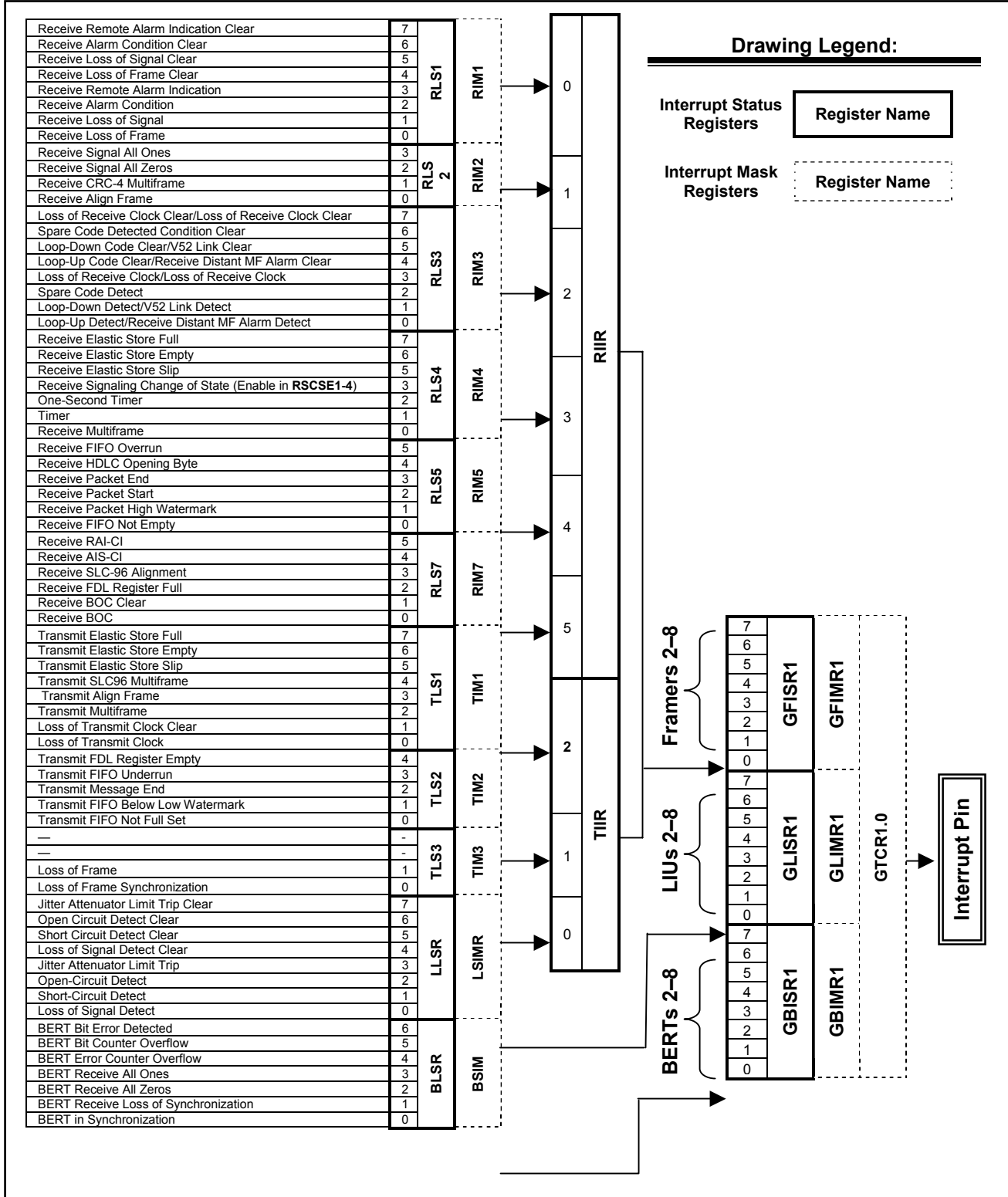
9.6 Per-Port Resources

Each port has an associated framer, LIU, BERT, jitter attenuator, and transmit/receive HDLC controller. Each of the per-port functions has its own register space.

9.7 Device Interrupts

[Figure 9-10](#) diagrams the flow of interrupt conditions from their source status bits through the multiple levels of information registers and mask bits to the interrupt pin. When an interrupt occurs, the host can read the global interrupt information registers [GFISR1](#), [GLISR1](#), and [GBISR1](#) to quickly identify which of the eight transceivers is (are) causing the interrupt(s). The host can then read the specific transceiver's interrupt information registers ([TIIR](#), [RIIR](#)) and the latched status registers ([LLSR](#), [BSR](#)) to further identify the source of the interrupt(s). If TIIR or RIIR is the source, the host reads the transmit latched status or the receive latched status registers for the source of the interrupt. All interrupt information register bits are real-time bits that clear once the appropriate interrupt has been serviced and cleared, as long as no additional, unmasked interrupt condition is present in the associated status register. All latched status bits must be cleared by the host writing a "1" to the bit location of the interrupt condition that has been serviced. Latched status bits that have been masked via the interrupt mask registers are masked from the interrupt information registers. The interrupt mask register bits prevent individual latched status conditions from generating an interrupt, but they do not prevent the latched status bits from being set. Therefore, when servicing interrupts, the user should XOR the latched status with the associated interrupt mask in order to exclude bits for which the user wished to prevent interrupt service. This architecture allows the application host to periodically poll the latched status bits for noninterrupt conditions, while using only one set of registers.

Figure 9-10. Device Interrupt Information Flow Diagram



9.8 System Backplane Interface

The DS26518 provides a versatile backplane interface that can be configured to:

- Transmit and receive two-frame elastic stores
- Mapping of T1 channels into a 2.048MHz backplane
- IBO mode for multiple framers to share the backplane signals
- Transmit and receive channel blocking capability
- Fractional T1/E1/J1 support
- Hardware-based (through the backplane interface) or processor-based signaling
- Flexible backplane clock providing frequencies of 2.048MHz, 4.096MHz, 8.192MHz, 16.384MHz
- Backplane clock and frame pulse (TSSYNClOn) generator

9.8.1 Elastic Stores

The DS26518 contains dual, two-frame elastic stores for each framer: one for the receive direction and one for the transmit direction. Both elastic stores are fully independent. The transmit- and receive-side elastic stores can be enabled/disabled independently of each other. Also, the transmit or receive elastic store can interface to either a 1.544MHz or 2.048/4.096/8.192/16.384MHz backplane without regard to the backplane rate for the other elastic store. All eight channels have their own TSYCLKn/RSYSCLKn pins, allowing a unique backplane system clock for each channel. This allows for maximum flexibility in the design of the backplane clock structure.

The elastic stores have two main purposes. First, they can be used for rate conversion. When the DS26518 is in the T1 mode, the elastic stores can rate convert the T1 data stream to a 2.048MHz backplane. In E1 mode the elastic store can rate convert the E1 data stream to a 1.544MHz backplane. Second, they can be used to absorb the differences in phase and frequency between the T1 or E1 clock and an asynchronous (i.e., not locked) backplane clock, which can be 1.544MHz or 2.048MHz. If the two clocks are not frequency locked, the elastic stores manage the rate difference and perform controlled slips, deleting or repeating frames of data in order to manage the difference between the network and the backplane.

If the elastic store is enabled while in E1 mode, then either CAS or CRC4 multiframe boundaries are indicated via the RMSYNcN output as controlled by the RSMS2 control bit ([RIOCR.1](#)). If the user selects to apply a 1.544MHz clock to the RSYSCLKn pin, the Receive Blank Channel Select Registers ([RBCS1–4](#)) determine which channels of the received E1 data stream will be deleted. In this mode an F-bit location is inserted into the RSERn data and set to one. Also, in 1.544MHz applications, the RCHBLKn output will not be active in channels 25 to 32 (or in other words, RCB4 is not active). If the two-frame elastic buffer either fills or empties, a controlled slip will occur. If the buffer empties, then a full frame of data will be repeated at RSERn and the [RLS4.5](#) and [RLS4.6](#) bits will be set to a one. If the buffer fills, then a full frame of data will be deleted and the [RLS4.5](#) and [RLS4.7](#) bits will be set to a one.

The elastic stores can also be used to multiplex T1 or E1 data streams into higher backplane rates. This is the Interleave Bus Option (IBO), which is discussed in Section [9.8.2](#). [Table 9-3](#) shows the registers related to the elastic stores.

Table 9-3. Registers Related to the Elastic Store

| REGISTER | FRAMER 1 ADDRESSES | FUNCTION |
|---|--------------------|--|
| Receive I/O Configuration Register (RIOCR) | 084h | Sync and clock selection for the receiver. |
| Receive Elastic Store Control Register (RESCR) | 085h | Receive elastic store control. |
| Receive Latched Status Register 4 (RLS4) | 093h | Receive elastic store empty full status. |
| Receive Interrupt Mask Register 4 (RIM4) | 0A3h | Receive interrupt mask for elastic store. |
| Transmit Elastic Store Control Register (TESCR) | 185h | Transmit elastic control such as minimum mode. |
| Transmit Latched Status Register 1 (TLS1) | 190h | Transmit elastic store latched status. |
| Transmit Interrupt Mask Register 1 (TIM1) | 1A0h | Transmit elastic store interrupt mask. |

Note: The addresses shown above are for Framer 1. Addresses for Framers 2 to 8 can be calculated using the following: Framer n = (Framer 1 address + (n - 1) x 200hex), where n = 2 to 8 for Framers 2 to 8.

9.8.1.1 Elastic Stores Initialization

There are two elastic store initializations that may be used to improve performance in certain applications: elastic store reset and elastic store align. Both of these involve the manipulation of the elastic store's read and write pointers and are useful primarily in synchronous applications (RSYSCLKn/TSYSCLKn are locked to RCLKn/TCLKn, respectively). The elastic store reset is used to minimize the delay through the elastic store. The elastic store align bit is used to center the read/write pointers to the extent possible.

Table 9-4. Elastic Store Delay After Initialization

| INITIALIZATION | REGISTER BIT | DELAY |
|------------------------------|-------------------------|-------------------------------------|
| Receive Elastic Store Reset | RESCR.2 | N bytes < Delay < 1 Frame + N bytes |
| Transmit Elastic Store Reset | TESCR.2 | N bytes < Delay < 1 Frame + N bytes |
| Receive Elastic Store Align | RESCR.3 | 1/2 Frame < Delay < 1 1/2 Frames |
| Transmit Elastic Store Align | TESCR.3 | 1/2 Frame < Delay < 1 1/2 Frames |

$N = 9$ for $RSZS = 0$; $N = 2$ for $RSZS = 1$

9.8.1.2 Minimum Delay Mode

Elastic store minimum delay mode may be used when the elastic store's system clock is locked to its network clock (i.e., RCLKn locked to RSYSCLKn for the receive side and TCLKn locked to TSYSCLKn for the transmit side). [RESCR.1](#) enables the receive elastic store minimum delay mode. When enabled, the elastic stores will be forced to a maximum depth of 32 bits instead of the normal two-frame depth. This feature is useful primarily in applications that interface to a 2.048MHz bus. Certain restrictions apply when minimum delay mode is used. In addition to the restriction mentioned above, RSYNCn must be configured as an output when the receive elastic store is in minimum delay mode, and TSYNCn must be configured as an output when transmit minimum delay mode is enabled. In this mode, the SYNC outputs are always in frame mode (multiframe outputs are not allowed). In a typical application RSYSCLKn and TSYSCLKn are locked to RCLKn, and RSYNCn (frame output mode) is connected to TSSYNClOn (frame input mode). The slip zone select bit (RSZS at [RESCR.4](#)) must be set to 1. All the slip contention logic in the framer is disabled (since slips cannot occur). On power-up after the RSYSCLKn and TSYSCLKn signals have locked to their respective network clock signals, the elastic store reset bit ([RESCR.2](#)) should be toggled from a zero to a one to ensure proper operation.

9.8.1.3 Additional Receive Elastic Store Information

If the receive-side elastic store is enabled, then the user must provide either a 1.544MHz or 2.048MHz clock at the RSYSCLKn pin. See Section [9.8.2](#) for higher rate system clock applications. The user has the option of either providing a frame/multiframe sync at the RSYNCn pin or having the RSYNCn pin provide a pulse on frame/multiframe boundaries. If signaling reinsertion is enabled, the robbed-bit signaling data is realigned to the multiframe sync input on RSYNCn. Otherwise, a multiframe sync input on RSYNCn is treated as a simple frame boundary by the elastic store. The framer will always indicate frame boundaries on the network side of the elastic store via the RFSYNCn output whether the elastic store is enabled or not. Multiframe boundaries will always be indicated via the RMSYNCn output. If the elastic store is enabled, then RMSYNCn will output the multiframe boundary on the backplane side of the elastic store. When the device is receiving T1 and the backplane is enabled for 2.048MHz operation, the RMSYNCn signal will output the T1 multiframe boundaries as delayed through the elastic store. When the device is receiving E1 and the backplane is enabled for 1.544MHz operation, the RMSYNCn signal will output the E1 multiframe boundaries as delayed through the elastic store.

If the user selects to apply a 2.048MHz clock to the RSYSCLKn pin, the user can use the backplane blank channel select registers ([RBCS1–4](#)) to determine which channels will have the data output at RSERn forced to all ones.

9.8.1.4 Receiving Mapped T1 Channels from a 2.048MHz Backplane

Setting the TSCLKM bit in [TIOCR.4](#) enables the transmit elastic store to operate with a 2.048MHz backplane (32 time slots / frame). In this mode the user can choose which of the backplane channels on TSERn will be mapped into the T1 data stream by programming the Transmit Blank Channel Select registers ([TBCS1–4](#)). A logic 1 in the associated bit location forces the transmit elastic store to ignore backplane data for that channel. Typically the user will want to program eight channels to be ignored. The default (power-up) configuration will ignore channels 25–32, so that the first 24 backplane channels are mapped into the T1 transmit data stream.

For example, if the user desired to transmit data from the 2.048MHz backplane channels 2–16 and 18–26, the TBCS registers should be programmed as follows:

[TBCS1](#) = 01h :: ignore backplane channel 1 ::
[TBCS2](#) = 00h
[TBCS3](#) = 01h :: ignore backplane channel 17 ::
[TBCS4](#) = FCh :: ignore backplane channels 27–32 ::

9.8.1.5 Mapping T1 Channels onto a 2.048MHz Backplane

Setting the RSCLKM bit in [RIOCR.4](#) will enable the receive elastic store to operate with a 2.048MHz backplane (32 time slots/frame). In this mode the user can choose which of the backplane channels on RSERn receive the T1 data by programming the Receive Blank Channel Select registers ([RBCS1–4](#)). A logic 1 in the associated bit location will force RSERn high for that backplane channel. Typically the user will want to program eight channels to be blanked. The default (power-up) configuration will blank channels 25 to 32, so that the 24 T1 channels are mapped into the first 24 channels of the 2.048MHz backplane. If the user chooses to blank channel 1 (TS0) by setting [RBCS1.0](#) = 1, then the F-bit will be passed into the MSB of TS0 on RSERn.

For example, if:

[RBCS1](#) = 01h
[RBCS2](#) = 00h
[RBCS3](#) = 01h
[RBCS4](#) = FCh

Then on RSERn:

Channel 1 (MSB) = F-bit
 Channel 1 (bits 1-7) = all ones
 Channels 2-16 = T1 channels 1-15
 Channel 17 = all ones
 Channels 18-26 = T1 channels 16-24
 Channels 27-32 = all ones

Note that when two or more sequential channels are chosen to be blanked, the receive slip zone select bit should be set to zero. If the blank channels are distributed (such as 1, 5, 9, 13, 17, 21, 25, 29), the RSZS bit can be set to one, which can provide a lower occurrence of slips in certain applications.

If the two-frame elastic buffer either fills or empties, a controlled slip will occur. If the buffer empties, then a full frame of data will be repeated at RSERn and the [RLS4.5](#) and [RLS4.6](#) bits will be set to a one. If the buffer fills, then a full frame of data will be deleted and the [RLS4.5](#) and [RLS4.7](#) bits will be set to a one.

9.8.1.6 Receiving Mapped E1 Transmit Channels from a 1.544MHz Backplane

The user can use the TSCLKM bit in [TIOCR.4](#) to enable the transmit elastic store to operate with a 1.544MHz backplane (24 channels / frame + F-bit). In this mode the user can choose which of the E1 time slots will have all-ones data inserted by programming the Transmit Blank Channel Select registers ([TBCS1–4](#)). A logic 1 in the associated bit location will cause the elastic store to force all ones at the outgoing E1 data for that channel. Typically the user will want to program eight channels to be blanked. The default (power-up) configuration will blank channels 25 to 32, so that the first 24 E1 channels are mapped from the 24 channels of the 1.544MHz backplane.

9.8.1.7 Mapping E1 Channels onto a 1.544MHz Backplane

The user can use the RSCLKM bit in [RIOCR.4](#) to enable the receive elastic store to operate with a 1.544MHz backplane (24 channels / frame + F-bit). In this mode the user can choose which of the E1 time slots will be ignored (not transmitted onto RSERn) by programming the Receive Blank Channel Select registers ([RBCS1–4](#)). A logic 1 in the associated bit location will cause the elastic store to ignore the incoming E1 data for that channel. Typically, the user will want to program eight channels to be ignored. The default (power-up) configuration will ignore channels 25 to 32, so that the first 24 E1 channels are mapped into the 24 channels of the 1.544MHz backplane. In this mode the F-bit location at RSERn is always set to 1.

For example, if the user wants to ignore E1 time slots 0 (channel 1) and TS 16 (channel 17), the RBCS registers would be programmed as follows:

[RBCS1](#) = 01h
[RBCS2](#) = 00h
[RBCS3](#) = 01h
[RBCS4](#) = FCh

9.8.2 IBO Multiplexing

The DS26518 offers two methods of multiplexing data streams onto a high-speed backplane bus. The traditional method of IBO operation that allows the user to gang signals together on the PCB is supported. RSERn and RSIGN will tri-state at the appropriate times to allow the ganging of these signals together.

The default method multiplexes the data streams internally and then outputs them on one pin, i.e., RSER1. For example, if the user wants to multiplex RSER[1:8] together to make a 16MHz high-speed bus, the data stream will be output on RSER1 only.

The selection between external ganging and internal multiplexing is made via [GTCR1.GIBO](#).

Note that in IBO mode, the channel block signals TCHBLKn and RCHBLKn are referenced to as TSYCLKn and RSYCLKn.

[Figure 9-11](#), [Figure 9-12](#), and [Figure 9-13](#) show the equivalent internal circuit for each IBO mode. These figures only show channels 1–8. [Table 9-5](#) describes the pin function changes for each mode of the IBO multiplexer.

Table 9-5. Registers Related to the IBO Multiplexer

| REGISTER | FRAMER 1 ADDRESSES | FUNCTION |
|--|--------------------|--|
| Global Transceiver Control Register 1 (GTCR1) | 00F0h | This is a global register used to specify ganged operation for the IBO. |
| Global Framer Control Register 1 (GFCR1) | 00F1h | This global register defines the number of devices per bus and bus speed. |
| Receive Interleave Bus Operation Control Register (RIBOC) | 088h | This register configures the per-port IBO enable and type of interleaving (channel vs. frame). |
| Transmit Interleave Bus Operation Control Register (TIBOC) | 188h | This register configures the per-port IBO enable and type of interleaving (channel vs. frame). |

Note: The addresses shown above are for Framer 1. Addresses for Framers 2 to 8 can be calculated using the following: Framer n = (Framer 1 address + (n - 1) x 200hex), where n = 2 to 8 for Framers 2 to 8.

Figure 9-11. IBO Multiplexer Equivalent Circuit—4.096MHz

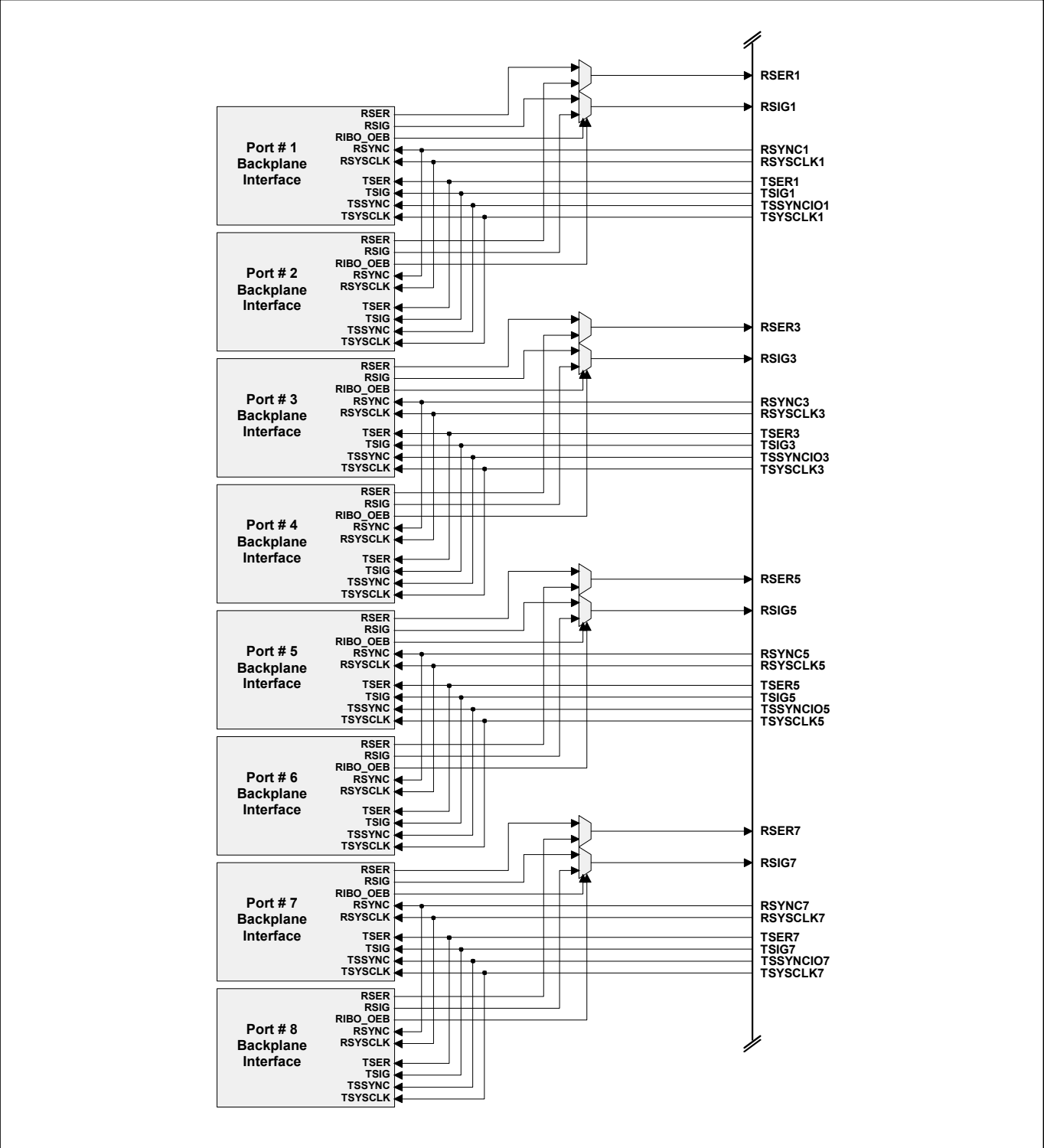


Figure 9-12. IBO Multiplexer Equivalent Circuit—8.192MHz

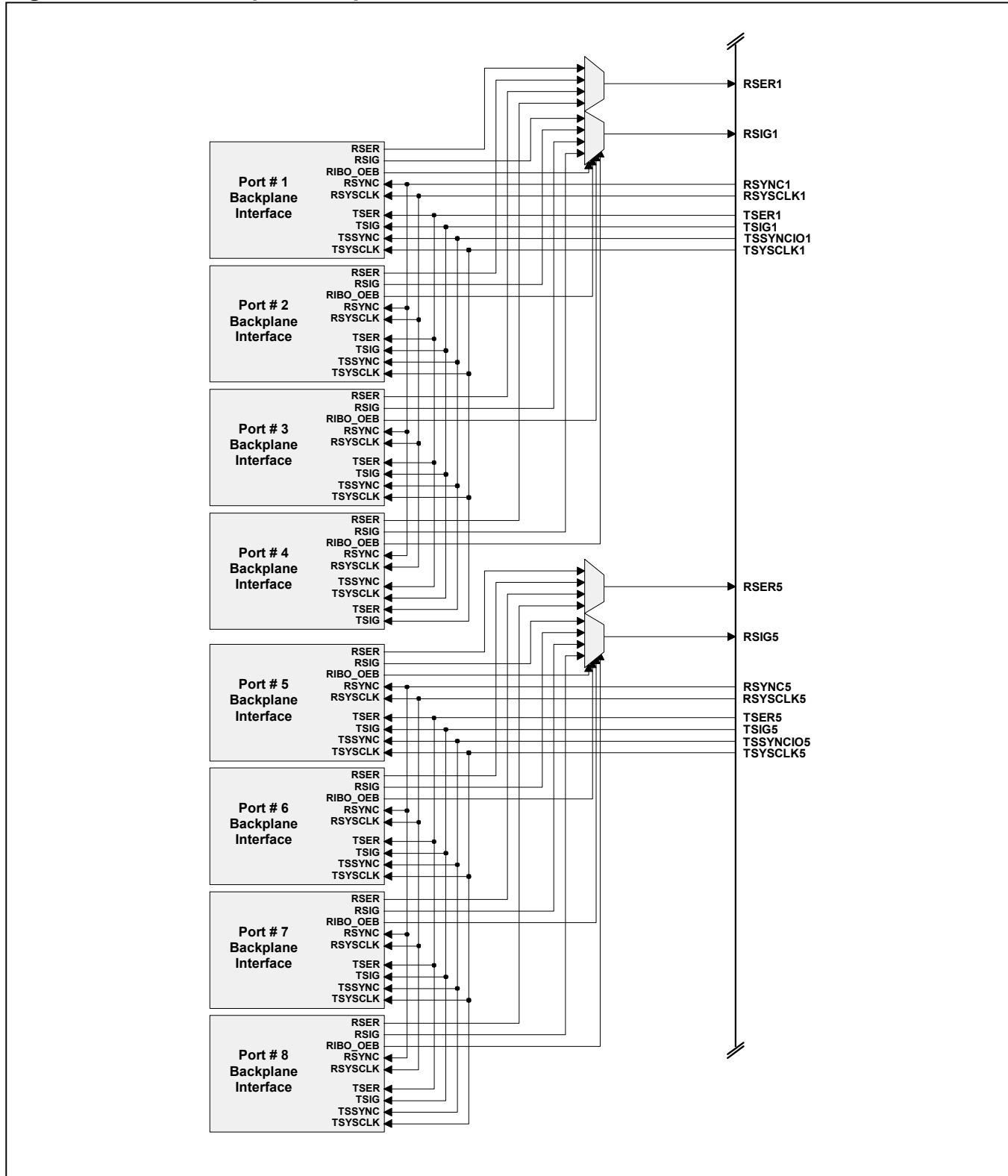


Figure 9-13. IBO Multiplexer Equivalent Circuit—16.384MHz

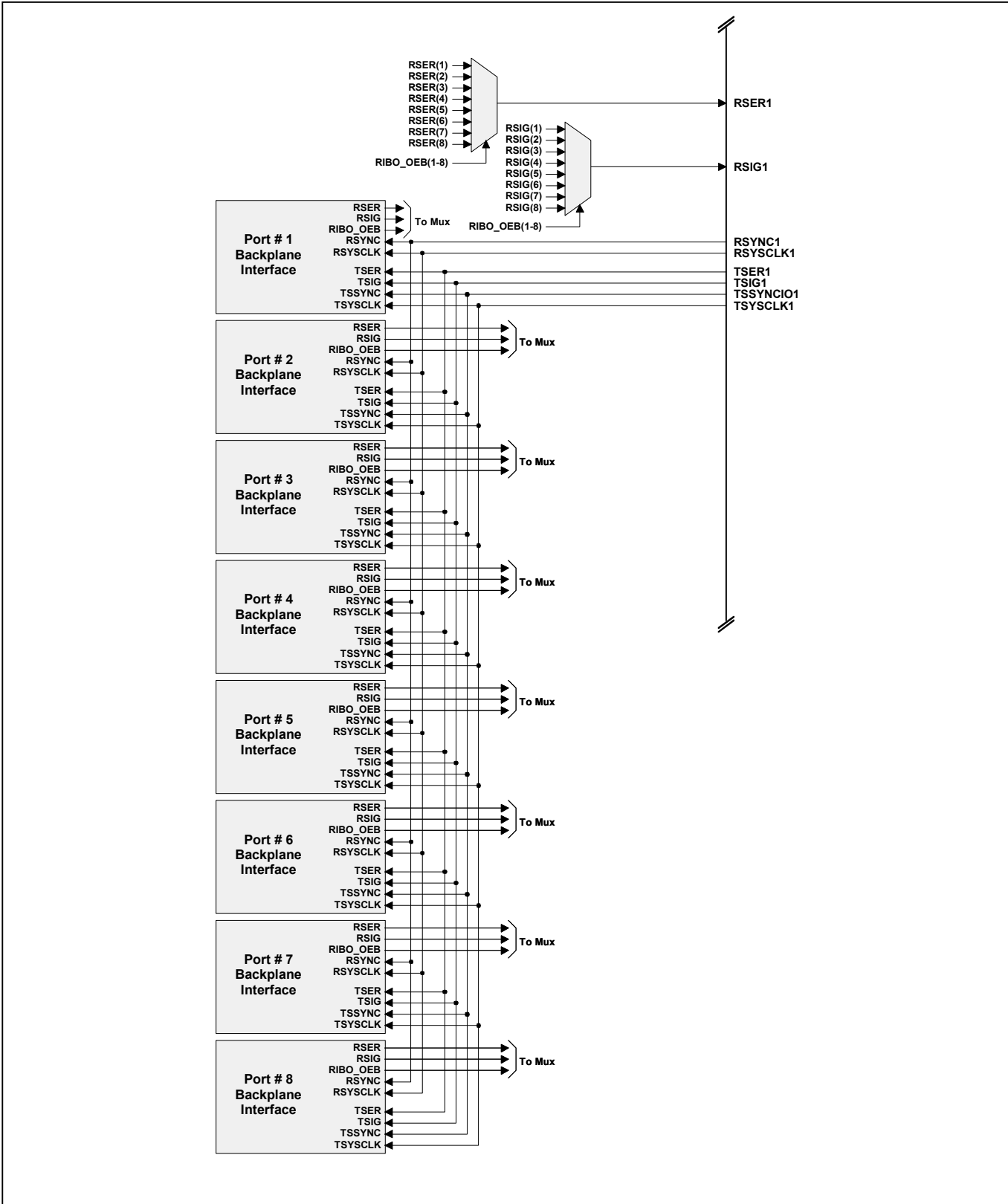


Table 9-6. RSERn Output Pin Definitions ([GTCR1.GIBO](#) = 0)

| PIN | NORMAL USE | 4.096MHz IBO | 8.192MHz IBO | 16.384MHz IBO |
|-------|--------------------------------|--|--|-----------------------------------|
| RSER1 | Receive Serial Data for Port 1 | Combined Receive Serial Data for Ports 1 and 2 | Combined Receive Serial Data for Ports 1–4 | Receive Serial Data for Ports 1–8 |
| RSER2 | Receive Serial Data for Port 2 | Reserved | Unused | Unused |
| RSER3 | Receive Serial Data for Port 3 | Combined Receive Serial Data for Ports 3 and 4 | Unused | Unused |
| RSER4 | Receive Serial Data for Port 4 | Unused | Unused | Unused |
| RSER5 | Receive Serial Data for Port 5 | Combined Receive Serial Data for Ports 5 and 6 | Combined Receive Serial Data for Ports 5–8 | Unused |
| RSER6 | Receive Serial Data for Port 6 | Unused | Unused | Unused |
| RSER7 | Receive Serial Data for Port 7 | Combined Receive Serial Data for Ports 7 and 8 | Unused | Unused |
| RSER8 | Receive Serial Data for Port 8 | Unused | Unused | Unused |

Table 9-7. RSIGn Output Pin Definitions ([GTCR1.GIBO](#) = 0)

| PIN | NORMAL USE | 4.096MHz IBO | 8.192MHz IBO | 16.384MHz IBO |
|-------|-----------------------------------|---|---|--------------------------------------|
| RSIG1 | Receive Signaling Data for Port 1 | Combined Receive Signaling Data for Ports 1 and 2 | Combined Receive Signaling Data for Ports 1–4 | Receive Signaling Data for Ports 1–8 |
| RSIG2 | Receive Signaling Data for Port 2 | Unused | Unused | Unused |
| RSIG3 | Receive Signaling Data for Port 3 | Combined Receive Signaling Data for Ports 3 and 4 | Unused | Unused |
| RSIG4 | Receive Signaling Data for Port 4 | Unused | Unused | Unused |
| RSIG5 | Receive Signaling Data for Port 5 | Combined Receive Signaling Data for Ports 5 and 6 | Combined Receive Signaling Data for Ports 5–8 | Unused |
| RSIG6 | Receive Signaling Data for Port 6 | Unused | Unused | Unused |
| RSIG7 | Receive Signaling Data for Port 7 | Combined Receive Signaling Data for Ports 7 and 8 | Unused | Unused |
| RSIG8 | Receive Signaling Data for Port 8 | Unused | Unused | Unused |

Table 9-8. TSERn Input Pin Definitions ([GTCR1.GIBO](#) = 0)

| PIN | NORMAL USE | 4.096MHz IBO | 8.192MHz IBO | 16.384MHz IBO |
|-------|---------------------------------|---|---|------------------------------------|
| TSER1 | Transmit Serial Data for Port 1 | Combined Transmit Serial Data for Ports 1 and 2 | Combined Transmit Serial Data for Ports 1–4 | Transmit Serial Data for Ports 1–8 |
| TSER2 | Transmit Serial Data for Port 2 | Unused | Unused | Unused |
| TSER3 | Transmit Serial Data for Port 3 | Combined Transmit Serial Data for Ports 3 and 4 | Unused | Unused |
| TSER4 | Transmit Serial Data for Port 4 | Unused | Unused | Unused |
| TSER5 | Transmit Serial Data for Port 5 | Combined Transmit Serial Data for Ports 5 and 6 | Combined Transmit Serial Data for Ports 5–8 | Unused |
| TSER6 | Transmit Serial Data for Port 6 | Unused | Unused | Unused |
| TSER7 | Transmit Serial Data for Port 7 | Combined Transmit Serial Data for Ports 7 and 8 | Unused | Unused |
| TSER8 | Transmit Serial Data for Port 8 | Unused | Unused | Unused |

Table 9-9. TSiGn Input Pin Definitions ([GTCR1.GIBO](#) = 0)

| PIN | NORMAL USE | 4.096MHz IBO | 8.192MHz IBO | 16.384MHz IBO |
|-------|------------------------------------|--|--|---------------------------------------|
| TSIG1 | Transmit Signaling Data for Port 1 | Combined Transmit Signaling Data for Ports 1 and 2 | Combined Transmit Signaling Data for Ports 1–4 | Transmit Signaling Data for Ports 1–8 |
| TSIG2 | Transmit Signaling Data for Port 2 | Unused | Unused | Unused |
| TSIG3 | Transmit Signaling Data for Port 3 | Combined Transmit Signaling Data for Ports 3 and 4 | Unused | Unused |
| TSIG4 | Transmit Signaling Data for Port 4 | Unused | Unused | Unused |
| TSIG5 | Transmit Signaling Data for Port 5 | Combined Transmit Signaling Data for Ports 5 and 6 | Combined Transmit Signaling Data for Ports 5–8 | Unused |
| TSIG6 | Transmit Signaling Data for Port 6 | Unused | Unused | Unused |
| TSIG7 | Transmit Signaling Data for Port 7 | Combined Transmit Signaling Data for Ports 7 and 8 | Unused | Unused |
| TSIG8 | Transmit Signaling Data for Port 8 | Unused | Unused | Unused |

Table 9-10. RSYNCn Input Pin Definitions ([GTCR1.GIBO](#) = 0)

| PIN | NORMAL USE | 4.096MHz IBO | 8.192MHz IBO | 16.384MHz IBO |
|--------|--------------------------------|---------------------------------------|-----------------------------------|-----------------------------------|
| RSYNC1 | Receive Frame Pulse for Port 1 | Receive Frame Pulse for Ports 1 and 2 | Receive Frame Pulse for Ports 1–4 | Receive Frame Pulse for Ports 1–8 |
| RSYNC2 | Receive Frame Pulse for Port 2 | Unused | Unused | Unused |
| RSYNC3 | Receive Frame Pulse for Port 3 | Receive Frame Pulse for Ports 3 and 4 | Unused | Unused |
| RSYNC4 | Receive Frame Pulse for Port 4 | Unused | Unused | Unused |
| RSYNC5 | Receive Frame Pulse for Port 5 | Receive Frame Pulse for Ports 5 and 6 | Receive Frame Pulse for Ports 5–8 | Unused |
| RSYNC6 | Receive Frame Pulse for Port 6 | Unused | Unused | Unused |
| RSYNC7 | Receive Frame Pulse for Port 7 | Receive Frame Pulse for Ports 7 and 8 | Unused | Unused |
| RSYNC8 | Receive Frame Pulse for Port 8 | Unused | Unused | Unused |

9.8.3 H.100 (CT Bus) Compatibility

The H.100 (or CT bus) is a synchronous, bit-serial, TDM transport bus operating at 8.192MHz. The H.100 standard also allows compatibility modes to operate at 2.048MHz, 4.096MHz, or 8.192MHz. The control bit H100EN ([RIOCR.5](#)), when combined with RSYNCINV and TSSYNClON, allows the DS26518 to accept a CT-bus-compatible frame-sync signal ($\overline{\text{CT_FRAME}}$) at the RSYNCn and TSSYNClOn (input mode) inputs. See [Figure 9-14](#) and [Figure 9-15](#).

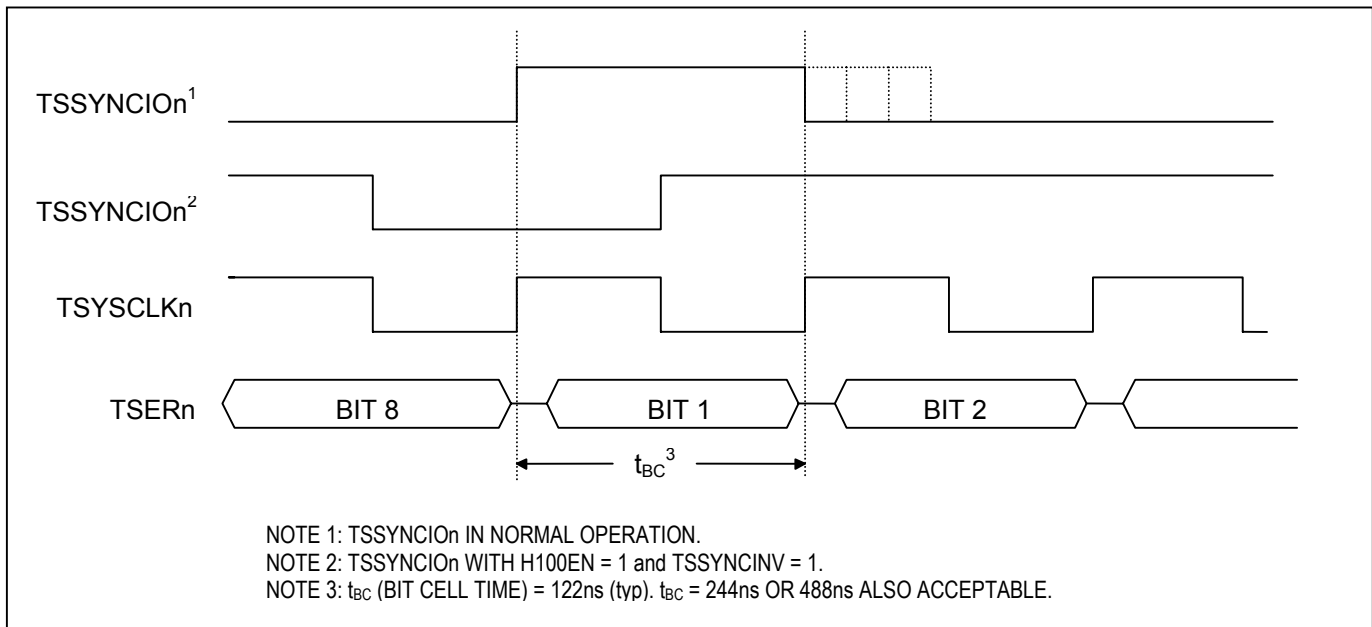
The following rules apply to the H100EN control bit:

- 1) The H100EN bit controls the sampling point for the RSYNCn (input mode) and TSSYNClOn (input mode) only. The RSYNCn output and other sync signals are not affected.
- 2) The H100EN bit would always be used in conjunction with the receive and transmit elastic store buffers.
- 3) The H100EN bit would typically be used with 8.192MHz IBO mode, but could also be used with 4.096MHz IBO mode or 2.048MHz backplane operation.
- 4) The H100EN bit in RIOCR controls both RSYNCn and TSSYNClOn (i.e., there is no separate control bit for the TSSYNClOn).
- 5) The H100EN bit does **not** invert the expected signal; RSYNCINV ([RIOCR](#)) and TSSYNClONV ([TIOCR](#)) must be set high to invert the inbound sync signals.

Figure 9-14. RSYNCn Input in H.100 (CT Bus) Mode



Figure 9-15. TSSYNClOn (Input Mode) Input in H.100 (CT Bus) Mode



9.8.4 Transmit and Receive Channel Blocking Registers

The Receive Channel Blocking Registers ([RCBR1](#)/[RCBR2](#)/[RCBR3](#)/[RCBR4](#)) and the Transmit Channel Blocking Registers ([TCBR1](#)/[TCBR2](#)/[TCBR3](#)/[TCBR4](#)) control the [RCHBLK_n](#) and [TCHBLK_n](#) pins, respectively. The [RCHBLK_n](#) and [TCHBLK_n](#) pins are user-programmable outputs that can be forced either high or low during individual channels. These outputs can be used to block clocks to a USART or LAPD controller in ISDN-PRI applications. When the appropriate bits are set to a one, the [RCHBLK_n](#) and [TCHBLK_n](#) pins will be held high during the entire corresponding channel time. When used with a T1 (1.544MHz) backplane, only [TCBR1](#) to [TCBR3](#) will be used. [TCBR4](#) is included to support an E1 (2.048MHz) backplane when the elastic store is configured for T1-to-E1 rate conversion (See Section [9.8.1](#)).

9.8.5 Transmit Fractional Support (Gapped Clock Mode)

The DS26518 can be programmed to output gapped clocks for selected channels in the receive and transmit paths to simplify connections into a USART or LAPD controller in Fractional T1/E1 or ISDN-PRI applications. When the gapped clock feature is enabled, a gated clock is output on the [TCHCLK](#) signal. The channel selection is controlled via the Transmit Gapped Clock Channel Select Registers ([TGCCS1](#)–4). The transmit path is enabled for gapped clock mode with the [TGCLKEN](#) bit ([TESCR](#).6). Both 56kbps and 64kbps channel formats are supported as determined by [TESCR](#).7. When 56kbps mode is selected, the clock corresponding to the data/control bit in the channel is omitted (only the seven most significant bits of the channel have clocks).

9.8.6 Receive Fractional Support (Gapped Clock Mode)

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9.9 Framers

The DS26518 framer cores are software selectable for T1, J1, or E1. The receive framer locates the frame and multiframe boundaries and monitors the data stream for alarms. It is also used for extracting and inserting signaling data, T1 FDL data, and E1 Si- and Sa-bit information. The receive-side framer decodes AMI, B8ZS line coding, synchronizes to the data stream, reports alarm information, counts framing/coding and CRC errors, and provides clock/data and frame-sync signals to the backplane interface section. Diagnostic capabilities include loopbacks, and 16-bit loop-up and loop-down code detection. The device contains a set of internal registers for host access and control of the device.

On the transmit side, clock, data, and frame-sync signals are provided to the framer by the backplane interface section. The framer inserts the appropriate synchronization framing patterns, alarm information, calculates and inserts the CRC codes, and provides the B8ZS (zero code suppression) and AMI line coding.

Both the transmit and receive path have an HDLC controller. The HDLC controller transmits and receives data via the framer block. The HDLC controller may be assigned to any time slot, portion of a time slot, or to FDL (T1). The HDLC controller has separate 64-byte Tx and Rx FIFO to reduce the amount of processor overhead required to manage the flow of data.

The backplane interface provides a versatile method of sending and receiving data from the host system. Elastic stores provide a method for interfacing to asynchronous systems, converting from a T1/E1 network to a 2.048MHz, 4.096MHz, 8.192MHz or N x 64kHz system backplane. The elastic stores also manage slip conditions (asynchronous interface). An IBO (Interleave Bus Option) is provided to allow multiple framers in the DS26518 to share a high-speed backplane.

9.9.1 T1 Framing

DS1 trunks contain 24 bytes of serial voice/data channels bundled with an overhead bit, the F-bit. The F-bit contains a fixed pattern for the receiver to delineate the frame boundaries. The F-bit is inserted once per frame at the beginning of the transmit frame boundary. The frames are further grouped into bundles of frames 12 for D4 and 24 for ESF.

The D4 and ESF framing modes are outlined in [Table 9-11](#) and [Table 9-12](#). In the D4 mode, framing bit for frame 12 is ignored if Japanese Yellow is selected. [Table 9-13](#) shows SLC-96 framing.

Table 9-11. D4 Framing Mode

| FRAME NUMBER | Ft | Fs | SIGNALING |
|--------------|----|----|-----------|
| 1 | 1 | | |
| 2 | | 0 | |
| 3 | 0 | | |
| 4 | | 0 | |
| 5 | 1 | | |
| 6 | | 1 | A |
| 7 | 0 | | |
| 8 | | 1 | |
| 9 | 1 | | |
| 10 | | 1 | |
| 11 | 0 | | |
| 12 | | 0 | B |

Table 9-12. ESF Framing Mode

| FRAME NUMBER | FRAMING | FDL | CRC | SIGNALING |
|--------------|---------|-----|------|-----------|
| 1 | | √ | | |
| 2 | | | CRC1 | |
| 3 | | √ | | |
| 4 | 0 | | | |
| 5 | | √ | | |
| 6 | | | CRC2 | √ |
| 7 | | √ | | |
| 8 | 0 | | | |
| 9 | | √ | | |
| 10 | | | CRC3 | |
| 11 | | √ | | |
| 12 | | | | √ |
| 13 | | √ | | |
| 14 | | | CRC4 | |
| 15 | | √ | | |
| 16 | 0 | | | |
| 17 | | √ | | √ |
| 18 | | | CRC5 | |
| 19 | | √ | | |
| 20 | 1 | | | |
| 21 | | √ | | |
| 22 | | | CRC6 | |
| 23 | | √ | | |
| 24 | 1 | | | √ |

Table 9-13. SLC-96 Framing

| FRAME NUMBER | Ft | Fs | SIGNALING |
|--------------|----|-----------------------|-----------|
| 1 | 1 | | |
| 2 | | 0 | |
| 3 | 0 | | |
| 4 | | 0 | |
| 5 | 1 | | |
| 6 | | 1 | A |
| 7 | 0 | | |
| 8 | | 1 | |
| 9 | 1 | | |
| 10 | | 1 | |
| 11 | 0 | | |
| 12 | | 0 | B |
| 13 | 1 | | |
| 14 | | 0 | |
| 15 | 0 | | |
| 16 | | 0 | |
| 17 | 1 | | |
| 18 | | 1 | C |
| 19 | 0 | | |
| 20 | | 1 | |
| 21 | 1 | | |
| 22 | | 1 | |
| 23 | 0 | | |
| 24 | | C1 (Concentrator Bit) | D |
| 25 | 1 | | |
| 26 | | C2 (Concentrator Bit) | |
| 27 | 0 | | |

| FRAME NUMBER | Ft | Fs | SIGNALING |
|--------------|----|------------------------|-----------|
| 28 | | C3 (Concentrator Bit) | |
| 29 | 1 | | |
| 30 | | C4 (Concentrator Bit) | A |
| 31 | 0 | | |
| 32 | | C5 (Concentrator Bit) | |
| 33 | 1 | | |
| 34 | | C6 (Concentrator Bit) | |
| 35 | 0 | | |
| 36 | | C7 (Concentrator Bit) | B |
| 37 | 1 | | |
| 38 | | C8 (Concentrator Bit) | |
| 39 | 0 | | |
| 40 | | C9 (Concentrator Bit) | |
| 41 | 1 | | |
| 42 | | C10 (Concentrator Bit) | C |
| 43 | 0 | | |
| 44 | | C11 (Concentrator Bit) | |
| 45 | 1 | | |
| 46 | | 0 (Spoiler Bit) | |
| 47 | 0 | | D |
| 48 | | 1 (Spoiler Bit) | |
| 49 | 1 | | |
| 50 | | 0 (Spoiler Bit) | |
| 51 | 0 | | |
| 52 | | M1 (Maintenance Bit) | |
| 53 | 1 | | |
| 54 | | M2 (Maintenance Bit) | A |
| 55 | 0 | | |
| 56 | | M3 (Maintenance Bit) | |
| 57 | 1 | | |
| 58 | | A1 (Alarm Bit) | |
| 59 | 0 | | |
| 60 | | A2 (Alarm Bit) | B |
| 61 | 1 | | |
| 62 | | S1 (Switch Bit) | |
| 63 | 0 | | |
| 64 | | S2 (Switch Bit) | |
| 65 | 1 | | C |
| 66 | | S3 (Switch Bit) | |
| 67 | 0 | | |
| 68 | | S4 (Switch Bit) | |
| 69 | 1 | | |
| 70 | | 1 (Spoiler Bit) | |
| 71 | 0 | | |
| 72 | | 0 | D |

9.9.2 E1 Framing

The E1 framing consists of FAS, NFAS detection as shown in [Table 9-14](#).

Table 9-14. E1 FAS/NFAS Framing

| CRC-4 FRAME # | TYPE | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 |
|---------------|------|----|---|---|-----|-----|-----|-----|-----|
| 0 | FAS | C1 | 0 | 0 | 1 | 1 | 0 | 1 | 1 |
| 1 | NFAS | 0 | 1 | A | Sa4 | Sa5 | Sa6 | Sa7 | Sa8 |
| 2 | FAS | C2 | 0 | 0 | 1 | 1 | 0 | 1 | 1 |
| 3 | NFAS | 0 | 1 | A | Sa4 | Sa5 | Sa6 | Sa7 | Sa8 |
| 4 | FAS | C3 | 0 | 0 | 1 | 1 | 0 | 1 | 1 |
| 5 | NFAS | 1 | 1 | A | Sa4 | Sa5 | Sa6 | Sa7 | Sa8 |
| 6 | FAS | C4 | 0 | 0 | 1 | 1 | 0 | 1 | 1 |
| 7 | NFAS | 0 | 1 | A | Sa4 | Sa5 | Sa6 | Sa7 | Sa8 |
| 8 | FAS | C1 | 0 | 0 | 1 | 1 | 0 | 1 | 1 |
| 9 | NFAS | 1 | 1 | A | Sa4 | Sa5 | Sa6 | Sa7 | Sa8 |
| 10 | FAS | C2 | 0 | 0 | 1 | 1 | 0 | 1 | 1 |
| 11 | NFAS | 1 | 1 | A | Sa4 | Sa5 | Sa6 | Sa7 | Sa8 |
| 12 | FAS | C3 | 0 | 0 | 1 | 1 | 0 | 1 | 1 |
| 13 | NFAS | E1 | 1 | A | Sa4 | Sa5 | Sa6 | Sa7 | Sa8 |
| 14 | FAS | C4 | 0 | 0 | 1 | 1 | 0 | 1 | 1 |
| 15 | NFAS | E2 | 1 | A | Sa4 | Sa5 | Sa6 | Sa7 | Sa8 |

C = C bits are the CRC-4 remainder; A = alarm bits; Sa = bits for data link.

[Table 9-15](#) shows the registers that are related to setting up the framing.

Table 9-15. Registers Related to Setting Up the Framer

| REGISTER | FRAMER 1 ADDRESSES | FUNCTION |
|--|--------------------|---|
| Transmit Master Mode Register (TMMR) | 180h | T1/E1 mode. |
| Transmit Control Register 1 (TCR1) | 181h | Source of the F-bit. |
| Transmit Control Register 2 (T1.TCR2) | 182h | F-bit corruption, selection of SLC-96. |
| Transmit Control Register 3 (TCR3) | 183h | ESF or D4 mode selection. |
| Receive Master Mode Register (RMMR) | 080h | T1/E1 selection for receiver. |
| Receive Control Register 1 (RCR1) | 081h | Resynchronization criteria for the framer. |
| Receive Control Register 2 (T1RCR2) | 014h | T1 remote alarm and OOF criteria. |
| Receive Control Register 2 (E1RCR2) | 082h | E1 receive loss of signal criteria selection. |
| Receive Latched Status Register 1 (RLS1) | 090h | Receive latched status 1. |
| Receive Interrupt Mask Register 1 (RIM1) | 0A0h | Receive interrupt mask 1. |
| Receive Latched Status Register 2 (RLS2) | 091h | Receive latched status 2. |
| Receive Interrupt Mask Register 2 (RIM2) | 0A1h | Receive interrupt mask 2. |
| Receive Latched Status Register 4 (RLS4) | 093h | Receive latched status 4. |
| Receive Interrupt Mask Register 4 (RIM4) | 0A3h | Receive interrupt mask 4. |
| Frames Out of Sync Count Register 1 (FOSCR1) | 054h | Framer out of sync register 1. |
| Frames Out of Sync Count Register 2 (FOSCR2) | 055h | Framer out of sync register 2. |
| E1 Receive Align Frame Register (E1RAF) | 064h | RAF byte. |
| E1 Receive Non-Align Frame Register (E1RNAF) | 065h | RNAF byte. |
| Transmit SLC-96 Data Link Register 1 (T1TSLC1) | 164h | Transmit SLC-96 bits. |
| Transmit SLC-96 Data Link Register 2 (T1TSLC2) | 165h | Transmit SLC-96 bits. |
| Transmit SLC-96 Data Link Register 3 (T1TSLC3) | 166h | Transmit SLC-96 bits. |
| Receive SLC-96 Data Link Register 1 (T1RSLC1) | 064h | Receive SLC-96 bits. |
| Receive SLC-96 Data Link Register 2 (T1RSLC2) | 065h | Receive SLC-96 bits. |
| Receive SLC-96 Data Link Register 3 (T1RSLC3) | 066h | Receive SLC-96 bits. |

Note: The addresses shown above are for Framer 1. Addresses for Framers 2 to 8 can be calculated using the following: Framer n = (Framer 1 address + $(n - 1) \times 200\text{hex}$); where $n = 2$ to 8 for Framers 2 to 8.

9.9.3 T1 Transmit Synchronizer

The DS26518 transmitter can identify the D4 or ESF frame boundary, as well as the CRC multiframe boundaries within the incoming NRZ data stream at TSERn. The TFM ([TCR3.2](#)) control bit determines whether the transmit synchronizer searches for the D4 or ESF multiframe. Additional control signals for the transmit synchronizer are located in the [TSYNCC](#) register. The latched status bit [TLS3.0](#) (LOFD) is provided to indicate that a loss of frame synchronization has occurred, and a real-time bit (LOF) which is set high when the synchronizer is searching for frame/multiframe alignment. The LOFD bit can be enabled to cause an interrupt condition on $\overline{\text{INTB}}$.

Note that when the transmit synchronizer is used, the TSYNCn signal should be set as an output (TSIO = 1) and the recovered frame-sync pulse will be output on this signal. The recovered CRC-4 multi-frame sync pulse will be output if enabled with [TIOCR.0](#) (TSM = 1).

Other key points concerning the E1 transmit synchronizer:

- 1) The Tx synchronizer is not operational when the transmit elastic store is enabled, including IBO modes.
- 2) The Tx synchronizer does not perform CRC-6 alignment verification (ESF mode) and does not verify CRC-4 codewords.

The Tx synchronizer cannot search for the CAS multiframe. [Table 9-16](#) shows the registers related to the transmit synchronizer.

Table 9-16. Registers Related to the Transmit Synchronizer

| REGISTER | FRAMER 1 ADDRESSES | FUNCTION |
|---|--------------------|---|
| Transmit Synchronizer Control Register (TSYNCC) | 18Eh | Resynchronization control for the transmit synchronizer. |
| Transmit Control Register 3 (TCR3) | 183h | TFM bit selects between D4 and ESF for the transmit synchronizer. |
| Transmit Latched Status Register 3 (TLS3) | 192h | Provides latched status for the transmit synchronizer. |
| Transmit Interrupt Mask Register 3 (TIM3) | 1A2h | Provides mask bits for the TLS3 status. |
| Transmit I/O Configuration Register (TIOCR) | 184h | TSYNCn should be set as an output. |

Note: The addresses shown above are for Framer 1. Addresses for Framers 2 to 8 can be calculated using the following: Framer n = (Framer 1 address + (n - 1) x 200hex); where n = 2 to 8 for Framers 2 to 8.

9.9.4 Signaling

The DS26518 supports both software and hardware-based signaling. Interrupts can be generated on changes of signaling data. The DS26518 is also equipped with receive-signaling freeze on loss of synchronization (OOF), carrier loss or change of frame alignment. The DS26518 also has hardware pins to indicate signaling freeze.

Features include the following:

- Flexible signaling support:
 - Software or hardware based
 - Interrupt generated on change of signaling data
 - Receive-signaling freeze on loss of frame, loss of signal, or change of frame alignment
- Hardware pins for carrier loss and signaling freeze indication

Table 9-17. Registers Related to Signaling

| REGISTER | FRAMER 1 ADDRESSES | FUNCTION |
|--|---|--|
| Transmit-Signaling Registers 1 to 16 (TS1 to TS16) | 140h to 14Bh (T1/J1) 140h to 14Fh (E1 CAS) | Transmit ABCD signaling. |
| Software-Signaling Insertion Enable Registers 1 to 4 (SSIE1 to SSIE4) | 118h, 119h, 11Ah, 11Bh | When enabled, signaling is inserted for the channel. |
| Transmit Hardware-Signaling Channel Select Registers 1 to 4 (THSCS1 to THSCS4) | 1C8h, 1C9h, 1CAh, 1CBh | Bits determine which channels will have signaling inserted in hardware-signaling mode. |
| Receive-Signaling Control Register (RSIGC) | 013h | Freeze control for receive signaling. |
| Receive-Signaling All-Ones Insertion Registers 1 to 3 (T1RSAOI1 to T1RSAOI3) | 038h, 039h, 03Ah | Registers for all-ones insertion (T1 mode only). |
| Receive-Signaling Registers 1 to 16 (RS1 to RS16) | 040h to 04Bh (T1/J1) 040h to 04Fh (E1) | Receive-signaling bytes. |
| Receive-Signaling Status Registers 1 to 4 (RSS1 to RSS4) | 098h to 09Ah (T1/J1) 98h to 9Fh (E1) | Receive-signaling change of status bits. |
| Receive-Signaling Change of State Enable Registers 1 to 4 (RSCSE1 to RSCSE4) | 0A8h, 0A9h, 0AAh, 0ABh | Receive-signaling change of state interrupt enable. |
| Receive Latched Status Register 4 (RLS4) | 093h | Receive-signaling change of state bit. |
| Receive Interrupt Mask Register 4 (RIM4) | 0A3h | Receive-signaling change of state interrupt mask bit. |
| Receive-Signaling Reinsertion Enable Registers 1 to 4 (RSI1 to RSI4) | 0C8h, 0C9h, 0CAh, 0CBh | Registers for signaling reinsertion. |

Note: The addresses shown above are for Framer 1. Addresses for Framers 2 to 8 can be calculated using the following: Framer n = (Framer 1 address + $(n - 1) \times 200\text{hex}$); where $n = 2$ to 8 for Framers 2 to 8.

9.9.4.1 Transmit-Signaling Operation

There are two methods to provide transmit-signaling data. These are processor based (i.e., software based) or hardware based. Processor-based refers to access through the transmit signaling registers, [TS1](#)–[TS16](#), while hardware based refers to using the TSIGn pins. Both methods can be used simultaneously.

9.9.4.1.1 Processor-Based Transmit Signaling

In processor-based mode, signaling data is loaded into the transmit-signaling registers ([TS1](#)–[TS16](#)) via the host interface. On multiframe boundaries, the contents of these registers are loaded into a shift register for placement in the appropriate bit position in the outgoing data stream. The user can utilize the transmit multiframe interrupt in the Transmit Latched Status Register 1 ([TLS1.2](#)) to know when to update the signaling bits. The user need not update any transmit signaling register for which there is no change of state for that register.

Each transmit-signaling register contains the robbed-bit signaling ([TCR1.4](#) in T1 mode) or TS16 CAS signaling ([TCR1.6](#) in E1 mode) for one time slot that will be inserted into the outgoing stream. Signaling data can be sourced from the TS registers on a per-channel basis by using the Software Signaling Insertion Enable Registers, [SSIE1](#)–[4](#).

In T1 ESF framing mode, there are four signaling bits per channel (A, B, C, and D). [TS1](#)–[TS12](#) contain a full multiframe of signaling data. In T1 D4 framing mode, there are only two signaling bits per channel (A and B). In T1 D4 framing mode, the framer uses A and B bit positions for the next multiframe. The C and D bit positions become 'don't care' in D4 mode.

In E1 mode, [TS16](#) carries the signaling information. This information can be in either CCS (Common Channel Signaling) or CAS (Channel Associated Signaling) format. The 32 time slots are referenced by two different channel number schemes in E1. In "channel" numbering, [TS0](#)–[TS31](#) are labeled channels 1 through 32. In "Phone Channel" numbering [TS1](#)–[TS15](#) are labeled channel 1 to channel 15 and [TS17](#)–[TS31](#) are labeled channel 15 to channel 30.

9.9.4.1.2 Time Slot Numbering Schemes

| TS | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | 25 | 26 | 27 | 28 | 29 | 30 | 31 |
|---------------|---|---|---|---|---|---|---|---|---|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Channel | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | 25 | 26 | 27 | 28 | 29 | 30 | 31 | 32 |
| Phone Channel | | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | 25 | 26 | 27 | 28 | 29 | 30 |

9.9.4.1.3 Hardware-Based Transmit Signaling

In hardware-based mode, signaling data is input via the TSIGn pin. This signaling PCM stream is buffered and inserted to the data stream being input at the TSERn pin.

Signaling data may be input via the Transmit Hardware-Signaling Channel Select Register ([THSCS1](#)) function. The framer can be set up to take the signaling data presented at the TSIGn pin and insert the signaling data into the PCM data stream that is being input at the TSERn pin. The user can control which channels are to have signaling data from the TSIGn pin inserted into them on a per-channel basis. The signaling insertion capabilities of the framer are available whether the transmit-side elastic store is enabled or disabled. If the elastic store is enabled, the backplane clock (TSYSCLKn) can be either 1.544MHz or 2.048MHz.

9.9.4.2 Receive-Signaling Operation

There are two methods to access receive-signaling data and provide transmit-signaling data: processor based (i.e., software based) or hardware based. Processor-based refers to access through the transmit- and receive-signaling registers, [RS1](#)–[RS16](#). Hardware based refers to the [RSIGN](#) pin. Both methods can be used simultaneously.

9.9.4.2.1 Processor-Based Receive Signaling

Signaling information is sampled from the receive data stream and copied into the Receive-Signaling Registers, [RS1](#)–[RS16](#). The signaling information in these registers is always updated on multiframe boundaries. This function is always enabled.

9.9.4.2.2 Change of State

To avoid constant monitoring of the receive-signaling registers, the DS26518 can be programmed to alert the host when any specific channel or channels undergo a change of their signaling state. [RSCSE1](#)–[4](#) are used to select which channels can cause a change of state indication. The change of state is indicated in Receive Latched Status Register 4 ([RLS4.3](#)). If signaling integration is enabled, the new signaling state must be constant for three multiframes before a change of state indication is indicated. The user can enable the [INTB](#) pin to toggle low upon detection of a change in signaling by setting the interrupt mask bit [RIM4.3](#). The signaling integration mode is global and cannot be enabled on a channel-by-channel basis.

The user can identify which channels have undergone a signaling change of state by reading the Receive-Signaling Status Registers ([RSS1](#)–[4](#)). The information from these registers will tell the user which [RSx](#) register to read for the new signaling data. All changes are indicated in the [RSS1](#)–[4](#) registers regardless of the [RSCSE1](#)–[4](#) registers.

9.9.4.2.3 Hardware-Based Receive Signaling

In hardware-based signaling the signaling data is can be obtained from the [RSERn](#) pin or the [RSIGN](#) pin. [RSIGN](#) is a signaling PCM stream output on a channel by channel basis from the signaling buffer. The T1 robbed bit or E1 TS16 signaling data is still present in the original data stream at [RSERn](#). The signaling buffer provides signaling data to the [RSIGN](#) pin and also allows signaling data to be reinserted into the original data stream in a different alignment that is determined by a multiframe signal from the [RSYNCn](#) pin. In this mode, the receive elastic store may be enabled or disabled. If the receive elastic store is enabled, then the backplane clock ([RSYCLKn](#)) can be either 1.544MHz or 2.048MHz. In the ESF framing mode, the ABCD signaling bits are output on [RSIGN](#) in the lower nibble of each channel. The [RSIGN](#) data is updated once a multiframe (3ms for T1 ESF, 1.5ms for T1 D4, 2ms for E1 CAS) unless a signaling freeze is in effect. In the D4 framing mode, the AB signaling bits are output twice on [RSIGN](#) in the lower nibble of each channel. Hence, bits 5 and 6 contain the same data as bits 7 and 8, respectively, in each channel.

9.9.4.2.4 Receive-Signaling Reinsertion at [RSERn](#)

In this mode, the user will provide a multiframe sync at the [RSYNCn](#) pin and the signaling data will be reinserted based on this alignment. In T1 mode, this results in two copies of the signaling data in the [RSERn](#) data stream. The original signaling data based on the Fs/ESF frame positions and the realigned data based on the user supplied multiframe sync applied at [RSYNCn](#). In voice channels this extra copy of signaling data is of little consequence. Reinsertion can be avoided in data channels since this feature is activated on a per-channel basis. For reinsertion, the elastic store must be enabled and for T1, the backplane clock can be either 1.544MHz or 2.048MHz. E1 signaling information cannot be reinserted into a 1.544MHz backplane.

Signaling reinsertion mode is enabled, on a per-channel basis by setting the receive-signaling reinsertion channel select bit high in the [RSI1](#)–[4](#) register. The channels that are to have signaling reinserted are selected by writing to the [RSI1](#)–[4](#) registers. In E1 mode, the user will generally select all channels or none for reinsertion.

9.9.4.2.5 Force Receive-Signaling All Ones

In T1 mode, the user can on a per-channel basis force the robbed-bit signaling bit positions to a one. This is done by using the Receive-Signaling All-Ones Insertion Registers ([T1RSAOI1](#)–[3](#)). The user sets the channel select bit in the [T1RSAOI1](#)–[3](#) registers to select the channels that are to have the signaling forced to one.

9.9.4.2.6 Receive-Signaling Freeze

The signaling data in the four multiframe signaling buffers will be frozen in a known good state upon either a loss of synchronization (OOF event), carrier loss, or change of frame alignment. In T1 mode, this action meets the requirements of BellCore TR-TSY-000170 for signaling freezing. To allow this freeze action to occur, the RSFE control bit ([RSIGC.1](#)) should be set high. The user can force a freeze by setting the RSFF control bit ([RSIGC.2](#)) high. The RSIGF output pin provides a hardware indication that a freeze is in effect. The four multiframe buffer provides a three multiframe delay in the signaling bits provided at the RSIGN pin (and at the RSERn pin if receive-signaling reinsertion is enabled). When freezing is enabled (RSFE = 1), the signaling data will be held in the last known good state until the corrupting error condition subsides. When the error condition subsides, the signaling data will be held in the old state for at least an additional 9ms (4.5ms in D4 framing mode, 6ms for E1 mode) before being allowed to be updated with new signaling data.

The receive-signaling registers are frozen and not updated during a loss of sync condition. They will contain the most recent signaling information before the LOF occurred.

9.9.4.3 Transmit SLC-96 Operation (T1 Mode Only)

In an SLC-96-based transmission scheme, the standard Fs-bit pattern is robbed to make room for a set of message fields. The SLC-96 multiframe is made up of six D4 superframes, hence it is 72 frames long. In the 72-frame SLC-96 multiframe, 36 of the framing bits are the normal Ft pattern and the other 36 bits are divided into alarm, maintenance, spoiler, and concentrator bits as well as 12-bits of the normal Fs pattern. Additional SLC-96 information can be found in BellCore document TR-TSY-000008. Registers related to the transmit FDL are shown in [Table 9-18](#).

Table 9-18. Registers Related to SLC-96

| REGISTER | FRAMER 1 ADDRESSES | FUNCTION |
|--|--------------------|--|
| Transmit FDL Register (T1TFDL) | 162h | For sending messages in transmit SLC-96 Ft/Fs bits. |
| Transmit SLC-96 Data Link Registers 1 to 3 (T1TSLC1:T1TSLC3) | 164h, 165h, 166h | Registers that control the SLC-96 overhead values. |
| Transmit Control Register 2 (T1.TCR2) | 182h | Transmit control for data selection source for the Ft/Fs bits. |
| Transmit Latched Status Register 1 (TLS1) | 190h | Status bit for indicating transmission of data link buffer. |
| Receive SLC-96 Data Link Registers 1 to 3 (T1RSLC1:T1RSLC3) | 064h, 065h, 066h | — |
| Receive Latched Status Register 7 (RLS7) | 096h | Receive SLC-96 alignment event. |

Note: The addresses shown above are for Framer 1. Addresses for Framers 2 to 8 can be calculated using the following: Framer n = (Framer 1 address + $(n - 1) \times 200\text{hex}$), where $n = 2$ to 8 for Framers 2 to 8.

The [T1TFDL](#) register is used to insert the SLC-96 message fields. To insert the SLC-96 message using the [T1TFDL](#) register, the user should configure the DS26518 as shown below:

- [T1.TCR2.6](#) (TSLC96) = 1 Enable Transmit SLC-96.
- [T1.TCR2.7](#) (TFDLS) = 0 Source FS bits via TFDL or SLC-96 formatter.
- [TCR3.2](#) (TFM) = 1 D4 framing mode.
- [TCR1.6](#) (TFPT) = 0 Do not “pass through” TSERn F-bits.

The DS26518 will automatically insert the 12-bit alignment pattern in the Fs bits for the SLC-96 data link frame. Data from the [T1TSLC1–3](#) will be inserted into the remaining Fs-bit locations of the SLC-96 multiframe. The status bit TSLC96 located at [TLS1.4](#) will set to indicate that the SLC-96 data link buffer has been transmitted and that the user should write new message data into [T1TSLC1–3](#). The host will have 9ms after the assertion of [TLS1.4](#) to write the registers [T1TSLC1–3](#). If no new data is provided in these registers, the previous values will be retransmitted.

9.9.4.4 Receive SLC-96 Operation (T1 Mode Only)

In an SLC-96-based transmission scheme, the standard Fs-bit pattern is robbed to make room for a set of message fields. The SLC-96 multiframe is made up of six D4 superframes, hence it is 72 frames long. In the 72-frame SLC-96 multiframe, 36 of the framing bits are the normal Ft pattern and the other 36-bits are divided into alarm, maintenance, spoiler, and concentrator bits as well as 12-bits of the normal Fs pattern. Additional SLC-96 information can be found in BellCore document TR-TSY-000008.

To enable the DS26518 to synchronize onto a SLC-96 pattern, the following configuration should be used:

- [RCR1.5](#) (RFM) = 1 Set to D4 framing mode.
- [RCR1.3](#) (SYNCC) = 1 Set to cross-couple Ft and Fs bits.
- [T1RCR2.4](#) (RSLC96) = 1 Enable SLC-96 synchronizer.
- [RCR1.7](#) (SYNCT) = 0 Set to minimum sync time.

The SLC-96 message bits can be extracted via the [T1RSLC1](#)–3 registers. The status bit RSLC96 located at [RLS7.3](#) is useful for retrieving SLC-96 message data. The RSLC96 bit will indicate when the framer has updated the data link registers [T1RSLC1](#)–3 with the latest message data from the incoming data stream. Once the RSLC96 bit is set, the user will have 9ms (or until the next RSLC96 interrupt) to retrieve the most recent message data from the [T1RSLC1](#)–3 registers. Note that RSLC96 will not set if the DS26518 is unable to detect the 12-bit SLC-96 alignment pattern.

9.9.5 T1 Data Link

9.9.5.1 T1 Transmit Bit-Oriented Code (BOC) Transmit Controller

The DS26518 contains a BOC generator on the transmit side and a BOC detector on the receive side. The BOC function is available only in T1 mode. [Table 9-19](#) shows the registers related to the transmit bit-oriented code.

Table 9-19. Registers Related to T1 Transmit BOC

| REGISTER | FRAMER 1 ADDRESSES | FUNCTION |
|--|--------------------|--|
| Transmit BOC Register (T1TBOC) | 163h | Transmit bit-oriented message code register. |
| Transmit HDLC-64 Control Register 2 (THC2) | 113h | Bit to enable sending of transmit BOC. |
| Transmit Control Register 1 (TCR1) | 181h | Determines the sourcing of the F-bit. |

Note: The addresses shown above are for Framer 1. Addresses for Framers 2 to 8 can be calculated using the following: Framer $n = (\text{Framer 1 address} + (n - 1) \times 200\text{hex})$, where $n = 2$ to 8 for Framers 2 to 8.

Bits 0 to 5 in the [T1TBOC](#) register contain the BOC message to be transmitted. Setting SBOC = 1 ([THC2.6](#)) causes the transmit BOC controller to immediately begin inserting the BOC sequence into the FDL bit position. The transmit BOC controller automatically provides the abort sequence. BOC messages will be transmitted as long as SBOC is set. Note that the TFPT ([TCR1.6](#)) control bit must be set to zero for the BOC message to overwrite F-bit information being sampled on TSERn.

9.9.5.1.1 To Transmit a BOC

- 1) Write 6-bit code into the [T1TBOC](#) register.
- 2) Set SBOC bit in [THC2](#) = 1.

9.9.5.2 Receive Bit-Oriented Code (BOC) Controller

The DS26528 framers contain a BOC generator on the transmit side and a BOC detector on the receive side. The BOC function is available only in T1, ESF mode in the data link bits. [Table 9-20](#) shows the registers related to the receive BOC operation.

Table 9-20. Registers Related to T1 Receive BOC

| REGISTER | FRAMER 1 ADDRESSES | FUNCTION |
|--|--------------------|---|
| Receive BOC Control Register (T1RBOCC) | 015h | Controls the receive BOC function. |
| Receive BOC Register (T1RBOC) | 063h | Receive bit-oriented message. |
| Receive Latched Status Register 7 (RLS7) | 096h | Indicates changes to the receive bit-oriented messages. |
| Receive Interrupt Mask Register 7 (RIM7) | 0A6h | Mask bits for RBOC for generation of interrupts. |

Note: The addresses shown above are for Framer 1. Addresses for Framers 2 to 8 can be calculated using the following: Framer $n = (\text{Framer 1 address} + (n - 1) \times 200\text{hex})$, where $n = 2$ to 8 for Framers 2 to 8.

In ESF mode, the DS26518 continuously monitors the receive message bits for a valid BOC message. The BOC detect (BD) status bit at [RLS7.0](#) will be set once a valid message has been detected for time determined by the receive BOC filter bits RBF0 and RBF1 in the [T1RBOCC](#) register. The 6-bit BOC message will be available in the RBOC register. Once the user has cleared the BD bit, it will remain clear until a new BOC is detected (or the same BOC is detected following a BOC clear event). The BOC clear (BC) bit at [RLS7.1](#) is set when a valid BOC is no longer being detected for a time determined by the receive BOC disintegration bits RBD0 and RBD1 in the [T1RBOCC](#) register.

The BD and BC status bits can create a hardware interrupt on the $\overline{\text{INTB}}$ signal as enabled by the associated interrupt mask bits in the [RIM7](#) register.

9.9.5.3 Legacy T1 Transmit FDL

It is recommended that the DS26518's built-in BOC or HDLC controllers be used for most applications requiring access to the FDL. [Table 9-21](#) shows the registers related to control of the transmit FDL.

Table 9-21. Registers Related to T1 Transmit FDL

| REGISTER | FRAMER 1 ADDRESSES | FUNCTION |
|---|--------------------|---------------------------------------|
| Transmit FDL Register (T1TFDL) | 162h | FDL code used to insert transmit FDL. |
| Transmit Control Register 2 (T1.TCR2) | 182h | Defines the source of the FDL. |
| Transmit Latched Status Register 2 (TLS2) | 191h | Transmit FDL empty bit. |
| Transmit Interrupt Mask Register 2 (TIM2) | 1A1h | Mask bit for TFDL empty. |

Note: The addresses shown above are for Framer 1. Addresses for Framers 2 to 8 can be calculated using the following: Framer n = (Framer 1 address + $(n - 1) \times 200\text{hex}$), where $n = 2$ to 8 for Framers 2 to 8.

When enabled with [T1.TCR2.7](#), the transmit section will shift out into the T1 data stream, either the FDL (in the ESF framing mode) or the Fs bits (in the D4 framing mode) contained in the Transmit FDL Register ([T1TFDL](#)). When a new value is written to the [T1TFDL](#), it will be multiplexed serially (LSB first) into the proper position in the outgoing T1 data stream. After the full eight bits has been shifted out, the framer will signal the host controller that the buffer is empty and that more data is needed by setting the [TLS2.4](#) bit to a one. $\overline{\text{INTB}}$ will also toggle low if enabled via [TIM2.4](#). The user has 2ms to update the [T1TFDL](#) with a new value. If the [T1TFDL](#) is not updated, the old value in the [T1TFDL](#) register will be transmitted once again. Note that in this mode, no zero stuffing will be applied to the FDL data. It is strongly suggested that the HDLC controller be used for FDL messaging applications.

In the D4 framing mode, the framer uses the [T1TFDL](#) register to insert the Fs framing pattern. To accomplish this the [T1TFDL](#) register must be programmed to 1Ch and [T1.TCR2.7](#) should be set to 0 (source Fs data from the [T1TFDL](#) register).

The [T1TFDL](#) register contains the Facility Data Link (FDL) information that is to be inserted on a byte basis into the outgoing T1 data stream. The LSB is transmitted first. In D4 mode, only the lower six bits are used.

9.9.5.4 Legacy T1 Receive FDL

It is recommended that the DS26518's built-in BOC or HDLC controllers be used for most applications requiring access to the FDL. [Table 9-22](#) shows the registers related to the receive FDL.

Table 9-22. Registers Related to T1 Receive FDL

| REGISTER | FRAMER 1 ADDRESSES | FUNCTION |
|--|--------------------|---|
| Receive FDL Register (T1RFDL) | 062h | FDL code used to receive FDL. |
| Receive Latched Status Register 7 (RLS7) | 096h | Receive FDL full bit is in this register. |
| Receive Interrupt Mask Register 7 (RIM7) | 0A6h | Mask bit for RFDL full. |

Note: The addresses shown above are for Framer 1. Addresses for Framers 2 to 8 can be calculated using the following: Framer n = (Framer 1 address + $(n - 1) \times 200\text{hex}$), where $n = 2$ to 8 for Framers 2 to 8.

In the receive section, the recovered FDL bits or Fs bits are shifted bit-by-bit into the Receive FDL Register ([T1RFDL](#)). Since the [T1RFDL](#) is 8 bits in length, it will fill up every 2ms (8 times 250 μs). The framer will signal an external controller that the buffer has filled via the [RLS7.2](#) bit. If enabled via [RIM7.2](#), the $\overline{\text{INTB}}$ pin will toggle low indicating that the buffer has filled and needs to be read. The user has 2ms to read this data before it is lost. Note that no zero destuffing is applied to the for the data provided through the [T1RFDL](#) register. The [T1RFDL](#) register reports the incoming Facility Data Link (FDL) or the incoming Fs bits. The LSB is received first. In D4 framing mode, [T1RFDL](#) updates on multiframe boundaries and reports only the Fs bits.

9.9.6 E1 Data Link

[Table 9-23](#) shows the registers related to E1 data link.

Table 9-23. Registers Related to E1 Data Link

| REGISTER | FRAMER 1 ADDRESSES | FUNCTION |
|--|------------------------------|--|
| E1 Receive Align Frame Register (E1RAF) | 064h | Receive frame alignment register. |
| E1 Receive Non-Align Frame Register Register (E1RNAF) | 065h | Receive nonframe alignment register. |
| E1 Received Si Bits of the Align Frame Register (E1RsiAF) | 066h | Receive Si bits of the frame alignment frames. |
| Received Si Bits of the Non-Align Frame Register (E1RSiNAF) | 067h | Receive Si bits of the nonframe alignment frames. |
| Received Sa4 to Sa8 Bits Register (E1RSa4 to E1RSa8) | 069h, 06Ah, 06Bh, 06Ch, 06Dh | Receive Sa bits. |
| Transmit Align Frame Register (E1TAF) | 164h | Transmit align frame register. |
| Transmit Non-Align Frame Register (E1TNAF) | 165h | Transmit non-align frame register. |
| Transmit Si Bits of the Align Frame Register (E1TSiAF) | 166h | Transmit Si bits of the frame alignment frames. |
| Transmit Si Bits of the Non-Align Frame Register (E1TSiNAF) | 167h | Transmit Si bits of the nonframe alignment frames. |
| Transmit Sa4 to Sa8 Bits Register (E1TSa4 to E1TSa8) | 169h, 16Ah, 16Bh, 16Ch, 16Dh | Transmit Sa4 to Sa8. |
| E1 Transmit Sa-Bit Control Register (E1TSACR) | 114h | Transmit sources of Sa control. |

Note: The addresses shown are for Framer 1. Addresses for Framers 2 to 8 can be calculated using the following: Framer n = (Framer 1 address + $(n - 1) \times 200\text{hex}$); where $n = 2$ to 8 for Framers 2 to 8.

9.9.6.1 Additional E1 Receive Sa- and Si-Bit Receive Operation (E1 Mode)

The DS26518, when operated in the E1 mode, provides for access to both the Sa and the Si bits via two methods. The first involves using the internal [E1RAF/E1RNAF](#) and [E1TAF/E1TNAF](#) registers. The second method involves an expanded version of the first method.

9.9.6.1.1 Internal Register Scheme Based on Double-Frame (Method 1)

On the receive side, the [E1RAF](#) and [E1RNAF](#) registers will always report the data as it received in the Sa and Si bit locations. The [E1RAF](#) and [E1RNAF](#) registers are updated on align frame boundaries. The setting of the Receive Align Frame bit in Receive Latched Status Register 2 ([RLS2.0](#)) will indicate that the contents of the RAF and RNAF have been updated. The host can use the [RLS2.0](#) bit to know when to read the [E1RAF](#) and [E1RNAF](#) registers. The host has 250µs to retrieve the data before it is lost.

9.9.6.1.2 Internal Register Scheme Based on CRC-4 Multiframe (Receive)

On the receive side, there is a set of eight registers ([E1RSiAF](#), [E1RSiNAF](#), [E1RRA](#), [E1RSa4](#) to [E1RSa8](#)) that report the Si and Sa bits as they are received. These registers are updated with the setting of the receive CRC-4 multiframe bit in Receive Latched Status Register 2 ([RLS2.1](#)). The host can use the [RLS2.1](#) bit to know when to read these registers. The user has 2ms to retrieve the data before it is lost. See the register descriptions for additional information.

9.9.6.1.3 Internal Register Scheme Based on CRC-4 Multiframe (Transmit)

On the transmit side there is a set of eight registers ([E1TSiAF](#), [E1TSiNAF](#), [E1TRA](#), [E1TSa4](#) to [E1TSa8](#)) that, via the E1 Transmit Sa-Bit Control Register ([E1TSACR](#)), can be programmed to insert both Si and Sa data. Data is sampled from these registers with the setting of the transmit multiframe bit in Transmit Latched Status Register 1 ([TLS1.3](#)). The host can use the [TLS1.3](#) bit to know when to update these registers. It has 2ms to update the data or else the old data will be retransmitted. See the register descriptions in Section [10](#) for more information.

9.9.6.2 Sa-Bit Monitoring and Reporting

In addition to the registers outlined above, the DS26518 provides status and interrupt capability in order to detect changes in the state of selected Sa bits. The [E1RSAIMR](#) register can be used to select which Sa bits are monitored for a change of state. When a change of state is detected in one of the enabled Sa bit positions, a status bit is set in the [RLS7](#) register via the SaXCD bit (bit 0). This status bit can in turn be used to generate an interrupt by unmasking [RIM7.0](#) (SaXCD). If multiple Sa bits have been enabled, the user can read the [SaBITS](#) register at address 06Eh to determine the current value of each Sa bit.

For the Sa6 bits, additional support is available to detect specific codewords per ETS 300 233. The Sa6CODE register will report the received Sa6 codeword. The codeword must be stable for a period of three submultiframes and be different from the previous stored value in order to be updated in this register. See the [Sa6CODE](#) register description for further details on the operation of this register and the values reported in it. An additional status bit is provided in [RLS7.1](#) (Sa6CD) to indicate if the received Sa6 codeword has changed. A mask bit is provided for this status bit in [RIM7](#) to allow for interrupt generation when enabled.

9.9.7 Maintenance and Alarms

The DS26518 provides extensive functions for alarm detection and generation. It also provides diagnostic functions for monitoring of performance and sending of diagnostic information:

- Real-time and latched status bits, interrupts and interrupt mask for transmitter and receiver
- LOS detection
- RIA detection and generation
- Error counters
- DS0 monitoring
- Milliwatt generation and detection
- Slip buffer status for transmit and receive

[Table 9-24](#) shows some of the registers related to maintenance and alarms.

Table 9-24. Registers Related to Maintenance and Alarms

| REGISTER | FRAMER 1 ADDRESSES | FUNCTION |
|--|--------------------|--|
| Receive Real-Time Status Register 1 (RRTS1) | 0B0h | Real-time receive status 1. |
| Receive Interrupt Mask Register 1(RIM1) | 0A0h | Real-time interrupt mask 1. |
| Receive Latched Status Register 2 (RLS2) | 091h | Real-time latched status 2. |
| Receive Real-Time Status Register 3 (RRTS3) | 0B2h | Real-time receive status 2. |
| Receive Latched Status Register 3 (RLS3) | 092h | Real-time latched status 3. |
| Receive Interrupt Mask Register 3 (RIM3) | 0A2h | Real-time interrupt mask 3. |
| Receive Interrupt Mask Register 4 (RIM4) | 0A3h | Real-time interrupt mask 3. |
| Receive Latched Status Register 7 (RLS7) | 096h | Real-time latched status 7. |
| Receive Interrupt Mask Register 7 (RIM7) | 0A6h | Real-time interrupt mask 7. |
| Transmit Latched Status Register 1 (TLS1) | 190h | Loss of transmit clock status, etc. |
| Transmit Latched Status Register 3 (Synchronizer) (TLS3) | 192h | Loss of frame status. |
| Receive DS0 Monitor Register (RDS0M) | 060h | Receive DS0 monitor. |
| Error-Counter Configuration Register (ERCNT) | 086h | Configuration of the error counters. |
| Line Code Violation Count Register 1 (LCVCR1) | 050h | Line code violation counter 1. |
| Line Code Violation Count Register 2 (LCVCR2) | 051h | Line code violation counter 2. |
| Path Code Violation Count Register 1 (PCVCR1) | 052h | Receive path code violation counter 1. |
| Path Code Violation Count Register 2 (PCVCR2) | 053h | Receive path code violation counter 2. |
| Frames Out of Sync Count Register 1 (FOSCR1) | 054h | Receive frame out of sync counter 1 |
| Frames Out of Sync Count Register 2 (FOSCR2) | 055h | Receive frame out of sync counter 2 |
| E-Bit Count Register 1 (E1EBCR1) | 056h | E-bit count register 1. |
| E-Bit Count Register 2 (E1EBCR2) | 057h | E-bit count register 2. |

Note: The addresses shown above are for Framer 1. Addresses for Framers 2 to 8 can be calculated using the following: Framer n = (Framer 1 address + $(n - 1) \times 200\text{hex}$), where $n = 2$ to 8 for Framers 2 to 8.

9.9.7.1 Status and Information Bit Operation

When a particular event has occurred (or is occurring), the appropriate bit in one of these registers will be set to a one. Status bits may operate in either a latched or real-time fashion. Some latched bits may be enabled to generate a hardware interrupt via the $\overline{\text{INTB}}$ signal.

9.9.7.1.1 Real-Time Bits

Some status bits operate in a real-time fashion. These bits are read-only and indicate the present state of an alarm or a condition. Real-time bits will remain stable, and valid during the host read operation. The current value of the internal status signals can be read at any time from the real-time status registers without changing any the latched status register bits.

9.9.7.1.2 Latched Bits

When an event or an alarm occurs and a latched bit is set to a one, it will remain set until cleared by the user. These bits typically respond on a change-of-state for an alarm, condition, or event; and operate in a read-then-write fashion. The user should read the value of the desired status bit, and then write a 1 to that particular bit location in order to clear the latched value (write a 0 to locations not to be cleared). Once the bit is cleared, it will not be set again until the event has occurred again.

9.9.7.1.3 Mask Bits

Some of the alarms and events can be either masked or unmasked from the interrupt pin via the Receive Interrupt Mask Registers ([RIM1](#), [RIM3](#), [RIM4](#), [RIM5](#), [RIM7](#)). When unmasked, the $\overline{\text{INTB}}$ signal will be forced low when the enabled event or condition occurs. The $\overline{\text{INTB}}$ pin will be allowed to return high (if no other unmasked interrupts are present) when the user reads then clears (with a write) the alarm bit that caused the interrupt to occur. Note that the latched status bit and the $\overline{\text{INTB}}$ pin will clear even if the alarm is still present.

Note that some conditions may have multiple status indications. For example, receive loss of frame (RLOF) provides the following indications:

| | |
|-----------------------------------|--|
| RRTS1.0 (RLOF) | Real-time indication that the receiver is not synchronized with incoming data stream. Read-only bit that remains high as long as the condition is present. |
| RLS1.0 (RLOFD) | Latched indication that the receiver has lost synchronization since the bit was last cleared. Bit will clear when written by the user, even if the condition is still present (rising edge detect of RRTS1.0). |
| RLS1.4 (RLOFC) | Latched indication that the receiver has reacquired synchronization since the bit was last cleared. Bit will clear when written by the user, even if the condition is still present (falling edge detect of RRTS1.0). |

9.9.8 Alarms

Table 9-25. T1 Alarm Criteria

| ALARM | | SET CRITERIA | CLEAR CRITERIA |
|---|---|---|---|
| AIS (Blue Alarm) (See Note 1) | | When over a 3ms window, 4 or fewer zeros are received. | When over a 3ms window, 5 or more zeros are received. |
| RAI (Yellow Alarm) | 1) D4 Bit 2 Mode (T1RCR2.0 = 0) | When bit 2 of 256 consecutive channels is set to zero for at least 254 occurrences. | When bit 2 of 256 consecutive channels is set to zero for less than 254 occurrences. |
| | 2) D4 12th F-Bit Mode (T1RCR2.0 = 1) (Note: This mode is also referred to as the "Japanese Yellow Alarm.") | When the 12th framing bit is set to one for two consecutive occurrences. | When the 12th framing bit is set to zero for two consecutive occurrences. |
| | 3) ESF Mode | When 16 consecutive patterns of 00FF appear in the FDL. | When 14 or fewer patterns of 00FF hex out of 16 possible appear in the FDL. |
| | 4) J1 ESF Mode (J1 LFA) | When 16 consecutive patterns of FFFF appear in the FDL. | When 14 or fewer patterns of FFFF hex out of 16 possible appear in the FDL. |
| LOS (Loss of Signal) (Note: This alarm is also referred to as receive carrier loss (RCL).) | | When 192 consecutive zeros are received. | When 14 or more ones out of 112 possible bit positions are received starting with the first one received. |

Note 1: The definition of the Alarm Indication Signal (Blue Alarm) is an unframed all-ones signal. AIS detectors should be able to operate properly in the presence of a 10E-3 error rate and they should not falsely trigger on a framed all-ones signal. The AIS alarm criteria in the DS26518 has been set to achieve this performance. It is recommended that the RAIS bit be qualified with the RLOF bit.

Note 2: The following terms are equivalent:
 RAIS = Blue Alarm
 RLOS = RCL
 RLOF = Loss of Frame (conventionally RLOS for Maxim devices)
 RRAI = Yellow Alarm

9.9.8.1 Transmit RAI

[Table 9-26](#) shows the registers related to the transmit RAI (Yellow Alarm).

Table 9-26. Registers Related to Transmit RAI (Yellow Alarm)

| REGISTER | FRAMER 1 ADDRESSES | FUNCTION |
|--|--------------------|---|
| Transmit Control Register 1 (TCR1 .TRA1) | 181h | Enable transmission of RAI. |
| Transmit Control Register 2 (T1.TCR2 .TRAIS) | 182h | Select RAI to be T1 or J1. |
| Transmit Control Register 4 (TCR4 .TRA1M) | 186h | Select RAI to be normal or RAI-CI for T1 ESF mode. |
| Transmit Control Register 2 (E1.TCR2 .ARA) | 182h | Selects automatic remote alarm generation in E1 mode. |

Note: The addresses shown above are for Framer 1. Addresses for Framers 2 to 8 can be calculated using the following: Framer n = (Framer 1 address + $(n - 1) \times 200\text{hex}$), where $n = 2$ to 8 for Framers 2 to 8.

9.9.8.2 Receive RAI

[Table 9-27](#) shows the registers related to the receive RAI (Yellow Alarm).

Table 9-27. Registers Related to Receive RAI (Yellow Alarm)

| REGISTER | FRAMER 1 ADDRESSES | FUNCTION |
|--|--------------------|-------------------------------|
| Receive Control Register 2 (T1RCR2.RRAIS) | 014h | Select RAI to be T1 or J1. |
| Receive Control Register 2 (T1RCR2.RAIE) | 014h | Integration Enable for T1 ESF |

Note: The addresses shown above are for Framer 1. Addresses for Framers 2 to 8 can be calculated using the following: Framer n = (Framer 1 address + $(n - 1) \times 200\text{hex}$), where $n = 2$ to 8 for Framers 2 to 8.

9.9.8.3 E1 Automatic Alarm Generation

The device can be programmed to automatically transmit AIS or remote alarm. When automatic AIS generation is enabled ([E1.TCR2.AAIS](#) = 1), the device monitors the receive-side framer to determine if any of the following conditions are present/loss of receive frame synchronization, AIS alarm (all ones) reception, or loss of receive carrier (or signal). If any one (or more) of the above conditions is present, then the framer will either force an AIS.

When automatic RAI generation is enabled ([E1.TCR2.ARA](#) = 1), the framer monitors the receive side to determine if any of the following conditions are present/ loss of receive frame synchronization, AIS alarm (all ones) reception, or loss of receive carrier (or signal) or if CRC-4 multiframe synchronization cannot be found within 128ms of FAS synchronization (if CRC-4 is enabled). If any one (or more) of the above conditions is present, then the framer will transmit a RAI alarm. RAI generation conforms to ETS 300 011 and ITU-T G.706 specifications.

Note: It is an illegal state to have both automatic AIS generation and automatic remote alarm generation enabled at the same time.

9.9.8.4 Receive AIS-CI and RAI-CI Detection

AIS-CI is a repetitive pattern of 1.26 seconds. It consists of 1.11 seconds of an unframed all-ones pattern and 0.15 seconds of all ones modified by the AIS-CI signature. The AIS-CI signature is a repetitive pattern 6176 bits in length in which, if the first bit is numbered bit 0, bits 3088, 3474 and 5790 are logical zeros and all other bits in the pattern are logical ones (T1.403). AIS-CI is an unframed pattern, so it is defined for all T1 framing formats. The RAIS-CI bit is set when the AIS-CI pattern has been detected and RAIS ([RRTS1.2](#)) is set. RAIS-CI is a latched bit that should be cleared by the host when read. RAIS-CI will continue to set approximately every 1.2 seconds that the condition is present. The host will need to ‘poll’ the bit, in conjunction with the normal AIS indicators to determine when the condition has cleared.

RAI-CI is a repetitive pattern within the ESF data link with a period of 1.08 seconds. It consists of sequentially interleaving 0.99 seconds of “00000000 11111111” (right-to-left) with 90 ms of “00111110 11111111”. The RRAI-CI bit is set when a bit oriented code of “00111110 11111111” is detected while RRAI ([RRTS1.3](#)) is set. The RRAI-CI detector uses the receive BOC filter bits (RBF0 and RBF1) located in RBOCC to determine the integration time for RAI-CI detection. Like RAIS-CI, the RRAI-CI bit is latched and should be cleared by the host when read. RRAI-CI will continue to set approximately every 1.1 seconds that the condition is present. The host will need to “poll” the bit, in conjunction with the normal RAI indicators to determine when the condition has cleared. It may be useful to enable the 200ms ESF RAI integration time with the RAIE control bit ([T1RCR2.1](#)) in networks that utilize RAI-CI.

9.9.8.5 T1 Receive-Side Digital Milliwatt Code Generation

Receive-side digital milliwatt code generation involves using the T1 Receive Digital Milliwatt Registers ([T1RDMWE1–3](#)) to determine which of the 24 T1 channels of the T1 line going to the backplane should be overwritten with a digital milliwatt pattern. The digital milliwatt code is an 8-byte repeating pattern that represents a 1kHz sine wave (1E/0B/0B/1E/9E/8B/8B/9E). Each bit in the T1RDMWEx registers represents a particular channel. If a bit is set to a one, then the receive data in that channel will be replaced with the digital milliwatt code. If a bit is set to zero, no replacement occurs.

9.9.9 Error Count Registers

The DS26518 contains four counters that are used to accumulate line coding errors, path errors, and synchronization errors. Counter update options include one second boundaries, 42ms (T1 mode only), 62.5ms (E1 mode only) or manually. See the Error Counter Configuration Register ([ERCNT](#)). When updated automatically, the user can use the interrupt from the timer to determine when to read these registers. All four counters will saturate at their respective maximum counts and they will not roll over. (**Note:** Only the Line Code Violation Count Register has the potential to overflow but the bit error would have to exceed 10E-2 before this would occur.)

The DS26518 can share the one-second timer from Port 1 across all ports. All DS26518 error/performance counters can be configured to update on the shared one-second source or a separate manual update signal input. See the [ERCNT](#) register for more information. By allowing multiple framer cores to synchronously latch their counters, the host software can be streamlined to read and process performance information from multiple spans in a more controlled manner.

9.9.9.1 Line Code Violation Count Register (LCVCR)

Either bipolar violations or code violations can be counted. Bipolar violations are defined as consecutive marks of the same polarity. In T1 mode, if the B8ZS mode is set for the receive side, then B8ZS codewords are not counted as BPVs. In E1 mode, if the HDB3 mode is set for the receive side, then HDB3 codewords are not counted as BPVs. If [ERCNT.0](#) is set, then the LVC counts code violations as defined in ITU-T O.161. Code violations are defined as consecutive bipolar violations of the same polarity. In most applications, the framer should be programmed to count BPVs when receiving AMI code and to count CVs when receiving B8ZS or HDB3 code. This counter increments at all times and is not disabled by loss of sync conditions. The counter saturates at 65,535 and will not rollover. The bit error rate on an E1 line would have to be greater than 10E-2 before the VCR would saturate. See [Table 9-28](#) and [Table 9-29](#) for details of exactly what the LCVCRs count.

Table 9-28. T1 Line Code Violation Counting Options

| COUNT EXCESSIVE ZEROS? (ERCNT.0) | B8ZS ENABLED? (RCR1.6) | WHAT IS COUNTED IN LCVCR1 , LCVCR2 |
|---|---|---|
| No | No | BPVs |
| Yes | No | BPVs + 16 consecutive zeros |
| No | Yes | BPVs (B8ZS/HDB3 codewords not counted) |
| Yes | Yes | BPVs + 8 consecutive zeros |

Table 9-29. E1 Line Code Violation Counting Options

| E1 CODE VIOLATION SELECT (ERCNT.0) | WHAT IS COUNTED IN LCVCR1 , LCVCR2 |
|---|---|
| 0 | BPVs |
| 1 | CVs |

9.9.9.2 Path Code Violation Count Register (PCVCR)

In T1 operation, the Path Code Violation Count Register records either Ft, Fs, or CRC-6 errors. When the receive side of a framer is set to operate in the T1 ESF framing mode, PCVCR will record errors in the CRC-6 codewords. When set to operate in the T1 D4 framing mode, PCVCR will count errors in the Ft framing bit position. Via the [ERCNT.2](#) bit, a framer can be programmed to also report errors in the Fs framing bit position. The PCVCR will be disabled during receive loss of synchronization (RLOF = 1) conditions. See [Table 9-30](#) for a detailed description of exactly what errors the PCVCR counts in T1 operation.

In E1 operation, the Path Code Violation Count Register records CRC-4 errors. Since the maximum CRC-4 count in a one second period is 1000, this counter cannot saturate. The counter is disabled during loss of sync at either the FAS or CRC-4 level; it will continue to count if loss of multiframe sync occurs at the CAS level.

The Path Code Violation Count Register 1 ([PCVCR1](#)) is the most significant word and the Path Code Violation Count Register 2 ([PCVCR2](#)) is the least significant word of a 16-bit counter that records path violations (PVs).

Table 9-30. T1 Path Code Violation Counting Arrangements

| FRAMING MODE | COUNT Fs ERRORS? | WHAT IS COUNTED IN PCVCR1 , PCVCR2 ? |
|--------------|------------------|--|
| D4 | No | Errors in the Ft pattern |
| D4 | Yes | Errors in both the Ft and Fs patterns |
| ESF | Don't Care | Errors in the CRC-6 codewords |

9.9.9.3 Frames Out of Sync Count Register (FOSCR)

The FOSCR is used to count the number of multiframes that the receive synchronizer is out of sync. This number is useful in ESF applications needing to measure the parameters loss of frame count (LOFC) and ESF error events as described in AT&T publication TR54016. When the FOSCR is operated in this mode, it is not disabled during receive loss of synchronization (RLOF = 1) conditions. The FOSCR has alternate operating mode whereby it will count either errors in the Ft framing pattern (in the D4 mode) or errors in the FPS framing pattern (in the ESF mode). When the FOSCR is operated in this mode, it is disabled during receive loss of synchronization (RLOF = 1) conditions. See [Table 9-31](#) for a detailed description of what the FOSCR is capable of counting.

In E1 mode, the FOSCR counts word errors in the frame alignment signal in time slot 0. This counter is disabled when RLOF is high. FAS errors will not be counted when the framer is searching for FAS alignment and/or synchronization at either the CAS or CRC-4 multiframe level. Since the maximum FAS word error count in a one-second period is 4000, this counter cannot saturate.

The Frames Out of Sync Count Register 1 ([FOSCR1](#)) is the most significant word and the Frames Out of Sync Count Register 2 ([FOSCR2](#)) is the least significant word of a 16-bit counter that records frames out of sync.

Table 9-31. T1 Frames Out of Sync Counting Arrangements

| FRAMING MODE (RCR1.5) | COUNT MOS OR F-BIT ERRORS (ERCNT.1) | WHAT IS COUNTED IN FOSCR1 , FOSCR2 |
|--|--|---|
| D4 | MOS | Number of multiframes out of sync |
| D4 | F-Bit | Errors in the Ft pattern |
| ESF | MOS | Number of multiframes out of sync |
| ESF | F-Bit | Errors in the FPS pattern |

9.9.9.4 E-Bit Counter (EBCR)

This counter is only available in E1 mode. The E-Bit Count Register 1 ([E1EBCR1](#)) is the most significant word and the E-Bit Count Register 2 ([E1EBCR2](#)) is the least significant word of a 16-bit counter that records far-end block errors (FEBE) as reported in the first bit of frames 13 and 15 on E1 lines running with CRC-4 multiframe. These count registers will increment once each time the received E-bit is set to zero. Since the maximum E-bit count in a one-second period is 1000, this counter cannot saturate. The counter is disabled during loss of sync at either the FAS or CRC-4 level; it will continue to count if loss of multiframe sync occurs at the CAS level.

9.9.10 DS0 Monitoring Function

The DS26518 can monitor one DS0 (64kbps) channel in the transmit direction and one DS0 channel in the receive direction at the same time. [Table 9-32](#) shows the registers related to the control of transmit and receive DS0.

Table 9-32. Registers Related to DS0 Monitoring

| REGISTER | FRAMER 1 ADDRESSES | FUNCTION |
|--|--------------------|-----------------------------------|
| Transmit DS0 Channel Monitor Select Register (TDS0SEL) | 189h | Transmit channel to be monitored. |
| Transmit DS0 Monitor Register (TDS0M) | 1BBh | Monitored data. |
| Receive Channel Monitor Select Register (RDS0SEL) | 012h | Receive channel to be monitored. |
| Receive DS0 Monitor Register (RDS0M) | 060h | Monitored data. |

Note: The addresses shown above are for Framer 1. Addresses for Framers 2 to 8 can be calculated using the following: Framer $n = (\text{Framer 1 address} + (n - 1) \times 200\text{hex})$, where $n = 2$ to 8 for Framers 2 to 8.

In the transmit direction the user will determine which channel is to be monitored by properly setting the TCM[4:0] bits in the [TDS0SEL](#) register. In the receive direction, the RCM[4:0] bits in the [RDS0SEL](#) register need to be properly set. The DS0 channel pointed to by the TCM[4:0] bits will appear in the Transmit DS0 Monitor Register ([TDS0M](#)) and the DS0 channel pointed to by the RCM[4:0] bits will appear in the Receive DS0 Monitor Register ([RDS0M](#)). The TCM[4:0] and RCM[4:0] bits should be programmed with the decimal decode of the appropriate T1 or E1 channel. T1 channels 1 to 24 map to register values 0 to 23. E1 channels 1 to 32 map to register values 0 to 31. For example, if DS0 channel 6 in the transmit direction and DS0 channel 15 in the receive direction needed to be monitored, then the following values would be programmed into TDS0SEL and RDS0SEL:

| | |
|----------|----------|
| TCM4 = 0 | RCM4 = 0 |
| TCM3 = 0 | RCM3 = 1 |
| TCM2 = 1 | RCM2 = 1 |
| TCM1 = 0 | RCM1 = 1 |
| TCM0 = 1 | RCM0 = 0 |

9.9.11 Transmit Per-Channel Idle Code Generation

Channel data can be replaced by an idle code on a per-channel basis in the transmit and receive directions.

The Transmit Idle Code Definition Registers ([TIDR1–32](#)) are provided to set the 8-bit idle code for each channel. The Transmit Channel Idle Code Enable registers ([TCICE1–4](#)) are used to enable idle code replacement on a per-channel basis.

9.9.12 Receive Per-Channel Idle Code Insertion

Channel data can be replaced by an idle code on a per-channel basis in the transmit and receive directions. The Receive Idle Code Definition Registers ([RIDR1–32](#)) are provided to set the 8-bit idle code for each channel. The Receive Channel Idle Code Enable Registers ([RCICE1–4](#)) are used to enable idle code replacement on a per-channel basis.

9.9.13 Per-Channel Loopback

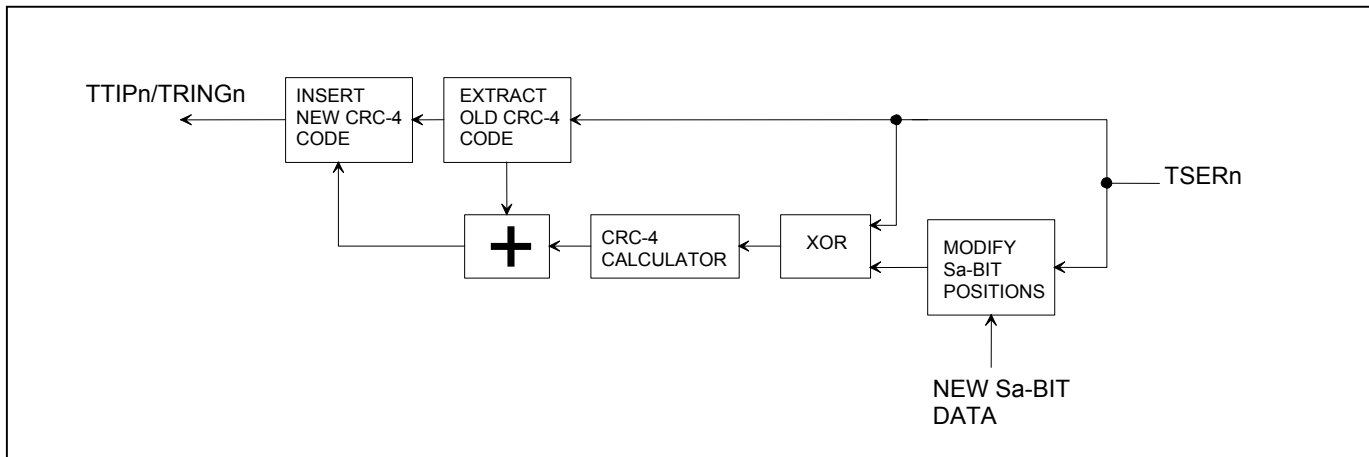
The Per-Channel Loopback Enable Registers ([PCL1–4](#)) determine which channels (if any) from the backplane should be replaced with the data from the receive side or in other words, off of the T1 or E1 line. If this loopback is enabled, then transmit and receive clocks and frame syncs must be synchronized. One method to accomplish this would be to tie RCLK_n to TCLK_n and RFSYNC_n to TSYNC_n. There are no restrictions on which channels can be looped back or on how many channels can be looped back.

Each of the bit positions in [PCL1–4](#)) represents a DS0 channel in the outgoing frame. When these bits are set to a one, data from the corresponding receive channel will replace the data on TSER_n for that channel.

9.9.14 E1 G.706 Intermediate CRC-4 Updating (E1 Mode Only)

The DS26518 can implement the G.706 CRC-4 recalculation at intermediate path points. When this mode is enabled, the data stream presented at TSER_n will already have the FAS/NFAS, CRC multiframe alignment word, and CRC-4 checksum in time slot 0. The user can modify the Sa-bit positions and this change in data content will be used to modify the CRC-4 checksum. This modification, however, will not corrupt any error information the original CRC-4 checksum may contain. In this mode of operation, TSYNC_n must be configured to multiframe mode. The data at TSER_n must be aligned to the TSYNC_n signal. If TSYNC_n is an input then the user must assert TSYNC_n aligned at the beginning of the multiframe relative to TSER_n. If TSYNC_n is an output, the user must multiframe align the data presented to TSER_n. This mode is enabled with the [TCR3.0](#) control bit (CRC4R). Note that the E1 transmitter must already be enabled for CRC insertion with the [TCR1.0](#) control bit (TCRC4). See [Figure 9-16](#).

Figure 9-16. CRC-4 Recalculate Method



9.9.15 T1 Programmable In-Band Loop Code Generator

The DS26518 can generate and detect a repeating bit pattern from one to eight bits or 16 bits in length. **This function is available only in T1 mode.**

Table 9-33. Registers Related to T1 In-Band Loop Code Generator

| REGISTER | FRAMER 1 ADDRESSES | FUNCTION |
|--|--------------------|---|
| Transmit Code Definition Register 1 (T1TCD1) | 1ACh | Pattern to be sent for loop code. |
| Transmit Code Definition Register 2 (T1TCD2) | 1ADh | Length of the pattern to be sent. |
| Transmit Control Register 3 (TCR3) | 183h | TLOOP bit for control of number of patterns being sent. |
| Transmit Control Register 4 (TCR4) | 186h | Length of the code being sent. |

Note: The addresses shown above are for Framer 1. Addresses for Framers 2 to 8 can be calculated using the following: Framer $n = (\text{Framer 1 address} + (n - 1) \times 200\text{hex})$, where $n = 2$ to 8 for Framers 2 to 8.

To transmit a pattern, the user will load the pattern to be sent into the Transmit Code Definition Registers ([T1TCD1](#) and [T1TCD2](#)) and select the proper length of the pattern by setting the TC0 and TC1 bits in Transmit Control Register 4 ([TCR4](#)). When generating a 1-, 2-, 4-, 8-, or 16-bit pattern both [T1TCD1](#) and [T1TCD2](#) must be filled with the proper code. Generation of a 3-, 5-, 6-, and 7-bit pattern only requires [T1TCD1](#) to be filled. Once this is accomplished, the pattern will be transmitted as long as the TLOOP control bit ([TCR3.0](#)) is enabled. Normally (unless the transmit formatter is programmed to not insert the F-bit position) the framer will overwrite the repeating pattern once every 193 bits to allow the F-bit position to be sent.

As an example, to transmit the standard “loop-up” code for Channel Service Units (CSUs), which is a repeating pattern of ...10000100001..., set TCD1 = 80h, TC0 = 0, TC1 = 0, and [TCR3.0](#) = 1.

9.9.16 T1 Programmable In-Band Loop Code Detection

The DS26518 can generate and detect a repeating bit pattern from one to eight bits or 16 bits in length. **This function is available only in T1 mode.**

Table 9-34. Registers Related to T1 In-Band Loop Code Detection

| REGISTER | FRAMER 1 ADDRESSES | FUNCTION |
|--|--------------------|--|
| Receive In-Band Code Control Register (T1RIBCC) | 082h | Used for selecting length of receive in-band loop code register. |
| Receive Up Code Definition Register 1 (T1RUPCD1) | 0ACh | Receive up code definition register 1. |
| Receive Up Code Definition Register 2 (T1RUPCD2) | 0ADh | Receive up code definition register 2. |
| Receive Down Code Definition Register 1 (T1RDNCD1) | 0AEh | Receive down code definition register 1. |
| Receive Down Code Definition Register 2 (T1RDNCD2) | 0AFh | Receive up code definition register 2. |
| Receive Spare Code Register 1 (T1RSCD1) | 09Ch | Receive spare code register 1. |
| Receive Spare Code Register 2 (T1RSCD2) | 09Dh | Receive spare code register 2. |
| Receive Real-Time Status Register 3 (RRTS3) | 0B2h | Real-time loop code detect. |
| Receive Latched Status Register 3 (RLS3) | 092h | Latched loop code detect bits. |
| Receive Interrupt Mask Register 3 (RIM3) | 0A2h | Mask for latched loop code detect bits. |

Note: The addresses shown above are for Framer 1. Addresses for Framers 2 to 8 can be calculated using the following: Framer $n = (\text{Framer 1 address} + (n - 1) \times 200\text{hex})$, where $n = 2$ to 8 for Framers 2 to 8.

The framer has three programmable pattern detectors. Typically, two of the detectors are used for “loop-up” and “loop-down” code detection. The user will program the codes to be detected in the Receive Up Code Definition Registers 1 and 2 ([T1RUPCD1](#) and [T1RUPCD2](#)) and the Receive Down Code Definition Registers 1 and 2 ([T1RDNCD1](#) and [T1RDNCD2](#)) registers and the length of each pattern will be selected via the [T1RIBCC](#) register. There is a third detector (spare) and it is defined and controlled via the [T1RSCD1/T1RSCD2](#) and [T1RSCC](#) registers. When detecting a 16-bit pattern both receive code definition registers are used together to form a 16-bit register. For 8-bit patterns, both receive code definition registers will be filled with the same value. Detection of a 1-, 2-, 3-, 4-, 5-, 6-, and 7-bit pattern only requires the first receive code definition register to be filled. The framer will detect repeating pattern codes in both framed and unframed circumstances with bit error rates as high as $10E-2$. The detectors can handle both F-bit inserted and F-bit overwrite patterns. Writing the least significant byte of receive code definition register resets the integration period for that detector. The code detector has a nominal integration period of 48ms. Hence, after about 48ms of receiving a valid code, the proper status bit (LUP, LDN, and LSP) will be set to a one. Note that real-time status bits, as well as latched set and clear bits are available for LUP, LDN and LSP ([RRTS3](#) and [RLS3](#)). Normally codes are sent for a period of 5 seconds. It is recommend that the software poll the framer every 50ms to 100ms until 5 seconds has elapsed to ensure that the code is continuously present.

9.9.17 Framer Payload Loopbacks

The framer, payload, and remote loopbacks are controlled by [RCR3](#).

Table 9-35. Register Related to Framer Payload Loopbacks

| RECEIVE CONTROL REGISTER 3 (RCR3) | FRAMER 1 ADDRESSES | FUNCTION |
|---|--------------------|--|
| Framer Loopback | 083h | Transmit data output from the framer is looped back to the receiver. |
| Payload Loopback | 083h | The 192-bit payload data is looped back to the transmitter. |
| Remote Loopback | 083h | Data recovered by the receiver is looped back to the transmitter. |

Note: The addresses shown above are for Framer 1. Addresses for Framers 2 to 8 can be calculated using the following: Framer n = (Framer 1 address + $(n - 1) \times 200\text{hex}$), where $n = 2$ to 8 for Framers 2 to 8.

9.10 HDLC Controllers

There are two HDLC controllers available for each port of the DS26518. HDLC-64 is the default HDLC controller, which is software compatible to the entire TEX series of SCTs. The HDLC-256 controller is available on the DS26518 beginning with die revision B1. (**Note:** Older DS26518 die revisions do not have this feature, so check the device errata.) [Table 9-36](#) describes the features available for each controller.

Table 9-36. HDLC-64/HDLC-256 Controller Features

| HDLC CONTROLLER | FIFO DEPTH (BYTES) | MAP TO FDL | MAP TO Sa BITS | MAP TO SINGLE DS0 | MAP TO MULTIPLE DS0s |
|-----------------|--------------------|------------|----------------|-------------------|----------------------|
| HDLC-64 | 64 | Yes | Yes | Yes | No |
| HDLC-256 | 256 | Yes | Yes | Yes | Yes, up to 32 |

9.10.1 HDLC-64 Controller

The DS26518 has an enhanced HDLC controller that can be mapped into a single time slot, or Sa4 to Sa8 bits (E1 mode), or the FDL (T1 mode). This HDLC controller has a 64-byte FIFO buffer in both the transmit and receive paths. The user can select any specific bits within the time slot(s) to assign to the HDLC-64 controller, as well as specific Sa bits (E1 mode).

The HDLC-64 controller performs all the necessary overhead for generating and receiving performance report messages (PRMs) as described in ANSI T1.403 and the messages as described in AT&T TR54016. The HDLC-64 controller automatically generates and detects flags, generates and checks the CRC checksum, generates and detects abort sequences, stuffs and destuffs zeros, and byte aligns to the data stream. The 64-byte buffers in the HDLC-64 controller are large enough to allow a full PRM to be received or transmitted without host intervention.

[Table 9-37](#) shows the registers related to the HDLC-64.

Table 9-37. Registers Related to the HDLC-64

| REGISTER | FRAMER 1 ADDRESSES | FUNCTION |
|---|--------------------|---|
| Receive HDLC-64 Control Register (RHC) | 010h | Mapping of the HDLC-64 to DS0 or FDL, Sa bits. |
| Receive HDLC-64 Bit Suppress Register (RHBSE) | 011h | Receive HDLC-64 bit suppression register. |
| Receive HDLC-64 FIFO Control Register (RHFC) | 087h | Determines the watermark of the receive HDLC-64 FIFO. |
| Receive HDLC-64 Packet Bytes Available Register (RHPBA) | 0B5h | Tells the user how many bytes are available in the receive HDLC-64 FIFO. |
| Receive HDLC-64 FIFO Register (RHF) | 0B6h | The actual FIFO data. |
| Receive Real-Time Status Register 5 (HDLC-64) (RRTS5) | 0B4h | Indicates the FIFO status. |
| Receive Latched Status Register 5 (HDLC-64) (RLS5) | 094h | Latched status. |
| Receive Interrupt Mask Register 5 (HDLC-64) (RIM5) | 0A4h | Interrupt mask for interrupt generation for the latched status. |
| Transmit HDLC-64 Control Register 1 (THC1) | 110h | Miscellaneous transmit HDLC-64 control. |
| Transmit HDLC-64 Bit Suppress Register (THBSE) | 111h | Transmit HDLC-64 bit suppress for bits not to be used. |
| Transmit HDLC-64 Control Register 2 (THC2) | 113h | HDLC-64 to DS0 channel selection and other control. |
| Transmit HDLC-64 FIFO Control Register (THFC) | 187h | Used to control the transmit HDLC-64 FIFO. |
| Transmit Real-Time Status Register 2 (HDLC-64) (TRTS2) | 1B1h | Indicates the real-time status of the transmit HDLC-64 FIFO. |
| Transmit Latched Status Register 2 (HDLC-64) (TLS2) | 191h | Indicates the FIFO status. |
| Transmit Interrupt Mask Register 2 (HDLC-64) (TIM2) | 1A1h | Interrupt mask for the latched status. |
| Transmit HDLC-64 FIFO Buffer Available Register (TFBA) | 1B3h | Indicates the number of bytes that can be written into the transmit FIFO. |
| Transmit HDLC-64 FIFO Register (THE) | 1B4h | Transmit HDLC-64 FIFO. |

Note: The addresses shown are for Framer 1. Addresses for Framers 2 to 8 can be calculated using the following: Framer $n = (\text{Framer 1 address} + (n - 1) \times 200\text{hex})$; where $n = 2$ to 8 for Framers 2 to 8.

9.10.1.1 HDLC-64 FIFO Control

Control of the transmit and receive FIFOs is accomplished via the Receive HDLC-64 FIFO Control ([RHFC](#)) and Transmit HDLC-64 FIFO Control ([THFC](#)) registers. The FIFO control registers set the watermarks for the FIFO.

When the receive FIFO fills above the high watermark, the RHWB bit ([RRTS5.1](#)) will be set. RHWB and TLWB are real-time bits and will remain set as long as the FIFO's write pointer is above the watermark. When the transmit FIFO empties below the low watermark, the TLWB bit in the [TRTS2](#) register will be set. TLWB is a real-time bit and will remain set as long as the transmit FIFO's write pointer is below the watermark. If enabled, this condition can also cause an interrupt via the $\overline{\text{INTB}}$ pin.

If the receive HDLC-64 FIFO does overrun the current packet being processed is dropped and the receive FIFO is emptied. The packet status bits in [RRTS5](#) and [RLS5.5](#) (ROVR) indicate an overrun.

9.10.1.2 Receive Packet Bytes Available

The lower 7 bits of the Receive HDLC-64 Packet Bytes Available Register ([RHPBA](#)) indicates the number of bytes (0 to 64) that can be read from the receive FIFO. The value indicated by this register informs the host as to how many bytes can be read from the receive FIFO without going past the end of a message. This value refers to one of four possibilities: the first part of a packet, the continuation of a packet, the last part of a packet, or a complete packet. After reading the number of bytes indicated by this register, the host then checks the HDLC-64 status registers for detailed message status.

If the value in the [RHPBA](#) register refers to the beginning portion of a message or continuation of a message, the MSB of the RHPBA register returns a value of 1. This indicates that the host can safely read the number of bytes returned by the lower 7 bits of the RHPBA register, but there is no need to check the information register since the packet has not yet terminated (successfully or otherwise).

9.10.1.3 HDLC-64 Status and Information

[RRTS5](#), [RLS5](#), and [TLS2](#) provide status information for the HDLC-64 controller. When a particular event has occurred (or is occurring), the appropriate bit in one of these registers will be set to a one. Some of the bits in these registers are latched and some are real-time bits that are not latched. This section contains register descriptions that list which bits are latched and which are real-time. With the latched bits, when an event occurs and a bit is set to a one, it will remain set until the user reads and clears that bit. The bit will be cleared when a 1 is written to the bit and it will not be set again until the event has occurred again. The real-time bits report the current instantaneous conditions that are occurring and the history of these bits is not latched.

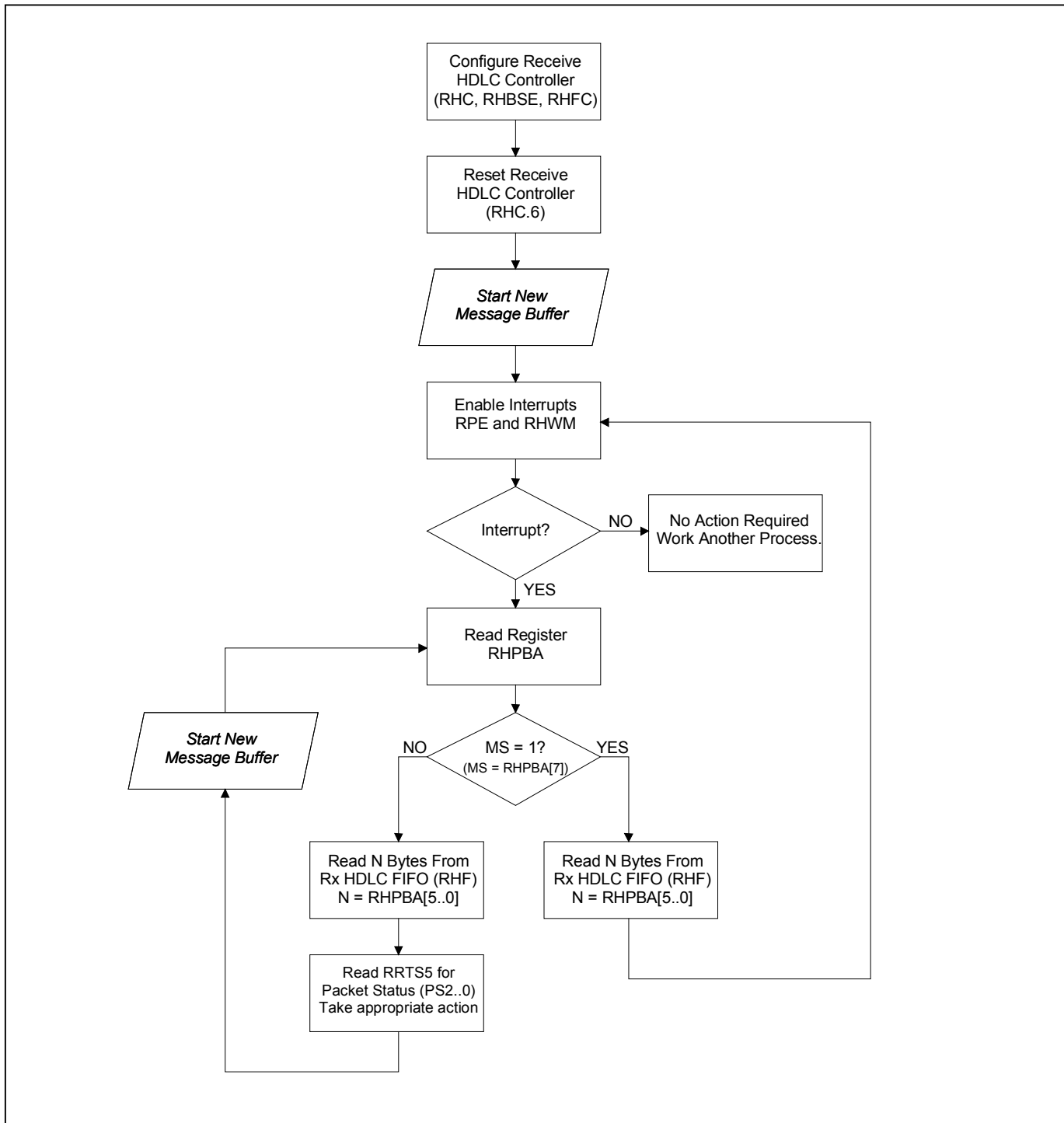
Like the other latched status registers, the user will follow a read of the status bit with a write. The byte written to the register will inform the device which of the latched bits the user wishes to clear (the real-time bits are not affected by writing to the status register). The user will write a byte to one of these registers, with a one in the bit positions he or she wishes to clear and a zero in the bit positions he or she does not wish to clear.

The HDLC-64 status registers [RLS5](#) and [TLS2](#) have the ability to initiate a hardware interrupt via the $\overline{\text{INTB}}$ output signal. Each of the events in this register can be either masked or unmasked from the interrupt pin via the HDLC-64 interrupt mask registers [RIM5](#) and [TIM2](#). Interrupts will force the $\overline{\text{INTB}}$ signal low when the event occurs. The $\overline{\text{INTB}}$ pin will be allowed to return high (if no other interrupts are present) when the user reads the event bit that caused the interrupt to occur.

9.10.1.4 Receive HDLC-64 Example

The HDLC-64 status registers in the DS26518 allow for flexible software interface to meet the user's preferences. When receiving HDLC-64 messages, the host can choose to be interrupt driven, to poll to desired status registers, or a combination of polling and interrupt processes can be used. [Figure 9-17](#) shows an example routine for using the DS26518 HDLC-64 receiver.

Figure 9-17. Receive HDLC-64 Message Example



9.10.2 Transmit HDLC-64 Controller

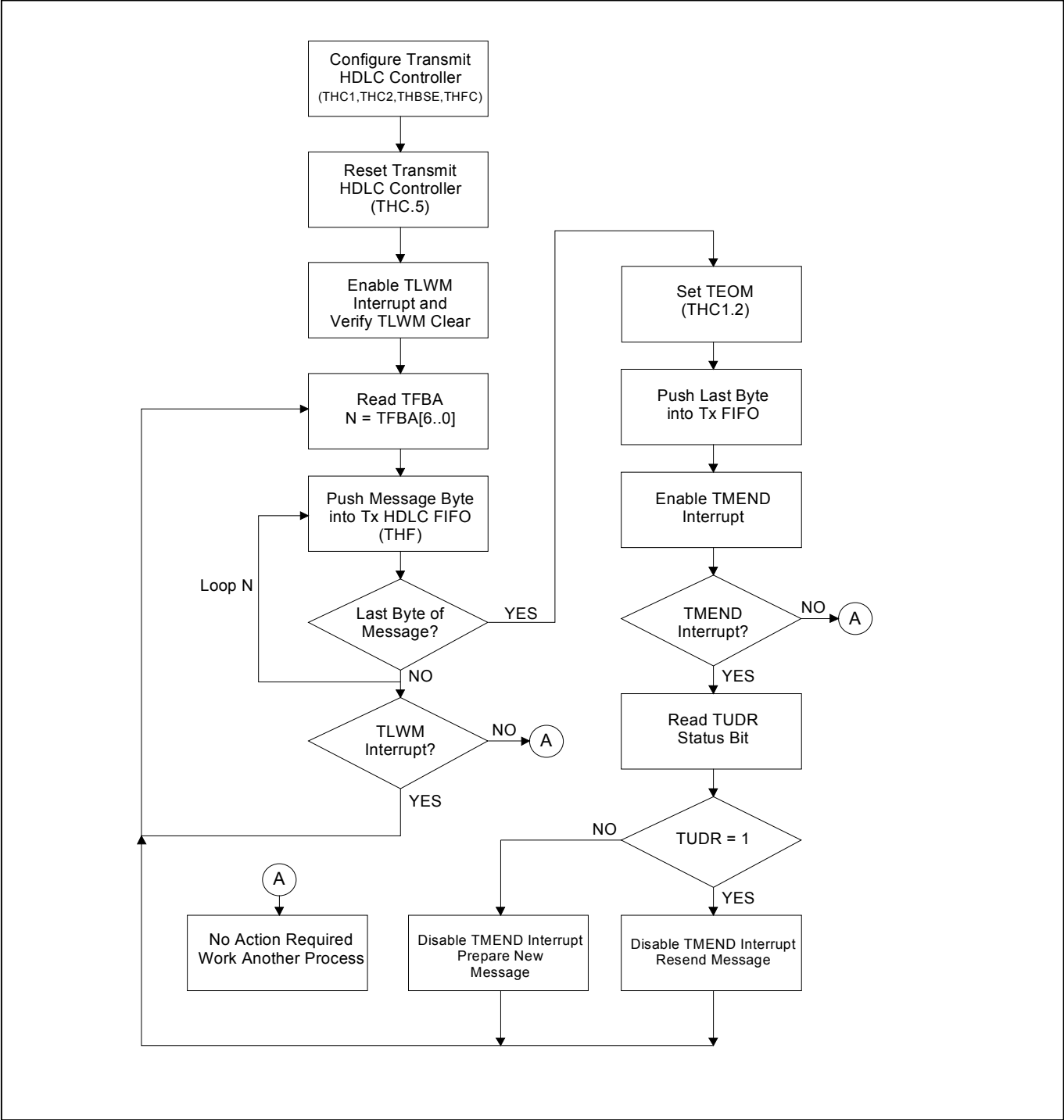
9.10.2.1 FIFO Information

The Transmit HDLC-64 FIFO Buffer Available Register ([TFBA](#)) indicates the number of bytes that can be written into the transmit FIFO. The count from this register informs the host as to how many bytes can be written into the transmit FIFO without overflowing the buffer. This is a real-time register. The count remains valid and stable during the read cycle.

9.10.2.2 Transmit HDLC-64 Example

The HDLC-64 status registers in the DS26518 allow for flexible software interface to meet the user's preferences. When transmitting HDLC-64 messages, the host can choose to be interrupt driven, or to poll to desired status registers, or a combination of polling and interrupt processes can be used. [Figure 9-18](#) shows an example routine for using the DS26518 HDLC-64 receiver.

Figure 9-18. Transmit HDLC-64 Message Example



9.10.3 HDLC-256 Controller

This device has an enhanced HDLC controller that can be mapped into up to 32 time slots, or Sa4 to Sa8 bits (E1 mode), or the FDL (T1 mode). This HDLC controller has a 256-byte FIFO buffer in both the transmit and receive paths. The user can select any specific bits within the time slot(s) to assign to the HDLC-256 controller as well as specific Sa bits (E1 mode).

The HDLC-256 controller performs all the necessary overhead for generating and receiving performance report messages (PRMs) as described in ANSI T1.403 and the messages as described in AT&T TR54016. The HDLC-256 controller automatically generates and detects flags, generates and checks the CRC checksum, generates and detects abort sequences, stuffs and destuffs zeros, and byte aligns to the data stream. The 256-byte buffers in the HDLC-256 controller are large enough to allow a full PRM to be received or transmitted without host intervention. They are also large enough to store an entire frame's worth of data before requiring host intervention.

[Table 9-38](#) shows the registers related to the HDLC-256.

Table 9-38. Registers Related to the HDLC-256

| REGISTER | FRAMER 1 ADDRESSES | FUNCTION |
|---|------------------------|---|
| Receive Expansion Port Control Register (HDLC-256) (RXPC) | 08Ah | Mapping of the HDLC-256 to time slots or FDL, Sa bits. |
| Receive HDLC-256 Channel Select Registers 1 to 4 (RHCS1 – RHCS4) | 0DCh, 0DDh, 0DEh, 0DFh | Selection of time slots to map data to the HDLC-256 port. |
| Receive HDLC-256 Bit Suppress Register (RHBS) | 08Dh | Receive HDLC-256 bit suppression register. |
| Receive HDLC-256 Control Register 1 (RH256CR1) | 1510h | Receive miscellaneous control. |
| Receive HDLC-256 Control Register 2 (RH256CR2) | 1511h | Receive HDLC-256 FIFO data level available. |
| Receive HDLC-256 Status Register (RH256SR) | 1514h | Indicates the FIFO status. |
| Receive HDLC-256 FIFO Data Registers 1 and 2 (RH256FDR1 and RH256FDR2) | 151Ch, 151Dh | The actual FIFO data. |
| Transmit Expansion Port Control Register (TXPC) | 18Ah | Mapping of the HDLC-256 to time slots or FDL, Sa bits. |
| Transmit HDLC-256 Channel Select Registers 1 to 4 (THCS1 – THCS4) | 1DCh, 1DDh, 1DEh, 1DFh | Selection of time slots to map data from the HDLC-256 port. |
| Transmit HDLC-256 Bit Suppress Register (THBS) | 18Dh | Transmit HDLC-256 bit suppress for bits not to be used. |
| Transmit HDLC-256 Control Register 1 (TH256CR1) | 1500h | Transmit miscellaneous control. |
| Transmit HDLC-256 Control Register 2 (TH256CR2) | 1501h | Indicates the number of bytes that can be written into the transmit FIFO. |
| Transmit HDLC-256 FIFO Data Registers 1 and 2 (TH256FDR1 and TH256FDR2) | 1502h, 1503h | Transmit HDLC-256 FIFO. |
| Transmit HDLC-256 Status Registers 1 and 2 (TH256SR1 and TH256SR2) | 1504h, 1505h | Indicates the real-time status of the transmit HDLC-256 FIFO. |

Note: The addresses shown are for Framer 1. Addresses for Framers 2 to 8 can be calculated using the following: Framer n = (Framer 1 address + $(n - 1) \times 200\text{hex}$); where $n = 2$ to 8 for Framers 2 to 8.

9.10.3.1 HDLC-256 FIFO Control

Control of the transmit and receive FIFOs is accomplished via the Receive HDLC-256 Control Register 2 ([RH256CR2](#)) and Transmit HDLC-256 Control Register 2 ([TH256CR2](#)). The FIFO control registers set the watermarks for the FIFO.

When the receive FIFO fills above the data available level, the RHDA bit ([RH256SR.0](#)) is set. RHDA and THDA are real-time bits and remain set as long as the FIFO's write pointer is above the data available level. When the transmit FIFO empties below the data storage available level, the THDA bit in the [TH256SR1](#) register is set. THDA is a real-time bit and remains set as long as the transmit FIFO's write pointer is below the level setting. If enabled, this condition can also cause an interrupt via the $\overline{\text{INTB}}$ pin.

If a packet start is received while the receive FIFO is full, the data is discarded and an FIFO overflow condition is declared ([RH256SRL.7](#)). If any other packet data is received while full, the current packet being transferred is marked with an abort indication, and a FIFO overflow condition is declared. Once an FIFO overflow condition is declared, the receive FIFO discards incoming data until a packet start is received while the receive FIFO has 16 or more bytes available for storage. If the receive FIFO is read while the FIFO is empty, the read is ignored and an invalid data indication given.

The transmit FIFO accepts data from the host until full. If the transmit FIFO is written to while the FIFO is full, the write is ignored, and an FIFO overflow condition is declared. If the transmit HDLC-256 controller attempts to read the transmit FIFO while it is empty, an FIFO underflow condition is declared.

The transmit FIFO fill level is available real-time in the Transmit HDLC-256 Status Register 2 ([TH256SR2](#)), indicating the number of bytes that can be written into the transmit FIFO.

9.10.3.2 HDLC-256 Status and Information

[RH256SRL](#), [RH256SR](#), [TH256SR1](#), [TH256SR2](#), and [TH256SRL](#) provide status information for the HDLC-256 controller. When a particular event has occurred (or is occurring), the appropriate bit in one of these registers is set to a 1. Some of the bits in these registers are latched and some are real-time bits that are not latched. This section contains register descriptions that list which bits are latched and which are real-time. With the latched bits, when an event occurs and a bit is set to a one, it remains set until the user reads and clears that bit. The bit is cleared when a 1 is written to the bit and it is not set again until the event has occurred again. The real-time bits report the current instantaneous conditions that are occurring and the history of these bits is not latched.

Like the other latched status registers, the user follows a read of the status bit with a write. The byte written to the register informs the device which of the latched bits the user wishes to clear (the real-time bits are not affected by writing to the status register). The user writes a byte to one of these registers, with a 1 in the bit positions he or she wishes to clear and a 0 in the bit positions he or she does not wish to clear.

The HDLC-256 status registers [RH256SRL](#) and [TH256SRL](#) can initiate a hardware interrupt via the $\overline{\text{INTB}}$ output signal. Each of the events in this register can be either masked or unmasked from the interrupt pin via the HDLC-256 interrupt enable registers, [TH256SR1E](#) and [RH256SR1E](#). Interrupts force the $\overline{\text{INTB}}$ signal low when the event occurs. The $\overline{\text{INTB}}$ pin is allowed to return high (if no other interrupts are present) when the user reads the event bit that caused the interrupt to occur.

9.10.3.3 Receive HDLC-256 Example

The HDLC-256 status registers in the DS26518 allow for flexible software interface to meet the user's preferences. When receiving HDLC-256 messages, the host can choose to be interrupt driven or to poll to desired status registers, or a combination of polling and interrupt processes can be used. [Figure 9-19](#) shows an example routine for using the DS26518 HDLC-256 receiver.

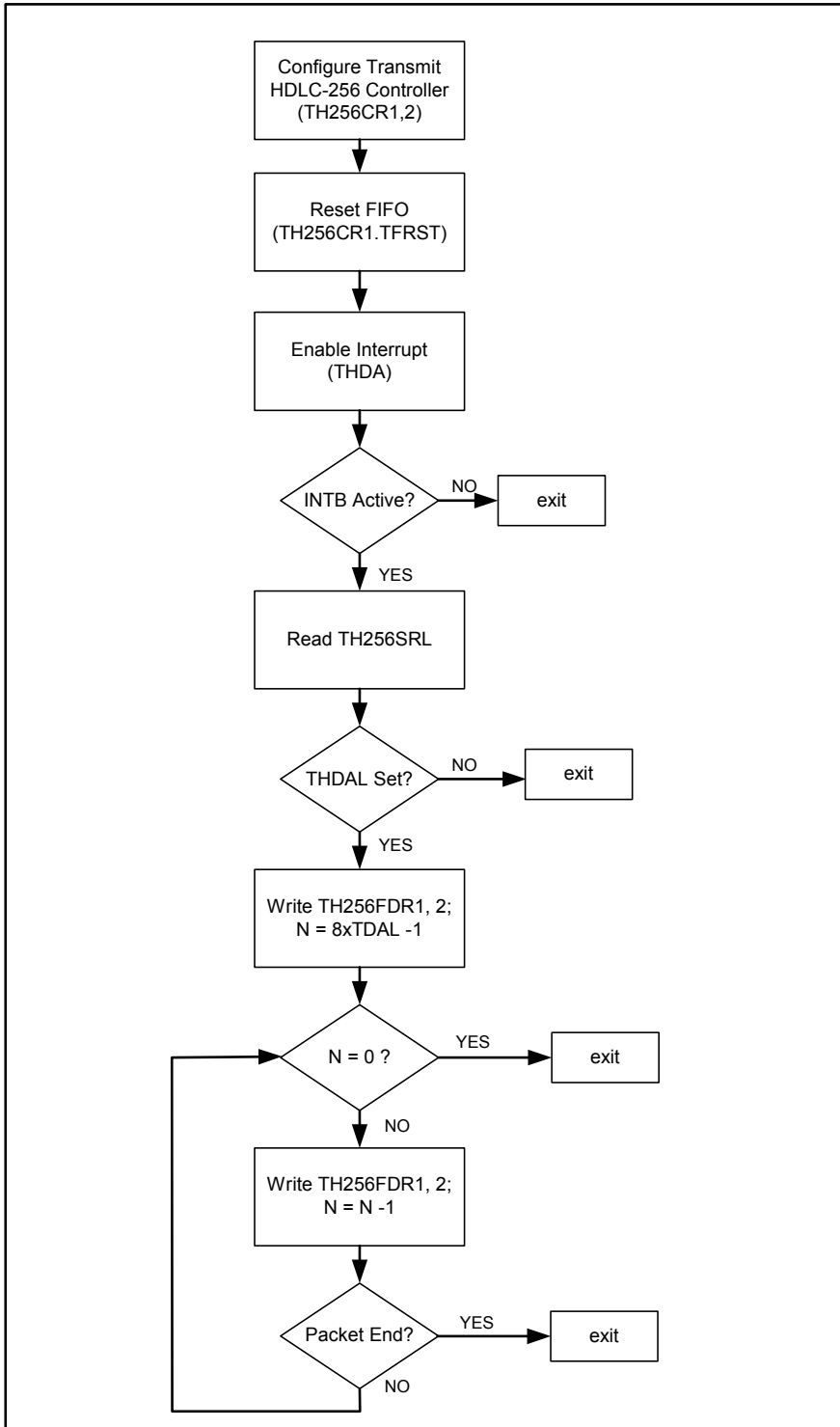
Figure 9-19. Receive HDLC-256 Message Example



9.10.3.4 Transmit HDLC-256 Example

The HDLC-256 status registers in the DS26518 allow for flexible software interface to meet the user's preferences. When transmitting HDLC-256 messages, the host can choose to be interrupt driven or to poll to desired status registers, or a combination of polling and interrupt processes can be used. [Figure 9-20](#) shows an example routine for using the DS26518 HDLC-256 receiver.

Figure 9-20. Transmit HDLC-256 Message Example



9.11 Power-Supply Decoupling

Table 9-39. Recommended Supply Decoupling

| SUPPLY PINS | DECOUPLING CAPACITANCE | NOTES |
|-------------|---|--|
| DVDD33/DVSS | $0.01\mu\text{F} + 0.1\mu\text{F} + 1\mu\text{F} + 10\mu\text{F}$ | — |
| DVDD18/DVSS | $0.01\mu\text{F} + 0.1\mu\text{F} + 1\mu\text{F} + 10\mu\text{F}$ | — |
| ATVDD/ATVSS | $0.1\mu\text{F} (x8) + 1\mu\text{F} (x4) + 10\mu\text{F} (x2)$ | It is recommended to use one $0.1\mu\text{F}$ capacitor for each ATVDD/ATVSS pair (8 total), one $1\mu\text{F}$ capacitor for every two ATVDD/ATVSS pairs (4 total), and two $10\mu\text{F}$ capacitors for the analog transmit supply pins. These capacitors should be located as close to the intended power pins as possible. |
| ARVDD/ARVSS | $0.1\mu\text{F} (x8) + 1\mu\text{F} (x4) + 10\mu\text{F} (x2)$ | It is recommended to use one $0.1\mu\text{F}$ capacitor for each ARVDD/ARVSS pair (8 total), one $1\mu\text{F}$ capacitor for every two ARVDD/ARVSS pairs (4 total), and two $10\mu\text{F}$ capacitors for the analog receive supply pins. These capacitors should be located as close to the intended power pins as possible. |
| ACVDD/ACVSS | $0.1\mu\text{F} + 1\mu\text{F} + 10\mu\text{F}$ | — |

9.12 Line Interface Units (LIUs)

The DS26518 has eight identical LIU transmit and receive front-ends for each of the eight framers. Each LIU contains three sections: the transmitter, which waveshapes and drives the network line; the receiver, which handles clock and data recovery; and the jitter attenuator. The DS26518 LIUs can switch between T1 or E1 networks without changing any external components on either the transmit or receive side. [Figure 9-21](#) shows a recommended circuit for software selected termination with protection. In this configuration the device can connect to 100 Ω T1 twisted pair, 110 Ω J1 twisted pair, 75 Ω or 120 Ω E1 twisted pair without additional component changes. The signals between the framer and LIU are not accessible by the user, thus the framer and LIU cannot be separated. The transmitters have fast high-impedance capability and can be individually powered down.

The DS26518's transmit waveforms meet the corresponding G.703 and T1.102 specifications. Internal software-selectable transmit termination is provided for 100 Ω T1 twisted pair, 110 Ω J1 twisted pair, 120 Ω E1 twisted pair and 75 Ω E1 coaxial applications. The receiver can connect to 100 Ω T1 twisted pair, 110 Ω J1 twisted pair, 120 Ω E1 twisted pair, and 75 Ω E1 coaxial. The receive LIU can function with a receive signal attenuation of up to 36dB for T1 mode and 43dB for E1 mode. The receiver sensitivity is programmable from 12dB to 43dB of cable loss. Also a monitor gain setting can be enabled to provide 14dB, 20dB, 26dB, and 32dB of resistive gain.

Figure 9-21. Network Connection—Longitudinal Protection



| NAME | DESCRIPTION | PART | MANUFACTURER | NOTES |
|----------------|---|------------|--------------------|---------|
| F1 to F4 | 1.25A Slow Blow Fuse | SMP 1.25 | Bel Fuse | 5 |
| | 1.25A Slow Blow Fuse | F1250T | Teccor Electronics | 5 |
| S1, S2 | 25V (max) Transient Suppressor | P0080SA MC | Teccor Electronics | 1, 5 |
| S3, S4, S5, S6 | 180V (max) Transient Suppressor | P1800SC MC | Teccor Electronics | 1, 4, 5 |
| S7, S8 | 40V (max) Transient Suppressor | P0300SC MC | Teccor Electronics | 1, 5 |
| T1 and T2 | Transformer 1:1CT and 1:2CT (3.3V, SMT) | PE-68678 | Pulse Engineering | 2, 3, 5 |
| T3 and T4 | Dual Common-Mode Choke (SMT) | PE-65857 | Pulse Engineering | 5 |
| R _T | Termination Resistor (120Ω, 110Ω, 100Ω, or 75Ω) | — | — | — |

- Note 1:** Changing S7 and S8 to P1800SC devices provides symmetrical voltage suppression between tip, ring, and ground.
- Note 2:** The layout from the transformers to the network interface is critical. Traces should be at least 25 mils wide and separated from other circuit lines by at least 150 mils. The area under this portion of the circuit should not contain power planes.
- Note 3:** Some T1 (never in E1) applications source or sink power from the network-side center taps of the Rx/Tx transformers.
- Note 4:** The ground trace connected to the S3/S4 pair and the S5/S6 pair should be at least 50 mils wide to conduct the extra current from a longitudinal power-cross event.
- Note 5:** Alternative component recommendations and line interface circuits can be found by contacting technical support at www.maxim-ic.com/support or in *Application Note 324*, which is available at www.maxim-ic.com/AN324.
- Note 6:** The 1μF capacitor in series with TTIPn is only necessary for G.703 clock sync applications.
- Note 7:** The 560pF on TTIPn/TRINGn must be tuned to your application.

9.12.1 LIU Operation

The analog AMI/HDB3 waveforms off of the E1 lines or the AMI/B8ZS waveform off of the T1 lines are transformer coupled into the RTIPn and RRINGn pins of the DS26518. The user has the option to use internal termination, software selectable for 75Ω/100Ω/110Ω/120Ω applications, or external termination. The LIU recovers clock and data from the analog signal and passes it through the jitter attenuation mux. The DS26518 contains an active filter that reconstructs the analog received signal for the nonlinear losses that occur in transmission. The receive circuitry also is configurable for various monitor applications. The device has a usable receive sensitivity of 0dB to -43dB for E1 and 0dB to -36dB for T1, which allows the device to operate on 0.63mm (22AWG) cables up to 2.5km (E1) and 6k feet (T1) in length. Data input to the transmit side of the LIU is sent via the jitter attenuation mux to the wave shaping circuitry and line driver. The DS26518 will drive the E1 or T1 line from the TTIPn and TRINGn pins via a coupling transformer. The line driver can handle both CEPT 30/ISDN-PRI lines for E1 and long-haul (CSU) or short-haul (DSX-1) lines for T1. The registers that control the LIU operation are shown in [Table 9-40](#).

Table 9-40. Registers Related to Control of the LIU

| REGISTER | FRAMER 1 ADDRESSES | FUNCTION |
|--|--------------------|---|
| Global Transceiver Clock Control Register 1 (GTCCR1) | 00F3h | MPS selections, backplane clock selections. |
| Global Software Reset Register 1 (GSRR1) | 00F6h | Software reset control for the LIU. |
| Global LIU Interrupt Status Register 1 (GLISR1) | 00FBh | Interrupt status bit for each of the eight LIUs. |
| Global LIU Interrupt Mask Register 1 (GLIMR1) | 00FEh | Interrupt mask register for the LIU. |
| LIU Transmit Receive Control Register (LTRCR) | 1000h | T1/J1/E1 selection, output tri-state, loss criteria. |
| LIU Transmit Impedance and Pulse Shape Selection Register (LTIPSR) | 1001h | Transmit pulse shape and impedance selection. |
| LIU Maintenance Control Register (LMCR) | 1002h | Transmit maintenance and jitter attenuation control register. |
| LIU Real Status Register (LRSR) | 1003h | LIU real-time status register. |
| LIU Status Interrupt Mask Register (LSIMR) | 1004h | LIU mask registers based on latched status bits. |
| LIU Latched Status Register (LLSR) | 1005h | LIU latched status bits related to loss, open circuit, etc. |
| LIU Receive Signal Level Register (LRSL) | 1006h | LIU receive signal level indicator. |
| LIU Receive Impedance and Sensitivity Monitor Register (LRISMR) | 1007h | LIU impedance match and sensitivity monitor. |

Note: The addresses shown above are for Framer 1. Addresses for Framers 2 to 8 can be calculated using the following: Framer n = (Framer 1 address + (n - 1) x 200hex), where n = 2 to 8 for Framers 2 to 8.

9.12.2 Transmitter

NRZ data arrives from the framer transmitter; the data is encoded with HDB3 or B8ZS or AMI. The encoded data passes through a jitter attenuator if it is enabled for the transmit path. A digital sequencer and DAC are used to generate transmit waveforms compliant with T1.102 and G.703 pulse templates.

A line driver is used to drive an internal matched impedance circuit for provision of 75 Ω , 100 Ω , 110 Ω , and 120 Ω terminations. A 560pF capacitor should be placed between TTIPn and TRINGn for each transmitter for proper operation, as noted in [Figure 9-21](#). The transmitter couples to the E1 or T1 transmit twisted pair (or coaxial cable in some E1 applications) via a 1:2 step-up transformer. In order for the device to create the proper waveforms, the transformer used must meet the specifications listed in [Table 9-42](#). The transmitter requires a transmit clock of 2.048MHz for E1 or 1.544MHz for T1/J1 operation.

The DS26518 drivers have a short-circuit and open-circuit detection driver-fail monitor. The TXENABLE pin can high impedance the transmitter outputs for protection switching. The individual transmitters can also be placed in high impedance through register settings. The DS26518 also has functionality for powering down the transmitters individually. The relevant telecommunications specification compliance is shown in [Table 9-41](#).

Table 9-41. Telecommunications Specification Compliance for DS26518 Transmitters

| TRANSMITTER FUNCTION | TELECOMMUNICATIONS COMPLIANCE |
|--|-------------------------------|
| T1 Telecom Pulse Template Compliance | ANSI T1.403 |
| T1 Telecom Pulse Template Compliance | ANSI T1.102 |
| Transmit Electrical Characteristics for E1 Transmission and Return Loss Compliance | ITU-T G.703 |

Table 9-42. Transformer Specifications

| SPECIFICATION | | RECOMMENDED VALUE |
|------------------------------------|-----------------------|--|
| Turns Ratio 3.3V Applications | | 1:1 (receive) and 1:2 (transmit) $\pm 2\%$ |
| Primary Inductance | | 600 μ H minimum |
| Leakage Inductance | | 1.0 μ H maximum |
| Intertwining Capacitance | | 40pF maximum |
| Transmit Transformer DC Resistance | Primary (Device Side) | 1.0 Ω maximum |
| | Secondary | 2.0 Ω maximum |
| Receive Transformer DC Resistance | Primary (Device Side) | 1.2 Ω maximum |
| | Secondary | 1.2 Ω maximum |

9.12.2.1 Transmit-Line Pulse Shapes

The DS26518 transmitters can be selected individually to meet the pulse templates for E1 and T1/J1 modes. The T1/J1 pulse template is shown in [Figure 9-22](#). The E1 pulse template is shown in [Figure 9-23](#). The transmit pulse shape can be configured for each LIU on an individual basis. The LIU transmit impedance selection registers can be used to select an internal transmit terminating impedance of 100Ω for T1, 110Ω for J1 mode, 75Ω or 120Ω for E1 mode or no internal termination for E1 or T1 mode. The transmit pulse shape and terminating impedance is selected by [LTIPSR](#) registers. The pulse shapes will be compliant to T1.102 and G.703. Pulse shapes are measured for compliance at the appropriate network interface (NI). For T1 long haul and E1, the pulse shape is measured at the far end. For T1 short haul, the pulse shape is measured at the near end.

Figure 9-22. T1/J1 Transmit Pulse Templates

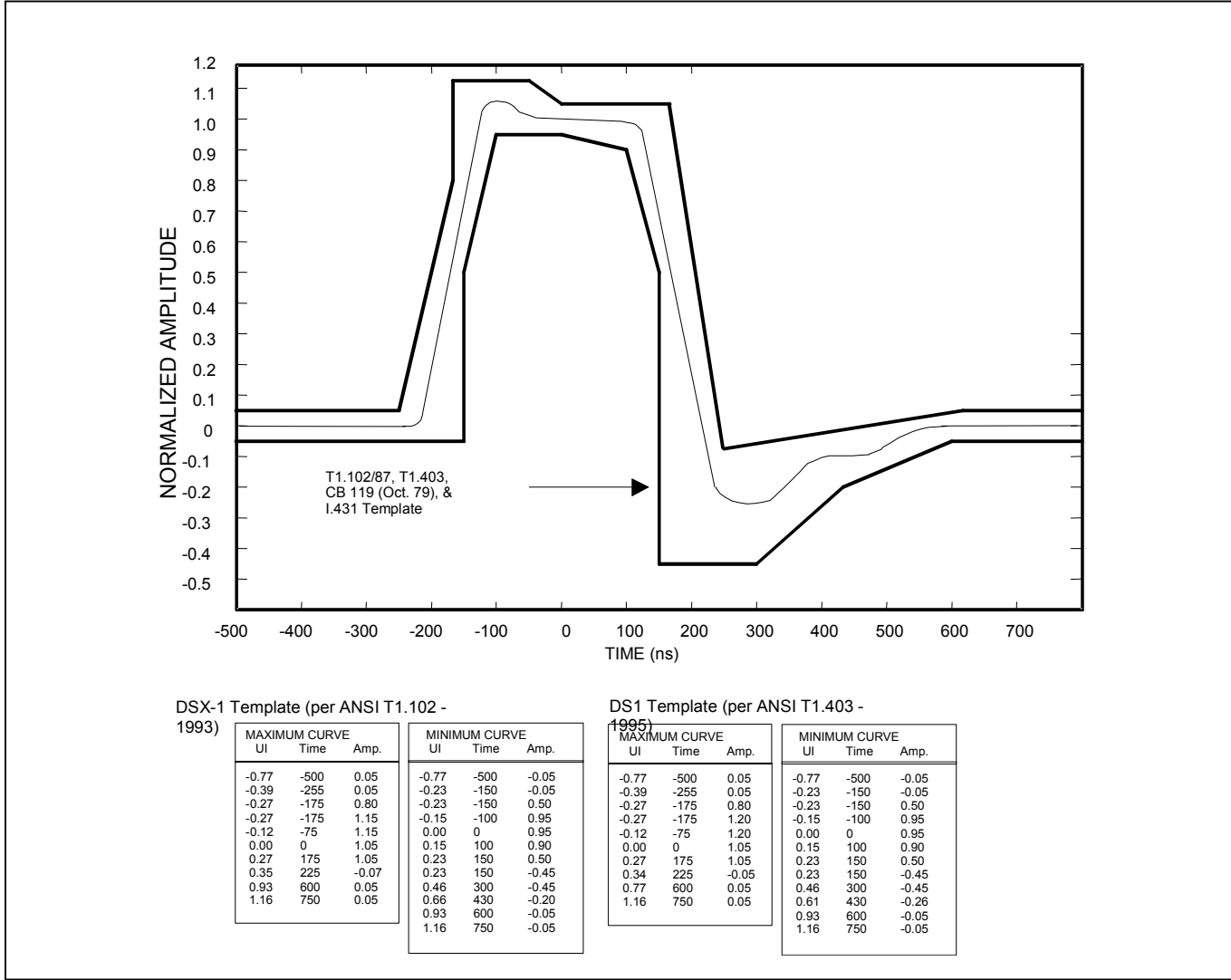


Figure 9-23. E1 Transmit Pulse Templates



9.12.2.2 Transmit G.703 Section 10 Synchronization Signal

The DS26518 can transmit a 2.048MHz square-wave synchronization clock as specified in Section 10 of ITU-T G.703. To use this mode, set the transmit G.703 synchronization clock bit (TG703) found in the LIU Transmit Impedance and Pulse Shape Selection Register ([LTIPSR](#)). This mode also requires a 1 μ F blocking capacitor between TTIPn and the transformer. Additionally, the following registers should be set to center the pulse to meet the pulse template:

If configuring for E1 75 Ω mode, set register address 0x1229 = 0xF8.

If configuring for E1 120 Ω mode, set register addresses 0x1229 = 0xF8 and 0x122D = 0x09.

9.12.2.3 Transmit Power-Down

The individual transmitters can be powered down by setting the TPDE bit in the LIU Maintenance Control Register ([LMCR](#)). Note that powering down the transmit LIU results in a high-impedance state for the corresponding TTIPn and TRINGn pins.

When transmit all ones (AIS) is invoked, continuous ones are transmitted using MCLK as the timing reference. Data input from the framer is ignored. AIS can be sent by setting a bit in the [LMCR](#) register. Transmit all ones will also be sent if the corresponding receiver goes into LOS state and the ATAIS bit is set in the [LMCR](#) register.

9.12.2.4 Transmit Short-Circuit Detector/Limiter

Each transmitter has an automatic short-circuit current limiter that activates when the load resistance is approximately 25 Ω or less. TSCS ([LRSR.2](#)) provides a real-time indication of when the current limiter is activated. The LIU Latched Status Register ([LLSR](#)) provides latched versions of the information, which can be used to activate an interrupt when enable via the [LSIMR](#) register.

9.12.2.5 Transmit Open-Circuit Detector

The DS26518 can also detect when the TTIPn or TRINGn outputs are open circuited. OCS ([LRSR.1](#)) will provide a real-time indication of when an open circuit is detected. Register [LLSR](#) provides latched versions of the information, which can be used to activate an interrupt when enabled via the [LSIMR](#) register. The open-circuit-detect feature is not available in T1 CSU operating modes (LBO 5, LBO 6, and LBO 7).

9.12.3 Receiver

9.12.3.1 Receive Internal Termination

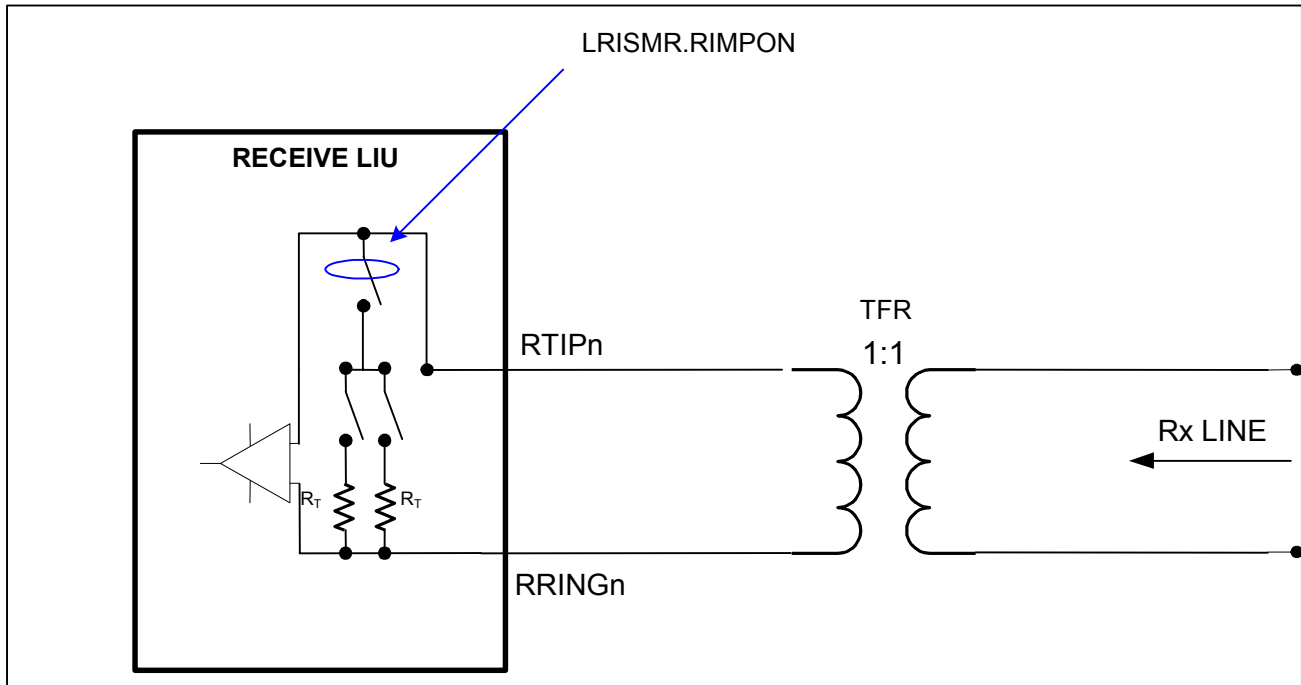
The DS26518 contains eight receivers. The termination circuit provides an analog switch that powers up in the open setting, providing high impedance to the receive line side. This is useful for redundancy applications and hot swapability.

Three termination methods are available:

- Partially internal impedance match with 120 Ω external resistor.
- Fully internal impedance match, no external resistor.
- External resistor termination, internal termination disabled.

See the [LRISMR](#) register for more details. Internal impedance match is configurable to 75 Ω , 100 Ω , 110 Ω , or 120 Ω termination by setting the appropriate RIMPM[1:0] bits. These bits must be configured to match line impedance even if internal termination is disabled.

[Figure 9-24](#) shows a diagram of the switch control of termination. If internal impedance match is disabled, the external resistor, R_T , must match the line impedance.

Figure 9-24. Receive LIU Termination Options

The device couples to the receive E1 or T1 twisted pair (or coaxial cable in 75Ω E1 applications) via a 1:1 or 2:1 transformer. See [Table 9-42](#) for transformer details.

Receive sensitivity is configurable by setting the appropriate RSMS[1:0] bits ([LRCR](#)).

The DS26518 uses a digital clock recovery system. The resultant E1, T1 or J1 clock derived from MCLK is multiplied by 16 via an internal PLL and fed to the clock recovery system. The clock recovery system uses the clock from the PLL circuit to form a 16 times oversampler, which is used to recover the clock and data. This oversampling technique offers outstanding performance to meet jitter tolerance specifications shown in [Figure 9-27](#).

Normally, the clock that is output at the RCLKn pin is the recovered clock from the E1 AMI/HDB3 or T1 AMI/B8ZS waveform presented at the RTIPn and RRINGn inputs. If the jitter attenuator ([LTRCR](#)) is placed in the receive path (as is the case in most applications), the jitter attenuator restores the RCLKn to an approximate 50% duty cycle. If the jitter attenuator is either placed in the transmit path or is disabled, the RCLKn output can exhibit slightly shorter high cycles of the clock. This is due to the highly over-sampled digital clock recovery circuitry. See [Table 13-3](#) for more details. When no signal is present at RTIPn and RRINGn, a receive carrier loss (RCL) condition will occur and the RCLKn will be derived from the MCLKT1 or MCLK E1 source (depending on the configuration).

9.12.3.2 Receive Level Indicator

The DS26518 will report the signal strength at RTIPn and RRINGn in approximately 2.5dB increments via RSL[3:0] located in the LIU Receive Signal Level Register ([LRSL](#)). This feature is helpful when trouble shooting line performance problems.

9.12.3.3 Receive G.703 Section 10 Synchronization Signal

The DS26518 can receive a 2.048MHz square-wave synchronization clock as specified in Section 10 of ITU-T G.703. To use this mode, set the receive G.703 clock bit (RG703) found in the LIU Receive Control Register ([LRCR.7](#)).

9.12.3.4 Receiver Monitor Mode

The receive equalizer is equipped with a monitor mode function that is used to overcome the signal attenuation caused by the resistive bridge used in monitoring applications. This function allows for a resistive gain of up to 32dB along with cable attenuation of 12dB to 30dB as shown in the LIU Receive Control Register ([LRCR](#)).

Figure 9-25. Typical Monitor Application



9.12.3.5 Loss of Signal

The DS26518 uses both the digital and analog loss-detection method in compliance with the latest T1.231 for T1/J1 and ITU-T G.775 or ETS 300 233 for E1 mode of operation.

LOS is detected if the receiver level falls below a threshold analog voltage for certain duration. Alternatively, this can be termed as having received “zeros” for a certain duration. The signal level and timing duration are defined in accordance with the T1.231 or G.775 or ETS 300 233 specifications.

For short-haul mode, the loss-detection thresholds are based on cable loss of 12dB to 18dB for both T1/J1 and E1 modes. The loss thresholds are selectable based on [Table 10-22](#). For long-haul mode, the LOS-detection threshold is based on cable loss of 30dB to 38dB for T1/J1 and 30dB to 45dB for E1 mode. Note there is no explicit bit called short-haul mode selection. Loss declaration level is set at 3dB lower than the maximum sensitivity setting programmed in [Table 10-22](#).

The loss state is exited when the receiver detects a certain ones density at the maximum sensitivity level or higher, which is 3dB higher than the loss-detection level. The loss-detection signal level and loss-reset signal level are defined with hysteresis to prevent the receiver from bouncing between “LOS” and “no LOS” states. [Table 9-43](#) outlines the specifications governing the loss function.

Table 9-43. T1.231, G.775, and ETS 300 233 Loss Criteria Specifications

| CRITERIA | STANDARD | | |
|----------------|---|--|---|
| | T1.231 | ITU-T G.775 | ETS 300 233 |
| Loss Detection | No pulses are detected for 175 \pm 75 bits. | No pulses are detected for duration of 10 to 255 bit periods. | No pulses are detected for a duration of 2048 bit periods or 1ms. |
| Loss Reset | Loss is terminated if a duration of 12.5% ones are detected over duration of 175 \pm 75 bits. Loss is not terminated if 8 consecutive zeros are found if B8ZS encoding is used. If B8ZS is not used, loss is not terminated if 100 consecutive pulses are zero. | The incoming signal has transitions for duration of 10 to 255 bit periods. | Loss reset criteria is not defined. |

9.12.3.6 ANSI T1.231 for T1 and J1 Modes

For short-haul mode, loss is declared if the received signal level is 3dB lower from the programmed value (based on [Table 10-22](#)) for a duration of 192-bit periods. Hence, if the sensitivity is programmed to be 12dB, loss is declared at 15dB.

LOS is reset if all the following criteria are met:

- 1) 24 or more ones are detected in a 192-bit period with a programmed sensitivity level measured at RTIPn and RRINGn.
- 2) During the 192 bits, fewer than 100 consecutive zeros are detected.

For long-haul mode, loss is detected if the received signal level is 3dB lower from the programmed value (based on [Table 10-22](#)) for a duration of 192-bit periods. Hence, if the sensitivity is programmed to be 30dB, the loss declaration level is 33dB.

LOS is reset if all the following criteria are met:

- 1) 24 or more ones are detected in a 192-bit period with a programmed sensitivity level measured at RTIPn and RRINGn.
- 2) During the 192 bits, fewer than 100 consecutive zeros are detected.

9.12.3.7 ITU-T G.775 for E1 Modes

For short-haul mode, loss is declared if the received signal level is 3dB lower from the programmed value (based on [Table 10-22](#)) for a duration of 192-bit periods. Hence, if the sensitivity is programmed to be 12dB, loss is declared at 15dB. LOS is reset if the receive signal level is greater than or equal to the programmed sensitivity level for a duration of 192-bit periods.

For long-haul mode, loss is detected if the received signal level is 3dB lower from the programmed value (based on [Table 10-22](#)) for a duration of 192-bit periods. Hence, if the sensitivity is programmed to be 30dB, the loss declaration level is 15dB. LOS is reset if the receive signal level is greater than or equal to the programmed sensitivity level for a duration of 192-bit periods.

9.12.3.8 ETS 200 233 for E1 Modes

For short-haul mode, loss is declared if the received signal level is 3dB lower from the programmed value (based on [Table 10-22](#)) continuous duration of 2048-bit periods (1ms). LOS is reset if the receive signal level is greater than or equal to the programmed sensitivity level for a duration of 192-bit periods.

For long-haul mode, loss is declared if the received signal level is 3dB lower from the programmed value (based on [Table 10-22](#)) continuous duration of 2048-bit periods (1ms). LOS is reset if the receive signal level is greater than or equal to the programmed sensitivity level for a duration of 192-bit periods.

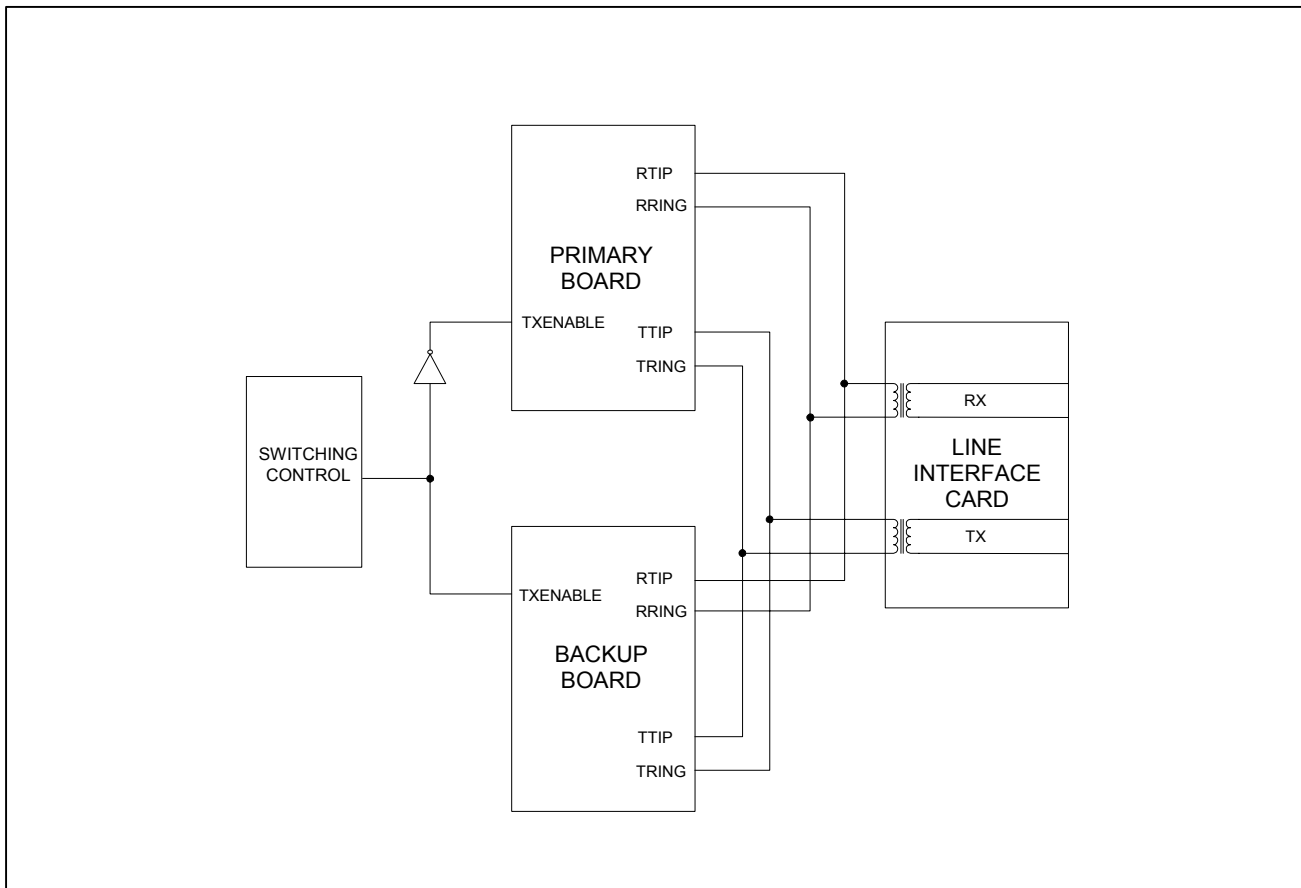
9.12.4 Hitless Protection Switching (HPS)

Many current redundancy protection implementations use mechanical relays to switch between primary and backup boards. The switching time in relays is typically in the milliseconds, making T1/E1 HPS impossible. The switching event will likely cause frame-synchronization loss in any equipment downstream, affecting the quality of service. The same is also true for tri-stating mechanisms that use software or inactive clocks for the triggering of HPS.

The DS26518 LIUs feature fast tristatable outputs for TTIP_n and TRING_n and fast disabling of internal impedance matching for RTIP_n and RRING_n within one-bit period. The TXENABLE pin is used for hitless protection circuits in combination with the [LTRCR.RHPM](#) bit. When low, the TXENABLE pin tri-states all eight transmitters, providing a high-impedance state on TTIP_n and TRING_n. If the RHPM bit is set, the TXENABLE pin, when low, will also disable the internal termination on RTIP_n and RRING_n on a per-port basis, providing a high impedance to the receive line.

This is a very useful function in that control can be done through a hardware pin, allowing a quick switch to the backup system for both the receiver and the transmitter. [Figure 9-26](#) shows a typical HPS application.

Figure 9-26. HPS Block Diagram



9.12.5 Jitter Attenuator

Each LIU contains a jitter attenuator that can be set to a depth of 32 or 128 bits via the JADS bits in the LIU Transmit and Receive Control Register ([LTRCR](#)).

The 128-bit mode is used in applications where large excursions of wander are expected. The 32-bit mode is used in delay sensitive applications. The characteristics of the attenuation are shown in [Figure 9-27](#). The jitter attenuator can be placed in either the receive path or the transmit path, or be disabled by appropriately setting the JAPS1 and JAPS0 bits in the LIU Transmit and Receive Control Register ([LTRCR](#)).

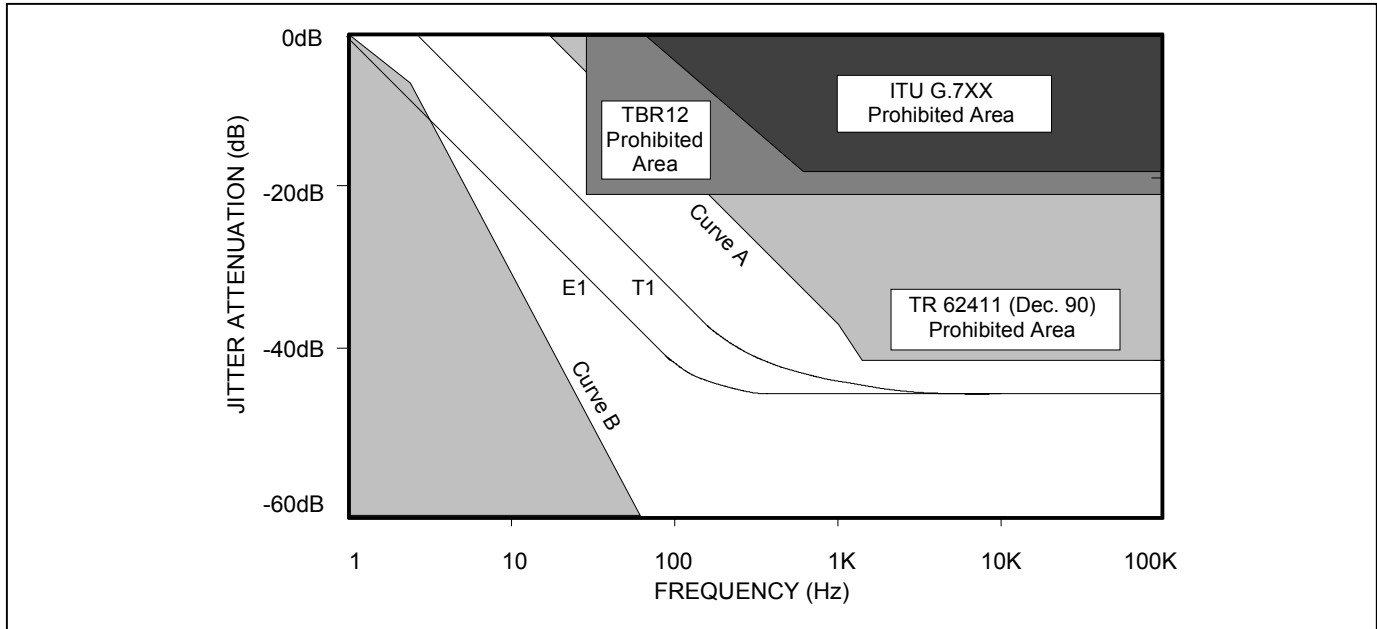
For the jitter attenuator to operate properly, a 2.048MHz, 1.544MHz, or a multiple of up to 8x clock must be applied at MCLK. See the Global Transceiver Clock Control Register 1 ([GTCCR1](#)) for MCLK options. ITU-T specification G.703 requires an accuracy of $\pm 50\text{ppm}$ for both T1/J1 and E1 applications. TR62411 and ANSI specs require an accuracy of $\pm 32\text{ppm}$ for T1/J1 interfaces. Circuitry adjusts either the recovered clock from the clock/data recovery block or the clock applied at the TCLKn pin to create a smooth jitter-free clock, which is used to clock data out of the jitter attenuator FIFO. It is acceptable to provide a gapped/bursty clock at the TCLKn pin if the jitter attenuator is placed in the transmit side. If the incoming jitter exceeds either $120U_{I_{P-P}}$ (buffer depth is 128-bits) or $28U_{I_{P-P}}$ (buffer depth is 32 bits), then the DS26518 will set the jitter attenuator limit trip (JALTS) bit in the LIU Latched Status Register ([LLSR.3](#)). In T1/J1 mode, the jitter attenuator corner frequency is 3.75Hz, and in E1 mode it is 0.6Hz.

The DS26518 jitter attenuator is compliant with the following specifications shown in [Table 9-44](#).

Table 9-44. Jitter Attenuator Standards Compliance

| |
|------------------------------------|
| Standard |
| ITU-T I.431, G.703, G.736, G.823 |
| ETS 300 011, TBR 12/13 |
| AT&T TR62411, TR43802 |
| TR-TSY 009, TR-TSY 253, TR-TSY 499 |

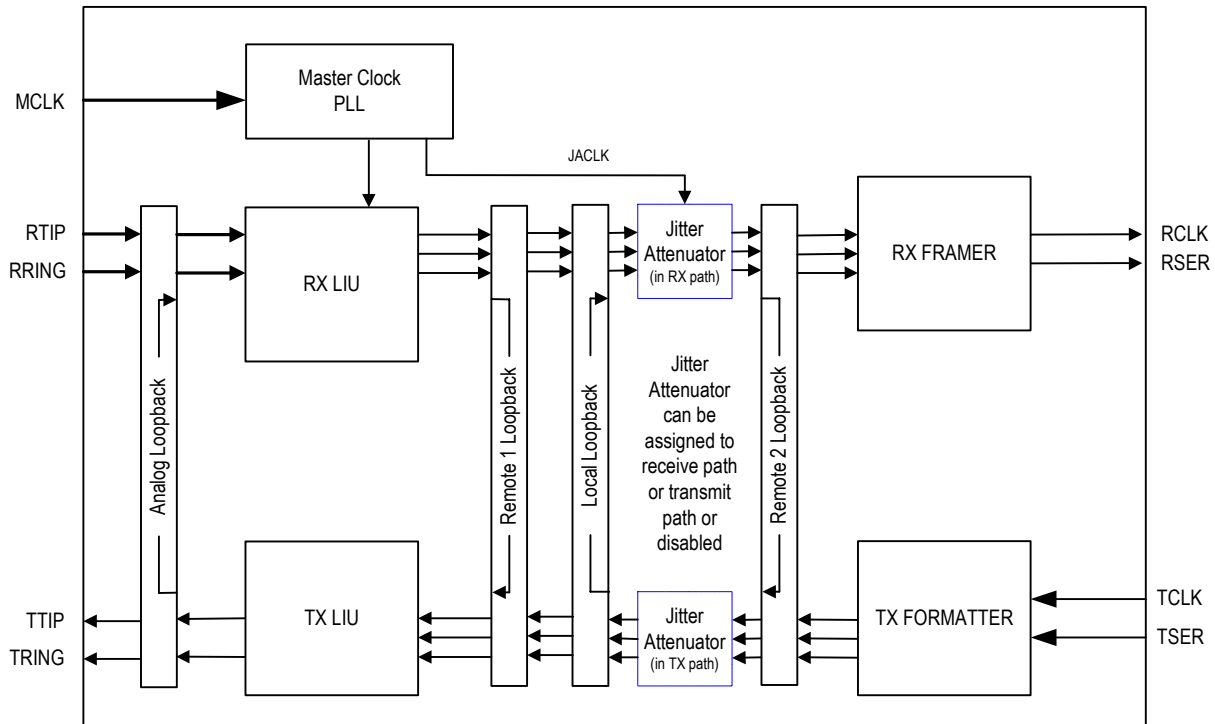
Figure 9-27. Jitter Attenuation



9.12.6 LIU Loopbacks

The DS26518 provides four LIU loopbacks for diagnostic purposes: Analog Loopback, Local Loopback, Remote Loopback 1, and Remote Loopback 2. Dual Loopback is a combination of Local Loopback and Remote Loopback 1. In the loopback diagrams that follow, TSERn, TCLKn, RSERn, and RCLKn are inputs/outputs from the framer.

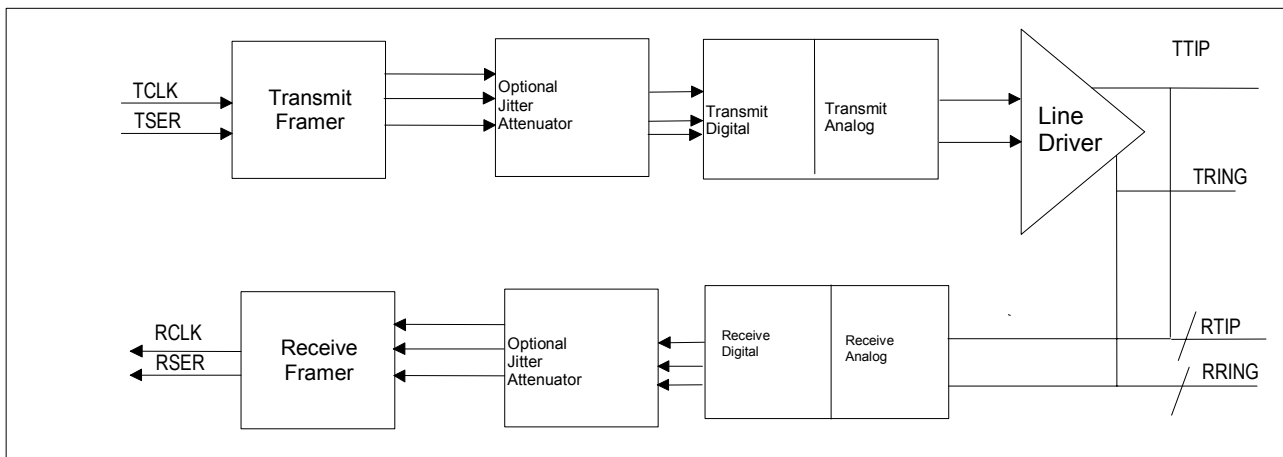
Figure 9-28. Loopback Diagram



9.12.6.1 Analog Loopback

The analog output of the transmitter TTIPn and TRINGn is looped back to RTIPn and RRINGn of the receiver. Data at RTIPn and RRINGn is ignored in analog loopback. This is shown in the [Figure 9-29](#).

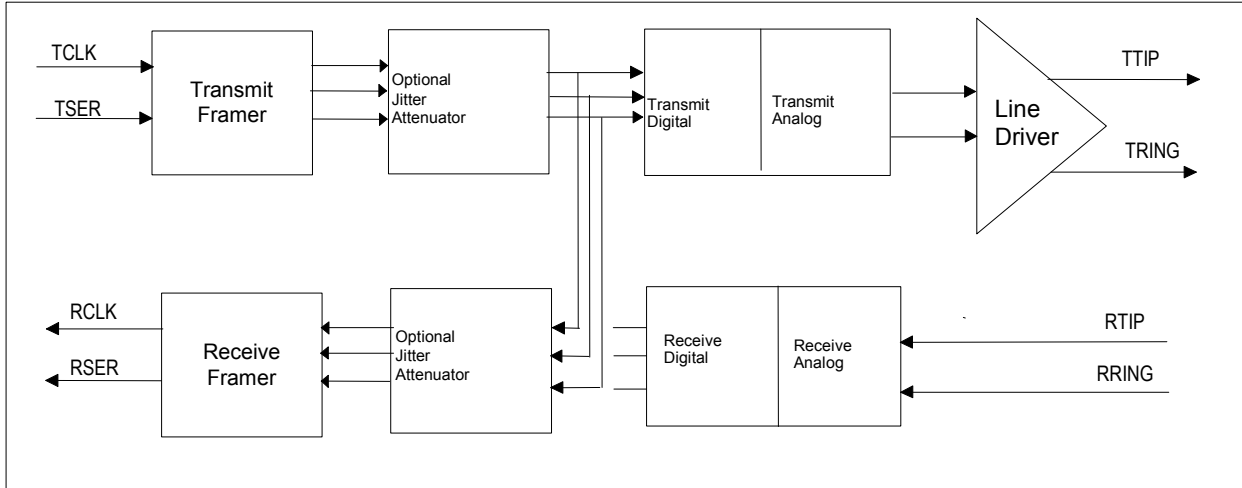
Figure 9-29. Analog Loopback



9.12.6.2 Local Loopback

The transmit system data is looped back to the receive framer. This data is also encoded and output on TTIPn and TRINGn. Signals at RTIPn and RRINGn are ignored. This loopback is conceptually shown in [Figure 9-30](#).

Figure 9-30. Local Loopback



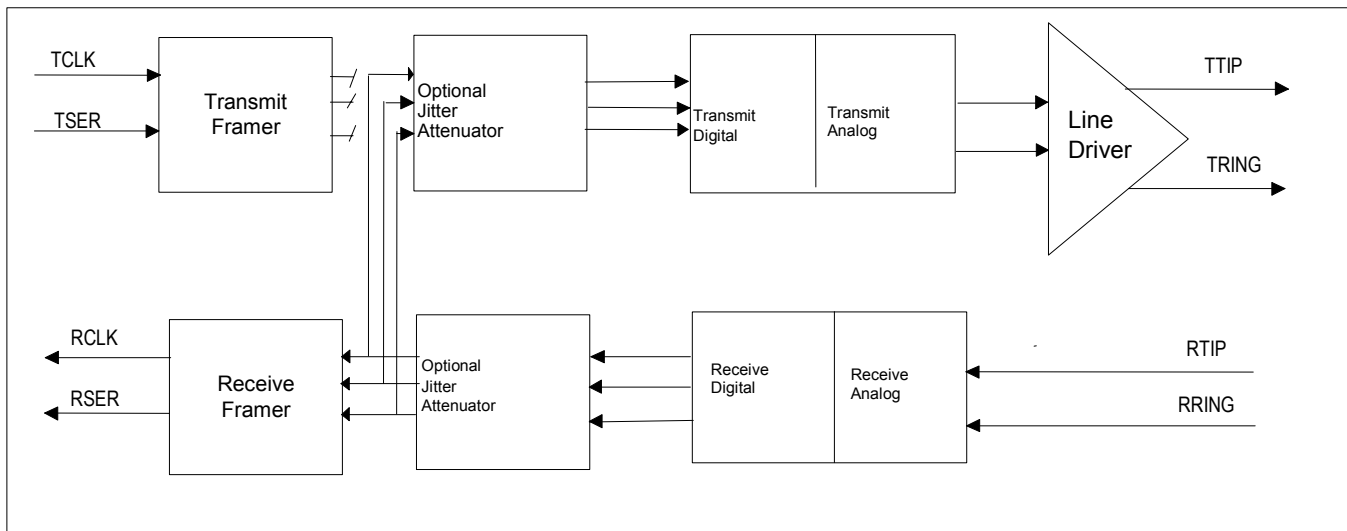
9.12.6.3 Remote Loopback 1

The outputs decoded from the receive LIU are looped back to the transmit LIU, not including the jitter attenuator in the path. Remote Loopback 2 includes the jitter attenuator in the loopback path. The inputs from the transmit framer are ignored during Remote Loopback 1.

9.12.6.4 Remote Loopback 2

The outputs decoded from the receive LIU are looped back to the transmit LIU, including the jitter attenuator. The inputs from the transmit framer are ignored during Remote Loopback 2. This loopback is conceptually shown in [Figure 9-31](#).

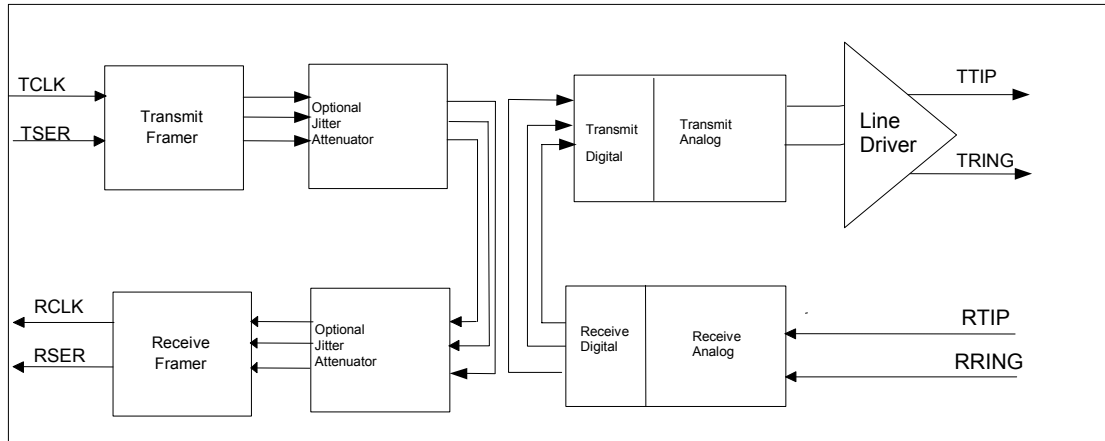
Figure 9-31. Remote Loopback 2



9.12.6.5 Dual Loopback

The inputs decoded from the receive LIU are looped back to the transmit LIU. The inputs from the transmit framer are looped back to the receiver with the optional jitter attenuator. Dual Loopback is a combination of Local Loopback and Remote Loopback 1. This loopback is invoked by setting the correct bits in the LIU Maintenance Control Register ([LMCR](#)). This loopback is conceptually shown in [Figure 9-32](#).

Figure 9-32. Dual Loopback



9.13 Bit Error-Rate Test Function (BERT)

The BERT (Bit Error Rate Tester) block can generate and detect both pseudorandom and repeating bit patterns. It is used to test and stress data-communication links. BERT functionality is dedicated for each of the transceivers. The registers related to the configure, control, and status of the BERT are shown in [Table 9-45](#).

Table 9-45. Registers Related to Configure, Control, and Status of BERT

| REGISTER | FRAMER 1 ADDRESSES | FUNCTION |
|--|------------------------|--|
| Global BERT Interrupt Status Register 1 (GBISR1) | 00FAh | When any of the 8 BERTs issue an interrupt, a bit is set. |
| Global BERT Interrupt Mask Register 1 (GBIMR1) | 00FDh | When any of the 8 BERTs issue an interrupt, a bit is set. |
| Receive Expansion Port Control Register (RXPC) | 08Ah | Enable for the receiver BERT. |
| Receive BERT Port Bit Suppress Register (RBPBS) | 08Bh | Bit suppression for the receive BERT. |
| Receive BERT Port Channel Select Registers 1 to 4 (RBPCS1–RBPCS4) | 0D4h, 0D5h, 0D6h, 0D7h | Channels to be enabled for the framer to accept data from the BERT pattern generator. |
| Transmit Expansion Port Control Register (TXPC) | 18Ah | Enable for the transmitter BERT. |
| Transmit BERT Port Bit Suppress Register (TBPBS) | 18Bh | Bit suppression for the transmit BERT. |
| Transmit BERT Port Channel Select Registers 1 to 4 (TBPCS1–TBPCS4) | 1D4h, 1D5h, 1D6h, 1D7h | Channels to be enabled for the framer to accept data from the transmit BERT pattern generator. |
| BERT Alternating Word Count Rate Register (BAWC) | 1100h | BERT alternating pattern count register. |
| BERT Repetitive Pattern Set Register 1 (BRP1) | 1101h | BERT repetitive pattern set register 1. |
| BERT Repetitive Pattern Set Register 2 (BRP2) | 1102h | BERT repetitive pattern set register 2. |
| BERT Repetitive Pattern Set Register 3 (BRP3) | 1103h | BERT repetitive pattern set register 3. |
| BERT Repetitive Pattern Set Register 4 (BRP4) | 1104h | BERT repetitive pattern set register 4. |
| BERT Control Register 1 (BC1) | 1105h | Pattern selection and misc control. |
| BERT Control Register 2 (BC2) | 1106h | BERT bit pattern length control. |
| BERT Bit Count Register 1 (BBC1) | 1107h | Increments for BERT bit clocks. |
| BERT Bit Count Register 2 (BBC2) | 1108h | BERT bit counter. |
| BERT Bit Count Register 3 (BBC3) | 1109h | BERT bit counter. |
| BERT Bit Count Register 4 (BBC4) | 110Ah | BERT bit counter. |
| BERT Error Count Register 1 (BEC1) | 110Bh | BERT error counter. |
| BERT Error Count Register 2 (BEC2) | 110Ch | BERT error counter. |
| BERT Error Count Register 3 (BEC3) | 110Dh | BERT error counter. |
| BERT Status Register (BSR) | 110Eh | Denotes synchronization loss and other status. |
| BERT Status Interrupt Mask Register (BSIM) | 110Fh | BERT interrupt mask. |
| BERT Control Register 3 (BC3) | 1400h | Pattern selection and misc control. |
| BERT Real-Time Status Register (BRSR) | 1401h | Denotes synchronization loss and other status. |
| BERT Latched Status Register 1 (BLSR1) | 1402h | Denotes synchronization loss and other status. |
| BERT Status Interrupt Mask Register 1 (BSIM1) | 1403h | BERT interrupt mask. |
| BERT Latched Status Register 2 (BLSR2) | 1404h | BERT error status. |
| BERT Status Interrupt Mask Register 2 (BSIM2) | 1405h | BERT interrupt mask. |

Note: The addresses shown above are for Framer 1. Addresses for Framers 2 to 8 can be calculated using the following: Framer N = (Framer 1 address + (n - 1) x 200hex); where n = 2 to 8 for Framers 2 to 8.

The BERT block can generate and detect the following patterns:

- The pseudorandom patterns 2E7-1, 2E9-1, 2E11-1, 2E15-1, and QRSS.
- A repetitive pattern from 1 to 32 bits in length.
- Alternating (16-bit) words that flip every 1 to 256 words.
- Daly pattern (modified 55 Octet pattern), 55 Octet pattern.

The BERT function must be enabled and configured in the [TXPC](#) and [RXPC](#) registers for each port. The BERT can then be assigned on a per-channel basis for both the transmitter and receiver, using the special per-channel function in the [TBPCS1-4](#) and [RBCS1-4](#) registers. Individual bit positions within the channels can be suppressed with the [TBPBS](#) and [RBPBS](#) registers. Using combinations of these functions, the BERT pattern can be transmitted and/or received in single or across multiple DS0s, contiguous or broken. Transmit and receive bandwidth assignments are independent of each other.

The BERT receiver has a 32-bit bit counter and a 24-bit error counter. The BERT receiver can generate interrupts on: a change in receive-synchronizer status, receive all zeros, receive all ones, error counter overflow, bit counter overflow, and bit error detection. Interrupts from each of these events can be masked within the BERT function via the BERT Status Interrupt Mask Register ([BSIM](#)). If the software detects that the BERT has reported an event, then the software must read the BERT Status Register ([BSR](#)) to determine which event(s) has occurred.

Beginning with die revision B1, the DS26518 has a new set of BERT registers to complement the original registers. These are located at 1400 hex. Additional features were added to support the 55 Octet pattern and the ability to byte-align to the DS0 time slot. In addition, a new set of status registers was added that is intended to replace the original status registers. The user now has the option to use either set of status registers, but it is recommended that he/she use the new ones as they are more complete and easier to use. The BERT Real-Time Status Register ([BRSR](#)) was added to provide better visibility of the status of the BERT.

9.13.1 BERT Repetitive Pattern Set

These registers must be properly loaded for the BERT to generate and synchronize to a repetitive pattern, a pseudorandom pattern, alternating word pattern, or a Daly pattern. For a repetitive pattern that is fewer than 32 bits, the pattern should be repeated so that all 32 bits are used to describe the pattern. For example, if the pattern was the repeating 5-bit pattern ...01101... (where the rightmost bit is the one sent first and received first), then BRP1 should be loaded with ADh, BRP2 with B5h, BRP3 with D6h, and BRP4 should be loaded with 5Ah. For a pseudo-random pattern, all four registers should be loaded with all ones (i.e., FFh). For an alternating word pattern, one word should be placed into BRP1 and BRP2 and the other word should be placed into BRP3 and BRP4. For example, if the DDS stress pattern "7E" is to be described, the user would place 00h in BRP1, 00h in BRP2, 7Eh in BRP3, and 7Eh in BRP4, and the alternating word counter would be set to 50 (decimal) to allow 100 bytes of 00h followed by 100 bytes of 7Eh to be sent and received.

9.13.2 BERT Error Counter

Once BERT has achieved synchronization, this 24-bit counter will increment for each data bit received in error. Toggling the LC control bit in BC1 can clear this counter. This counter saturates when full and will set the BECO status bit in the [BSR](#) register.

10. DEVICE REGISTERS

Thirteen address bits are used to control the settings of the registers. The registers control functions of the framers, LIUs, and BERTs within the DS26518. The map is divided into eight framers, followed by eight LIUs and eight BERTs. Global registers (applicable to all eight transceivers and BERTs) are located within the address space of Framer 1.

The register details are provided in the following tables. The framer registers bits are provided for Framer 1 and address bits A[12:8] determine the framer addressed.

10.1 Register Listings

The framer registers have an offset of 200 hex, the LIU registers have an offset of 20 hex, and the BERT registers have an offset of 10 hex for each transceiver.

Table 10-1. Register Address Ranges (in Hex)

| CHANNEL | GLOBAL | RECEIVE FRAMER | TRANSMIT FRAMER | LIU | BERT | EXTENDED BERT | HDLC-256 |
|---------|-----------|----------------|-----------------|-----------|-----------|---------------|-----------|
| — | 00F0–00FF | — | — | — | — | — | — |
| CH1 | — | 0000–00EF | 0100–01EF | 1000–101F | 1100–110F | 1400–140F | 1500–151F |
| CH2 | — | 0200–02EF | 0300–03EF | 1020–103F | 1110–111F | 1410–141F | 1520–153F |
| CH3 | — | 0400–04EF | 0500–05EF | 1040–105F | 1120–112F | 1420–142F | 1540–155F |
| CH4 | — | 0600–06EF | 0700–07EF | 1060–107F | 1130–113F | 1430–143F | 1560–157F |
| CH5 | — | 0800–08EF | 0900–09EF | 1080–109F | 1140–114F | 1440–144F | 1580–159F |
| CH6 | — | 0A00–0AEF | 0B00–0BEF | 10A0–10BF | 1150–115F | 1450–145F | 15A0–15BF |
| CH7 | — | 0C00–0CEF | 0D00–0DEF | 10C0–10DF | 1160–116F | 1460–146F | 15C0–15DF |
| CH8 | — | 0E00–0EEF | 0F00–0FEF | 10E0–10FF | 1170–117F | 1470–147F | 15E0–15FF |

10.1.1 Global Register List

Table 10-2. Global Register List

| GLOBAL REGISTER LIST | | | |
|----------------------|------------------------|---|-----|
| ADDRESS | NAME | DESCRIPTION | R/W |
| 00F0h | GTCCR1 | Global Transceiver Control Register 1 | R/W |
| 00F1h | GFCR1 | Global Framer Control Register 1 | R/W |
| 00F2h | GTCCR3 | Global Transceiver Control Register 3 | R/W |
| 00F3h | GTCCR1 | Global Transceiver Clock Control Register 1 | R/W |
| 00F4h | GTCCR3 | Global Transceiver Clock Control Register 3 | R/W |
| 00F5h | GHISR | Global HDLC-256 Interrupt Status Register | R |
| 00F6h | GSRR1 | Global Software Reset Register 1 | R/W |
| 00F7h | GHIMR | Global HDLC-256 Interrupt Mask Register | R/W |
| 00F8h | IDR | Device Identification Register | R |
| 00F9h | GFISR1 | Global Framer Interrupt Status Register 1 | R |
| 00FAh | GBISR1 | Global BERT Interrupt Status Register 1 | R |
| 00FBh | GLISR1 | Global LIU Interrupt Status Register 1 | R |
| 00FCh | GFIMR1 | Global Framers Interrupt Mask Register 1 | RW |
| 00FDh | GBIMR1 | Global BERT Interrupt Mask Register 1 | RW |
| 00FEh | GLIMR1 | Global LIU Interrupt Mask Register 1 | RW |

Note 1: Reserved registers should only be written with all zeros.

Note 2: The global registers are located in the framer address space. The corresponding address space for the other seven framers is "Reserved" and should be initialized with all zeros for proper operation.

10.1.2 Framer Register List

Table 10-3. Framer Register List

Note that only Framer 1 address is presented here. The same set of registers definitions applies for transceivers 2 to 8 in accordance with the DS26518 map offsets. Transceiver offset is $[(n - 1) \times 200 \text{ hex}]$, where n designates the transceiver in question.

| FRAMER REGISTER LIST | | | |
|----------------------|--------------------------|--|-----|
| ADDRESS | NAME | DESCRIPTION | R/W |
| 000h | E1RDMWE1 | E1 Receive Digital Milliwatt Enable Register 1 | R/W |
| 001h | E1RDMWE2 | E1 Receive Digital Milliwatt Enable Register 2 | R/W |
| 002h | E1RDMWE3 | E1 Receive Digital Milliwatt Enable Register 3 | R/W |
| 003h | E1RDMWE4 | E1 Receive Digital Milliwatt Enable Register 4 | R/W |
| 004h–00Fh | — | Reserved | — |
| 010h | RHC | Receive HDLC-64 Control Register | R/W |
| 011h | RHBSE | Receive HDLC-64 Bit Suppress Register | R/W |
| 012h | RDS0SEL | Receive Channel Monitor Select Register | R/W |
| 013h | RSIGC | Receive-Signaling Control Register | R/W |
| 014h | T1RCR2 | Receive Control Register 2 (T1 Mode) | R/W |
| | E1RSAIMR | Receive Sa-Bit Interrupt Mask Register (E1 Mode) | |
| 015h | T1RBOCC | Receive BOC Control Register (T1 Mode Only) | R/W |
| 016h–01Fh | — | Reserved | — |
| 020h | RIDR1 | Receive Idle Code Definition Register 1 | R/W |
| 021h | RIDR2 | Receive Idle Code Definition Register 2 | R/W |
| 022h | RIDR3 | Receive Idle Code Definition Register 3 | R/W |
| 023h | RIDR4 | Receive Idle Code Definition Register 4 | R/W |
| 024h | RIDR5 | Receive Idle Code Definition Register 5 | R/W |
| 025h | RIDR6 | Receive Idle Code Definition Register 6 | R/W |
| 026h | RIDR7 | Receive Idle Code Definition Register 7 | R/W |
| 027h | RIDR8 | Receive Idle Code Definition Register 8 | R/W |
| 028h | RIDR9 | Receive Idle Code Definition Register 9 | R/W |
| 029h | RIDR10 | Receive Idle Code Definition Register 10 | R/W |
| 02Ah | RIDR11 | Receive Idle Code Definition Register 11 | R/W |
| 02Bh | RIDR12 | Receive Idle Code Definition Register 12 | R/W |
| 02Ch | RIDR13 | Receive Idle Code Definition Register 13 | R/W |
| 02Dh | RIDR14 | Receive Idle Code Definition Register 14 | R/W |
| 02Eh | RIDR15 | Receive Idle Code Definition Register 15 | R/W |
| 02Fh | RIDR16 | Receive Idle Code Definition Register 16 | R/W |
| 030h | RIDR17 | Receive Idle Code Definition Register 17 | R/W |
| 031h | RIDR18 | Receive Idle Code Definition Register 18 | R/W |
| 032h | RIDR19 | Receive Idle Code Definition Register 19 | R/W |
| 033h | RIDR20 | Receive Idle Code Definition Register 20 | R/W |
| 034h | RIDR21 | Receive Idle Code Definition Register 21 | R/W |
| 035h | RIDR22 | Receive Idle Code Definition Register 22 | R/W |
| 036h | RIDR23 | Receive Idle Code Definition Register 23 | R/W |
| 037h | RIDR24 | Receive Idle Code Definition Register 24 | R/W |
| 038h | T1RSAOI1 | Receive-Signaling All-Ones Insertion Register 1 (T1 Mode Only) | R/W |
| | RIDR25 | Receive Idle Code Definition Register 25 (E1 Mode) | |
| 039h | T1RSAOI2 | Receive-Signaling All-Ones Insertion Register 2 (T1 Mode Only) | R/W |
| | RIDR26 | Receive Idle Code Definition Register 26 (E1 Mode) | |
| 03Ah | T1RSAOI3 | Receive-Signaling All-Ones Insertion Register 3 (T1 Mode Only) | R/W |
| | RIDR27 | Receive Idle Code Definition Register 27 (E1 Mode) | |
| 03B | RIDR28 | Receive Idle Code Definition Register 28 (E1 Mode) | — |
| 03Ch | T1RDMWE1 | T1 Receive Digital Milliwatt Enable Register 1 (T1 Mode Only) | R/W |
| | RIDR29 | Receive Idle Code Definition Register 29 (E1 Mode) | |
| 03Dh | T1RDMWE2 | T1 Receive Digital Milliwatt Enable Register 2 (T1 Mode Only) | R/W |

| FRAMER REGISTER LIST | | | |
|----------------------|--------------------------|---|-----|
| ADDRESS | NAME | DESCRIPTION | R/W |
| | RIDR30 | Receive Idle Code Definition Register 30 (E1 Mode) | |
| 03Eh | T1RDMWE3 | T1 Receive Digital Milliwatt Enable Register 3 (T1 Mode Only) | R/W |
| | RIDR31 | Receive Idle Code Definition Register 31 (E1 Mode) | |
| 03Fh | RIDR32 | Receive Idle Code Definition Register 32 (E1 Mode) | — |
| 040h | RS1 | Receive-Signaling Register 1 | R |
| 041h | RS2 | Receive-Signaling Register 2 | R |
| 042h | RS3 | Receive-Signaling Register 3 | R |
| 043h | RS4 | Receive-Signaling Register 4 | R |
| 044h | RS5 | Receive-Signaling Register 5 | R |
| 045h | RS6 | Receive-Signaling Register 6 | R |
| 046h | RS7 | Receive-Signaling Register 7 | R |
| 047h | RS8 | Receive-Signaling Register 8 | R |
| 048h | RS9 | Receive-Signaling Register 9 | R |
| 049h | RS10 | Receive-Signaling Register 10 | R |
| 04Ah | RS11 | Receive-Signaling Register 11 | R |
| 04Bh | RS12 | Receive-Signaling Register 12 | R |
| 04Ch | RS13 | Receive-Signaling Register 13 (E1 Mode only) | — |
| 04Dh | RS14 | Receive-Signaling Register 14 (E1 Mode only) | — |
| 04Eh | RS15 | Receive-Signaling Register 15 (E1 Mode only) | — |
| 04Fh | RS16 | Receive-Signaling Register 16 (E1 Mode only) | — |
| 050h | LCVCR1 | Line Code Violation Count Register 1 | R |
| 051h | LCVCR2 | Line Code Violation Count Register 2 | R |
| 052h | PCVCR1 | Path Code Violation Count Register 1 | R |
| 053h | PCVCR2 | Path Code Violation Count Register 2 | R |
| 054h | FOSCR1 | Frames Out of Sync Count Register 1 | R |
| 055h | FOSCR2 | Frames Out of Sync Count Register 2 | R |
| 056h | E1EBCR1 | E-Bit Count 1 (E1 Mode Only) | R |
| 057h | E1EBCR2 | E-Bit Count 2 (E1 Mode Only) | R |
| 058h | FEACR1 | Error Count A Register 1 | R/W |
| 059h | FEACR2 | Error Count A Register 2 | R/W |
| 05Ah | FEBCR1 | Error Count B Register 1 | R/W |
| 05Bh | FEBCR2 | Error Count B Register 2 | R/W |
| 060h | RDS0M | Receive DS0 Monitor Register | R |
| 061h | — | Reserved | — |
| 062h | T1RFDL | Receive FDL Register (T1 Mode) | R |
| | E1RRTS7 | Receive Real-Time Status Register 7 (E1 Mode) | |
| 063h | T1RBOC | Receive BOC Register (T1 Mode) | R |
| 064h | T1RSLC1 | Receive SLC-96 Data Link Register 1 (T1 Mode) | R |
| | E1RAF | E1 Receive Align Frame Register (E1 Mode) | |
| 065h | T1RSLC2 | Receive SLC-96 Data Link Register 2 (T1 Mode) | R |
| | E1RNAF | E1 Receive Non-Align Frame Register (E1 Mode) | |
| 066h | T1RSLC3 | Receive SLC-96 Data Link Register 3 (T1 Mode) | R |
| | E1RSiAF | E1 Received Si Bits of the Align Frame Register (E1 Mode) | |
| 067h | E1RSiNAF | Received Si Bits of the Non-Align Frame Register (E1 Mode) | R |
| 068h | E1RRA | Received Remote Alarm Register (E1 Mode) | R |
| 069h | E1RSa4 | E1 Receive Sa4 Bits Register (E1 Mode Only) | R |
| 06Ah | E1RSa5 | E1 Receive Sa5 Bits Register (E1 Mode Only) | R |
| 06Bh | E1RSa6 | E1 Receive Sa6 Bits Register (E1 Mode Only) | R |
| 06Ch | E1RSa7 | E1 Receive Sa7 Bits Register (E1 Mode Only) | R |
| 06Dh | E1RSa8 | Receive Sa8 Bits Register (E1 Mode Only) | R |
| 06Eh | SaBITS | E1 Receive SaX Bits Register | R |
| 06Fh | Sa6CODE | Received Sa6 Codeword Register | R |
| 070h–07Fh | — | Reserved | — |

| FRAMER REGISTER LIST | | | |
|----------------------|--------------------------|--|-----|
| ADDRESS | NAME | DESCRIPTION | R/W |
| 080h | RMMR | Receive Master Mode Register | R/W |
| 081h | RCR1 | Receive Control Register 1 (T1 Mode) | R/W |
| | RCR1 | Receive Control Register 1 (E1 Mode) | |
| 082h | T1RIBCC | Receive In-Band Code Control Register (T1 Mode) | R/W |
| | E1RCR2 | Receive Control Register 2 (E1 Mode) | |
| 083h | RCR3 | Receive Control Register 3 | R/W |
| 084h | RIOCR | Receive I/O Configuration Register | R/W |
| 085h | RESCR | Receive Elastic Store Control Register | R/W |
| 086h | ERCNT | Error-Counter Configuration Register | R/W |
| 087h | RHFC | Receive HDLC-64 FIFO Control Register | R/W |
| 088h | RIBOC | Receive Interleave Bus Operation Control Register | R/W |
| 089h | T1RSCC | In-Band Receive Spare Control Register (T1 Mode Only) | R/W |
| 08Ah | RXPC | Receive Expansion Port Control Register (HDLC-256) | R/W |
| 08Bh | RBPBS | Receive BERT Port Bit Suppress Register | R/W |
| 08Ch | — | Reserved | — |
| 08Dh | RHBS | Receive HDLC-256 Bit Suppress Register | R/W |
| 08Eh–08Fh | — | Reserved | — |
| 090h | RLS1 | Receive Latched Status Register 1 | R/W |
| 091h | RLS2 | Receive Latched Status Register 2 (T1 Mode) | R/W |
| | RLS2 | Receive Latched Status Register 2 (E1 Mode) | |
| 092h | RLS3 | Receive Latched Status Register 3 (T1 Mode) | R/W |
| | RLS3 | Receive Latched Status Register 3 (E1 Mode) | |
| 093h | RLS4 | Receive Latched Status Register 4 | R/W |
| 094h | RLS5 | Receive Latched Status Register 5 (HDLC-64) | R/W |
| 095h | — | Reserved | — |
| 096h | RLS7 | Receive Latched Status Register 7 (T1 Mode) | R/W |
| | RLS7 | Receive Latched Status Register 7 (E1 Mode) | |
| 097h | — | Reserved | — |
| 098h | RSS1 | Receive-Signaling Status Register 1 | R/W |
| 099h | RSS2 | Receive-Signaling Status Register 2 | R/W |
| 09Ah | RSS3 | Receive-Signaling Status Register 3 | R/W |
| 09Bh | RSS4 | Receive-Signaling Status Register 4 (E1 Mode Only) | R/W |
| 09Ch | T1RSCD1 | Receive Spare Code Definition Register 1 (T1 Mode Only) | R/W |
| 09Dh | T1RSCD2 | Receive Spare Code Definition Register 2 (T1 Mode Only) | R/W |
| 09Eh | — | Reserved | — |
| 09Fh | RIIR | Receive Interrupt Information Register | R/W |
| 0A0h | RIM1 | Receive Interrupt Mask Register 1 | R/W |
| 0A1h | RIM2 | Receive Interrupt Mask Register 2 (E1 Mode Only) | R/W |
| 0A2h | RIM3 | Receive Interrupt Mask Register 3 (T1 Mode) | R/W |
| | RIM3 | Receive Interrupt Mask Register 3 (E1 Mode) | |
| 0A3h | RIM4 | Receive Interrupt Mask Register 4 | R/W |
| 0A4h | RIM5 | Receive Interrupt Mask Register 5 (HDLC-64) | R/W |
| 0A5h | — | Reserved | — |
| 0A6h | RIM7 | Receive Interrupt Mask Register 7 (BOC:FDL) (T1 Mode) | R/W |
| | RIM7 | Receive Interrupt Mask Register 7 (BOC:FDL) (E1 Mode) | |
| 0A7h | — | Reserved | — |
| 0A8h | RSCSE1 | Receive-Signaling Change of State Enable Register 1 | R/W |
| 0A9h | RSCSE2 | Receive-Signaling Change of State Enable Register 2 | R/W |
| 0AAh | RSCSE3 | Receive-Signaling Change of State Enable Register 3 | R/W |
| 0ABh | RSCSE4 | Receive-Signaling Change of State Enable Register 4 (E1 Mode Only) | — |
| 0ACh | T1RUPCD1 | Receive Up Code Definition Register 1 (T1 Mode Only) | R/W |
| 0ADh | T1RUPCD2 | Receive Up Code Definition Register 2 (T1 Mode Only) | R/W |
| 0AEh | T1RDNCD1 | Receive Down Code Definition Register 1 (T1 Mode Only) | R/W |

| FRAMER REGISTER LIST | | | |
|----------------------|---------------------------------|--|-----|
| ADDRESS | NAME | DESCRIPTION | R/W |
| 0AFh | T1RDNCD2 | Receive Down Code Definition Register 2 (T1 Mode Only) | R/W |
| 0B0h | RRTS1 | Receive Real-Time Status Register 1 | R |
| 0B1h | — | Reserved | — |
| 0B2h | RRTS3 | Receive Real-Time Status Register 3 (T1 Mode) | R |
| | RRTS3 | Receive Real-Time Status Register 3 (E1 Mode) | |
| 0B3h | — | Reserved | — |
| 0B4h | RRTS5 | Receive Real-Time Status Register 5 (HDLC-64) | R |
| 0B5h | RHPBA | Receive HDLC-64 Packet Bytes Available Register | R |
| 0B6h | RHF | Receive HDLC-64 FIFO Register | R |
| 0B7h–0BFh | — | Reserved | — |
| 0C0h | RBCS1 | Receive Blank Channel Select Register 1 | R/W |
| 0C1h | RBCS2 | Receive Blank Channel Select Register 2 | R/W |
| 0C2h | RBCS3 | Receive Blank Channel Select Register 3 | R/W |
| 0C3h | RBCS4 | Receive Blank Channel Select Register 4 (E1 Mode Only) | R/W |
| 0C4h | RCBR1 | Receive Channel Blocking Register 1 | R/W |
| 0C5h | RCBR2 | Receive Channel Blocking Register 2 | R/W |
| 0C6h | RCBR3 | Receive Channel Blocking Register 3 | R/W |
| 0C7h | RCBR4 | Receive Channel Blocking Register 4 (E1 Mode Only) | R/W |
| 0C8h | RSI1 | Receive-Signaling Reinsertion Enable Register 1 | R/W |
| 0C9h | RSI2 | Receive-Signaling Reinsertion Enable Register 2 | R/W |
| 0CAh | RSI3 | Receive-Signaling Reinsertion Enable Register 3 | R/W |
| 0CBh | RSI4 | Receive-Signaling Reinsertion Enable Register 4 (E1 Mode Only) | R/W |
| 0CCh | RGCCS1 | Receive Gapped Clock Channel Select Register 1 | R/W |
| 0CDh | RGCCS2 | Receive Gapped Clock Channel Select Register 2 | R/W |
| 0CEh | RGCCS3 | Receive Gapped Clock Channel Select Register 3 | R/W |
| 0CFh | RGCCS4 | Receive Gapped Clock Channel Select Register (E1 Mode Only) | R/W |
| 0D0h | RCICE1 | Receive Channel Idle Code Enable Register 1 | R/W |
| 0D1h | RCICE2 | Receive Channel Idle Code Enable Register 2 | R/W |
| 0D2h | RCICE3 | Receive Channel Idle Code Enable Register 3 | R/W |
| 0D3h | RCICE4 | Receive Channel Idle Code Enable Register 4 (E1 Mode Only) | R/W |
| 0D4h | RBPCS1 | Receive BERT Port Channel Select Register 1 | R/W |
| 0D5h | RBPCS2 | Receive BERT Port Channel Select Register 2 | R/W |
| 0D6h | RBPCS3 | Receive BERT Port Channel Select Register 3 | R/W |
| 0D7h | RBPCS4 | Receive BERT Port Channel Select Register 4 (E1 Mode Only) | R/W |
| 0D8h–0DBh | — | Reserved | — |
| 0DCh | RHCS1 | Receive HDLC-256 Channel Select Register 1 | R/W |
| 0DDh | RHCS2 | Receive HDLC-256 Channel Select Register 2 | R/W |
| 0DEh | RHCS3 | Receive HDLC-256 Channel Select Register 3 | R/W |
| 0DFh | RHCS4 | Receive HDLC-256 Channel Select Register 4 (E1 Mode Only) | R/W |
| 0E0h–0EFh | — | Reserved | — |
| 0F0h–0FFh | Global Registers (Section 10.3) | See the Global Register list in Table 10-2 . Note that this space is “Reserved” in Framers 2 to 8. | R/W |
| 100h | TDMWE1 | Transmit Digital Milliwatt Enable Register 1 (T1 and E1 Modes) | R/W |
| 101h | TDMWE2 | Transmit Digital Milliwatt Enable Register 2 (T1 and E1 Modes) | R/W |
| 102h | TDMWE3 | Transmit Digital Milliwatt Enable Register 3 (T1 and E1 Modes) | R/W |
| 103h | TDMWE4 | Transmit Digital Milliwatt Enable Register 4 (T1 and E1 Modes) | R/W |
| 104h | TJBE1 | Transmit Jammed Bit Eight Stuffing Register 1 | R/W |
| 105h | TJBE2 | Transmit Jammed Bit Eight Stuffing Register 2 | R/W |
| 106h | TJBE3 | Transmit Jammed Bit Eight Stuffing Register 3 | R/W |
| 107h | TJBE4 | Transmit Jammed Bit Eight Stuffing Register 4 | R/W |
| 108h | TDDS1 | Transmit DDS Zero Code Register 1 | R/W |
| 109h | TDDS2 | Transmit DDS Zero Code Register 2 | R/W |

| FRAMER REGISTER LIST | | | |
|----------------------|-------------------------|---|-----|
| ADDRESS | NAME | DESCRIPTION | R/W |
| 10Ah | TDDS3 | Transmit DDS Zero Code Register 3 | R/W |
| 110h | THC1 | Transmit HDLC-64 Control Register 1 | R/W |
| 111h | THBSE | Transmit HDLC-64 Bit Suppress Register | R/W |
| 112h | — | Reserved | — |
| 113h | THC2 | Transmit HDLC-64 Control Register 2 | R/W |
| 114h | E1TSACR | E1 Transmit Sa-Bit Control Register (E1 Mode) | R/W |
| 115h–117h | — | Reserved | — |
| 118h | SSIE1 | Software-Signaling Insertion Enable Register 1 | R/W |
| 119h | SSIE2 | Software-Signaling Insertion Enable Register 2 | R/W |
| 11Ah | SSIE3 | Software-Signaling Insertion Enable Register 3 | R/W |
| 11Bh | SSIE4 | Software-Signaling Insertion Enable Register 4 (E1 Mode Only) | R/W |
| 11Ch–11Fh | — | Reserved | — |
| 120h | TIDR1 | Transmit Idle Code Definition Register 1 | R/W |
| 121h | TIDR2 | Transmit Idle Code Definition Register 2 | R/W |
| 122h | TIDR3 | Transmit Idle Code Definition Register 3 | R/W |
| 123h | TIDR4 | Transmit Idle Code Definition Register 4 | R/W |
| 124h | TIDR5 | Transmit Idle Code Definition Register 5 | R/W |
| 125h | TIDR6 | Transmit Idle Code Definition Register 6 | R/W |
| 126h | TIDR7 | Transmit Idle Code Definition Register 7 | R/W |
| 127h | TIDR8 | Transmit Idle Code Definition Register 8 | R/W |
| 128h | TIDR9 | Transmit Idle Code Definition Register 9 | R/W |
| 129h | TIDR10 | Transmit Idle Code Definition Register 10 | R/W |
| 12Ah | TIDR11 | Transmit Idle Code Definition Register 11 | R/W |
| 12Bh | TIDR12 | Transmit Idle Code Definition Register 12 | R/W |
| 12Ch | TIDR13 | Transmit Idle Code Definition Register 13 | R/W |
| 12Dh | TIDR14 | Transmit Idle Code Definition Register 14 | R/W |
| 12Eh | TIDR15 | Transmit Idle Code Definition Register 15 | R/W |
| 12Fh | TIDR16 | Transmit Idle Code Definition Register 16 | R/W |
| 130h | TIDR17 | Transmit Idle Code Definition Register 17 | R/W |
| 131h | TIDR18 | Transmit Idle Code Definition Register 18 | R/W |
| 132h | TIDR19 | Transmit Idle Code Definition Register 19 | R/W |
| 133h | TIDR20 | Transmit Idle Code Definition Register 20 | R/W |
| 134h | TIDR21 | Transmit Idle Code Definition Register 21 | R/W |
| 135h | TIDR22 | Transmit Idle Code Definition Register 22 | R/W |
| 136h | TIDR23 | Transmit Idle Code Definition Register 23 | R/W |
| 137h | TIDR24 | Transmit Idle Code Definition Register 24 | R/W |
| 138h | TIDR25 | Transmit Idle Code Definition Register 25 (E1 Mode Only) | R/W |
| 139h | TIDR26 | Transmit Idle Code Definition Register 26 (E1 Mode Only) | R/W |
| 13Ah | TIDR27 | Transmit Idle Code Definition Register 27 (E1 Mode Only) | R/W |
| 13Bh | TIDR28 | Transmit Idle Code Definition Register 28 (E1 Mode Only) | R/W |
| 13Ch | TIDR29 | Transmit Idle Code Definition Register 29 (E1 Mode Only) | R/W |
| 13Dh | TIDR30 | Transmit Idle Code Definition Register 30 (E1 Mode Only) | R/W |
| 13Eh | TIDR31 | Transmit Idle Code Definition Register 31 (E1 Mode Only) | R/W |
| 13Fh | TIDR32 | Transmit Idle Code Definition Register 32 (E1 Mode Only) | R/W |
| 140h | TS1 | Transmit-Signaling Register 1 | R/W |
| 141h | TS2 | Transmit-Signaling Register 2 | R/W |
| 142h | TS3 | Transmit-Signaling Register 3 | R/W |
| 143h | TS4 | Transmit-Signaling Register 4 | R/W |
| 144h | TS5 | Transmit-Signaling Register 5 | R/W |
| 145h | TS6 | Transmit-Signaling Register 6 | R/W |
| 146h | TS7 | Transmit-Signaling Register 7 | R/W |
| 147h | TS8 | Transmit-Signaling Register 8 | R/W |
| 148h | TS9 | Transmit-Signaling Register 9 | R/W |

| FRAMER REGISTER LIST | | | |
|----------------------|--------------------------|---|-----|
| ADDRESS | NAME | DESCRIPTION | R/W |
| 149h | TS10 | Transmit-Signaling Register 10 | R/W |
| 14Ah | TS11 | Transmit-Signaling Register 11 | R/W |
| 14Bh | TS12 | Transmit-Signaling Register 12 | R/W |
| 14Ch | TS13 | Transmit-Signaling Register 13 | R/W |
| 14Dh | TS14 | Transmit-Signaling Register 14 | R/W |
| 14Eh | TS15 | Transmit-Signaling Register 15 | R/W |
| 14Fh | TS16 | Transmit-Signaling Register 16 | R/W |
| 150h | TCICE1 | Transmit Channel Idle Code Enable Register 1 | R/W |
| 151h | TCICE2 | Transmit Channel Idle Code Enable Register 2 | R/W |
| 152h | TCICE3 | Transmit Channel Idle Code Enable Register 3 | R/W |
| 153h | TCICE4 | Transmit Channel Idle Code Enable Register 4 (E1 Mode Only) | R/W |
| 154h–161h | — | Reserved | — |
| 162h | T1TFDL | Transmit FDL Register (T1 Mode Only) | R/W |
| 163h | T1TBOC | Transmit BOC Register (T1 Mode Only) | R/W |
| 164h | T1TSLC1 | Transmit SLC-96 Data Link Register 1 (T1 Mode) | R/W |
| | E1TAF | Transmit Align Frame Register (E1 Mode) | |
| 165h | T1TSLC2 | Transmit SLC-96 Data Link Register 2 (T1 Mode) | R/W |
| | E1TNAF | Transmit Non-Align Frame Register (E1 Mode) | |
| 166h | T1TSLC3 | Transmit SLC-96 Data Link Register 3 (T1 Mode) | R/W |
| | E1TSiAF | Transmit Si Bits of the Align Frame Register (E1 Mode) | |
| 167h | E1TSiNAF | Transmit Si Bits of the Non-Align Frame Register (E1 Mode Only) | R/W |
| 168h | E1TRA | Transmit Remote Alarm Register (E1 Mode) | R/W |
| 169h | E1TSa4 | Transmit Sa4 Bits Register (E1 Mode Only) | R/W |
| 16Ah | E1TSa5 | Transmit Sa5 Bits Register (E1 Mode Only) | R/W |
| 16Bh | E1TSa6 | Transmit Sa6 Bits Register (E1 Mode Only) | R/W |
| 16Ch | E1TSa7 | Transmit Sa7 Bits Register (E1 Mode Only) | R/W |
| 16Dh | E1TSa8 | Transmit Sa8 Bits Register (E1 Mode Only) | R/W |
| 16Eh–17Fh | — | Reserved | — |
| 180h | TMMR | Transmit Master Mode Register | R/W |
| 181h | TCR1 | Transmit Control Register 1 (T1 Mode) | R/W |
| | TCR1 | Transmit Control Register 1 (E1 Mode) | |
| 182h | T1.TCR2 | Transmit Control Register 2 (T1 Mode) | R/W |
| | E1.TCR2 | Transmit Control Register 2 (E1 Mode) | |
| 183h | TCR3 | Transmit Control Register 3 | R/W |
| 184h | TIOCR | Transmit I/O Configuration Register | R/W |
| 185h | TESCR | Transmit Elastic Store Control Register | R/W |
| 186h | TCR4 | Transmit Control Register 4 (T1 Mode Only) | R/W |
| 187h | THFC | Transmit HDLC-64 FIFO Control Register | R/W |
| 188h | TIBOC | Transmit Interleave Bus Operation Control Register | R/W |
| 189h | TDS0SEL | Transmit DS0 Channel Monitor Select Register | R/W |
| 18Ah | TXPC | Transmit Expansion Port Control Register | R/W |
| 18Bh | TBPBS | Transmit BERT Port Bit Suppress Register | R/W |
| 18Ch | — | Reserved | — |
| 18Dh | THBS | Transmit HDLC-256 Bit Suppress Register | R/W |
| 18Eh | TSYNCC | Transmit Synchronizer Control Register | R/W |
| 18Fh | — | Reserved | — |
| 190h | TLS1 | Transmit Latched Status Register 1 | R/W |
| 191h | TLS2 | Transmit Latched Status Register 2 (HDLC-64) | R/W |
| 192h | TLS3 | Transmit Latched Status Register 3 (Synchronizer) | R/W |
| 193h–19Eh | — | Reserved | — |
| 19Fh | TIIR | Transmit Interrupt Information Register | R/W |
| 1A0h | TIM1 | Transmit Interrupt Mask Register 1 | R/W |
| 1A1h | TIM2 | Transmit Interrupt Mask Register 2 (HDLC-64) | R/W |

| FRAMER REGISTER LIST | | | |
|----------------------|------------------------|--|-----|
| ADDRESS | NAME | DESCRIPTION | R/W |
| 1A2h | TIM3 | Transmit Interrupt Mask Register 3 (Synchronizer) | R/W |
| 1A3h–1ABh | — | Reserved | — |
| 1ACh | T1TCD1 | Transmit Code Definition Register 1 (T1 Mode Only) | R/W |
| 1ADh | T1TCD2 | Transmit Code Definition Register 2 (T1 Mode Only) | R/W |
| 1AEh–1B0h | — | Reserved | — |
| 1B1h | TRTS2 | Transmit Real-Time Status Register 2 (HDLC-64) | R |
| 1B2h | — | Reserved | — |
| 1B3h | TFBA | Transmit HDLC-64 FIFO Buffer Available Register | R |
| 1B4h | THF | Transmit HDLC-64 FIFO Register | W |
| 1B5h–1BAh | — | Reserved | — |
| 1BBh | TDS0M | Transmit DS0 Monitor Register | R |
| 1BCh–1BFh | — | Reserved | — |
| 1C0h | TBCS1 | Transmit Blank Channel Select Register 1 | R/W |
| 1C1h | TBCS2 | Transmit Blank Channel Select Register 2 | R/W |
| 1C2h | TBCS3 | Transmit Blank Channel Select Register 3 | R/W |
| 1C3h | TBCS4 | Transmit Blank Channel Select Register 4 (E1 Mode Only) | R/W |
| 1C4h | TCBR1 | Transmit Channel Blocking Register 1 | R/W |
| 1C5h | TCBR2 | Transmit Channel Blocking Register 2 | R/W |
| 1C6h | TCBR3 | Transmit Channel Blocking Register 3 | R/W |
| 1C7h | TCBR4 | Transmit Channel Blocking Register 4 (E1 Mode Only) | R/W |
| 1C8h | THSCS1 | Transmit Hardware-Signaling Channel Select Register 1 | R/W |
| 1C9h | THSCS2 | Transmit Hardware-Signaling Channel Select Register 2 | R/W |
| 1CAh | THSCS3 | Transmit Hardware-Signaling Channel Select Register 3 | R/W |
| 1CBh | THSCS4 | Transmit Hardware-Signaling Channel Select Register 4 (E1 Mode Only) | R/W |
| 1CCh | TGCCS1 | Transmit Gapped-Clock Channel Select Register 1 | R/W |
| 1CDh | TGCCS2 | Transmit Gapped-Clock Channel Select Register 2 | R/W |
| 1CEh | TGCCS3 | Transmit Gapped-Clock Channel Select Register 3 | R/W |
| 1CFh | TGCCS4 | Transmit Gapped-Clock Channel Select Register 4 (E1 Mode Only) | R/W |
| 1D0h | PCL1 | Per-Channel Loopback Enable Register 1 | R/W |
| 1D1h | PCL2 | Per-Channel Loopback Enable Register 2 | R/W |
| 1D2h | PCL3 | Per-Channel Loopback Enable Register 3 | R/W |
| 1D3h | PCL4 | Per-Channel Loopback Enable Register 4 (E1 Mode Only) | R/W |
| 1D4h | TBPCS1 | Transmit BERT Port Channel Select Register 1 | R/W |
| 1D5h | TBPCS2 | Transmit BERT Port Channel Select Register 2 | R/W |
| 1D6h | TBPCS3 | Transmit BERT Port Channel Select Register 3 | R/W |
| 1D7h | TBPCS4 | Transmit BERT Port Channel Select Register 4 (E1 Mode Only) | R/W |
| 1DCh | THCS1 | Transmit HDLC-256 Channel Select Register 1 | R/W |
| 1DDh | THCS2 | Transmit HDLC-256 Channel Select Register 2 | R/W |
| 1DEh | THCS3 | Transmit HDLC-256 Channel Select Register 3 | R/W |
| 1DFh | THCS4 | Transmit HDLC-256 Channel Select Register 4 (E1 Mode Only) | R/W |
| 1E0h–1FFh | — | Reserved | — |

10.1.3 LIU Register List

Table 10-4. LIU Register List

Note that only the LIU 1 address is presented here. The same set of registers definitions applies for LIUs 2 to 8 in accordance with the DS26518 map offsets. LIU offset is $[1000 + (n - 1) \times 20 \text{ hex}]$, where n designates the LIU in question.

| LIU REGISTER LIST | | | |
|-------------------|------------------------|---|-----|
| ADDRESS | NAME | DESCRIPTION | R/W |
| 1000h | LTRCR | LIU Transmit Receive Control Register | R/W |
| 1001h | LTIPSR | LIU Transmit Impedance and Pulse Shape Selection Register | R/W |
| 1002h | LMCR | LIU Maintenance Control Register | R/W |
| 1003h | LRSR | LIU Real Status Register | R |
| 1004h | LSIMR | LIU Status Interrupt Mask Register | R/W |
| 1005h | LLSR | LIU Latched Status Register | R/W |
| 1006h | LRSL | LIU Receive Signal Level Register | R |
| 1007 | LRISMR | LIU Receive Impedance and Sensitivity Monitor Register | R/W |
| 1008h | LRCR | LIU Receive Control Register | R/W |
| 1009h–101Fh | — | Reserved | — |

10.1.4 BERT Register List

Table 10-5. BERT Register List

Note that only the BERT 1 address is presented here. The same set of registers definitions applies for BERTs 2 to 8 in accordance with the DS26518 map offsets. BERT offset is $[1100 + (n - 1) \times 10 \text{ hex}]$, where n designates the BERT channel in question.

| BERT REGISTER LIST | | | |
|--------------------|-----------------------|---|-----|
| ADDRESS | NAME | DESCRIPTION | R/W |
| 1100h | BAWC | BERT Alternating Word Count Rate Register | R |
| 1101h | BRP1 | BERT Repetitive Pattern Set Register 1 | R/W |
| 1102h | BRP2 | BERT Repetitive Pattern Set Register 2 | R/W |
| 1103h | BRP3 | BERT Repetitive Pattern Set Register 3 | R/W |
| 1104h | BRP4 | BERT Repetitive Pattern Set Register 4 | R/W |
| 1105h | BC1 | BERT Control Register 1 | R/W |
| 1106h | BC2 | BERT Control Register 2 | R/W |
| 1107h | BBC1 | BERT Bit Count Register 1 | R |
| 1108h | BBC2 | BERT Bit Count Register 2 | R |
| 1109h | BBC3 | BERT Bit Count Register 3 | R |
| 110Ah | BBC4 | BERT Bit Count Register 4 | R |
| 110Bh | BEC1 | BERT Error Count Register 1 | R |
| 110Ch | BEC2 | BERT Error Count Register 2 | R |
| 110Dh | BEC3 | BERT Error Count Register 3 | R |
| 110Eh | BSR | BERT Status Register | R |
| 110Fh | BSIM | BERT Status Interrupt Mask Register | R/W |
| 1400h | BC3 | BERT Control Register 3 | R/W |
| 1401h | BRSR | BERT Real-Time Status Register | R |
| 1402h | BLSR1 | BERT Latched Status Register 1 | R/W |
| 1403h | BSIM1 | BERT Status Interrupt Mask Register 1 | R/W |
| 1404h | BLSR2 | BERT Latched Status Register 2 | R/W |
| 1405h | BSIM2 | BERT Status Interrupt Mask Register 2 | R/W |

10.1.5 HDLC-256 Register List

Table 10-6. HDLC-256 Register List

Note that only the HDLC-256 1 address is presented here. The same set of registers definitions applies for HDLC-256s 2 to 8 in accordance with the DS26518 map offsets. HDLC-256 offset is $\{1500 + (n - 1) \times 20 \text{ hex}\}$, where n designates the HDLC-256 in question.

| HDLC-256 REGISTER LIST | | | |
|------------------------|---------------------------|--|-----|
| ADDRESS | NAME | DESCRIPTION | R/W |
| 1500h | TH256CR1 | Transmit HDLC-256 Control Register 1 | R/W |
| 1501h | TH256CR2 | Transmit HDLC-256 Control Register 2 | R/W |
| 1502h | TH256FDR1 | Transmit HDLC-256 FIFO Data Register 1 | R/W |
| 1503h | TH256FDR2 | Transmit HDLC-256 FIFO Data Register 2 | R/W |
| 1504h | TH256SR1 | Transmit HDLC-256 Status Register 1 | R |
| 1505h | TH256SR2 | Transmit HDLC-256 Status Register 2 | R |
| 1506h | TH256SRL | Transmit HDLC-256 Status Register Latched | R/W |
| 1507h | — | Reserved | — |
| 1508h | TH256SRIE | Transmit HDLC-256 Status Register Interrupt Enable | R/W |
| 1509h | — | Reserved | — |
| 150Ah | — | Reserved | — |
| 150Bh | — | Reserved | — |
| 150Ch | — | Reserved | — |
| 150Dh | — | Reserved | — |
| 150Eh | — | Reserved | — |
| 150Fh | — | Reserved | — |
| 1510h | RH256CR1 | Receive HDLC-256 Control Register 1 | R/W |
| 1511h | RH256CR2 | Receive HDLC-256 Control Register 2 | R/W |
| 1512h | — | Reserved | — |
| 1513h | — | Reserved | — |
| 1514h | RH256SR | Receive HDLC-256 Status Register | R |
| 1515h | — | Reserved | — |
| 1516h | RH256SRL | Receive HDLC-256 Status Register Latched | R/W |
| 1517h | — | Reserved | — |
| 1518h | RH256SRIE | Receive HDLC-256 Status Register Interrupt Enable | R/W |
| 1519h | — | Reserved | — |
| 151Ah | — | Reserved | — |
| 151Bh | — | Reserved | — |
| 151Ch | RH256FDR1 | Receive HDLC-256 FIFO Data Register 1 | R |
| 151Dh | RH256FDR2 | Receive HDLC-256 FIFO Data Register 2 | R |
| 151Eh | — | Reserved | — |
| 151Fh | — | Reserved | — |

10.2 Register Bit Maps

10.2.1 Global Register Bit Map

Table 10-7. Global Register Bit Map

| ADDR | NAME | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
|-------|------------------------|-----------|------------|------------|-----------|----------|----------|------------|-----------|
| 00F0h | GTCR1 | GPSEL3 | GPSEL2 | GPSEL1 | — | 528MD | GIBO | GCLE | GIPI |
| 00F1h | GFCR1 | IBOMS1 | IBOMS0 | BPCLK1 | BPCLK0 | — | RFMSS | TCBCS | RCBCS |
| 00F2h | GTCR3 | — | — | — | — | — | — | TSSYNCOSEL | TSYNCSSEL |
| 00F3h | GTCCR1 | BPREFSEL3 | BPREFSEL2 | BPREFSEL1 | BPREFSEL0 | BFREQSEL | FREQSEL | MPS1 | MPS0 |
| 00F4h | GTCCR3 | | RSYSCLKSEL | TSYSCLKSEL | TCLKSEL | CLKOSEL3 | CLKOSEL2 | CLKOSEL1 | CLKOSEL0 |
| 00F5h | GHISR | HIS8 | HIS7 | HIS6 | HIS5 | HIS4 | HIS3 | HIS2 | HIS1 |
| 00F6h | GSRR1 | — | — | — | — | H256RST | LRST | BRST | FRST |
| 00F7h | GHIMR | HIM8 | HIM7 | HIM6 | HIM5 | HIM4 | HIM3 | HIM2 | HIM1 |
| 00F8h | IDR | ID7 | ID6 | ID5 | ID4 | ID3 | ID2 | ID1 | ID0 |
| 00F9h | GFISR1 | FIS8 | FIS7 | FIS6 | FIS5 | FIS4 | FIS3 | FIS2 | FIS1 |
| 00FAh | GBISR1 | BIS8 | BIS7 | BIS6 | BIS5 | BIS4 | BIS3 | BIS2 | BIS1 |
| 00FBh | GLISR1 | LIS8 | LIS7 | LIS6 | LIS5 | LIS4 | LIS3 | LIS2 | LIS1 |
| 00FCh | GFIMR1 | FIM8 | FIM7 | FIM6 | FIM5 | FIM4 | FIM3 | FIM2 | FIM1 |
| 00FDh | GBIMR1 | BIM8 | BIM7 | BIM6 | BIM5 | BIM4 | BIM3 | BIM2 | BIM1 |
| 00FEh | GLIMR1 | LIM8 | LIM7 | LIM6 | LIM5 | LIM4 | LIM3 | LIM2 | LIM1 |

10.2.2 Framer Register Bit Map

Table 10-8 contains the framer registers of the DS26518. Some registers have dual functionality based on the selection of T1/J1 or E1 operating mode in the [RMMR](#) and [TMMR](#) registers. These dual-function registers are shown below using two lines of text. The first line of text is the bit functionality for T1/J1 mode. The second line is the bit functionality in E1 mode, in *italics*. Bits that are not used for an operating mode are denoted with a single dash “—”. When there is only one set of bit definitions listed for a register, the bit functionality does not change with respect to the selection of T1/J1 or E1 mode. All registers not listed are reserved and should be initialized with a value of 00h for proper operation. The addresses shown are for Framer 1. Addresses for Framers 2 to 8 can be calculated using the following formula: Address for Framer n = (Framer 1 address + (n - 1) x 200hex).

Table 10-8. Framer Register Bit Map

| ADDR | NAME | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
|---------------|--------------------------|-------|-------|-------|---------------|---------------|---------------|---------------|---------------|
| 000h | E1RDMWE1 | CH8 | CH7 | CH6 | CH5 | CH4 | CH3 | CH2 | CH1 |
| 001h | E1RDMWE2 | CH16 | CH15 | CH14 | CH13 | CH12 | CH11 | CH10 | CH9 |
| 002h | E1RDMWE3 | CH24 | CH23 | CH22 | CH21 | CH20 | CH19 | CH18 | CH17 |
| 003h | E1RDMWE4 | CH32 | CH31 | CH30 | CH29 | CH28 | CH27 | CH26 | CH25 |
| 004h– 00Fh | — | — | — | — | — | — | — | — | — |
| 010h | RHC | RCRCD | RHR | RHMS | RHCS4 | RHCS3 | RHCS2 | RHCS1 | RHCS0 |
| 011h | RHBSE | BSE8 | BSE7 | BSE6 | BSE5 | BSE4 | BSE3 | BSE2 | BSE1 |
| 012h | RDS0SEL | — | — | — | RCM4 | RCM3 | RCM2 | RCM1 | RCM0 |
| 013h | RSIGC | — | — | — | RFSA1 | — | RSFF | RSFE | RSIE |
| | | — | — | — | CASMS | — | RSFF | RSFE | RSEI |
| 014h | T1RCR2 | — | — | — | RSLC96 | OOF2 | OOF1 | RAIIE | RRAIS |
| | E1RSAIMR | — | — | — | <i>RSa4IM</i> | <i>RSa5IM</i> | <i>RSa6IM</i> | <i>RSa7IM</i> | <i>RSa8IM</i> |
| 015h | T1RBOCC | RBR | — | RBD1 | RBD0 | — | RBF1 | RBF0 | — |
| 016h– 01Fh | — | — | — | — | — | — | — | — | — |
| 020h | RIDR1 | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
| 021h | RIDR2 | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
| 022h | RIDR3 | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
| 023h | RIDR4 | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
| 024h | RIDR5 | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
| 025h | RIDR6 | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
| 026h | RIDR7 | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
| 027h | RIDR8 | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
| 028h | RIDR9 | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
| 029h | RIDR10 | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
| 02Ah | RIDR11 | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
| 02Bh | RIDR12 | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
| 02Ch | RIDR13 | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
| 02Dh | RIDR14 | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
| 02Eh | RIDR15 | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
| 02Fh | RIDR16 | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
| 030h | RIDR17 | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
| 031h | RIDR18 | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
| 032h | RIDR19 | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
| 033h | RIDR20 | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
| 034h | RIDR21 | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
| 035h | RIDR22 | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
| 036h | RIDR23 | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
| 037h | RIDR24 | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |

| ADDR | NAME | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
|------|--------------------------|---------------|---------------|---------------|---------------|---------------|---------------|---------------|---------------|
| 038h | T1RSAOI1 | CH8 | CH7 | CH6 | CH5 | CH4 | CH3 | CH2 | CH1 |
| | <i>RIDR25</i> | <i>C7</i> | <i>C6</i> | <i>C5</i> | <i>C4</i> | <i>C3</i> | <i>C2</i> | <i>C1</i> | <i>C0</i> |
| 039h | T1RSAOI2 | CH16 | CH15 | CH14 | CH13 | CH12 | CH11 | CH10 | CH9 |
| | <i>RIDR26</i> | <i>C7</i> | <i>C6</i> | <i>C5</i> | <i>C4</i> | <i>C3</i> | <i>C2</i> | <i>C1</i> | <i>C0</i> |
| 03Ah | T1RSAOI3 | CH24 | CH23 | CH22 | CH21 | CH20 | CH19 | CH18 | CH17 |
| | <i>RIDR27</i> | <i>C7</i> | <i>C6</i> | <i>C5</i> | <i>C4</i> | <i>C3</i> | <i>C2</i> | <i>C1</i> | <i>C0</i> |
| 03Bh | <i>RIDR28</i> | — | — | — | — | — | — | — | — |
| | | <i>C7</i> | <i>C6</i> | <i>C5</i> | <i>C4</i> | <i>C3</i> | <i>C2</i> | <i>C1</i> | <i>C0</i> |
| 03Ch | T1RDMWE1 | CH8 | CH7 | CH6 | CH5 | CH4 | CH3 | CH2 | CH1 |
| | <i>RIDR29</i> | <i>C7</i> | <i>C6</i> | <i>C5</i> | <i>C4</i> | <i>C3</i> | <i>C2</i> | <i>C1</i> | <i>C0</i> |
| 03Dh | T1RDMWE2 | CH16 | CH15 | CH14 | CH13 | CH12 | CH11 | CH10 | CH9 |
| | <i>RIDR30</i> | <i>C7</i> | <i>C6</i> | <i>C5</i> | <i>C4</i> | <i>C3</i> | <i>C2</i> | <i>C1</i> | <i>C0</i> |
| 03Eh | T1RDMWE3 | CH24 | CH23 | CH22 | CH21 | CH20 | CH19 | CH18 | CH17 |
| | <i>RIDR31</i> | <i>C7</i> | <i>C6</i> | <i>C5</i> | <i>C4</i> | <i>C3</i> | <i>C2</i> | <i>C1</i> | <i>C0</i> |
| 03Fh | <i>RIDR32</i> | — | — | — | — | — | — | — | — |
| | | <i>C7</i> | <i>C6</i> | <i>C5</i> | <i>C4</i> | <i>C3</i> | <i>C2</i> | <i>C1</i> | <i>C0</i> |
| 040h | RS1 | CH1-A | CH1-B | CH1-C | CH1-D | CH13-A | CH13-B | CH13-C | CH13-D |
| | | <i>0</i> | <i>0</i> | <i>0</i> | <i>0</i> | <i>X</i> | <i>Y</i> | <i>X</i> | <i>X</i> |
| 041h | RS2 | CH2-A | CH2-B | CH2-C | CH2-D | CH14-A | CH14-B | CH14-C | CH14-D |
| | | <i>CH1-A</i> | <i>CH1-B</i> | <i>CH1-C</i> | <i>CH1-D</i> | <i>CH16-A</i> | <i>CH16-B</i> | <i>CH16-C</i> | <i>CH16-D</i> |
| 042h | RS3 | CH3-A | CH3-B | CH3-C | CH3-D | CH15-A | CH15-B | CH15-C | CH15-D |
| | | <i>CH2-A</i> | <i>CH2-B</i> | <i>CH2-C</i> | <i>CH2-D</i> | <i>CH17-A</i> | <i>CH17-B</i> | <i>CH17-C</i> | <i>CH17-D</i> |
| 043h | RS4 | CH4-A | CH4-B | CH4-C | CH4-D | CH16-A | CH16-B | CH16-C | CH16-D |
| | | <i>CH3-A</i> | <i>CH3-B</i> | <i>CH3-C</i> | <i>CH3-D</i> | <i>CH18-A</i> | <i>CH18-B</i> | <i>CH18-C</i> | <i>CH18-D</i> |
| 044h | RS5 | CH5-A | CH5-B | CH5-C | CH5-D | CH17-A | CH17-B | CH17-C | CH17-D |
| | | <i>CH4-A</i> | <i>CH4-B</i> | <i>CH4-C</i> | <i>CH4-D</i> | <i>CH19-A</i> | <i>CH19-B</i> | <i>CH19-C</i> | <i>CH19-D</i> |
| 045h | RS6 | CH6-A | CH6-B | CH6-C | CH6-D | CH18-A | CH18-B | CH18-C | CH18-D |
| | | <i>CH5-A</i> | <i>CH5-B</i> | <i>CH5-C</i> | <i>CH5-D</i> | <i>CH20-A</i> | <i>CH20-B</i> | <i>CH20-C</i> | <i>CH20-D</i> |
| 046h | RS7 | CH7-A | CH7-B | CH7-C | CH7-D | CH19-A | CH19-B | CH19-C | CH19-D |
| | | <i>CH6-A</i> | <i>CH6-B</i> | <i>CH6-C</i> | <i>CH6-D</i> | <i>CH21-A</i> | <i>CH21-B</i> | <i>CH21-C</i> | <i>CH21-D</i> |
| 047h | RS8 | CH8-A | CH8-B | CH8-C | CH8-D | CH20-A | CH20-B | CH20-C | CH20-D |
| | | <i>CH7-A</i> | <i>CH7-B</i> | <i>CH7-C</i> | <i>CH7-D</i> | <i>CH22-A</i> | <i>CH22-B</i> | <i>CH22-C</i> | <i>CH22-D</i> |
| 048h | RS9 | CH9-A | CH9-B | CH9-C | CH9-D | CH21-A | CH21-B | CH21-C | CH21-D |
| | | <i>CH8-A</i> | <i>CH8-B</i> | <i>CH8-C</i> | <i>CH8-D</i> | <i>CH23-A</i> | <i>CH23-B</i> | <i>CH23-C</i> | <i>CH23-D</i> |
| 049h | RS10 | CH10-A | CH10-B | CH10-C | CH10-D | CH22-A | CH22-B | CH22-C | CH22-D |
| | | <i>CH9-A</i> | <i>CH9-B</i> | <i>CH9-C</i> | <i>CH9-D</i> | <i>CH24-A</i> | <i>CH24-B</i> | <i>CH24-C</i> | <i>CH24-D</i> |
| 04Ah | RS11 | CH11-A | CH11-B | CH11-C | CH11-D | CH23-A | CH23-B | CH23-C | CH23-D |
| | | <i>CH10-A</i> | <i>CH10-B</i> | <i>CH10-C</i> | <i>CH10-D</i> | <i>CH25-A</i> | <i>CH25-B</i> | <i>CH25-C</i> | <i>CH25-D</i> |
| 04Bh | RS12 | CH12-A | CH12-B | CH12-C | CH12-D | CH24-A | CH24-B | CH24-C | CH24-D |
| | | <i>CH11-A</i> | <i>CH11-B</i> | <i>CH11-C</i> | <i>CH11-D</i> | <i>CH26-A</i> | <i>CH26-B</i> | <i>CH26-C</i> | <i>CH26-D</i> |
| 04Ch | <i>RS13</i> | — | — | — | — | — | — | — | — |
| | | <i>CH12-A</i> | <i>CH12-B</i> | <i>CH12-C</i> | <i>CH12-D</i> | <i>CH27-A</i> | <i>CH27-B</i> | <i>CH27-C</i> | <i>CH27-D</i> |
| 04Dh | <i>RS14</i> | — | — | — | — | — | — | — | — |
| | | <i>CH13-A</i> | <i>CH13-B</i> | <i>CH13-C</i> | <i>CH13-D</i> | <i>CH28-A</i> | <i>CH28-B</i> | <i>CH28-C</i> | <i>CH28-D</i> |
| 04Eh | <i>RS15</i> | — | — | — | — | — | — | — | — |
| | | <i>CH14-A</i> | <i>CH14-B</i> | <i>CH14-C</i> | <i>CH14-D</i> | <i>CH29-A</i> | <i>CH29-B</i> | <i>CH29-C</i> | <i>CH29-D</i> |
| 04Fh | <i>RS16</i> | — | — | — | — | — | — | — | — |
| | | <i>CH15-A</i> | <i>CH15-B</i> | <i>CH15-C</i> | <i>CH15-D</i> | <i>CH30-A</i> | <i>CH30-B</i> | <i>CH30-C</i> | <i>CH30-D</i> |

| ADDR | NAME | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
|---------------|---------------------------|---------|-----------|---------|---------|---------|---------|--------|--------|
| 050h | LCVCR1 | LCVC15 | LCVC14 | LCVC13 | LCVC12 | LCVC11 | LCVC10 | LCVC9 | LCVC8 |
| 051h | LCVCR2 | LCVC7 | LCVC6 | LCVC5 | LCVC4 | LCVC3 | LCVC2 | LCVC1 | LCVC0 |
| 052h | PCVCR1 | PCVC15 | PCVC14 | PCVC13 | PCVC12 | PCVC11 | PCVC10 | PCVC9 | PCVC8 |
| 053h | PCVCR2 | PCVC7 | PCVC6 | PCVC5 | PCVC4 | PCVC3 | PCVC2 | PCVC1 | PCVC0 |
| 054h | FOSCR1 | FOS15 | FOS14 | FOS13 | FOS12 | FOS11 | FOS10 | FOS9 | FOS8 |
| 055h | FOSCR2 | FOS7 | FOS6 | FOS5 | FOS4 | FOS3 | FOS2 | FOS1 | FOS0 |
| 056h | E1EBCR1 | EB15 | EB14 | EB13 | EB12 | EB11 | EB10 | EB9 | EB8 |
| 057h | E1EBCR2 | EB7 | EB6 | EB5 | EB4 | EB3 | EB2 | EB1 | EB0 |
| 058h | FEACR1 | FEACR15 | FEACR14 | FEACR13 | FEACR12 | FEACR11 | FEACR10 | FEACR9 | FEACR8 |
| 059h | FEACR2 | FEACR7 | FEACR6 | FEACR5 | FEACR4 | FEACR3 | FEACR2 | FEACR1 | FEACR0 |
| 05Ah | FEBCR1 | FEBCR15 | FEBCR14 | FEBCR13 | FEBCR12 | FEBCR11 | FEBCR10 | FEBCR9 | FEBCR8 |
| 05Bh | FEBCR2 | FEBCR7 | FEBCR6 | FEBCR5 | FEBCR4 | FEBCR3 | FEBCR2 | FEBCR1 | FEBCR0 |
| 060h | RDS0M | B1 | B2 | B3 | B4 | B5 | B6 | B7 | B8 |
| 061h | — | — | — | — | — | — | — | — | — |
| 062h | T1RFDL | RFDL7 | RFDL6 | RFDL5 | RFDL4 | RFDL3 | RFDL2 | RFDL1 | RFDL0 |
| | E1RRTS7 | CSC5 | CSC4 | CSC3 | CSC2 | CSC0 | CRC4SA | CASSA | FASSA |
| 063h | T1RBOC | — | — | RBOC5 | RBOC4 | RBOC3 | RBOC2 | RBOC1 | RBOC0 |
| 064h | T1RSLC1 | C8 | C7 | C6 | C5 | C4 | C3 | C2 | C1 |
| | E1RAF | Si | 0 | 0 | 1 | 1 | 0 | 1 | 1 |
| 065h | T1RSLC2 | M2 | M1 | S=0 | S=1 | S=0 | C11 | C10 | C9 |
| | E1RNAF | Si | 1 | A | Sa4 | Sa5 | Sa6 | Sa7 | Sa8 |
| 066h | T1RSLC3 | S=1 | S4 | S3 | S2 | S1 | A2 | A1 | M3 |
| | E1RsiAF | SiF14 | SiF12 | SiF10 | SiF8 | SiF6 | SiF4 | SiF2 | SiF0 |
| 067h | E1RSiNAF | SiF15 | SiF13 | SiF11 | SiF9 | SiF7 | SiF5 | SiF3 | SiF1 |
| 068h | E1RRA | RRAF15 | RRAF13 | RRAF11 | RRAF9 | RRAF7 | RRAF5 | RRAF3 | RRAF1 |
| 069h | E1RSa4 | RSa4F15 | RSa4F13 | RSa4F11 | RSa4F9 | RSa4F7 | RSa4F5 | RSa4F3 | RSa4F1 |
| 06Ah | E1RSa5 | RSa5F15 | RSa5F13 | RSa5F11 | RSa5F9 | RSa5F7 | RSa5F5 | RSa5F3 | RSa5F1 |
| 06Bh | E1RSa6 | RSa6F15 | RSa6F13 | RSa6F11 | RSa6F9 | RSa6F7 | RSa6F5 | RSa6F3 | RSa6F1 |
| 06Ch | E1RSa7 | RSa7F15 | RSa7F13 | RSa7F11 | RSa7F9 | RSa7F7 | RSa7F5 | RSa7F3 | RSa7F1 |
| 06Dh | E1RSa8 | RSa8F15 | RSa8F13 | RSa8F11 | RSa8F9 | RSa8F7 | RSa8F5 | RSa8F3 | RSa8F1 |
| 06Eh | SaBITS | — | — | — | Sa4 | Sa5 | Sa6 | Sa7 | Sa8 |
| 06Fh | Sa6CODE | — | — | — | — | Sa6n | Sa6n | Sa6n | Sa6n |
| 070h– 07Fh | — | — | — | — | — | — | — | — | — |
| 080h | RMMR | FRM_EN | INIT_DONE | DRSS | — | — | — | SFTRST | T1/E1 |
| 081h | RCR1 (T1) | SYNCT | RB8ZS | RFM | ARC | SYNCC | RJC | SYNCE | RESYNC |
| | RCR1 (E1) | — | RHDB3 | RSIGM | RG802 | RCRC4 | FRC | SYNCE | RESYNC |
| 082h | T1RIBCC | — | — | RUP2 | RUP1 | RUP0 | RDN2 | RDN1 | RDN0 |
| | E1RCR2 | — | — | — | — | — | — | — | RLOSA |
| 083h | RCR3 | — | uALAW | RSERC | BINV1 | BINV0 | — | PLB | FLB |
| 084h | RIOCR | RCLKINV | RSYNCCINV | H100EN | RSCLKM | RSMS | RSIO | RSMS2 | RSMS1 |
| | | RCLKINV | RSYNCCINV | H100EN | RSCLKM | — | RSIO | RSMS2 | RSMS1 |
| 085h | RESCR | RDATFMT | RGCLKEN | — | RSZS | RESALGN | RESR | RESMDM | RESE |
| 086h | ERCNT | 1SECS | MCUS | MECU | ECUS | EAMS | FSBE | MOSCRF | LCVCRF |
| | | 1SECS | MCUS | MECU | ECUS | EAMS | — | — | LCVCRF |
| 087h | RHFC | — | — | — | — | — | — | RFHWM1 | RFHWM0 |
| 088h | RIBOC | — | — | — | IBOSEL | IBOEN | — | — | — |
| 089h | T1RSCC | — | — | — | — | — | RSC2 | RSC1 | RSC0 |
| 08Ah | RXPC | RHMS | RHEN | — | — | — | RBPDIR | RBPBUS | RBPEN |
| | | RHMS | RHEN | — | — | — | RBPDIR | — | RBPEN |

| ADDR | NAME | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
|---------------|---------------------------|--------------|--------------|----------------|--------------|--------------|-------------|----------------|--------------|
| 08Bh | RBPBS | BPBSE8 | BPBSE7 | BPBSE6 | BPBSE5 | BPBSE4 | BPBSE3 | BPBSE2 | BPBSE1 |
| 08Ch | — | — | — | — | — | — | — | — | — |
| 08Dh | RHBS | RHBSE8 | RHBSE7 | RHBSE6 | RHBSE5 | RHBSE4 | RHBSE3 | RHBSE2 | RHBSE1 |
| 08Eh– 08Fh | — | — | — | — | — | — | — | — | — |
| 090h | RLS1 | RRAIC | RAISC | RLOSC | RLOFC | RRAID | RAISD | RLOSD | RLOFD |
| 091h | RLS2 (T1) | — | — | COFA | 8ZD | 16ZD | SEFE | B8ZS | FBE |
| | RLS2 (E1) | — | <i>CRCRC</i> | <i>CASRC</i> | <i>FASRC</i> | <i>RSA1</i> | <i>RSA0</i> | <i>RCMF</i> | <i>RAF</i> |
| 092h | RLS3 (T1) | LORCC | LSPC | LDNC | LUPC | LORCD | LSPD | LDND | LUPD |
| | RLS3 (E1) | <i>LORCC</i> | — | <i>V52LNKC</i> | <i>RDMAC</i> | <i>LORCD</i> | — | <i>V52LNKD</i> | <i>RDMAD</i> |
| 093h | RLS4 | RESF | RESEM | RSLIP | — | RSCOS | 1SEC | TIMER | RMF |
| 094h | RLS5 | — | — | ROVR | RHOBT | RPE | RPS | RHWMS | RNES |
| 096h | RLS7 (T1) | — | — | RRAI-CI | RAIS-CI | RSLC96 | RFDLF | BC | BD |
| | RLS7 (E1) | — | — | — | — | — | — | <i>Sa6CD</i> | <i>SaXCD</i> |
| 097h | — | — | — | — | — | — | — | — | — |
| 098h | RSS1 | CH8 | CH7 | CH6 | CH5 | CH4 | CH3 | CH2 | CH1 |
| 099h | RSS2 | CH16 | CH15 | CH14 | CH13 | CH12 | CH11 | CH10 | CH9 |
| 09Ah | RSS3 | CH24 | CH23 | CH22 | CH21 | CH20 | CH19 | CH18 | CH17 |
| 09Bh | RSS4 | — | — | — | — | — | — | — | — |
| | | <i>CH32</i> | <i>CH31</i> | <i>CH30</i> | <i>CH29</i> | <i>CH28</i> | <i>CH27</i> | <i>CH26</i> | <i>CH25</i> |
| 09Ch | T1RSCD1 | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
| | | — | — | — | — | — | — | — | — |
| 09Dh | T1RSCD2 | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
| | | — | — | — | — | — | — | — | — |
| 09Eh | — | — | — | — | — | — | — | — | — |
| 09Fh | RIIR | — | RLS7 | RLS6* | RLS5 | RLS4 | RLS3 | RLS2** | RLS1 |
| 0A0h | RIM1 | RRAIC | RAISC | RLOSC | RLOFC | RRAID | RAISD | RLOSD | RLOFD |
| 0A1h | RIM2 | — | — | — | — | — | — | — | — |
| | | — | — | — | — | <i>RSA1</i> | <i>RSA0</i> | <i>RCMF</i> | <i>RAF</i> |
| 0A2h | RIM3 (T1) | LORCC | LSPC | LDNC | LUPC | LORCD | LSPD | LDND | LUPD |
| | RIM3 (E1) | <i>LORCC</i> | — | <i>V52LNKC</i> | <i>RDMAC</i> | <i>LORCD</i> | — | <i>V52LNKD</i> | <i>RDMAD</i> |
| 0A3h | RIM4 | RESF | RESEM | RSLIP | — | RSCOS | 1SEC | TIMER | RMF |
| 0A4h | RIM5 | — | — | ROVR | RHOBT | RPE | RPS | RHWMS | RNES |
| 0A6h | RIM7 (T1) | — | — | RRAI-CI | RAIS-CI | RSLC96 | RFDLF | BC | BD |
| | RIM7 (E1) | — | — | — | — | — | — | <i>Sa6CD</i> | <i>SaXCD</i> |
| 0A8h | RSCSE1 | CH8 | CH7 | CH6 | CH5 | CH4 | CH3 | CH2 | CH1 |
| 0A9h | RSCSE2 | CH16 | CH15 | CH14 | CH13 | CH12 | CH11 | CH10 | CH9 |
| 0AAh | RSCSE3 | CH24 | CH23 | CH22 | CH21 | CH20 | CH19 | CH18 | CH17 |
| 0ABh | RSCSE4 | — | — | — | — | — | — | — | — |
| | | <i>CH32</i> | <i>CH31</i> | <i>CH30</i> | <i>CH29</i> | <i>CH28</i> | <i>CH27</i> | <i>CH26</i> | <i>CH25</i> |
| 0ACh | T1RUPCD1 | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
| | | — | — | — | — | — | — | — | — |
| 0ADh | T1RUPCD2 | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
| | | — | — | — | — | — | — | — | — |
| 0AEh | T1RDNCD1 | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
| | | — | — | — | — | — | — | — | — |
| 0AFh | T1RDNCD2 | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
| | | — | — | — | — | — | — | — | — |
| 0B0h | RRTS1 | — | — | — | — | RRAI | RAIS | RLOS | RLOF |
| 0B1h | — | — | — | — | — | — | — | — | — |

| ADDR | NAME | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
|---------------|----------------------------|-------|-------|-------|-------|-------|-------|--------|-------------|
| 0B2h | RRTS3 (T1) | — | — | — | — | LORC | LSP | LDN | LUP |
| | RRTS3 (E1) | — | — | — | — | LORC | — | V52LNK | RDMA |
| 0B3h | — | — | — | — | — | — | — | — | — |
| 0B4h | RRTS5 | — | PS2 | PS1 | PS0 | — | — | RHWM | RNE |
| 0B5h | RHPBA | MS | RPBA6 | RPBA5 | RPBA4 | RPBA3 | RPBA2 | RPBA1 | RPBA0 |
| 0B6h | RHF | RHD7 | RHD6 | RHD5 | RHD4 | RHD3 | RHD2 | RHD1 | RHD0 |
| 0B7h– 0BFh | — | — | — | — | — | — | — | — | — |
| 0C0h | RBCS1 | CH8 | CH7 | CH6 | CH5 | CH4 | CH3 | CH2 | CH1 |
| 0C1h | RBCS2 | CH16 | CH15 | CH14 | CH13 | CH12 | CH11 | CH10 | CH9 |
| 0C2h | RBCS3 | CH24 | CH23 | CH22 | CH21 | CH20 | CH19 | CH18 | CH17 |
| 0C3h | RBCS4 | — | — | — | — | — | — | — | — |
| | | CH32 | CH31 | CH30 | CH29 | CH28 | CH27 | CH26 | CH25 |
| 0C4h | RCBR1 | CH8 | CH7 | CH6 | CH5 | CH4 | CH3 | CH2 | CH1 |
| 0C5h | RCBR2 | CH16 | CH15 | CH14 | CH13 | CH12 | CH11 | CH10 | CH9 |
| 0C6h | RCBR3 | CH24 | CH23 | CH22 | CH21 | CH20 | CH19 | CH18 | CH17 |
| 0C7h | RCBR4 | — | — | — | — | — | — | — | — |
| | | CH32 | CH31 | CH30 | CH29 | CH28 | CH27 | CH26 | CH25(F-bit) |
| 0C8h | RSI1 | CH8 | CH7 | CH6 | CH5 | CH4 | CH3 | CH2 | CH1 |
| 0C9h | RSI2 | CH16 | CH15 | CH14 | CH13 | CH12 | CH11 | CH10 | CH9 |
| 0CAh | RSI3 | CH24 | CH23 | CH22 | CH21 | CH200 | CH19 | CH18 | CH17 |
| 0CBh | RSI4 | — | — | — | — | — | — | — | — |
| | | CH32 | CH31 | CH30 | CH29 | CH28 | CH27 | CH26 | CH25 |
| 0CCh | RGCCS1 | CH8 | CH7 | CH6 | CH5 | CH4 | CH3 | CH2 | CH1 |
| 0CDh | RGCCS2 | CH16 | CH15 | CH14 | CH13 | CH12 | CH11 | CH10 | CH9 |
| 0CEh | RGCCS3 | CH24 | CH23 | CH22 | CH21 | CH20 | CH19 | CH18 | CH17 |
| 0CFh | RGCCS4 | — | — | — | — | — | — | — | — |
| | | CH32 | CH31 | CH30 | CH29 | CH28 | CH27 | CH26 | CH25(F-bit) |
| 0D0h | RCICE1 | CH8 | CH7 | CH6 | CH5 | CH4 | CH3 | CH2 | CH1 |
| 0D1h | RCICE2 | CH16 | CH15 | CH14 | CH13 | CH12 | CH11 | CH10 | CH9 |
| 0D2h | RCICE3 | CH24 | CH23 | CH22 | CH21 | CH20 | CH19 | CH18 | CH17 |
| 0D3h | RCICE4 | — | — | — | — | — | — | — | — |
| | | CH32 | CH31 | CH30 | CH29 | CH28 | CH27 | CH26 | CH25 |
| 0D4h | RBPCS1 | CH8 | CH7 | CH6 | CH5 | CH4 | CH3 | CH2 | CH1 |
| 0D5h | RBPCS2 | CH16 | CH15 | CH14 | CH13 | CH12 | CH11 | CH10 | CH9 |
| 0D6h | RBPCS3 | CH24 | CH23 | CH22 | CH21 | CH20 | CH19 | CH18 | CH17 |
| 0D7h | RBPCS4 | — | — | — | — | — | — | — | — |
| | | CH32 | CH31 | CH30 | CH29 | CH28 | CH27 | CH26 | CH25 |
| 0D8h– 0DBh | — | — | — | — | — | — | — | — | — |
| 0DCh | RHCS1 | CH8 | CH7 | CH6 | CH5 | CH4 | CH3 | CH2 | CH1 |
| 0DDh | RHCS2 | CH16 | CH15 | CH14 | CH13 | CH12 | CH11 | CH10 | CH9 |
| 0DEh | RHCS3 | CH24 | CH23 | CH22 | CH21 | CH20 | CH19 | CH18 | CH17 |
| 0DFh | RHCS4 | — | — | — | — | — | — | — | — |
| | | CH32 | CH31 | CH30 | CH29 | CH28 | CH27 | CH26 | CH25 |
| 0E0h– 0EFh | — | — | — | — | — | — | — | — | — |
| 100h | TDMWE1 | CH8 | CH7 | CH6 | CH5 | CH4 | CH3 | CH2 | CH1 |
| 101h | TDMWE2 | CH16 | CH15 | CH14 | CH13 | CH12 | CH11 | CH10 | CH9 |
| 102h | TDMWE3 | CH24 | CH23 | CH22 | CH21 | CH20 | CH19 | CH18 | CH17 |
| 103h | TDMWE4 | CH32 | CH31 | CH30 | CH29 | CH28 | CH27 | CH26 | CH25 |

| ADDR | NAME | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
|---------------|-------------------------|-------|-------|-------|-------|-------|-------|-------|-------|
| 104h | TJBE1 | CH8 | CH7 | CH6 | CH5 | CH4 | CH3 | CH2 | CH1 |
| 105h | TJBE2 | CH16 | CH15 | CH14 | CH13 | CH12 | CH11 | CH10 | CH9 |
| 106h | TJBE3 | CH24 | CH23 | CH22 | CH21 | CH20 | CH19 | CH18 | CH17 |
| 107h | TJBE4 | CH32 | CH31 | CH30 | CH29 | CH28 | CH27 | CH26 | CH25 |
| 108h | TDDS1 | CH8 | CH7 | CH6 | CH5 | CH4 | CH3 | CH2 | CH1 |
| 109h | TDDS2 | CH16 | CH15 | CH14 | CH13 | CH12 | CH11 | CH10 | CH9 |
| 10Ah | TDDS3 | CH24 | CH23 | CH22 | CH21 | CH20 | CH19 | CH18 | CH17 |
| 110h | THC1 | NOFS | TEOML | THR | THMS | TFS | TEOM | TZSD | TCRCD |
| 111h | THBSE | TBSE8 | TBSE7 | TBSE6 | TBSE5 | TBSE4 | TBSE3 | TBSE2 | TBSE1 |
| 112h | — | — | — | — | — | — | — | — | — |
| 113h | THC2 | TABT | SBOC | THCEN | THCS4 | THCS3 | THCS2 | THCS1 | THCS0 |
| | | TABT | — | THCEN | THCS4 | THCS3 | THCS2 | THCS1 | THCS0 |
| 114h | E1TSACR | SiAF | SiNAF | RA | Sa4 | Sa5 | Sa6 | Sa7 | Sa8 |
| 115h– 117h | — | — | — | — | — | — | — | — | — |
| 118h | SSIE1 | CH8 | CH7 | CH6 | CH5 | CH4 | CH3 | CH2 | CH1 |
| 119h | SSIE2 | CH16 | CH15 | CH14 | CH13 | CH12 | CH11 | CH10 | CH9 |
| 11Ah | SSIE3 | CH24 | CH23 | CH22 | CH21 | CH20 | CH19 | CH18 | CH17 |
| 11Bh | SSIE4 | — | — | — | — | — | — | — | — |
| | | CH32 | CH31 | CH30 | CH29 | CH28 | CH27 | CH26 | CH25 |
| 11Ch– 11Fh | — | — | — | — | — | — | — | — | — |
| 120h | TIDR1 | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
| 121h | TIDR2 | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
| 122h | TIDR3 | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
| 123h | TIDR4 | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
| 124h | TIDR5 | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
| 125h | TIDR6 | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
| 126h | TIDR7 | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
| 127h | TIDR8 | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
| 128h | TIDR9 | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
| 129h | TIDR10 | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
| 12Ah | TIDR11 | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
| 12Bh | TIDR12 | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
| 12Ch | TIDR13 | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
| 12Dh | TIDR14 | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
| 12Eh | TIDR15 | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
| 12Fh | TIDR16 | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
| 130h | TIDR17 | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
| 131h | TIDR18 | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
| 132h | TIDR19 | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
| 133h | TIDR20 | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
| 134h | TIDR21 | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
| 135h | TIDR22 | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
| 136h | TIDR23 | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
| 137h | TIDR24 | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
| 138h | TIDR25 | — | — | — | — | — | — | — | — |
| | | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
| 139h | TIDR26 | — | — | — | — | — | — | — | — |
| | | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |

| ADDR | NAME | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
|------|--------|--------|--------|--------|--------|--------|--------|--------|--------|
| 13Ah | TIDR27 | — | — | — | — | — | — | — | — |
| | | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
| 13Bh | TIDR28 | — | — | — | — | — | — | — | — |
| | | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
| 13Ch | TIDR29 | — | — | — | — | — | — | — | — |
| | | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
| 13Dh | TIDR30 | — | — | — | — | — | — | — | — |
| | | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
| 13Eh | TIDR31 | — | — | — | — | — | — | — | — |
| | | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
| 13Fh | TIDR32 | — | — | — | — | — | — | — | — |
| | | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
| 140h | TS1 | CH1-A | CH1-B | CH1-C | CH1-D | CH13-A | CH13-B | CH13-C | CH13-D |
| | | 0 | 0 | 0 | 0 | X | Y | X | X |
| 141h | TS2 | CH2-A | CH2-B | CH2-C | CH2-D | CH14-A | CH14-B | CH14-C | CH14-D |
| | | CH1-A | CH1-B | CH1-C | CH1-D | CH16-A | CH16-B | CH16-C | CH16-D |
| 142h | TS3 | CH3-A | CH3-B | CH3-C | CH3-D | CH15-A | CH15-B | CH15-C | CH15-D |
| | | CH2-A | CH2-B | CH2-C | CH2-D | CH17-A | CH17-B | CH17-C | CH17-D |
| 143h | TS4 | CH4-A | CH4-B | CH4-C | CH4-D | CH16-A | CH16-B | CH16-C | CH16-D |
| | | CH3-A | CH3-B | CH3-C | CH3-D | CH18-A | CH18-B | CH18-C | CH18-D |
| 144h | TS5 | CH5-A | CH5-B | CH5-C | CH5-D | CH17-A | CH17-B | CH17-C | CH17-D |
| | | CH4-A | CH4-B | CH4-C | CH4-D | CH19-A | CH19-B | CH19-C | CH19-D |
| 145h | TS6 | CH6-A | CH6-B | CH6-C | CH6-D | CH18-A | CH18-B | CH18-C | CH18-D |
| | | CH5-A | CH5-B | CH5-C | CH5-D | CH20-A | CH20-B | CH20-C | CH20-D |
| 146h | TS7 | CH7-A | CH7-B | CH7-C | CH7-D | CH19-A | CH19-B | CH19-C | CH19-D |
| | | CH6-A | CH6-B | CH6-C | CH6-D | CH21-A | CH21-B | CH21-C | CH21-D |
| 147h | TS8 | CH8-A | CH8-B | CH8-C | CH8-D | CH20-A | CH20-B | CH20-C | CH20-D |
| | | CH7-A | CH7-B | CH7-C | CH7-D | CH22-A | CH22-B | CH22-C | CH22-D |
| 148h | TS9 | CH9-A | CH9-B | CH9-C | CH9-D | CH21-A | CH21-B | CH21-C | CH21-D |
| | | CH8-A | CH8-B | CH8-C | CH8-D | CH23-A | CH23-B | CH23-C | CH23-D |
| 149h | TS10 | CH10-A | CH10-B | CH10-C | CH10-D | CH22-A | CH22-B | CH22-C | CH22-D |
| | | CH9-A | CH9-B | CH9-C | CH9-D | CH24-A | CH24-B | CH24-C | CH24-D |
| 14Ah | TS11 | CH11-A | CH11-B | CH11-C | CH11-D | CH23-A | CH23-B | CH23-C | CH23-D |
| | | CH10-A | CH10-B | CH10-C | CH10-D | CH25-A | CH25-B | CH25-C | CH25-D |
| 14Bh | TS12 | CH12-A | CH12-B | CH12-C | CH12-D | CH24-A | CH24-B | CH24-C | CH24-D |
| | | CH11-A | CH11-B | CH11-C | CH11-D | CH26-A | CH26-B | CH26-C | CH26-D |
| 14Ch | TS13 | — | — | — | — | — | — | — | — |
| | | CH12-A | CH12-B | CH12-C | CH12-D | CH27-A | CH27-B | CH27-C | CH27-D |
| 14Dh | TS14 | — | — | — | — | — | — | — | — |
| | | CH13-A | CH13-B | CH13-C | CH13-D | CH28-A | CH28-B | CH28-C | CH28-D |
| 14Eh | TS15 | — | — | — | — | — | — | — | — |
| | | CH14-A | CH14-B | CH14-C | CH14-D | CH29-A | CH29-B | CH29-C | CH29-D |
| 14Fh | TS16 | — | — | — | — | — | — | — | — |
| | | CH15-A | CH15-B | CH15-C | CH15-D | CH30-A | CH30-B | CH30-C | CH30-D |
| 150h | TCICE1 | CH8 | CH7 | CH6 | CH5 | CH4 | CH3 | CH2 | CH1 |
| 151h | TCICE2 | CH16 | CH15 | CH14 | CH13 | CH12 | CH11 | CH10 | CH9 |
| 152h | TCICE3 | CH24 | CH23 | CH22 | CH21 | CH20 | CH19 | CH18 | CH17 |
| 153h | TCICE4 | — | — | — | — | — | — | — | — |
| | | CH32 | CH31 | CH30 | CH29 | CH28 | CH27 | CH26 | CH25 |

| ADDR | NAME | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
|-----------|------------------------------|----------------|-----------------|------------------|---------------|---------------|---------------|---------------|---------------|
| 154h–161h | — | — | — | — | — | — | — | — | — |
| 162h | T1TFDL | TFDL7 | TFDL6 | TFDL5 | TFDL4 | TFDL3 | TFDL2 | TFDL1 | TFDL0 |
| | | — | — | — | — | — | — | — | — |
| 163h | T1TBOC | — | — | TBOC5 | TBOC4 | TBOC3 | TBOC2 | TBOC1 | TBOC0 |
| | | — | — | — | — | — | — | — | — |
| 164h | T1TSLC1 | C8 | C7 | C6 | C5 | C4 | C3 | C2 | C1 |
| | E1TAF | <i>Si</i> | 0 | 0 | 1 | 1 | 0 | 1 | 1 |
| 165h | T1TSLC2 | M2 | M1 | S=0 | S=1 | S=0 | C11 | C10 | C9 |
| | E1TNAF | <i>Si</i> | 1 | A | Sa4 | Sa5 | Sa6 | Sa7 | Sa8 |
| 166h | T1TSLC3 | S=1 | S4 | S3 | S2 | S1 | A2 | A1 | M3 |
| | E1TSiAF | <i>TSiF14</i> | <i>TSiF12</i> | <i>TSiF10</i> | <i>TSiF8</i> | <i>TSiF6</i> | <i>TSiF4</i> | <i>TSiF2</i> | <i>TSiF0</i> |
| 167h | E1TSiNAF | — | — | — | — | — | — | — | — |
| | | <i>TsiF15</i> | <i>TSiF13</i> | <i>TSiF11</i> | <i>TSiF9</i> | <i>TSiF7</i> | <i>TSiF5</i> | <i>TSiF3</i> | <i>TSiF1</i> |
| 168h | E1TRA | — | — | — | — | — | — | — | — |
| | | <i>TRAF15</i> | <i>TRAF13</i> | <i>TRAF11</i> | <i>TRAF9</i> | <i>TRAF7</i> | <i>TRAF5</i> | <i>TRAF3</i> | <i>TRAF1</i> |
| 169h | E1TSa4 | — | — | — | — | — | — | — | — |
| | | <i>TSa4F15</i> | <i>TSa4F13</i> | <i>TSa4F11</i> | <i>TSa4F9</i> | <i>TSa4F7</i> | <i>TSa4F5</i> | <i>TSa4F3</i> | <i>TSa4F1</i> |
| 16Ah | E1TSa5 | — | — | — | — | — | — | — | — |
| | | <i>TSa5F15</i> | <i>TSa5F13</i> | <i>TSa5F11</i> | <i>TSa5F9</i> | <i>TSa5F7</i> | <i>TSa5F5</i> | <i>TSa5F3</i> | <i>TSa5F1</i> |
| 16Bh | E1TSa6 | — | — | — | — | — | — | — | — |
| | | <i>TSa6F15</i> | <i>TSa6F13</i> | <i>TSa6F11</i> | <i>TSa6F9</i> | <i>TSa6F7</i> | <i>TSa6F5</i> | <i>TSa6F3</i> | <i>TSa6F1</i> |
| 16Ch | E1TSa7 | — | — | — | — | — | — | — | — |
| | | <i>TSa7F15</i> | <i>TSa7F13</i> | <i>TSa7F11</i> | <i>TSa7F9</i> | <i>TSa7F7</i> | <i>TSa7F5</i> | <i>TSa7F3</i> | <i>TSa7F1</i> |
| 16Dh | E1TSa8 | — | — | — | — | — | — | — | — |
| | | <i>TSa8F15</i> | <i>TSa8F13</i> | <i>TSa8F11</i> | <i>TSa8F9</i> | <i>TSa8F7</i> | <i>TSa8F5</i> | <i>TSa8F3</i> | <i>TSa8F1</i> |
| 16Eh–17Fh | — | — | — | — | — | — | — | — | |
| 180h | TMMR | FRM_EN | INIT_DONE | — | — | — | — | SFTRST | T1/E1 |
| 181h | TCR1 (T1) | TJC | TFPT | TCPT | TSSE | GB7S | TB8ZS | TAIS | TRAI |
| | TCR1 (E1) | <i>TTP</i> | <i>T16S</i> | <i>TG802</i> | <i>TSiS</i> | <i>TSA1</i> | <i>THDB3</i> | <i>TAIS</i> | <i>TCRC4</i> |
| 182h | T1.TCR2 (T1) | TFDLS | TSLC96 | TDDSEN | FBCT2 | FBCT1 | TRAI | — | TB7ZS |
| | E1.TCR2 (E1) | <i>AEBE</i> | <i>AAIS</i> | <i>ARA</i> | — | — | — | — | — |
| 183h | TCR3 | — | — | TCSS1 | TCSS0 | MFRS | TFM | IBPV | TLOOP |
| | | — | — | <i>TCSS1</i> | <i>TCSS0</i> | <i>MFRS</i> | — | <i>IBPV</i> | <i>CRC4R</i> |
| 184h | TIOCR | TCLKINV | TSYNCINV | TSSYNCINV | TSCLKM | TSSM | TSIO | TSDW | TSM |
| | | <i>TCLKINV</i> | <i>TSYNCINV</i> | <i>TSSYNCINV</i> | <i>TSCLKM</i> | <i>TSSM</i> | <i>TSIO</i> | — | <i>TSM</i> |
| 185h | TESCR | TDAFMT | TGCLKEN | — | TSZS | TESALGN | TESR | TESMDM | TESE |
| 186h | TCR4 | <i>uALAW</i> | <i>BINV1</i> | <i>BINV0</i> | <i>TJBEN</i> | <i>TRAIM</i> | <i>TAISM</i> | <i>TC1</i> | <i>TC0</i> |
| | | <i>uALAW</i> | <i>BINV1</i> | <i>BINV0</i> | <i>TJBEN</i> | — | — | — | — |
| 187h | THFC | — | — | — | — | — | — | TFLWM1 | TFLWM0 |
| 188h | TIBOC | — | — | — | IBOSEL | IBOEN | — | — | — |
| 189h | TDS0SEL | — | — | — | TCM4 | TCM3 | TCM2 | TCM1 | TCM0 |
| 18Ah | TXPC | THMS | THEN | — | — | — | TBPDIR | TBPFUS | TBPEN |
| | | <i>THMS</i> | <i>THEN</i> | — | — | — | <i>TBPDIR</i> | — | <i>TBPEN</i> |
| 18Bh | TBPBS | BPBSE8 | BPBSE7 | BPBSE6 | BPBSE5 | BPBSE4 | BPBSE3 | BPBSE2 | BPBSE1 |
| 18Ch | — | — | — | — | — | — | — | — | — |
| 18Dh | THBS | THBSE8 | THBSE7 | THBSE6 | THBSE5 | THBSE4 | THBSE3 | THBSE2 | THBSE1 |

| ADDR | NAME | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
|---------------|------------------------|-------|-------|-------|--------|-------|-------|-------|-----------|
| 18Eh | TSYNCC | — | — | — | — | — | TSEN | SYNCE | RESYNC |
| | | — | — | — | — | CRC4 | TSEN | SYNCE | RESYNC |
| 18Fh | — | — | — | — | — | — | — | — | — |
| 190h | TLS1 | TESF | TESEM | TSLIP | TSLC96 | — | TMF | LOTCC | LOTC |
| | | TESF | TESEM | TSLIP | — | TAF | TMF | LOTCC | LOTC |
| 191h | TLS2 | — | — | — | TFDLE | TUDR | TMEND | TLWMS | TNFS |
| | | — | — | — | — | TUDR | TMEND | TLWMS | TNFS |
| 192h | TLS3 | — | — | — | — | — | — | LOF | LOFD |
| 193h– 19Eh | — | — | — | — | — | — | — | — | — |
| 19Fh | TIIR | — | — | — | — | — | TLS3 | TLS2 | TLS1 |
| 1A0h | TIM1 | TESF | TESEM | TSLIP | TSLC96 | — | TMF | LOTCC | LOTC |
| | | TESF | TESEM | TSLIP | — | TAF | TMF | LOTCC | LOTC |
| 1A1h | TIM2 | — | — | — | TFDLE | TUDR | TMEND | TLWMS | TNFS |
| | | — | — | — | — | TUDR | TMEND | TLWMS | TNFS |
| 1A2h | TIM3 | — | — | — | — | — | — | — | LOFD |
| 1A3h– 1ABh | — | — | — | — | — | — | — | — | — |
| 1ACh | T1TCD1 | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
| | | — | — | — | — | — | — | — | — |
| 1ADh | T1TCD2 | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
| | | — | — | — | — | — | — | — | — |
| 1AEh– 1B0h | — | — | — | — | — | — | — | — | — |
| 1B1h | TRTS2 | — | — | — | — | EMPTY | TFULL | TLWM | TNF |
| 1B2h | — | — | — | — | — | — | — | — | — |
| 1B3h | TFBA | — | TFBA6 | TFBA5 | TFBA4 | TFBA3 | TFBA2 | TFBA1 | TFBA0 |
| 1B4h | THF | THD7 | THD6 | THD5 | THD4 | THD3 | THD2 | THD1 | THD0 |
| 1B5h– 1BAh | — | — | — | — | — | — | — | — | — |
| 1BBh | TDS0M | B1 | B2 | B3 | B4 | B5 | B6 | B7 | B8 |
| 1BCh– 1BFh | — | — | — | — | — | — | — | — | — |
| 1C0h | TBCS1 | CH8 | CH7 | CH6 | CH5 | CH4 | CH3 | CH2 | CH1 |
| 1C1h | TBCS2 | CH16 | CH15 | CH14 | CH13 | CH12 | CH11 | CH10 | CH9 |
| 1C2h | TBCS3 | CH24 | CH23 | CH22 | CH21 | CH20 | CH19 | CH18 | CH17 |
| 1C3h | TBCS4 | — | — | — | — | — | — | — | — |
| | | CH32 | CH31 | CH30 | CH29 | CH28 | CH27 | CH26 | CH25 |
| 1C4h | TCBR1 | CH8 | CH7 | CH6 | CH5 | CH4 | CH3 | CH2 | CH1 |
| 1C5h | TCBR2 | CH16 | CH15 | CH14 | CH13 | CH12 | CH11 | CH10 | CH9 |
| 1C6h | TCBR3 | CH24 | CH23 | CH22 | CH21 | CH20 | CH19 | CH18 | CH17 |
| 1C7h | TCBR4 | — | — | — | — | — | — | — | — |
| | | CH32 | CH31 | CH30 | CH29 | CH28 | CH27 | CH26 | CH25:Fbit |
| 1C8h | THSCS1 | CH8 | CH7 | CH6 | CH5 | CH4 | CH3 | CH2 | CH1 |
| 1C9h | THSCS2 | CH16 | CH15 | CH14 | CH13 | CH12 | CH11 | CH10 | CH9 |
| 1CAh | THSCS3 | CH24 | CH23 | CH22 | CH21 | CH20 | CH19 | CH18 | CH17 |
| 1CBh | THSCS4 | — | — | — | — | — | — | — | — |
| | | CH32 | CH31 | CH30 | CH29 | CH28 | CH27 | CH26 | CH25 |
| 1CCh | TGCCS1 | CH8 | CH7 | CH6 | CH5 | CH4 | CH3 | CH2 | CH1 |
| 1CDh | TGCCS2 | CH16 | CH15 | CH14 | CH13 | CH12 | CH11 | CH10 | CH9 |
| 1CEh | TGCCS3 | CH24 | CH23 | CH22 | CH21 | CH20 | CH19 | CH18 | CH17 |

| ADDR | NAME | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
|---------------|------------------------|-------|-------|-------|-------|-------|-------|-------|-------------|
| 1CFh | TGCCS4 | — | — | — | — | — | — | — | — |
| | | CH32 | CH31 | CH30 | CH29 | CH28 | CH27 | CH26 | CH25(F-bit) |
| 1D0h | PCL1 | CH8 | CH7 | CH6 | CH5 | CH4 | CH3 | CH2 | CH1 |
| 1D1h | PCL2 | CH16 | CH15 | CH14 | CH13 | CH12 | CH11 | CH10 | CH9 |
| 1D2h | PCL3 | CH24 | CH23 | CH22 | CH21 | CH20 | CH19 | CH18 | CH17 |
| 1D3h | PCL4 | — | — | — | — | — | — | — | — |
| | | CH32 | CH31 | CH30 | CH29 | CH28 | CH27 | CH26 | CH25 |
| 1D4h | TBPCS1 | CH8 | CH7 | CH6 | CH5 | CH4 | CH3 | CH2 | CH1 |
| 1D5h | TBPCS2 | CH16 | CH15 | CH14 | CH13 | CH12 | CH11 | CH10 | CH9 |
| 1D6h | TBPCS3 | CH24 | CH23 | CH22 | CH21 | CH20 | CH19 | CH18 | CH17 |
| 1D7h | TBPCS4 | — | — | — | — | — | — | — | — |
| | | CH32 | CH31 | CH30 | CH29 | CH28 | CH27 | CH26 | CH25 |
| 1DCh | THCS1 | CH8 | CH7 | CH6 | CH5 | CH4 | CH3 | CH2 | CH1 |
| 1DDh | THCS2 | CH16 | CH15 | CH14 | CH13 | CH12 | CH11 | CH10 | CH9 |
| 1DEh | THCS3 | CH24 | CH23 | CH22 | CH21 | CH20 | CH19 | CH18 | CH17 |
| 1DFh | THCS4 | — | — | — | — | — | — | — | — |
| | | CH32 | CH31 | CH30 | CH29 | CH28 | CH27 | CH26 | CH32 |
| 1E0h– 1FFh | — | — | — | — | — | — | — | — | — |

*RLS6 is reserved for future use.

**Currently, RLS2 does not create an interrupt, therefore this bit is not used in T1 mode.

10.2.3 LIU Register Bit Map

Table 10-9. LIU Register Bit Map

| ADDR | NAME | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
|-----------------|------------------------|---------|---------|--------|--------|---------|--------|---------|--------|
| 1000h | LTRCR | — | RHPM | JADS1 | JADS0 | JAPS1 | JAPS0 | T1J1E1S | LSC |
| 1001h | LTIPSR | TG703 | TIMPTON | TIMPL1 | TIMPL0 | — | L2 | L1 | L0 |
| 1002h | LMCR | TAIS | ATAIS | LB2 | LB1 | LB0 | TPDE | RPDE | TE |
| 1003h | LRSR | — | — | OEQ | UEQ | RSCS | TSCS | OCS | LOSS |
| 1004h | LSIMR | JALTCIM | OCCIM | SCCIM | LOSCIM | JALTSIM | OCDIM | SCDIM | LOSDIM |
| 1005h | LLSR | JALTC | OCC | SCC | LOSC | JALTS | OCD | SCD | LOSD |
| 1006h | LRSL | RSL3 | RSL2 | RLS1 | RLS0 | — | — | — | — |
| 1007h | LRISMR | — | RIMPON | — | — | — | RIMP2 | RIMP1 | RIMP0 |
| 1008h | LRRCR | RG703 | — | — | — | RTR | RMONEN | RSMS1 | RSMS0 |
| 1009h– 101Fh | Test Registers | — | — | — | — | — | — | — | — |

10.2.4 BERT Register Bit Map

Table 10-10. BERT Register Bit Map

| ADDR | NAME | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
|-------|-----------------------|--------|--------|--------|--------|--------|--------|--------|--------|
| 1100h | BAWC | ACNT7 | ACNT6 | ACNT5 | ACNT4 | ACNT3 | ACNT2 | ACNT1 | ACNT0 |
| 1101h | BRP1 | RPAT7 | RPAT6 | RPAT5 | RPAT4 | RPAT3 | RPAT2 | RPAT1 | RPAT0 |
| 1102h | BRP2 | RPAT15 | RPAT14 | RPAT13 | RPAT12 | RPAT11 | RPAT10 | RPAT9 | RPAT8 |
| 1103h | BRP3 | RPAT23 | RPAT22 | RPAT21 | RPAT20 | RPAT19 | RPAT18 | RPAT17 | RPAT16 |
| 1104h | BRP4 | RPAT31 | RPAT30 | RPAT29 | RPAT28 | RPAT27 | RPAT26 | RPAT25 | RPAT24 |
| 1105h | BC1 | TC | TINV | RINV | PS2 | PS1 | PS0 | LC | RESYNC |
| 1106h | BC2 | EIB2 | EIB1 | EIB0 | SBE | RPL3 | RPL2 | RPL1 | RPL0 |
| 1107h | BBC1 | BBC7 | BBC6 | BBC5 | BBC4 | BBC3 | BBC2 | BBC1 | BBC0 |
| 1108h | BBC2 | BBC15 | BBC14 | BBC13 | BBC12 | BBC11 | BBC10 | BBC9 | BBC8 |
| 1109h | BBC3 | BBC23 | BBC22 | BBC21 | BBC20 | BBC19 | BBC18 | BBC17 | BBC16 |
| 110Ah | BBC4 | BBC31 | BBC30 | BBC29 | BBC28 | BBC27 | BBC26 | BBC25 | BBC24 |
| 110Bh | BEC1 | EC7 | EC6 | EC5 | EC4 | EC3 | EC2 | EC1 | EC0 |
| 110Ch | BEC2 | EC15 | EC14 | EC13 | EC12 | EC11 | EC10 | EC9 | EC8 |
| 110Dh | BEC3 | EC23 | EC22 | EC21 | EC20 | EC19 | EC18 | EC17 | EC16 |
| 110Eh | BSR | — | BBED | RBA01 | RSYNC | BRA1 | BRA0 | BRLOS | BSYNC |
| 110Fh | BSIM | — | BBED | — | — | BRA1 | BRA0 | BRLOS | BSYNC |
| 1400h | BC3 | — | — | — | — | — | — | 55OCT | BALIGN |
| 1401h | BRSR | — | — | — | — | BRA1 | BRA0 | BRLOS | BSYNC |
| 1402h | BLSR1 | BRA1C | BRA0C | BRLOSC | BSYNCC | BRA1D | BRA0D | BRLOSD | BSYNCD |
| 1403h | BSIM1 | BRA1C | BRA0C | BRLOSC | BSYNCC | BRA1D | BRA0D | BRLOSD | BSYNCD |
| 1404h | BLSR2 | — | — | — | — | — | BED | BBCO | BECO |
| 1405h | BSIM2 | — | — | — | — | — | BED | BBCO | BECO |

10.2.5 HDLC-256 Register Bit Map

Table 10-11. HDLC-256 Register Bit Map

| ADDR | NAME | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
|-----------------|---------------------------|-------|-------|-------|-------|-------|-------|-------|--------|
| 1500h | TH256CR1 | — | TPSD | TFEI | TIFV | TBRE | TDIE | TFPD | TFRST |
| 1501h | TH256CR2 | — | — | — | TDAL4 | TDAL3 | TDAL2 | TDAL1 | TDAL0 |
| 1502h | TH256FDR1 | — | — | — | — | — | — | — | TDPE |
| 1503h | TH256FDR2 | TFD7 | TFD6 | TFD5 | TFD4 | TFD3 | TFD2 | TFD1 | TFD0 |
| 1504h | TH256SR1 | — | — | — | — | — | TFF | TFE | THDA |
| 1505h | TH256SR2 | — | — | TFFL5 | TFFL4 | TFFL3 | TFFL2 | TFFL1 | TFFL0 |
| 1506h | TH256SRL | — | — | TFOL | TFUL | TPEL | — | TFEL | THDAL |
| 1507h | — | — | — | — | — | — | — | — | — |
| 1508h | TH256SRIE | — | — | TFOIE | TFUIE | TPEIE | — | TFEIE | THDAIE |
| 1509h– 150Fh | — | — | — | — | — | — | — | — | — |
| 1510h | RH256CR1 | — | — | — | — | RBRE | RDIE | RFPD | RFRST |
| 1511h | RH256CR2 | — | — | — | RDAL4 | RDAL3 | RDAL2 | RDAL1 | RDAL0 |
| 1512h | — | — | — | — | — | — | — | — | — |
| 1513h | — | — | — | — | — | — | — | — | — |
| 1514h | RH256SR | — | — | — | — | — | RFF | RFE | RHDA |
| 1515h | — | — | — | — | — | — | — | — | — |
| 1516h | RH256SRL | RFOL | — | — | RPEL | RPSL | RFFL | — | RHDAL |
| 1517h | — | — | — | — | — | — | — | — | — |
| 1518h | RH256SRIE | RFOIE | — | — | RPEIE | RPSIE | RFFIE | — | RHDAIE |
| 1519h | — | — | — | — | — | — | — | — | — |
| 151Ah | — | — | — | — | — | — | — | — | — |
| 151Bh | — | — | — | — | — | — | — | — | — |
| 151Ch | RH256FDR1 | — | — | — | — | RPS2 | RPS1 | RPS0 | RFDV |
| 151Dh | RH256FDR2 | RFD7 | RFD6 | RFD5 | RFD4 | RFD3 | RFD2 | RFD1 | RFD0 |
| 151Eh | — | — | — | — | — | — | — | — | — |
| 151Fh | — | — | — | — | — | — | — | — | — |

10.3 Global Register Definitions

Functions contained in the global registers include: framer reset, LIU reset, device ID, BERT interrupt status, framer interrupt status, IBO configuration, MCLK configuration, and BPCLK1 configuration. The global registers bit descriptions are presented below.

Table 10-12. Global Register Set

| ADDRESS | NAME | DESCRIPTION | R/W |
|---------|------------------------|---|-----|
| 00F0h | GTCCR1 | Global Transceiver Control Register 1 | R/W |
| 00F1h | GFCR1 | Global Framer Control Register 1 | R/W |
| 00F2h | GTCCR3 | Global Transceiver Control Register 3 | R/W |
| 00F3h | GTCCR1 | Global Transceiver Clock Control Register 1 | R/W |
| 00F4h | GTCCR3 | Global Transceiver Clock Control Register 3 | R/W |
| 00F5h | GHISR | Global HDLC-256 Interrupt Status Register | R |
| 00F6h | GSRR1 | Global Software Reset Register 1 | R/W |
| 00F7h | GHIMR | Global HDLC-256 Interrupt Mask Register | R/W |
| 00F8h | IDR | Device Identification Register | R |
| 00F9h | GFISR1 | Global Framer Interrupt Status Register 1 | R |
| 00FAh | GBISR1 | Global BERT Interrupt Status Register 1 | R |
| 00FBh | GLISR1 | Global LIU Interrupt Status Register 1 | R |
| 00FCh | GFIMR1 | Global Framers Interrupt Mask Register 1 | R/W |
| 00FDh | GBIMR1 | Global BERT Interrupt Mask Register 1 | R/W |
| 00FEh | GLIMR1 | Global LIU Interrupt Mask Register 1 | R/W |

Note 1: Reserved registers should only be written with all zeros.

Note 2: The global registers are located in the framer address space. The corresponding address space for the other seven framers is "Reserved" and should be initialized with all zeros for proper operation.

Register Name **GTCR1**
 Register Description: **Global Transceiver Control Register 1**
 Register Address: **00F0h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|--------|--------|--------|---|-------|------|------|------|
| Name | GPSEL3 | GPSEL2 | GPSEL1 | — | 528MD | GIBO | GCLE | GIPI |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 7 to 5: General-Purpose I/O Pins Select (GPSEL[3:1])

Table 10-13. Output Status Control

| GPSEL[3:1] | RLF/LTC[8:1] | AL/RSIGF/FLOS[8:1] |
|------------|--------------|--------------------|
| 000 | RLF | AL |
| 001 | LTC | AL |
| 010 | RLF | RSIGF |
| 011 | LTC | RSIGF |
| 100 | RLF | FLOS |
| 101 | LTC | FLOS |
| 110 | Reserved | Reserved |
| 111 | Reserved | Reserved |

Bit 3: DS26528 Mode (528MD)

0 = Normal operation.

1 = Pin definitions switch to DS26528 pins to obtain pin compatibility with the DS26528.

| Normal Operation | 528MD |
|---------------------|--------------------|
| RSYSCLK[8:2] | RLF/LTC[8:2] |
| RSYSCLK1 | RSYSCLK1 |
| CLKO | RLF/LTC1 |
| TSYSCLK[8:2] | AL/RSIGF/FLOS[8:2] |
| TSYSCLK1 | TSYSCLK1 |
| SPI_SEL | AL/RSIGF/FLOS1 |
| TSYNC/TSSYNCIO[8:1] | TSYNC[8:1] |
| (Tie low—unused) | TSSYNCIO |

Bit 2: Ganged IBO Enable (GIBO). This bit is used to select either the internal mux for IBO operation or an external “wire-OR” operation. Normally this bit should be set = 0 and the internal mux used.

0 = Use internal IBO mux.

1 = Externally “wire-OR” TSERn and RSERn for IBO operation.

Note: Setting GIBO disables the internal IBO mux. [GFCR1](#) must be set to inform the framers of the IBO configuration.

Bit 1: Global Counter Latch Enable (GCLE). A low-to-high transition on this bit will, when enabled, latch the framer performance monitor counters. Each framer can be independently enabled to accept this input. This bit must be cleared and set again to perform another counter latch.

Bit 0: Global Interrupt Pin Inhibit (GIPI)

0 = Normal Operation. Interrupt pin ($\overline{\text{INTB}}$) will toggle low on an unmasked interrupt condition.

1 = Interrupt Inhibit. Interrupt pin ($\overline{\text{INTB}}$) is forced high (inactive) when this bit is set.

Register Name: **GFCR1**
 Description: **Global Framer Control Register 1**
 Register Address: **00F1h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|--------|--------|--------|--------|---|-------|-------|-------|
| Name | IBOMS1 | IBOMS0 | BPCLK1 | BPCLK0 | — | RFMSS | TCBCS | RCBCS |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 7 and 6: Interleave Bus Operation Mode Select 1 and 0 (IBOMS[1:0]). These bits determine the configuration of the IBO (interleaved bus) multiplexer and inform the framers of the IBO configuration. These bits should be used in conjunction with the Rx and Tx IBO control registers within each of the framer units. These bits control Channels 1 to 8. Additional information concerning the IBO multiplexer is given in Section [9.8.2](#). These bits must be set whether using the internal IBO mux or externally ganging the pins.

| IBOMS1 | IBOMS0 | IBO Mode |
|--------|--------|-------------------------------|
| 0 | 0 | IBO disabled. |
| 0 | 1 | 2 devices on bus (4.096MHz). |
| 1 | 0 | 4 devices on bus (8.192MHz). |
| 1 | 1 | 8 devices on bus (16.384MHz). |

Bits 5 and 4: Backplane Clock Select 1 and 0 (BPCLK[1:0]). These bits determine the clock frequency output on the BPCLK1 pin.

| BPCLK1 | BPCLK0 | BPCLK1 Frequency |
|--------|--------|------------------|
| 0 | 0 | 2.048MHz |
| 0 | 1 | 4.096MHz |
| 1 | 0 | 8.192MHz |
| 1 | 1 | 16.384MHz |

Bit 2: Receive Frame/Multiframe Sync Select (RFMSS). This bit controls the function of all eight RMSYNcn/RFSYNcn pins.

- 0 = RMSYNC/RFSYNC[8:1] pins output RFSYNC[8:1] (Receive Frame Sync)
- 1 = RMSYNC/RFSYNC[8:1] pins output RMSYNC[8:1] (Receive Multiframe Sync)

Bit 1: Transmit Channel Block/Clock Select (TCBCS). This bit controls the function of all eight TCHBLKn/TCHCLKn pins.

- 0 = TCHBLK/TCHCLK[8:1] pins output TCHBLK[8:1] (Transmit Channel Block)
- 1 = TCHBLK/TCHCLK[8:1] pins output TCHCLK[8:1] (Transmit Channel Clock)

Bit 0: Receive Channel Block/Clock Select (RCBCS). This bit controls the function of all eight RCHBLKn/RCHCLKn pins.

- 0 = RCHBLK/RCHCLK[8:1] pins output RCHBLK[8:1] (Receive Channel Block)
- 1 = RCHBLK/RCHCLK[8:1] pins output RCHCLK[8:1] (Receive Channel Clock)

Register Name: **GTCR3**
 Register Description: **Global Transceiver Control Register 3**
 Register Address: **00F2h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|---|---|---|---|---|-------------|----------|
| Name | — | — | — | — | — | — | TSSYNCEOSEL | TSYNCSEL |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 1: Transmit System Synchronization I/O Select (TSSYNCEOSEL)

0 = TSSYNCEO[8:1] are inputs on TSYNC/TSSYNCEO[8:1] pins
 1 = TSSYNCEO[8:1] are outputs synchronous to BPCLK1.

Bit 0: TSYNCn/TSSYNCEO Pin Select (TSYNCSEL)

0 = TSYNCn is selected for TSYNC/TSSYNCEO[8:1] pins
 1 = TSSYNCEO is selected for TSYNC/TSSYNCEO[8:1] pins

Note: If TSYNCn is selected, control of TSYNCn (I/O) is via the [TIOCR](#) register. TSSYNCEO is normally selected when transmit elastic stores are enabled.

Register Name: **GTCCR1**
 Register Description: **Global Transceiver Clock Control Register 1**
 Register Address: **00F3h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|-----------|-----------|-----------|-----------|----------|---------|------|------|
| Name | BPREFSEL3 | BPREFSEL2 | BPREFSEL1 | BPREFSEL0 | BFREQSEL | FREQSEL | MPS1 | MPS0 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 7 to 4: Backplane Clock Reference Selects (BPREFSEL[3:0]). These bits select which reference clock source will be used for BPCLK1 generation. The BPCLK1 can be generated from LIU's 1 to 8 recovered clocks, an external reference, or derivatives of MCLK input. This is shown in [Table 10-15](#). See [Figure 9-9](#) for additional information.

Bit 3: Backplane Frequency Select (BFREQSEL). In conjunction with BPRFSEL[3:0], this bit identifies the reference clock frequency used by the DS26518 backplane clock generation circuit. Note that the setting of this bit should match the T1E1 selection for the LIU whose recovered clock is being used to generate the backplane clock. See [Figure 9-9](#) for additional information.

0 = Backplane reference clock is 2.048MHz.

1 = Backplane reference clock is 1.544MHz.

Bit 2: Frequency Selection (FREQSEL). In conjunction with the MPS[1:0] bits, this bit selects the external MCLK frequency of the signal input at the MCLK pin of the DS26518.

0 = The external master clock is 2.048MHz or multiple thereof.

1 = The external master clock is 1.544MHz or multiple thereof.

Bits 1 and 0: Master Period Select 1 and 0 (MPS[1:0]). In conjunction with the FREQSEL bit, these bits select the external MCLK frequency of the signal input at the MCLK pin of the DS26518. This is shown in [Table 10-14](#).

Table 10-14. Master Clock Input Selection

| FREQSEL | MPS1 | MPS0 | MCLK (MHz \pm 50ppm) |
|---------|------|------|---------------------------|
| 0 | 0 | 0 | 2.048 |
| 0 | 0 | 1 | 4.096 |
| 0 | 1 | 0 | 8.192 |
| 0 | 1 | 1 | 16.384 |
| 1 | 0 | 0 | 1.544 |
| 1 | 0 | 1 | 3.088 |
| 1 | 1 | 0 | 6.176 |
| 1 | 1 | 1 | 12.352 |

Table 10-15. Backplane Reference Clock Select

| BPREFSEL3 | BPREFSEL2 | BPREFSEL1 | BPREFSEL0 | BFREQSEL | REFERENCE CLOCK SOURCE |
|-----------|-----------|-----------|-----------|----------|--|
| 0 | 0 | 0 | 0 | 0 | 2.048MHz RCLK1 |
| 0 | 0 | 0 | 0 | 1 | 1.544MHz RCLK1 |
| 0 | 0 | 0 | 1 | 0 | 2.048MHz RCLK2 |
| 0 | 0 | 0 | 1 | 1 | 1.544MHz RCLK2 |
| 0 | 0 | 1 | 0 | 0 | 2.048MHz RCLK3 |
| 0 | 0 | 1 | 0 | 1 | 1.544MHz RCLK3 |
| 0 | 0 | 1 | 1 | 0 | 2.048MHz RCLK4 |
| 0 | 0 | 1 | 1 | 1 | 1.544MHz RCLK4 |
| 0 | 1 | 0 | 0 | 0 | 2.048MHz RCLK5 |
| 0 | 1 | 0 | 0 | 1 | 1.544MHz RCLK5 |
| 0 | 1 | 0 | 1 | 0 | 2.048MHz RCLK6 |
| 0 | 1 | 0 | 1 | 1 | 1.544MHz RCLK6 |
| 0 | 1 | 1 | 0 | 0 | 2.048MHz RCLK7 |
| 0 | 1 | 1 | 0 | 1 | 1.544MHz RCLK7 |
| 0 | 1 | 1 | 1 | 0 | 2.048MHz RCLK8 |
| 0 | 1 | 1 | 1 | 1 | 1.544MHz RCLK8 |
| 1 | 0 | 0 | 0 | 0 | 2.048MHz derived from MCLK. (REFCLKIO is an output.) |
| 1 | 0 | 0 | 0 | 1 | 1.544MHz derived from MCLK. (REFCLKIO is an output.) |
| 1 | 0 | 0 | 1 | 0 | 2.048MHz external clock input at REFCLKIO. (REFCLKIO is an input.) |
| 1 | 0 | 0 | 1 | 1 | 1.544MHz external clock input at REFCLKIO. (REFCLKIO is an input.) |

Register Name: **GTCCR3**
 Register Description: **Global Transceiver Clock Control Register 3**
 Register Address: **00F4h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|------------|------------|---------|---------|---------|---------|---------|
| Name | — | RSYSCLKSEL | TSYSCLKSEL | TCLKSEL | CKOSEL3 | CKOSEL2 | CKOSEL1 | CKOSEL0 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 6: RSYCLKn Select (RSYSCLKSEL)

- 0 = Use RSYCLKn pins for each receive system clock (Channels 1–8).
- 1 = Use BPCLK1 as the master clock for all eight receive system clocks (Channels 1–8).

Bit 5: TSYSCLKn Select (TSYSCLKSEL)

- 0 = Use TSYSCLKn pins for each transmit system clock (Channels 1–8).
- 1 = Use BPCLK1 as the master clock for all eight transmit system clocks (Channels 1–8).

Bit 4: TCLKn Select (TCLKSEL)

- 0 = Use TCLKn pins for each of the transmit clock (Channels 1–8).
- 1 = Use REFCLKIO as the master clock for all eight transmit clocks (Channels 1–8).

Bits 3 to 0: Clock Out Frequency Select (CKOSEL[3:0]). CLKO output pin will use MCLK (1.544MHz or 2.048MHz or scaled version) as its reference. The following table shows how to configure for each frequency. For best jitter performance use a 2.048MHz oscillator for MCLK.

| CKOSEL[3:0] | CLKO (kHz) |
|-------------|------------|
| 0000 | 2048 |
| 0001 | 4096 |
| 0010 | 8192 |
| 0011 | 16384 |
| 0100 | 1544 |
| 0101 | 3088 |
| 0110 | 6176 |
| 0111 | 12352 |
| 1000 | 1536 |
| 1001 | 3072 |
| 1010 | 6144 |
| 1011 | 12288 |
| 1100 | 32 |
| 1101 | 64 |
| 1110 | 128 |
| 1111 | 256 |

Register Name: **GHISR**
 Register Description: **Global HDLC-256 Interrupt Status Register**
 Register Address: **00F5h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|------|------|------|------|------|------|------|------|
| Name | HIS8 | HIS7 | HIS6 | HIS5 | HIS4 | HIS3 | HIS2 | HIS1 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

The GHISR register reports the HDLC-256 interrupt status for Channels 1 through 8. A logic one in the associated bit location indicates an HDLC-256 has set its interrupt signal.

Bit 7: HDLC-256 Interrupt Status 8 (HIS8)

0 = HDLC-256 8 has not issued an interrupt.
 1 = HDLC-256 8 has issued an interrupt.

Bit 6: HDLC-256 Interrupt Status 7 (HIS7)

0 = HDLC-256 7 has not issued an interrupt.
 1 = HDLC-256 7 has issued an interrupt.

Bit 5: HDLC-256 Interrupt Status 6 (HIS6)

0 = HDLC-256 6 has not issued an interrupt.
 1 = HDLC-256 6 has issued an interrupt.

Bit 4: HDLC-256 Interrupt Status 5 (HIS5)

0 = HDLC-256 5 has not issued an interrupt.
 1 = HDLC-256 5 has issued an interrupt.

Bit 3: HDLC-256 Interrupt Status 4 (HIS4)

0 = HDLC-256 4 has not issued an interrupt.
 1 = HDLC-256 4 has issued an interrupt.

Bit 2: HDLC-256 Interrupt Status 3 (HIS3)

0 = HDLC-256 3 has not issued an interrupt.
 1 = HDLC-256 3 has issued an interrupt.

Bit 1: HDLC-256 Interrupt Status 2 (HIS2)

0 = HDLC-256 2 has not issued an interrupt.
 1 = HDLC-256 2 has issued an interrupt.

Bit 0: HDLC-256 Interrupt Status 1 (HIS1)

0 = HDLC-256 1 has not issued an interrupt.
 1 = HDLC-256 1 has issued an interrupt.

Register Name: **GSRR1**
 Register Description: **Global Software Reset Register 1**
 Register Address: **00F6h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|---|---|---|---------|------|------|------|
| Name | — | — | — | — | H256RST | LRST | BRST | FRST |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 3: HDLC-256 Software Reset (H256RST). HDLC-256 Channels 1–8 logic and registers are reset with a 0-to-1 transition in this bit. The reset is released when a zero is written to this bit.

0 = Normal operation.

1 = Reset HDLC-256 channels 1–8.

Note: HDLC-64 circuits are reset by the framer software reset.

Bit 2: LIU Software Reset (LRST). LIU Channels 1–8 logic and registers are reset with a 0-to-1 transition in this bit. The reset is released when a zero is written to this bit.

0 = Normal operation.

1 = Reset LIU channels 1–8.

Bit 1: BERT Software Reset (BRST). BERT Channels 1–8 logic and registers are reset with a 0-to-1 transition in this bit. The reset is released when a zero is written to this bit.

0 = Normal operation.

1 = Reset BERT channels 1–8.

Bit 0: Framer Software Reset (FRST). Framers 1-8 to logic and registers are reset with a 0-to-1 transition in this bit. The reset is released when a zero is written to this bit.

0 = Normal operation.

1 = Reset framers 1–8.

Register Name: **GHIMR**
 Register Description: **Global HDLC-256 Interrupt Mask Register**
 Register Address: **00F7h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|------|------|------|------|------|------|------|------|
| Name | HIM8 | HIM7 | HIM6 | HIM5 | HIM4 | HIM3 | HIM2 | HIM1 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7: HDLC-256 Interrupt Mask 8 (HIM8)

0 = Interrupt masked.
 1 = Interrupt enabled.

Bit 6: HDLC-256 Interrupt Mask 7 (HIM7)

0 = Interrupt masked.
 1 = Interrupt enabled.

Bit 5: HDLC-256 Interrupt Mask 6 (HIM6)

0 = Interrupt masked.
 1 = Interrupt enabled.

Bit 4: HDLC-256 Interrupt Mask 5 (HIM5)

0 = Interrupt masked.
 1 = Interrupt enabled.

Bit 3: HDLC-256 Interrupt Mask 4 (HIM4)

0 = Interrupt masked.
 1 = Interrupt enabled.

Bit 2: HDLC-256 Interrupt Mask 3 (HIM3)

0 = Interrupt masked.
 1 = Interrupt enabled.

Bit 1: HDLC-256 Interrupt Mask 2 (HIM2)

0 = Interrupt masked.
 1 = Interrupt enabled.

Bit 0: HDLC-256 Interrupt Mask 1 (HIM1)

0 = Interrupt masked.
 1 = Interrupt enabled.

Register Name: **IDR**
 Register Description: **Device Identification Register**
 Register Address: **00F8h**

| | | | | | | | | |
|---------|-----|-----|-----|-----|-----|-----|-----|-----|
| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | ID7 | ID6 | ID5 | ID4 | ID3 | ID2 | ID1 | ID0 |
| Default | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 |

Bits 7 to 3: Device ID (ID[7:3]). The upper five bits of the IDR are used to display the DS26518 ID.

Table 10-16. Device ID Codes in this Product Family

| DEVICE | ID7 | ID6 | ID5 | ID4 | ID3 |
|---------|-----|-----|-----|-----|-----|
| DS26519 | 1 | 1 | 0 | 1 | 1 |
| DS26518 | 1 | 1 | 0 | 1 | 0 |
| | | | | | |
| DS26528 | 0 | 1 | 0 | 1 | 1 |
| DS26524 | 0 | 1 | 1 | 0 | 0 |
| DS26522 | 0 | 1 | 1 | 0 | 1 |
| DS26521 | 0 | 1 | 1 | 1 | 0 |

Bits 2 to 0: Silicon Revision Bits (ID[2:0]). The lower three bits of the IDR are used to display a sequential number denoting the die revision of the chip. The initial silicon revision = "000" and is incremented with each silicon revision. This value is not the same as the two-character device revision on the top brand of the device. This is due to the fact that portions of the device assembly other than the silicon may change, causing the device revision increment on the brand without having a revision of the silicon. ID0 is the LSB of a decimal code that represents the chip revision.

Register Name: **GFISR1**
 Register Description: **Global Framer Interrupt Status Register 1**
 Register Address: **00F9h**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|------|------|------|------|------|------|------|------|
| Name | FIS8 | FIS7 | FIS6 | FIS5 | FIS4 | FIS3 | FIS2 | FIS1 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

The GFISR1 register reports the framer interrupt status for the T1/E1 framers of Channels 1 to 8. A logic one in the associated bit location indicates a framer has set its interrupt signal.

Bit 7: Framer Interrupt Status 8 (FIS8)

0 = Framer 8 has not issued an interrupt.

1 = Framer 8 has issued an interrupt.

Bit 6: Framer Interrupt Status 7 (FIS7)

0 = Framer 7 has not issued an interrupt.

1 = Framer 7 has issued an interrupt.

Bit 5: Framer Interrupt Status 6 (FIS6)

0 = Framer 6 has not issued an interrupt.

1 = Framer 6 has issued an interrupt.

Bit 4: Framer Interrupt Status 5 (FIS5)

0 = Framer 5 has not issued an interrupt.

1 = Framer 5 has issued an interrupt.

Bit 3: Framer Interrupt Status 4 (FIS4)

0 = Framer 4 has not issued an interrupt.

1 = Framer 4 has issued an interrupt.

Bit 2: Framer Interrupt Status 3 (FIS3)

0 = Framer 3 has not issued an interrupt.

1 = Framer 3 has issued an interrupt.

Bit 1: Framer Interrupt Status 2 (FIS2)

0 = Framer 2 has not issued an interrupt.

1 = Framer 2 has issued an interrupt.

Bit 0: Framer Interrupt Status 1 (FIS1)

0 = Framer 1 has not issued an interrupt.

1 = Framer 1 has issued an interrupt.

Register Name: **GBISR1**
 Register Description: **Global BERT Interrupt Status Register 1**
 Register Address: **00FAh**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|------|------|------|------|------|------|------|------|
| Name | BIS8 | BIS7 | BIS6 | BIS5 | BIS4 | BIS3 | BIS2 | BIS1 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

The GBISR1 register reports the interrupt status for the T1/E1 bit error rate testers (BERT) of Channels 1 to 8. A logic one in the associated bit location indicates a BERT has set its interrupt signal.

Bit 7: BERT Interrupt Status 8 (BIS8)

0 = BERT 8 has not issued an interrupt.
 1 = BERT 8 has issued an interrupt.

Bit 6: BERT Interrupt Status 7 (BIS7)

0 = BERT 7 has not issued an interrupt.
 1 = BERT 7 has issued an interrupt.

Bit 5: BERT Interrupt Status 6 (BIS6)

0 = BERT 6 has not issued an interrupt.
 1 = BERT 6 has issued an interrupt.

Bit 4: BERT Interrupt Status 5 (BIS5)

0 = BERT 5 has not issued an interrupt.
 1 = BERT 5 has issued an interrupt.

Bit 3: BERT Interrupt Status 4 (BIS4)

0 = BERT 4 has not issued an interrupt.
 1 = BERT 4 has issued an interrupt.

Bit 2: BERT Interrupt Status 3 (BIS3)

0 = BERT 3 has not issued an interrupt.
 1 = BERT 3 has issued an interrupt.

Bit 1: BERT Interrupt Status 2 (BIS2)

0 = BERT 2 has not issued an interrupt.
 1 = BERT 2 has issued an interrupt.

Bit 0: BERT Interrupt Status 1 (BIS1)

0 = BERT 1 has not issued an interrupt.
 1 = BERT 1 has issued an interrupt.

Register Name: **GLISR1**
 Register Description: **Global LIU Interrupt Status Register 1**
 Register Address: **00FBh**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|------|------|------|------|------|------|------|------|
| Name | LIS8 | LIS7 | LIS6 | LIS5 | LIS4 | LIS3 | LIS2 | LIS1 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

The GLISR1 register reports the LIU interrupt status for the T1/E1 LIUs of Channels 1 to 8. A logic one in the associated bit location indicates a LIU has set its interrupt signal.

Bit 7: LIU Interrupt Status 8 (LIS8)

0 = LIU 8 has not issued an interrupt.
 1 = LIU 8 has issued an interrupt.

Bit 6: LIU Interrupt Status 7 (LIS7)

0 = LIU 7 has not issued an interrupt.
 1 = LIU 7 has issued an interrupt.

Bit 5: LIU Interrupt Status 6 (LIS6)

0 = LIU 6 has not issued an interrupt.
 1 = LIU 6 has issued an interrupt.

Bit 4: LIU Interrupt Status 5 (LIS5)

0 = LIU 5 has not issued an interrupt.
 1 = LIU 5 has issued an interrupt.

Bit 3: LIU Interrupt Status 4 (LIS4)

0 = LIU 4 has not issued an interrupt.
 1 = LIU 4 has issued an interrupt.

Bit 2: LIU Interrupt Status 3 (LIS3)

0 = LIU 3 has not issued an interrupt.
 1 = LIU 3 has issued an interrupt.

Bit 1: LIU Interrupt Status 2 (LIS2)

0 = LIU 2 has not issued an interrupt.
 1 = LIU 2 has issued an interrupt.

Bit 0: LIU Interrupt Status 1 (LIS1)

0 = LIU 1 has not issued an interrupt.
 1 = LIU 1 has issued an interrupt.

Register Name: **GFIMR1**
 Register Description: **Global Framer Interrupt Mask Register 1**
 Register Address: **00FCh**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|------|------|------|------|------|------|------|------|
| Name | FIM8 | FIM7 | FIM6 | FIM5 | FIM4 | FIM3 | FIM2 | FIM1 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7: Framer 8 Interrupt Mask (FIM8)

0 = Interrupt masked.
 1 = Interrupt enabled.

Bit 6: Framer 7 Interrupt Mask (FIM7)

0 = Interrupt masked.
 1 = Interrupt enabled.

Bit 5: Framer 6 Interrupt Mask (FIM6)

0 = Interrupt masked.
 1 = Interrupt enabled.

Bit 4: Framer 5 Interrupt Mask (FIM5)

0 = Interrupt masked.
 1 = Interrupt enabled.

Bit 3: Framer 4 Interrupt Mask (FIM4)

0 = Interrupt masked.
 1 = Interrupt enabled.

Bit 2: Framer 3 Interrupt Mask (FIM3)

0 = Interrupt masked.
 1 = Interrupt enabled.

Bit 1: Framer 2 Interrupt Mask (FIM2)

0 = Interrupt masked.
 1 = Interrupt enabled.

Bit 0: Framer 1 Interrupt Mask (FIM1)

0 = Interrupt masked.
 1 = Interrupt enabled.

Register Name: **GBIMR1**
 Register Description: **Global BERT Interrupt Mask Register 1**
 Register Address: **00FDh**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|------|------|------|------|------|------|------|------|
| Name | BIM8 | BIM7 | BIM6 | BIM5 | BIM4 | BIM3 | BIM2 | BIM1 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7: BERT Interrupt Mask 8 (BIM8)

0 = Interrupt masked.
 1 = Interrupt enabled.

Bit 6: BERT Interrupt Mask 7 (BIM7)

0 = Interrupt masked.
 1 = Interrupt enabled.

Bit 5: BERT Interrupt Mask 6 (BIM6)

0 = Interrupt masked.
 1 = Interrupt enabled.

Bit 4: BERT Interrupt Mask 5 (BIM5)

0 = Interrupt masked.
 1 = Interrupt enabled.

Bit 3: BERT Interrupt Mask 4 (BIM4)

0 = Interrupt masked.
 1 = Interrupt enabled.

Bit 2: BERT Interrupt Mask 3 (BIM3)

0 = Interrupt masked.
 1 = Interrupt enabled.

Bit 1: BERT Interrupt Mask 2 (BIM2)

0 = Interrupt masked.
 1 = Interrupt enabled.

Bit 0: BERT Interrupt Mask 1 (BIM1)

0 = Interrupt masked.
 1 = Interrupt enabled.

Register Name: **GLIMR1**
 Register Description: **Global LIU Interrupt Mask Register 1**
 Register Address: **00FEh**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|------|------|------|------|------|------|------|------|
| Name | LIM8 | LIM7 | LIM6 | LIM5 | LIM4 | LIM3 | LIM2 | LIM1 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7: LIU Interrupt Mask 8 (LIM8)

0 = Interrupt masked.
 1 = Interrupt enabled.

Bit 6: LIU Interrupt Mask 7 (LIM7)

0 = Interrupt masked.
 1 = Interrupt enabled.

Bit 5: LIU Interrupt Mask 6 (LIM6)

0 = Interrupt masked.
 1 = Interrupt enabled.

Bit 4: LIU Interrupt Mask 5 (LIM5)

0 = Interrupt masked.
 1 = Interrupt enabled.

Bit 3: LIU Interrupt Mask 4 (LIM4)

0 = Interrupt masked.
 1 = Interrupt enabled.

Bit 2: LIU Interrupt Mask 3 (LIM3)

0 = Interrupt masked.
 1 = Interrupt enabled.

Bit 1: LIU Interrupt Mask 2 (LIM2)

0 = Interrupt masked.
 1 = Interrupt enabled.

Bit 0: LIU Interrupt Mask 1 (LIM1)

0 = Interrupt masked.
 1 = Interrupt enabled.

10.4 Framer Register Descriptions

10.4.1 Receive Register Descriptions

See [Table 10-3](#) for the complete framer register list.

Register Name: **RHC**
 Register Description: **Receive HDLC-64 Control Register**
 Register Address: **010h + (200h x (n - 1)) : where n = 1 to 8**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|-------|-----|------|-------|-------|-------|-------|-------|
| Name | RCRCD | RHR | RHMS | RHCS4 | RHCS3 | RHCS2 | RHCS1 | RHCS0 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7: Receive CRC-16 Display (RCRCD)

- 0 = Do not write received CRC-16 code to FIFO (default).
- 1 = Write received CRC-16 code to FIFO after last octet of packet.

Bit 6: Receive HDLC-64 Reset (RHR). Will reset the receive HDLC-64 controller and flush the receive FIFO. Note that this bit is a acknowledged reset. The host should set this bit and the DS26518 will clear it once the reset operation is complete. The DS26518 will complete the HDLC-64 reset within 2 frames.

- 0 = Normal operation.
- 1 = Reset receive HDLC-64 controller and flush the receive FIFO.

Bit 5: Receive HDLC-64 Mapping Select (RHMS)

- 0 = Receive HDLC-64 assigned to channels.
- 1 = Receive HDLC-64 assigned to FDL (T1 mode), Sa bits (E1 mode).

Bits 4 to 0: Receive HDLC-64 Channel Select 4 to 0 (RHCS[4:0]). These bits determine which DS0 is mapped to the HDLC-64 controller when enabled with RHMS = 0. RHCS[4:0] = all 0s selects channel 1, RHCS[4:0] = all 1s selects channel 32 (E1). A change to the receive HDLC-64 channel select is acknowledged only after a receive HDLC-64 reset (RHR).

Register Name: **RHBSE**
 Register Description: **Receive HDLC-64 Bit Suppress Register**
 Register Address: **011h + (200h x (n - 1)) : where n = 1 to 8**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|------|------|------|------|------|------|------|------|
| Name | BSE8 | BSE7 | BSE6 | BSE5 | BSE4 | BSE3 | BSE2 | BSE1 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7: Receive Channel Bit 8 Suppress (BSE8). MSB of the channel. Set to one to stop this bit from being used.

Bit 6: Receive Channel Bit 7 Suppress (BSE7). Set to one to stop this bit from being used.

Bit 5: Receive Channel Bit 6 Suppress (BSE6). Set to one to stop this bit from being used.

Bit 4: Receive Channel Bit 5 Suppress (BSE5). Set to one to stop this bit from being used.

Bit 3: Receive Channel Bit 4 Suppress (BSE4). Set to one to stop this bit from being used.

Bit 2: Receive Channel Bit 3 Suppress (BSE3). Set to one to stop this bit from being used.

Bit 1: Receive Channel Bit 2 Suppress (BSE2). Set to one to stop this bit from being used.

Bit 0: Receive Channel Bit 1 Suppress (BSE1). LSB of the channel. Set to one to stop this bit from being used.

Register Name: **RDS0SEL**
 Register Description: **Receive Channel Monitor Select Register**
 Register Address: **012h + (200h x (n - 1)) : where n = 1 to 8**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|---|---|------|------|------|------|------|
| Name | — | — | — | RCM4 | RCM3 | RCM2 | RCM1 | RCM0 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 4 to 0: Receive Channel Monitor Bits (RCM[4:0]). RCM0 is the LSB of a 5-bit channel select that determines which receive DS0 channel data will appear in the RDS0M register.

Register Name: **RSIGC**
 Register Description: **Receive-Signaling Control Register**
 Register Address: **013h + (200h x (n - 1)) : where n = 1 to 8**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|---|---|-------|---|------|------|------|
| Name | — | — | — | RFSA1 | — | RSFF | RSFE | RSIE |
| | — | — | — | CASMS | — | RSFF | RSFE | RSIE |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 4 (T1 Mode): Receive Force Signaling All Ones (RFSA1)

0 = Do not force robbed bit signaling to all ones.

1 = Force signaling bits to all ones on a per-channel basis according to the [T1RSAOI1–3](#) registers.

Bit 4 (E1 Mode): CAS Mode Select (CASMS)

0 = The DS26518 will initiate a resync when two consecutive multiframe alignment signals have been received with an error.

1 = The DS26518 will initiate a resync when two consecutive multiframe alignment signals have been received with an error, or 1 multiframe has been received with all the bits in time slot 16 in state 0.

Alignment criteria is met when at least one bit in state 1 is present in the time slot 16 preceding the multiframe alignment signal first detected (G.732 alternate criteria).

Bit 2: Receive-Signaling Force Freeze (RSFF). Freezes receive-side signaling at RSIGn (and RSERn if receive-signaling reinsertion is enabled); will override receive freeze enable (RFE).

0 = Do not force a freeze event.

1 = Force a freeze event.

Bit 1: Receive-Signaling Freeze Enable (RSFE)

0 = No freezing of receive signaling data will occur.

1 = Allow freezing of receive signaling data at RSIGn (and RSERn if receive-signaling reinsertion is enabled).

Bit 0: Receive-Signaling Integration Enable (RSIE)

0 = Signaling changes of state reported on any change in selected channels.

1 = Signaling must be stable for three multiframes in order for a change of state to be reported.

Register Name: **T1RCR2 (T1 Mode)**
 Register Description: **Receive Control Register 2**
 Register Address: **014h + (200h x (n - 1)) : where n = 1 to 8**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|---|---|--------|------|------|-------|-------|
| Name | — | — | — | RSLC96 | OOF2 | OOF1 | RAIIE | RRAIS |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 4: Receive SLC-96 Synchronizer Enable (RSLC96). See Section [9.9.4.4](#) for SLC-96 details.

0 = The SLC-96 synchronizer is disabled.

1 = The SLC-96 synchronizer is enabled.

BITS 3 AND 2: OUT OF FRAME SELECT BITS (OOF[2:1])

| OOF2 | OOF1 | OUT OF FRAME CRITERIA |
|------|------|-------------------------|
| 0 | 0 | 2/4 frame bits in error |
| 0 | 1 | 2/5 frame bits in error |
| 1 | 0 | 2/6 frame bits in error |
| 1 | 1 | 2/6 frame bits in error |

Bit 1: Receive RAI Integration Enable (RAIIE). The ESF RAI indication can be interrupted for a period not to exceed 100ms per interruption (T1.403). In ESF mode, setting RAIIE will cause the RAI status from the DS26518 to be integrated for 200ms.

0 = RAI detects when 16 consecutive patterns of 00FF appear in the FDL.

RAI clears when 14 or fewer patterns of 00FF hex out of 16 possible appear in the FDL.

1 = RAI detects when the condition has been present for greater than 200ms.

RAI clears when the condition has been absent for greater than 200ms.

Bit 0: Receive-Side Remote Alarm Select (RRAIS)

0 = Receive framer detects T1 remote alarm.

D4—Zeros in bit 2 of all channels.

ESF—00FF pattern in FDL.

1 = Receive Framer detects J1 Remote Alarm.

D4—A one in the S-bit position of frame 12.

ESF—all ones in FDL.

Register Name: **E1RSAIMR (E1 Mode Only)**
 Register Description: **Receive Sa Bit Interrupt Mask Register**
 Register Address: **014h + (200h x (n - 1)) : where n = 1 to 8**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|---|---|--------|--------|--------|--------|--------|
| Name | — | — | — | RSa4IM | RSa5IM | RSa6IM | RSa7IM | RSa8IM |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 4: Sa4 Change Detect Interrupt Mask (RSa4IM). This bit will enable the change detect interrupt for the Sa4 bits. Any change of state of the Sa4 bit will then generate an interrupt in RLS7.0 to indicate the change of state.

0 = Interrupt masked.
 1 = Interrupt enabled.

Bit 3: Sa5 Change Detect Interrupt Mask (RSa5IM). This bit will enable the change detect interrupt for the Sa5 bits. Any change of state of the Sa5 bit will then generate an interrupt in RLS7.0 to indicate the change of state.

0 = Interrupt masked.
 1 = Interrupt enabled.

Bit 2: Sa6 Change Detect Interrupt Mask (RSa6IM). This bit will enable the change detect interrupt for the Sa6 bits. Any change of state of the Sa6 bit will then generate an interrupt in RLS7.0 to indicate the change of state.

0 = Interrupt masked.
 1 = Interrupt enabled.

Bit 1: Sa7 Change Detect Interrupt Mask (RSa7IM). This bit will enable the change detect interrupt for the Sa7 bits. Any change of state of the Sa7 bit will then generate an interrupt in RLS7.0 to indicate the change of state.

0 = Interrupt masked.
 1 = Interrupt enabled.

Bit 0: Sa8 Change Detect Interrupt Mask (RSa8IM). This bit will enable the change detect interrupt for the Sa8 bits. Any change of state of the Sa8 bit will then generate an interrupt in RLS7.0 to indicate the change of state.

0 = Interrupt masked.
 1 = Interrupt enabled.

Register Name: **T1RBOCC (T1 Mode Only)**
 Register Description: **Receive BOC Control Register**
 Register Address: **015h + (200h x (n - 1)) : where n = 1 to 8**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|-----|---|------|------|---|------|------|---|
| Name | RBR | — | RBD1 | RBD0 | — | RBF1 | RBF0 | — |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7: Receive BOC Reset (RBR). The host should set this bit to force a reset of the BOC circuitry. Note that this is an acknowledged reset—that is, the host needs only to set the bit and the DS26518 will clear it once the reset operation is complete (less than 250 μ s). Modifications to the RBF[1:0] and RBD[1:0] bits will not be applied to the BOC controller until a BOC reset has been completed.

Bits 5 and 4: Receive BOC Disintegration Bits (RBD[1:0]). The BOC disintegration filter sets the number of message bits that must be received without a valid BOC to set the BC bit indicating that a valid BOC is no longer being received.

| RBD1 | RBD0 | CONSECUTIVE MESSAGE BITS FOR BOC CLEAR IDENTIFICATION |
|------|------|---|
| 0 | 0 | 16 |
| 0 | 1 | 32 |
| 1 | 0 | 48 |
| 1 | 1 | 64 (See Note 1) |

Bits 2 and 1: Receive BOC Filter Bits (RBF[1:0]). The BOC filter sets the number of consecutive patterns that must be received without error prior to an indication of a valid message.

| RBF1 | RBF0 | CONSECUTIVE BOC CODES FOR VALID SEQUENCE IDENTIFICATION |
|------|------|---|
| 0 | 0 | None |
| 0 | 1 | 3 |
| 1 | 0 | 5 |
| 1 | 1 | 7 (See Note 1) |

Note 1: The DS26518's BOC controller does not integrate and disintegrate concurrently. Therefore, if the maximum integration time and the maximum disintegration time are used together, BOC messages that repeat fewer than 11 times may not be detected.

Register Name: **RIDR1 to RIDR32**
 Register Description: **Receive Idle Code Definition Registers 1 to 32**
 Register Address: **020h to 03Fh + (200h x (n - 1)) : where n = 1 to 8**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|----|----|----|----|----|----|----|----|
| Name | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 7 to 0: Per-Channel Idle Code Bits (C[7:0]). C0 is the LSB of the code (this bit is transmitted last). Address 20h is for channel 1. Address 37h is for channel 24. Address 3Fh is for channel 32. RIDR25–RIDR32 are E1 mode only.

Register Name: **T1RSAOI1, T1RSAOI2, T1RSAOI3 (T1 Mode Only)**
 Register Description: **Receive-Signaling All-Ones Insertion Registers 1 to 3**
 Register Address: **038h, 039h, 03Ah + (200h x (n - 1)) : where n = 1 to 8**

| Bit # Name | (MSB) | | | | | | | (LSB) | |
|---------------|-------|------|------|------|------|------|------|-------|-----------------|
| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
| | CH8 | CH7 | CH6 | CH5 | CH4 | CH3 | CH2 | CH1 | T1RSAOI1 |
| | CH16 | CH15 | CH14 | CH13 | CH12 | CH11 | CH10 | CH9 | T1RSAOI2 |
| | CH24 | CH23 | CH22 | CH21 | CH20 | CH19 | CH18 | CH17 | T1RSAOI3 |

Setting any of the CH[1:24] bits in the T1RSAOI1 to T1RSAOI3 registers will cause signaling data to be replaced with logic ones as reported on RSERn. The RSIgn signal will continue to report received signaling data. Note that this feature must be enabled with control bit [RSIGC.4](#).

Register Name: **T1RDMWE1, T1RDMWE2, T1RDMWE3**
 Register Description: **T1 Receive Digital Milliwatt Enable Registers 1 to 3**
 Register Address: **03Ch, 03Dh, 03Eh + (200h x (n - 1)) : where n = 1 to 8**

| Bit # Name | (MSB) | | | | | | | (LSB) | |
|---------------|-------|------|------|------|------|------|------|-------|-----------------|
| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
| | CH8 | CH7 | CH6 | CH5 | CH4 | CH3 | CH2 | CH1 | T1RDMWE1 |
| | CH16 | CH15 | CH14 | CH13 | CH12 | CH11 | CH10 | CH9 | T1RDMWE2 |
| | CH24 | CH23 | CH22 | CH21 | CH20 | CH19 | CH18 | CH17 | T1RDMWE3 |

Bits 7 to 0: Receive Digital Milliwatt Enable for Channels 1 to 24 (CH[1:24])

0 = Does not affect the receive data associated with this channel.

1 = Replace the receive data associated with this channel with digital milliwatt code.

Register Name: **RS1 to RS16**
 Register Description: **Receive-Signaling Registers 1 to 16**
 Register Address: **040h to 04Fh + (200h x (n - 1)) : where n = 1 to 8**

T1 Mode:

| Bit # Name | (MSB) | | | | (LSB) | | | | |
|---------------|--------|--------|--------|--------|--------|--------|--------|-------------|--|
| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
| CH1-A | CH1-B | CH1-C | CH1-D | CH13-A | CH13-B | CH13-C | CH13-D | RS1 | |
| CH2-A | CH2-B | CH2-C | CH2-D | CH14-A | CH14-B | CH14-C | CH14-D | RS2 | |
| CH3-A | CH3-B | CH3-C | CH3-D | CH15-A | CH15-B | CH15-C | CH15-D | RS3 | |
| CH4-A | CH4-B | CH4-C | CH4-D | CH16-A | CH16-B | CH16-C | CH16-D | RS4 | |
| CH5-A | CH5-B | CH5-C | CH5-D | CH17-A | CH17-B | CH17-C | CH17-D | RS5 | |
| CH6-A | CH6-B | CH6-C | CH6-D | CH18-A | CH18-B | CH18-C | CH18-D | RS6 | |
| CH7-A | CH7-B | CH7-C | CH7-D | CH19-A | CH19-B | CH19-C | CH19-D | RS7 | |
| CH8-A | CH8-B | CH8-C | CH8-D | CH20-A | CH20-B | CH20-C | CH20-D | RS8 | |
| CH9-A | CH9-B | CH9-C | CH9-D | CH21-A | CH21-B | CH21-C | CH21-D | RS9 | |
| CH10-A | CH10-B | CH10-C | CH10-D | CH22-A | CH22-B | CH22-C | CH22-D | RS10 | |
| CH11-A | CH11-B | CH11-C | CH11-D | CH23-A | CH23-B | CH23-C | CH23-D | RS11 | |
| CH12-A | CH12-B | CH12-C | CH12-D | CH24-A | CH24-B | CH24-C | CH24-D | RS12 | |

E1 Mode:

| Bit # Name | (MSB) | | | | (LSB) | | | | |
|---------------|--------|--------|--------|--------|--------|--------|--------|-------------|------------|
| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
| | 0 | 0 | 0 | 0 | X | Y | X | X | RS1 |
| CH1-A | CH1-B | CH1-C | CH1-D | CH16-A | CH16-B | CH16-C | CH16-D | RS2 | |
| CH2-A | CH2-B | CH2-C | CH2-D | CH17-A | CH17-B | CH17-C | CH17-D | RS3 | |
| CH3-A | CH3-B | CH3-C | CH3-D | CH18-A | CH18-B | CH18-C | CH18-D | RS4 | |
| CH4-A | CH4-B | CH4-C | CH4-D | CH19-A | CH19-B | CH19-C | CH19-D | RS5 | |
| CH5-A | CH5-B | CH5-C | CH5-D | CH20-A | CH20-B | CH20-C | CH20-D | RS6 | |
| CH6-A | CH6-B | CH6-C | CH6-D | CH21-A | CH21-B | CH21-C | CH21-D | RS7 | |
| CH7-A | CH7-B | CH7-C | CH7-D | CH22-A | CH22-B | CH22-C | CH22-D | RS8 | |
| CH8-A | CH8-B | CH8-C | CH8-D | CH23-A | CH23-B | CH23-C | CH23-D | RS9 | |
| CH9-A | CH9-B | CH9-C | CH9-D | CH24-A | CH24-B | CH24-C | CH24-D | RS10 | |
| CH10-A | CH10-B | CH10-C | CH10-D | CH25-A | CH25-B | CH25-C | CH25-D | RS11 | |
| CH11-A | CH11-B | CH11-C | CH11-D | CH26-A | CH26-B | CH26-C | CH26-D | RS12 | |
| CH12-A | CH12-B | CH12-C | CH12-D | CH27-A | CH27-B | CH27-C | CH27-D | RS13 | |
| CH13-A | CH13-B | CH13-C | CH13-D | CH28-A | CH28-B | CH28-C | CH28-D | RS14 | |
| CH14-A | CH14-B | CH14-C | CH14-D | CH29-A | CH29-B | CH29-C | CH29-D | RS15 | |
| CH15-A | CH15-B | CH15-C | CH15-D | CH30-A | CH30-B | CH30-C | CH30-D | RS16 | |

In the ESF framing mode, there can be up to four signaling bits per channel (A, B, C, and D). In the D4 framing mode, there are only two signaling bits per channel (A and B). In the D4 framing mode, the framer will repeat the A and B signaling data in the C and D bit locations. Therefore, when the framer is operated in D4 framing mode, the user will need to retrieve the signaling bits every 1.5ms as opposed to 3ms for ESF mode. The receive-signaling registers are frozen and not updated during a loss of sync condition. They will contain the most recent signaling information before the "OOF" occurred.

Register Name: **LCVCR1**
 Register Description: **Line Code Violation Count Register 1**
 Register Address: **050h + (200h x (n - 1)) : where n = 1 to 8**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|--------|--------|--------|--------|--------|--------|-------|-------|
| Name | LCVC15 | LCVC14 | LCVC13 | LCVC12 | LCVC11 | LCVC10 | LCVC9 | LCVC8 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 7 to 0: Line Code Violation Counter Bits 15 to 8 (LCVC[15:8]). LCV15 is the MSB of the 16-bit code violation count.

Register Name: **LCVCR2**
 Register Description: **Line Code Violation Count Register 2**
 Register Address: **051h + (200h x (n - 1)) : where n = 1 to 8**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|-------|-------|-------|-------|-------|-------|-------|-------|
| Name | LCVC7 | LCVC6 | LCVC5 | LCVC4 | LCVC3 | LCVC2 | LCVC1 | LCVC0 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 7 to 0: Line Code Violation Counter Bits 7 to 0 (LCVC[7:0]). LCV0 is the LSB of the 16-bit code violation count.

Register Name: **PCVCR1**
 Register Description: **Path Code Violation Count Register 1**
 Register Address: **052h + (200h x (n - 1)) : where n = 1 to 8**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|--------|--------|--------|--------|--------|--------|-------|-------|
| Name | PCVC15 | PCVC14 | PCVC13 | PCVC12 | PCVC11 | PCVC10 | PCVC9 | PCVC8 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 7 to 0: Path Code Violation Counter Bits 15 to 8 (PCVC[15:8]). PCVC15 is the MSB of the 16-bit path code violation count.

Register Name: **PCVCR2**
 Register Description: **Path Code Violation Count Register 2**
 Register Address: **053h + (200h x (n - 1)) : where n = 1 to 8**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|-------|-------|-------|-------|-------|-------|-------|-------|
| Name | PCVC7 | PCVC6 | PCVC5 | PCVC4 | PCVC3 | PCVC2 | PCVC1 | PCVC0 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 7 to 0: Path Code Violation Counter Bits 7 to 0 (PCVC[7:0]). PCVC0 is the LSB of the 16-bit path code violation count.

Register Name: **FOSCR1**
 Register Description: **Frames Out of Sync Count Register 1**
 Register Address: **054h + (200h x (n - 1)) : where n = 1 to 8**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|-------|-------|-------|-------|-------|-------|------|------|
| Name | FOS15 | FOS14 | FOS13 | FOS12 | FOS11 | FOS10 | FOS9 | FOS8 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 7 to 0: Frames Out of Sync Counter Bits 15 to 8 (FOS[15:8]). FOS15 is the MSB of the 16-bit frames out of sync count.

Register Name: **FOSCR2**
 Register Description: **Frames Out of Sync Count Register 2**
 Register Address: **055h + (200h x (n - 1)) : where n = 1 to 8**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|------|------|------|------|------|------|------|------|
| Name | FOS7 | FOS6 | FOS5 | FOS4 | FOS3 | FOS2 | FOS1 | FOS0 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 7 to 0: Frames Out of Sync Counter Bits 7 to 0 (FOS[7:0]). FOS0 is the LSB of the 16-bit frames out of sync count.

Register Name: **E1EBCR1 (E1 Mode Only)**
 Register Description: **E-Bit Count Register 1**
 Register Address: **056h + (200h x (n - 1)) : where n = 1 to 8**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|------|------|------|------|------|------|-----|-----|
| Name | EB15 | EB14 | EB13 | EB12 | EB11 | EB10 | EB9 | EB8 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 7 to 0: E-Bit Counter Bits 15 to 8 (EB[15:8]). EB15 is the MSB of the 16-bit E-bit count.

Register Name: **E1EBCR2 (E1 Mode Only)**
 Register Description: **E-Bit Count Register 2**
 Register Address: **057h + (200h x (n - 1)) : where n = 1 to 8**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|-----|-----|-----|-----|-----|-----|-----|-----|
| Name | EB7 | EB6 | EB5 | EB4 | EB3 | EB2 | EB1 | EB0 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 7 to 0: E-Bit Counter Bits 7 to 0 (EB[7:0]). EB0 is the LSB of the 16-bit E-bit count.

Register Name: **FEACR1**
 Register Description: **Error Count A Register 1**
 Register Address: **058h + (200h x (n - 1)) : where n = 1 to 8**

| | | | | | | | | |
|---------|---------|---------|---------|---------|---------|---------|--------|--------|
| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | FEACR15 | FEACR14 | FEACR13 | FEACR12 | FEACR11 | FEACR10 | FEACR9 | FEACR8 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 7 to 0: Error Count A Register 1 Bits 15 to 8 (FEACR[15:8]). FEACR15 is the MSB of the 16-bit Far End A Counter.

Register Name: **FEACR2**
 Register Description: **Error Count A Register 2**
 Register Address: **059h + (200h x (n - 1)) : where n = 1 to 8**

| | | | | | | | | |
|---------|--------|--------|--------|--------|--------|--------|--------|--------|
| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | FEACR7 | FEACR6 | FEACR5 | FEACR4 | FEACR3 | FEACR2 | FEACR1 | FEACR0 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 7 to 0: Error Count A Register 2 Bits 7 to 0 (FEACR[7:0]). FEACR0 is the LSB of the 16-bit Far End A Counter.

Register Name: **FEBR1**
 Register Description: **Error Count B Register 1**
 Register Address: **05Ah + (200h x (n - 1)) : where n = 1 to 8**

| | | | | | | | | |
|---------|--------|--------|--------|--------|--------|--------|-------|-------|
| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | FEBR15 | FEBR14 | FEBR13 | FEBR12 | FEBR11 | FEBR10 | FEBR9 | FEBR8 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 7 to 0: Error Count B Register 1 Bits 15 to 8 (FEBR[15:8]). FEBR15 is the MSB of the 16-bit Far End Error B Counter.

Register Name: **FEBR2**
 Register Description: **Error Count B Register 2**
 Register Address: **05Bh + (200h x (n - 1)) : where n = 1 to 8**

| | | | | | | | | |
|---------|-------|-------|-------|-------|-------|-------|-------|-------|
| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | FEBR7 | FEBR6 | FEBR5 | FEBR4 | FEBR3 | FEBR2 | FEBR1 | FEBR0 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 7 to 0: Error Count B Register 2 Bits 7 to 0 (FEBR[7:0]). FEBR0 is the LSB of the 16-bit Far End Error B Counter.

Register Name: **RDS0M**
Register Description: **Receive DS0 Monitor Register**
Register Address: **060h + (200h x (n - 1)) : where n = 1 to 8**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|----|----|----|----|----|----|----|----|
| Name | B1 | B2 | B3 | B4 | B5 | B6 | B7 | B8 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 7 to 0: Receive DS0 Channel Bits (B[1:8]). Receive channel data that has been selected by the Receive Channel Monitor Select Register ([RDS0SEL](#)). B8 is the LSB of the DS0 channel (last bit to be received).

Register Name: **T1RFDL (T1 Mode)**
 Register Description: **Receive FDL Register**
 Register Address: **062h + (200h x (n - 1)) : where n = 1 to 8**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|-------|-------|-------|-------|-------|-------|-------|-------|
| Name | RFDL7 | RFDL6 | RFDL5 | RFDL4 | RFDL3 | RFDL2 | RFDL1 | RFDL0 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Note: This register has an alternate definition for E1 mode. See [E1RRTS7](#).

Bit 7: Receive FDL Bit 7 (RFDL7). MSB of the received FDL code.

Bit 6: Receive FDL Bit 6 (RFDL6)

Bit 5: Receive FDL Bit 5 (RFDL5)

Bit 4: Receive FDL Bit 4 (RFDL4)

Bit 3: Receive FDL Bit 3 (RFDL3)

Bit 2: Receive FDL Bit 2 (RFDL2)

Bit 1: Receive FDL Bit 1 (RFDL1)

Bit 0: Receive FDL Bit 0 (RFDL0). LSB of the received FDL code.

Register Name: **E1RRTS7 (E1 Mode)**
 Register Description: **Receive Real-Time Status Register 7**
 Register Address: **062h + (200h x (n - 1)) : where n = 1 to 8**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|------|------|------|------|------|--------|-------|-------|
| Name | CSC5 | CSC4 | CSC3 | CSC2 | CSC0 | CRC4SA | CASSA | FASSA |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Note: This register has an alternate definition for T1 mode. See [T1RFDL](#). All bits in this register are real-time (not latched).

Bits 7 to 3: CRC-4 Sync Counter Bits (CSC[5:2] and CSC0). The CRC-4 sync counter increments each time the 8ms CRC-4 multiframe search times out. The counter is cleared when the framer has successfully obtained synchronization at the CRC-4 level. The counter can also be cleared by disabling the CRC-4 mode ([RCR1.3](#) = 0). This counter is useful for determining the amount of time the framer has been searching for synchronization at the CRC-4 level. ITU-T G.706 suggests that if synchronization at the CRC-4 level cannot be obtained within 400 ms, then the search should be abandoned and proper action taken. The CRC-4 sync counter will saturate (not rollover). CSC0 is the LSB of the 6-bit counter. (**Note:** CSC1 is omitted to allow resolution to > 400ms using 5 bits.)

Bit 2: CRC-4 MF Sync Active (CRC4SA). Set while the synchronizer is searching for the CRC-4 MF alignment word.

Bit 1: CAS MF Sync Active (CASSA). Set while the synchronizer is searching for the CAS MF alignment word.

Bit 0: FAS Sync Active (FASSA). Set while the synchronizer is searching for alignment at the FAS level.

Register Name: **T1RBOC (T1 Mode)**
 Register Description: **Receive BOC Register**
 Register Address: **$63h + (200h \times (n - 1))$: where $n = 1$ to 8**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|---|-------|-------|-------|-------|-------|-------|
| Name | — | — | RBOC5 | RBOC4 | RBOC3 | RBOC2 | RBOC1 | RBOC0 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 5: BOC Bit 5 (RBOC5)

Bit 4: BOC Bit 4 (RBOC4)

Bit 3: BOC Bit 3 (RBOC3)

Bit 2: BOC Bit 2 (RBOC2)

Bit 1: BOC Bit 1 (RBOC1)

Bit 0: BOC Bit 0 (RBOC0)

The T1RBOC register always contains the last valid BOC received. The Receive FDL Register ([T1RFDL](#)) reports the incoming Facility Data Link (FDL) or the incoming Fs bits. The LSB is received first. In D4 framing mode, RFDL updates on multiframe boundaries and reports the six Fs bits in RFDL[5:0].

Register Name: **T1RSLC1, T1RSLC2, T1RSLC3 (T1 Mode)**
 Register Description: **Receive SLC96 Data Link Registers**
 Register Address: **064h, 065h, 066h + (200h x (n - 1)) : where n = 1 to 8**

| Bit # | (MSB) | | | | (LSB) | | | | |
|-------|-------|----|-----|-----|-------|-----|-----|----|----------------|
| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
| Name | C8 | C7 | C6 | C5 | C4 | C3 | C2 | C1 | T1RSLC1 |
| | M2 | M1 | S=0 | S=1 | S=0 | C11 | C10 | C9 | T1RSLC2 |
| | S=1 | S4 | S3 | S2 | S1 | A2 | A1 | M3 | T1RSLC3 |

Note: These registers have an alternate definition for E1 mode. See [E1RAF](#), [E1RNAF](#), and [E1RsiAF](#).

Register Name: **E1RAF (E1 Mode)**
 Register Description: **E1 Receive Align Frame Register**
 Register Address: **064h + (200h x (n - 1)) : where n = 1 to 8**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|----|---|---|---|---|---|---|---|
| Name | Si | 0 | 0 | 1 | 1 | 0 | 1 | 1 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Note: This register has an alternate definition for T1 mode. See [T1RSLC1](#).

Bit 7: International Bit (Si)

Bit 6: Frame Alignment Signal Bit (0)

Bit 5: Frame Alignment Signal Bit (0)

Bit 4: Frame Alignment Signal Bit (1)

Bit 3: Frame Alignment Signal Bit (1)

Bit 2: Frame Alignment Signal Bit (0)

Bit 1: Frame Alignment Signal Bit (1)

Bit 0: Frame Alignment Signal Bit (1)

Register Name: **E1RNAF (E1 Mode)**
 Register Description: **E1 Receive Non-Align Frame Register**
 Register Address: **065h + (200h x (n - 1)) : where n = 1 to 8**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|----|---|---|-----|-----|-----|-----|-----|
| Name | Si | 1 | A | Sa4 | Sa5 | Sa6 | Sa7 | Sa8 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Note: This register has an alternate definition for T1 mode. See [T1RSLC2](#).

Bit 7: International Bit (Si)

Bit 6: Frame Non-Alignment Signal Bit (1)

Bit 5: Remote Alarm (A)

Bit 4: Additional Bit 4 (Sa4)

Bit 3: Additional Bit 5 (Sa5)

Bit 2: Additional Bit 6 (Sa6)

Bit 1: Additional Bit 7 (Sa7)

Bit 0: Additional Bit 8 (Sa8)

Register Name: **E1RsiAF (E1 Mode)**
 Register Description: **Received Si Bits of the Align Frame**
 Register Address: **066h + (200h x (n - 1)) : where n = 1 to 8**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|-------|-------|-------|------|------|------|------|------|
| Name | SiF14 | SiF12 | SiF10 | SiF8 | SiF6 | SiF4 | SiF2 | SiF0 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Note: This register has an alternate definition for T1 mode. See [T1RSLC3](#).

Bit 7: Si Bit of Frame 14 (SiF14)

Bit 6: Si Bit of Frame 12 (SiF12)

Bit 5: Si Bit of Frame 10 (SiF10)

Bit 4: Si Bit of Frame 8 (SiF8)

Bit 3: Si Bit of Frame 6 (SiF6)

Bit 2: Si Bit of Frame 4 (SiF4)

Bit 1: Si Bit of Frame 2 (SiF2)

Bit 0: Si Bit of Frame 0 (SiF0)

Register Name: **E1RSiNAF (E1 Mode Only)**
 Register Description: **Receive Si Bits of the Non-Align Frame Register**
 Register Address: **067h + (200h x (n - 1)) : where n = 1 to 8**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|-------|-------|-------|------|------|------|------|------|
| Name | SiF15 | SiF13 | SiF11 | SiF9 | SiF7 | SiF5 | SiF3 | SiF1 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7: Si Bit of Frame 15 (SiF15)

Bit 6: Si Bit of Frame 13 (SiF13)

Bit 5: Si Bit of Frame 11 (SiF11)

Bit 4: Si Bit of Frame 9 (SiF9)

Bit 3: Si Bit of Frame 7 (SiF7)

Bit 2: Si Bit of Frame 5 (SiF5)

Bit 1: Si Bit of Frame 3 (SiF3)

Bit 0: Si Bit of Frame 1 (SiF1)

Register Name: **E1RRA (E1 Mode Only)**
 Register Description: **Receive Remote Alarm Register**
 Register Address: **068h + (200h x (n - 1)) : where n = 1 to 8**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|--------|--------|--------|-------|-------|-------|-------|-------|
| Name | RRAF15 | RRAF13 | RRAF11 | RRAF9 | RRAF7 | RRAF5 | RRAF3 | RRAF1 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7: Remote Alarm Bit of Frame 15 (RRAF15)

Bit 6: Remote Alarm Bit of Frame 13 (RRAF13)

Bit 5: Remote Alarm Bit of Frame 11 (RRAF11)

Bit 4: Remote Alarm Bit of Frame 9 (RRAF9)

Bit 3: Remote Alarm Bit of Frame 7 (RRAF7)

Bit 2: Remote Alarm Bit of Frame 5 (RRAF5)

Bit 1: Remote Alarm Bit of Frame 3 (RRAF3)

Bit 0: Remote Alarm Bit of Frame 1 (RRAF1)

Register Name: **E1RSa4 (E1 Mode Only)**
 Register Description: **Received Sa4 Bits Register**
 Register Address: **069h + (200h x (n - 1)) : where n = 1 to 8**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---------|---------|---------|--------|--------|--------|--------|--------|
| Name | RSa4F15 | RSa4F13 | RSa4F11 | RSa4F9 | RSa4F7 | RSa4F5 | RSa4F3 | RSa4F1 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7: Sa4 Bit of Frame 15 (RSa4F15)

Bit 6: Sa4 Bit of Frame 13 (RSa4F13)

Bit 5: Sa4 Bit of Frame 11 (RSa4F11)

Bit 4: Sa4 Bit of Frame 9 (RSa4F9)

Bit 3: Sa4 Bit of Frame 7 (RSa4F7)

Bit 2: Sa4 Bit of Frame 5 (RSa4F5)

Bit 1: Sa4 Bit of Frame 3 (RSa4F3)

Bit 0: Sa4 Bit of Frame 1 (RSa4F1)

Register Name: **E1RSa5 (E1 Mode Only)**
 Register Description: **Received Sa5 Bits Register**
 Register Address: **06Ah + (200h x (n - 1)) : where n = 1 to 8**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---------|---------|---------|--------|--------|--------|--------|--------|
| Name | RSa5F15 | RSa5F13 | RSa5F11 | RSa5F9 | RSa5F7 | RSa5F5 | RSa5F3 | RSa5F1 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7: Sa5 Bit of Frame 15 (RSa5F15)

Bit 6: Sa5 Bit of Frame 13 (RSa5F13)

Bit 5: Sa5 Bit of Frame 11 (RSa5F11)

Bit 4: Sa5 Bit of Frame 9 (RSa5F9)

Bit 3: Sa5 Bit of Frame 7 (RSa5F7)

Bit 2: Sa5 Bit of Frame 5 (RSa5F5)

Bit 1: Sa5 Bit of Frame 3 (RSa5F3)

Bit 0: Sa5 Bit of Frame 1 (RSa5F1)

Register Name: **E1RSa6 (E1 Mode Only)**
 Register Description: **Received Sa6 Bits Register**
 Register Address: **06Bh + (200h x (n - 1)) : where n = 1 to 8**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---------|---------|---------|--------|--------|--------|--------|--------|
| Name | RSa6F15 | RSa6F13 | RSa6F11 | RSa6F9 | RSa6F7 | RSa6F5 | RSa6F3 | RSa6F1 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7: Sa6 Bit of Frame 15 (RSa6F15)

Bit 6: Sa6 Bit of Frame 13 (RSa6F13)

Bit 5: Sa6 Bit of Frame 11 (RSa6F11)

Bit 4: Sa6 Bit of Frame 9 (RSa6F9)

Bit 3: Sa6 Bit of Frame 7 (RSa6F7)

Bit 2: Sa6 Bit of Frame 5 (RSa6F5)

Bit 1: Sa6 Bit of Frame 3 (RSa6F3)

Bit 0: Sa6 Bit of Frame 1 (RSa6F1)

Register Name: **E1RSa7 (E1 Mode Only)**
 Register Description: **Received Sa7 Bits Register**
 Register Address: **06Ch + (200h x (n - 1)) : where n = 1 to 8**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---------|---------|---------|--------|--------|--------|--------|--------|
| Name | RSa7F15 | RSa7F13 | RSa7F11 | RSa7F9 | RSa7F7 | RSa7F5 | RSa7F3 | RSa7F1 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7: Sa7 Bit of Frame 15 (RSa7F15)

Bit 6: Sa7 Bit of Frame 13 (RSa7F13)

Bit 5: Sa7 Bit of Frame 11 (RSa7F11)

Bit 4: Sa7 Bit of Frame 9 (RSa7F9)

Bit 3: Sa7 Bit of Frame 7 (RSa7F7)

Bit 2: Sa7 Bit of Frame 5 (RSa7F5)

Bit 1: Sa7 Bit of Frame 3 (RSa7F3)

Bit 0: Sa7 Bit of Frame 1 (RSa7F1)

Register Name: **E1RSa8 (E1 Mode Only)**
 Register Description: **Received Sa8 Bits Register**
 Register Address: **06Dh + (200h x (n - 1)) : where n = 1 to 8**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---------|---------|---------|--------|--------|--------|--------|--------|
| Name | RSa8F15 | RSa8F13 | RSa8F11 | RSa8F9 | RSa8F7 | RSa8F5 | RSa8F3 | RSa8F1 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7: Sa8 Bit of Frame 15 (RSa8F15)

Bit 6: Sa8 Bit of Frame 13 (RSa8F13)

Bit 5: Sa8 Bit of Frame 11 (RSa8F11)

Bit 4: Sa8 Bit of Frame 9 (RSa8F9)

Bit 3: Sa8 Bit of Frame 7 (RSa8F7)

Bit 2: Sa8 Bit of Frame 5 (RSa8F5)

Bit 1: Sa8 Bit of Frame 3 (RSa8F3)

Bit 0: Sa8 Bit of Frame 1 (RSa8F1)

Register Name: **SaBITS**
 Register Description: **Received SaX Bits Register**
 Register Address: **06Eh + (200h x (n - 1)) : where n = 1 to 8**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|---|---|-----|-----|-----|-----|-----|
| Name | — | — | — | Sa4 | Sa5 | Sa6 | Sa7 | Sa8 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

This register indicates the last received SaX bit. This can be used in conjunction with the [RLS7](#) register to determine which SaX bits have changed. The user can program which Sa bit positions should be monitored via the [E1RSAIMR](#) register, and when a change is detected through an interrupt in [RLS7.0](#), the user can determine which bit has changed by reading this register and comparing it with previous known values.

Bit 4: Last Received Sa4 Bit (Sa4)

Bit 3: Last Received Sa5 Bit (Sa5)

Bit 2: Last Received Sa6 Bit (Sa6)

Bit 1: Last Received Sa7 Bit (Sa7)

Bit 0: Last Received Sa8 Bit (Sa8)

Register Name: **Sa6CODE**
 Register Description: **Received Sa6 Codeword Register**
 Register Address: **06Fh + (200h x (n - 1)) : where n = 1 to 8**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|---|---|---|------|------|------|------|
| Name | — | — | — | — | Sa6n | Sa6n | Sa6n | Sa6n |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

This register will report the received Sa6 codeword per ETS 300 233. The bits are monitored on a submultiframe asynchronous basis, so the pattern reported could be one of multiple patterns that would represent a valid codeword. The table below indicates which patterns reported in this register correspond to a given valid Sa6 codeword.

Bits 3 to 0: Sa6 Codeword Bit (Sa6n)

| VALID Sa6 CODE | POSSIBLE REPORTED PATTERNS |
|----------------|----------------------------|
| Sa6_8 | 1000, 0100, 0010, 0001 |
| Sa6_A | 1010, 0101 |
| Sa6_C | 110, 0110, 0011, 1001 |
| Sa6_E | 1110, 0111, 1011, 1101 |
| Sa6_F | 1111 |

Register Name: **RMMR**
 Register Description: **Receive Master Mode Register**
 Register Address: **080h + (200h x (n - 1)) : where n = 1 to 8**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|--------|-----------|------|---|---|---|--------|-------|
| Name | FRM_EN | INIT_DONE | DRSS | — | — | — | SFTRST | T1/E1 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7: Framer Enable (FRM_EN). This bit must be set to the desired state before writing INIT_DONE.
 0 = Framer disabled—held in low-power state.
 1 = Framer enabled—all features active.

Bit 6: Initialization Done (INIT_DONE). The user must set this bit once he has written the configuration registers. The host is required to write or clear all device registers prior to setting this bit. Once INIT_DONE is set, the DS26518 will check the FRM_EN bit and, if enabled, will begin operation based on the initial configuration.

Bit 5: Disable Receive-Side Synchronizer (DRSS). This bit must be set to the desired state before writing INIT_DONE.
 0 = Synchronizer enabled.
 1 = Synchronizer disabled.

Bit 1: Soft Reset (SFTRST). Level sensitive “soft” reset. Should be taken high, then low to reset the receiver.
 0 = Normal operation.
 1 = Reset the receiver.

Note: This reset does not clear the registers.

Bit 0: Receiver T1/E1 Mode Select (T1/E1). Sets operating mode for receiver only! This bit must be set to the desired state before writing INIT_DONE.
 0 = T1 operation.
 1 = E1 operation.

Register Name: **RCR1 (T1 Mode)**
 Register Description: **Receive Control Register 1**
 Register Address: **081h + (200h x (n - 1)) : where n = 1 to 8**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|-------|-------|-----|-----|-------|-----|-------|--------|
| Name | SYNCT | RB8ZS | RFM | ARC | SYNCC | RJC | SYNCE | RESYNC |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Note: This register has an alternate definition for E1 mode. See [RCR1](#).

Bit 7: Sync Time (SYNCT)

- 0 = Qualify 10 bits.
- 1 = Qualify 24 bits.

Bit 6: Receive B8ZS Enable (RB8ZS)

- 0 = B8ZS disabled.
- 1 = B8ZS enabled.

Bit 5: Receive Frame Mode Select (RFM)

- 0 = ESF framing mode.
- 1 = D4 framing mode.

Bit 4: Auto Resync Criteria (ARC)

- 0 = Resync on OOF or LOS event.
- 1 = Resync on OOF only.

Bit 3: Sync Criteria (SYNCC)

In D4 Framing Mode:

- 0 = Search for Ft pattern, then search for Fs pattern.
- 1 = Cross couple Ft and Fs pattern.

In ESF Framing Mode:

- 0 = Search for FPS pattern only.
- 1 = Search for FPS and verify with CRC-6.

Bit 2: Receive Japanese CRC-6 Enable (RJC)

- 0 = Use ANSI:AT&T:ITU-T CRC-6 calculation (normal operation).
- 1 = Use Japanese standard JT-G704 CRC-6 calculation.

Bit 1: Sync Enable (SYNCE)

- 0 = Auto resync enabled.
- 1 = Auto resync disabled.

Bit 0: Resynchronize (RESYNC). When toggled from low to high, a resynchronization of the receive-side framer is initiated. Must be cleared and set again for a subsequent resync.

Register Name: **RCR1 (E1 Mode)**
 Register Description: **Receive Control Register 1**
 Register Address: **081h + (200h x (n - 1)) : where n = 1 to 8**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|-------|-------|-------|-------|-----|-------|--------|
| Name | — | RHDB3 | RSIGM | RG802 | RCRC4 | FRC | SYNCE | RESYNC |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Note: This register has an alternate definition for T1 mode. See [RCR1](#).

Bit 6: Receive HDB3 Enable (RHDB3)

0 = HDB3 disabled.
 1 = HDB3 enabled (decoded per O.162).

Bit 5: Receive Signaling Mode Select (RSIGM)

0 = CAS signaling mode.
 1 = CCS signaling mode.

Bit 4: Receive G.802 Enable (RG802). See [Figure 11-30](#) for details.

0 = Do not force RCHBLK_n high during bit 1 of time slot 26.
 1 = Force RCHBLK_n high during bit 1 of time slot 26.

Bit 3: Receive CRC-4 Enable (RCRC4)

0 = CRC-4 disabled.
 1 = CRC-4 enabled.

Bit 2: Frame Resync Criteria (FRC)

0 = Resync if FAS received in error three consecutive times.
 1 = Resync if FAS or bit 2 of non-FAS is received in error three consecutive times.

Bit 1: Sync Enable (SYNCE)

0 = Auto resync enabled.
 1 = Auto resync disabled.

Bit 0: Resynchronize (RESYNC). When toggled from low to high, a resynchronization of the receive-side framer is initiated. Must be cleared and set again for a subsequent resync.

Register Name: **T1RIBCC (T1 Mode)**
 Register Description: **Receive In-Band Code Control Register**
 Register Address: **082h + (200h x (n - 1)) : where n = 1 to 8**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|---|------|------|------|------|------|------|
| Name | — | — | RUP2 | RUP1 | RUP0 | RDN2 | RDN1 | RDN0 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Note: This register has an alternate definition for E1 mode. See [E1RCR2](#).

Bits 5 to 3: Receive Up Code Length Definition Bits (RUP[2:0])

| RUP2 | RUP1 | RUP0 | LENGTH SELECTED |
|------|------|------|-----------------|
| 0 | 0 | 0 | 1 bits |
| 0 | 0 | 1 | 2 bits |
| 0 | 1 | 0 | 3 bits |
| 0 | 1 | 1 | 4 bits |
| 1 | 0 | 0 | 5 bits |
| 1 | 0 | 1 | 6 bits |
| 1 | 1 | 0 | 7 bits |
| 1 | 1 | 1 | 8 : 16 bits |

Bits 2 to 0: Receive Down Code Length Definition Bits (RDN[2:0])

| RDN2 | RDN1 | RDN0 | LENGTH SELECTED |
|------|------|------|-----------------|
| 0 | 0 | 0 | 1 bits |
| 0 | 0 | 1 | 2 bits |
| 0 | 1 | 0 | 3 bits |
| 0 | 1 | 1 | 4 bits |
| 1 | 0 | 0 | 5 bits |
| 1 | 0 | 1 | 6 bits |
| 1 | 1 | 0 | 7 bits |
| 1 | 1 | 1 | 8 : 16 bits |

Register Name: **E1RCR2 (E1 Mode)**
 Register Description: **Receive Control Register 2**
 Register Address: **082h + (200h x (n - 1)) : where n = 1 to 8**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|---|---|---|---|---|---|-------|
| Name | — | — | — | — | — | — | — | RLOSA |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Note: This register has an alternate definition for T1 mode. See [T1RIBCC](#).

Bit 0: Receive Loss of Signal Alternate Criteria (RLOSA). Defines the criteria for a loss of signal condition.

0 = LOS declared upon 255 consecutive zeros (125µs).

1 = LOS declared upon 2048 consecutive zeros (1ms).

Register Name: **RCR3**
 Register Description: **Receive Control Register 3**
 Register Address: **083h + (200h x (n - 1)) : where n = 1 to 8**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|-------|-------|-------|-------|---|-----|-----|
| Name | — | uALAW | RSERC | BINV1 | BINV0 | — | PLB | FLB |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 6: u-Law or A-Law Digital Milliwatt Code Select (uALAW)

0 = u-law code is inserted based on [T1RDMWE1](#)–3 or [E1RDMWE1](#)–4 registers.
 1 = A-law code is inserted based on [T1RDMWE1](#)–3 or [E1RDMWE1](#)–4 registers.

Bit 5: RSERn Control (RSERC)

0 = Allow RSERn to output data as received under all conditions (normal operation).
 1 = Force RSERn to one under loss of frame alignment conditions.

Bits 4 and 3: Receive Bit Inversion (BINV[1:0])

00 = No inversion.
 01 = Invert framing.
 10 = Invert signaling.
 11 = Invert payload.

Bit 1: Payload Loopback (PLB)

0 = Loopback disabled.
 1 = Loopback enabled.

When PLB is enabled, the following will occur:

- 1) Data will be transmitted on TTIPn and TRINGn synchronous with RCLKn instead of TCLKn.
- 2) All the receive-side signals will continue to operate normally.
- 3) The TCHCLKn and TCHBLKn signals are forced low.
- 4) Data at the TSERn, TDATA n, and TSiGn pins is ignored.

In a PLB situation, the DS26518 will loop the 192 bits (248 for E1) of payload data (with BPVs corrected) from the receive section back to the transmit section. The transmitter will follow the frame alignment provided by the receiver. The receive frame boundary is automatically fed into the transmit section, such that the transmit frame position is locked to the receiver (i.e., TSYNCn is sourced from RSYNCn). The FPS framing pattern, CRC-6 calculation, and the FDL bits (FAS word, Si, Sa, E bits, and CRC-4 for E1) are not looped back, they are reinserted by the DS26518 (i.e., the transmit section will modify the payload as if it was input at TSERn).

Bit 0: Framing Loopback (FLB)

0 = loopback disabled
 1 = loopback enabled

This loopback is useful in testing and debugging applications. In FLB, the DS26518 will loop data from the transmit side back to the receive side. When FLB is enabled, the following will occur:

- 1) (T1 mode) an unframed all-ones code will be transmitted at TTIPn and TRINGn.
 (E1 mode) normal data will be transmitted at TTIPn and TRINGn.
- 2) Data at RTIPn and RRINGn will be ignored.
- 3) All receive-side signals will take on timing synchronous with TCLKn instead of RCLKn.
 Note that it is not acceptable to have RCLKn tied to TCLKn during this loopback because this will cause an unstable condition.

Register Name: **E1RDMWE1, E1RDMWE2, E1RDMWE3, E1RDMWE4**
 Register Description: **E1 Receive Digital Milliwatt Enable Registers 1 to 4**
 Register Address: **000h, 001h, 002h, 003h + (200h x (n - 1)) : where n = 1 to 8**

| Bit # Name | (MSB) | | | | (LSB) | | | | |
|---------------|-------|------|------|------|-------|------|------|------|-----------------|
| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
| | CH8 | CH7 | CH6 | CH5 | CH4 | CH3 | CH2 | CH1 | E1RDMWE1 |
| | CH16 | CH15 | CH14 | CH13 | CH12 | CH11 | CH10 | CH9 | E1RDMWE2 |
| | CH24 | CH23 | CH22 | CH21 | CH20 | CH19 | CH18 | CH17 | E1RDMWE3 |
| | CH32 | CH31 | CH30 | CH29 | CH28 | CH27 | CH26 | CH25 | E1RDMWE4 |

Bits 7 to 0: E1 Receive Digital Milliwatt Enable for Channels 1 to 32 (CH[1:32])

0 = Do not affect the receive data associated with this channel.

1 = Replace the receive data associated with this channel with digital milliwatt code.

Register Name: **TDMWE1, TDMWE2, TDMWE3, TDMWE4 (T1 and E1 Modes)**
 Register Description: **Transmit Digital Milliwatt Enable Registers 1 to 4**
 Register Address: **100h, 101h, 102h, 103h + (200h x (n - 1)) : where n = 1 to 8**

| Bit # Name | (MSB) | | | | (LSB) | | | | |
|---------------|-------|------|------|------|-------|------|------|------|---------------|
| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
| | CH8 | CH7 | CH6 | CH5 | CH4 | CH3 | CH2 | CH1 | TDMWE1 |
| | CH16 | CH15 | CH14 | CH13 | CH12 | CH11 | CH10 | CH9 | TDMWE2 |
| | CH24 | CH23 | CH22 | CH21 | CH20 | CH19 | CH18 | CH17 | TDMWE3 |
| | CH32 | CH31 | CH30 | CH29 | CH28 | CH27 | CH26 | CH25 | TDMWE4 |

Bits 7 to 0: Transmit Digital Milliwatt Enable for Channels 1 to 32 (CH[1:32])

0 = Do not affect the transmit data associated with this channel.

1 = Replace the transmit data associated with this channel with digital milliwatt code.

Register Name: **RIOCR**
 Register Description: **Receive I/O Configuration Register**
 Register Address: **084h + (200h x (n - 1)) : where n = 1 to 8**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|----------------|-----------------|---------------|---------------|------|-------------|--------------|--------------|
| Name | RCLKINV | RSYNCINV | H100EN | RSCLKM | RSMS | RSIO | RSMS2 | RSMS1 |
| | <i>RCLKINV</i> | <i>RSYNCINV</i> | <i>H100EN</i> | <i>RSCLKM</i> | — | <i>RSIO</i> | <i>RSMS2</i> | <i>RSMS1</i> |
| Default | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |

Bit 7: RCLKn Invert (RCLKINV)

0 = No inversion.
 1 = Invert RCLKn.

Bit 6: RSYNCn Invert (RSYNCINV)

0 = No inversion.
 1 = Invert RSYNCn as either input or output.

Bit 5: H.100 Sync Mode (H100EN). See Section [9.8.3](#) for more information.

0 = Normal operation.
 1 = RSYNCn and TSSYNClOn signals are shifted.

Bit 4: RSYCLKn Mode Select (RSCLKM)

0 = If RSYCLKn is 1.544MHz.
 1 = If RSYCLKn is 2.048MHz or IBO enabled.

Bit 3: RSYNCn Multiframe Skip Control (RSMS) (T1 Mode Only). Useful in framing format conversions from D4 to ESF. This function is not available when the receive-side elastic store is enabled. RSYNCn must be set to output multiframe pulses.

0 = RSYNCn will output a pulse at every multiframe.
 1 = RSYNCn will output a pulse at every other multiframe.

Bit 2: RSYNCn I/O Select (RSIO). (**Note:** This bit must be set to zero when elastic store is disabled.) The default value for this bit is a logic 1 so that the default state of RSYNCn is as an input.

0 = RSYNCn is an output.
 1 = RSYNCn is an input (only valid if elastic store enabled).

Bit 1: RSYNCn Mode Select 2 (RSMS2)

T1: RSYNCn pin must be programmed in the output frame mode.

0 = do not pulse double wide in signaling frames.

1 = do pulse double wide in signaling frames.

E1: RSYNCn pin must be programmed in the output multiframe mode.

0 = RSYNCn outputs CAS multiframe boundaries.

1 = RSYNCn outputs CRC-4 multiframe boundaries.

In E1 mode, RSMS2 also selects which multiframe signal is available at the RMSYNCn pin, regardless of the configuration for RSYNCn. When RSMS2 = 0, RMSYNCn outputs CAS multiframe boundaries; when RSMS2 = 1, RMSYNCn outputs CRC-4 multiframe boundaries.

Bit 0: RSYNC Mode Select 1 (RSMS1). Selects frame or multiframe pulse when RSYNCn pin is in output mode. In input mode (elastic store must be enabled) multiframe mode is only useful when receive signaling reinsertion is enabled.

0 = Frame mode.
 1 = Multiframe mode.

Register Name: **RESCR**
 Register Description: **Receive Elastic Store Control Register**
 Register Address: **085h + (200h x (n - 1)) : where n = 1 to 8**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---------|---------|---|------|---------|------|--------|------|
| Name | RDATFMT | RGCLKEN | — | RSZS | RESALGN | RESR | RESMDM | RESE |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7: Receive Channel Data Format (RDATFMT)

0 = 64kbps (data contained in all 8 bits).
 1 = 56kbps (data contained in 7 out of the 8 bits).

Bit 6: Receive Gapped Clock Enable (RGCLKEN)

0 = RCHCLKn functions normally.
 1 = Enable gapped bit clock output on RCHCLKn.

Note: *RGPKEN and RDATFMT are not associated with the elastic store and will be explained in the fractional support section.*

Bit 4: Receive Slip Zone Select (RSZS). This bit determines the minimum distance allowed between the elastic store read and write pointers before forcing a controlled slip. This bit is only applies during T1 to E1 or E1 to T1 conversion applications.

0 = Force a slip at 9 bytes or less of separation (used for clustered blank channels).
 1 = Force a slip at 2 bytes or less of separation (used for distributed blank channels and minimum delay mode).

Bit 3: Receive Elastic Store Align (RESALGN). Setting this bit from a zero to a one will force the receive elastic store's write/read pointers to a minimum separation of half a frame. No action will be taken if the pointer separation is already greater or equal to half a frame. If pointer separation is less than half a frame, the command will be executed and the data will be disrupted. Should be toggled after RSYCLKn has been applied and is stable. Must be cleared and set again for a subsequent align.

Bit 2: Receive Elastic Store Reset (RESR). Setting this bit from a zero to a one will force the read pointer into the same frame that the write pointer is exiting, minimizing the delay through the elastic store. If this command should place the pointers within the slip zone (see bit 4), then an immediate slip will occur and the pointers will move back to opposite frames. Should be toggled after RSYCLKn has been applied and is stable. Do not leave this bit set HIGH.

Bit 1: Receive Elastic Store Minimum Delay Mode (RESMDM)

0 = Elastic stores operate at full two-frame depth.
 1 = Elastic stores operate at 32-bit depth.

Bit 0: Receive Elastic Store Enable (RESE)

0 = Elastic store is bypassed.
 1 = Elastic store is enabled.

Register Name: **ERCNT**
 Register Description: **Error Counter Configuration Register**
 Register Address: **086h + (200h x (n - 1)) : where n = 1 to 8**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|--------------|-------------|-------------|-------------|-------------|------|--------|---------------|
| Name | 1SECS | MCUS | MECU | ECUS | EAMS | FSBE | MOSCRF | LCVCRF |
| | <i>1SECS</i> | <i>MCUS</i> | <i>MECU</i> | <i>ECUS</i> | <i>EAMS</i> | — | — | <i>LCVCRF</i> |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7: One-Second Select (1SECS). This bit allows for synchronization of the error counter updates between multiple ports. When `ERCNT.3 = 0`, setting this bit (on a specific framer) will update the framer's error counters on the transition of the one-second timer from framer 1. Note that this bit should always be clear for framer 1.

- 0 = Use the one-second timer that is internal to the framer.
- 1 = Use the one-second timer from framer 1 to latch updates.

Bit 6 : Manual Counter Update Select (MCUS). When manual update mode is enabled with `EAMS`, this bit can be used to allow the incoming `LATCH_CNT` signal to latch all counters. Useful for synchronously latching counters of multiple DS26518 cores located on the same die.

- 0 = `MECU` is used to manually latch counters.
- 1 = Counters are latched on the rising edge of the `LATCH_CNT` signal.

Bit 5: Manual Error Counter Update (MECU). When enabled by `ERCNT.3`, the changing of this bit from a 0 to a 1 allows the next clock cycle to load the error counter registers with the latest counts and reset the counters. The user must wait a minimum of 250µs before reading the error count registers to allow for proper update.

Bit 4: Error Counter Update Select (ECUS)

T1 mode:

- 0 = Update error counters once a second.
- 1 = Update error counters every 42ms (333 frames).

E1 mode:

- 0 = Update error counters once a second.
- 1 = Update error counters every 62.5ms (500 frames).

Bit 3: Error Accumulation Mode Select (EAMS)

- 0 = Automatic updating of error counters enabled. The state of `ERCNT.4` determines accumulation time (timed update).
- 1 = User toggling of `ERCNT.5` determines accumulation time (manual update).

Bit 2: PCVCR Fs-Bit Error Report Enable (FSBE) (T1 Mode Only)

- 0 = Do not report bit errors in Fs-bit position; only Ft-bit position.
- 1 = Report bit errors in Fs-bit position as well as Ft-bit position.

Bit 1: Multiframe Out of Sync Count Register Function Select (MOSCRF) (T1 Mode Only)

- 0 = Count errors in the framing bit position.
- 1 = Count the number of multiframes out of sync.

Bit 0: T1 Line Code Violation Count Register Function Select (LCVCRF)

- 0 = Do not count excessive zeros.
- 1 = Count excessive zeros.

Register Name: **RHFC**
 Register Description: **Receive HDLC-64 FIFO Control Register**
 Register Address: **087h + (200h x (n - 1)) : where n = 1 to 8**

| | | | | | | | | |
|---------|---|---|---|---|---|---|--------|--------|
| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | — | — | — | — | — | — | RFHWM1 | RFHWM0 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 1 and 0 : Receive FIFO High Watermark Select (RFHWM[1:0])

| RFHWM1 | RFHWM0 | Receive FIFO Watermark |
|--------|--------|------------------------|
| 0 | 0 | 4 bytes |
| 0 | 1 | 16 bytes |
| 1 | 0 | 32 bytes |
| 1 | 1 | 48 bytes |

Register Name: **RIBOC**
 Register Description: **Receive Interleave Bus Operation Control Register**
 Register Address: **088h + (200h x (n - 1)) : where n = 1 to 8**

| | | | | | | | | |
|---------|---|---|---|--------|-------|---|---|---|
| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | — | — | — | IBOSEL | IBOEN | — | — | — |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 4: Interleave Bus Operation Select (IBOSEL). This bit selects channel or frame interleave mode.

0 = Channel Interleave

1 = Frame Interleave

Bit 3: Interleave Bus Operation Enable (IBOEN)

0 = Interleave Bus Operation disabled.

1 = Interleave Bus Operation enabled.

Register Name: **T1RSCC (T1 Mode Only)**
 Register Description: **In-Band Receive Spare Control Register**
 Register Address: **089h + (200h x (n - 1)) : where n = 1 to 8**

| | | | | | | | | |
|---------|---|---|---|---|---|------|------|------|
| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | — | — | — | — | — | RSC2 | RSC1 | RSC0 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 2 to 0: Receive Spare Code Length Definition Bits (RSC[2:0])

| RSC2 | RSC1 | RSC0 | LENGTH SELECTED |
|------|------|------|-----------------|
| 0 | 0 | 0 | 1 bits |
| 0 | 0 | 1 | 2 bits |
| 0 | 1 | 0 | 3 bits |
| 0 | 1 | 1 | 4 bits |
| 1 | 0 | 0 | 5 bits |
| 1 | 0 | 1 | 6 bits |
| 1 | 1 | 0 | 7 bits |
| 1 | 1 | 1 | 8 : 16 bits |

Register Name: **RXPC**
 Register Description: **Receive Expansion Port Control Register (HDLC-256)**
 Register Address: **08Ah + (200h x (n - 1)) : where n = 1 to 8**

| | | | | | | | | |
|---------|-------------|-------------|---|---|---|---------------|--------|--------------|
| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | RHMS | RHEN | — | — | — | RBPDIR | RBPFUS | RBPEN |
| | <i>RHMS</i> | <i>RHEN</i> | — | — | — | <i>RBPDIR</i> | — | <i>RBPEN</i> |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7 (T1 Mode): Receive HDLC-256 Mode Select (RHMS)

0 = Receive HDLC-256 assigned to time slots

1 = Receive HDLC-256 assigned to FDL bits

Bit 7 (E1 Mode): Receive HDLC-256 Mode Select (RHMS)

0 = Receive HDLC-256 assigned to time slots

1 = Receive HDLC-256 assigned to the Sa bits

Bit 6: Receive HDLC-256 Enable (RHEN)

0 = Receive HDLC-256 is not active.

1 = Receive HDLC-256 is active.

Bit 2: Receive BERT Port Direction Control (RBPDIR)

0 = Normal (line) operation. Rx BERT port receives data from the receive framer.

1 = System (backplane) operation. Rx BERT port receives data from the transmit path. The transmit path enters the receive BERT on the line side of the elastic store (if enabled).

Bit 1: Receive BERT Port Framed/Unframed Select (RBPFUS) (T1 Mode Only)

0 = The DS26518's receive BERT will *not* clock data from the F-bit position (framed).

1 = The DS26518's receive BERT will clock data from the F-bit position (unframed).

Bit 0: Receive BERT Port Enable (RBPEN)

0 = Receive BERT port is not active.

1 = Receive BERT port is active.

Register Name: **RBPBS**
 Register Description: **Receive BERT Port Bit Suppress Register**
 Register Address: **08Bh + (200h x (n - 1)) : where n = 1 to 8**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|--------|--------|--------|--------|--------|--------|--------|--------|
| Name | BPBSE8 | BPBSE7 | BPBSE6 | BPBSE5 | BPBSE4 | BPBSE3 | BPBSE2 | BPBSE1 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7: Receive Channel Bit 8 Suppress (BPBSE8). MSB of the channel. Set to one to stop this bit from being used.

Bit 6: Receive Channel Bit 7 Suppress (BPBSE7). Set to one to stop this bit from being used.

Bit 5: Receive Channel Bit 6 Suppress (BPBSE6). Set to one to stop this bit from being used.

Bit 4: Receive Channel Bit 5 Suppress (BPBSE5). Set to one to stop this bit from being used.

Bit 3: Receive Channel Bit 4 Suppress (BPBSE4). Set to one to stop this bit from being used.

Bit 2: Receive Channel Bit 3 Suppress (BPBSE3). Set to one to stop this bit from being used.

Bit 1: Receive Channel Bit 2 Suppress (BPBSE2). Set to one to stop this bit from being used.

Bit 0: Receive Channel Bit 1 Suppress (BPBSE1). LSB of the channel. Set to one to stop this bit from being used.

Register Name: **RHBS**
 Register Description: **Receive HDLC-256 Bit Suppress Register**
 Register Address: **08Dh**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|--------|--------|--------|--------|--------|--------|--------|--------|
| Name | RHBSE8 | RHBSE7 | RHBSE6 | RHBSE5 | RHBSE4 | RHBSE3 | RHBSE2 | RHBSE1 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7: Receive Channel Bit 8 Suppress (RHBSE8). MSB of the channel. Set to one to stop this bit from being used.

Bit 6: Receive Channel Bit 7 Suppress (RHBSE7). Set to one to stop this bit from being used.

Bit 5: Receive Channel Bit 6 Suppress (RHBSE6). Set to one to stop this bit from being used.

Bit 4: Receive Channel Bit 5 Suppress/Sa4 Bit Suppress (RHBSE5). Set to one to stop this bit from being used.

Bit 3: Receive Channel Bit 4 Suppress/Sa5 Bit Suppress (RHBSE4). Set to one to stop this bit from being used.

Bit 2: Receive Channel Bit 3 Suppress/Sa6 Bit Suppress (RHBSE3). Set to one to stop this bit from being used.

Bit 1: Receive Channel Bit 2 Suppress/Sa7 Bit Suppress (RHBSE2). Set to one to stop this bit from being used.

Bit 0: Receive Channel Bit 1 Suppress/Sa8 Bit Suppress (RHBSE1). LSB of the channel. Set to one to stop this bit from being used.

Register Name: **RLS1**
 Register Description: **Receive Latched Status Register 1**
 Register Address: **090h + (200h x (n - 1)) : where n = 1 to 8**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|-------|-------|-------|-------|-------|-------|-------|-------|
| Name | RRAIC | RAISC | RLOSC | RLOFC | RRAID | RAISD | RLOSD | RLOFD |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Note: All bits in this register are latched and can create interrupts.

Bit 7: Receive Remote Alarm Indication Condition Clear (RRAIC). Falling edge detect of RRAI. Set when a RRAI condition has cleared.

Bit 6: Receive Alarm Indication Signal Condition Clear (RAISC). Falling edge detect of RAIS. Set when a RAIS condition has cleared.

Bit 5: Receive Loss of Signal Condition Clear (RLOSC). Falling edge detect of RLOS. Set when an RLOS condition has cleared.

Bit 4: Receive Loss of Frame Condition Clear (RLOFC). Falling edge detect of RLOF. Set when an RLOF condition has cleared.

Bit 3: Receive Remote Alarm Indication Condition Detect (RRAID). Rising edge detect of RRAI. Set when a remote alarm is received at RRINGn and RTIPn.

Bit 2: Receive Alarm Indication Signal Condition Detect (RAISD). Rising edge detect of RAIS. Set when an unframed all-ones code is received at RRINGn and RTIPn.

Bit 1: Receive Loss of Signal Condition Detect (RLOSD). Rising edge detect of RLOS. Set when 192 consecutive zeros have been detected at RRINGn and RTIPn.

Bit 0: Receive Loss of Frame Condition Detect (RLOFD). Rising edge detect of RLOF. Set when the DS26518 has lost synchronized to the received data stream.

Register Name: **RLS2 (T1 Mode)**
 Register Description: **Receive Latched Status Register 2**
 Register Address: **091h + (200h x (n - 1)) : where n = 1 to 8**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|---|------|-----|------|------|------|-----|
| Name | — | — | COFA | 8ZD | 16ZD | SEFE | B8ZS | FBE |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Note: All bits in these register are latched. This register does not create interrupts. See [RLS2](#) for E1 Mode.

Bit 5: Change of Frame Alignment Event (COFA). Set when the last resync resulted in a change of frame or multiframe alignment.

Bit 4: Eight Zero Detect Event (8ZD). Set when a string of at least eight consecutive zeros (regardless of the length of the string) have been received at RRINGn and RTIPn.

Bit 3: Sixteen Zero Detect Event (16ZD). Set when a string of at least sixteen consecutive zeros (regardless of the length of the string) have been received at RRINGn and RTIPn.

Bit 2: Severely Errored Framing Event (SEFE). Set when 2 out of 6 framing bits (Ft or FPS) are received in error.

Bit 1: B8ZS Codeword Detect Event (B8ZS). Set when a B8ZS codeword is detected at RRINGn and RTIPn independent of whether the B8ZS mode is selected or not. Useful for automatically setting the line coding.

Bit 0: Frame Bit Error Event (FBE). Set when a Ft (D4) or FPS (ESF) framing bit is received in error.

Register Name: **RLS2 (E1 Mode)**
 Register Description: **E1 Receive Latched Status Register 2**
 Register Address: **091h + (200h x (n - 1)) : where n = 1 to 8**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|-------|-------|-------|------|------|------|-----|
| Name | — | CRCRC | CASRC | FASRC | RSA1 | RSA0 | RCMF | RAF |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Note: All bits in this register are latched. Bits 0 to 3 can cause interrupts. There is no associated real-time register. See [RLS2](#) for T1 Mode.

Bit 6: CRC Resync Criteria Met Event (CRCRC). Set when 915:1000 codewords are received in error.

Bit 5: CAS Resync Criteria Met Event (CASRC). Set when 2 consecutive CAS MF alignment words are received in error.

Bit 4: FAS Resync Criteria Met Event (FASRC). Set when 3 consecutive FAS words are received in error.

Bit 3: Receive Signaling All Ones Event (RSA1). Set when the contents of time slot 16 contains fewer than three zeros over 16 consecutive frames. This alarm is not disabled in the CCS signaling mode.

Bit 2: Receive Signaling All Zeros Event (RSA0). Set when over a full MF, time slot 16 contains all zeros.

Bit 1: Receive CRC-4 Multiframe Event (RCMF). Set on CRC-4 multiframe boundaries; will continue to be set every 2ms on an arbitrary boundary if CRC-4 is disabled.

Bit 0: Receive Align Frame Event (RAF). Set approximately every 250µs to alert the host that Si and Sa bits are available in the RAF and RRAF registers.

Register Name: **RLS3 (T1 Mode)**
 Register Description: **Receive Latched Status Register 3**
 Register Address: **092h + (200h x (n - 1)) : where n = 1 to 8**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|-------|------|------|------|-------|------|------|------|
| Name | LORCC | LSPC | LDNC | LUPC | LORCD | LSPD | LDND | LUPD |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Note: All bits in this register are latched and can create interrupts. See [RLS3](#) for E1 Mode.

Bit 7: Loss of Receive Clock Condition Clear (LORCC). Falling edge detect of LORC. Set when an LORC condition was detected and then removed.

Bit 6: Spare Code Detected Condition Clear (LSPC). Falling edge detect of LSP. Set when a spare-code match condition was detected and then removed.

Bit 5: Loop-Down Code Detected Condition Clear (LDNC). Falling edge detect of LDN. Set when a loop-down condition was detected and then removed.

Bit 4: Loop-Up Code Detected Condition Clear (LUPC). Falling edge detect of LUP. Set when a loop-up condition was detected and then removed.

Bit 3: Loss of Receive Clock Condition Detect (LORCD). Rising edge detect of LORC. Set when the RCLKn pin has not transitioned for one channel time.

Bit 2: Spare Code Detected Condition Detect (LSPD). Rising edge detect of LSP. Set when the spare code as defined in the [T1RSCD1:T1RSCD2](#) registers is being received.

Bit 1: Loop-Down Code Detected Condition Detect (LDND). Rising edge detect of LDN. Set when the loop-down code as defined in the [T1RDNCD1:T1RDNCD2](#) register is being received.

Bit 0: Loop-Up Code Detected Condition Detect (LUPD). Rising edge detect of LUP. Set when the loop-up code as defined in the [T1RUPCD1:T1RUPCD2](#) register is being received.

Register Name: **RLS3 (E1 Mode)**
 Register Description: **Receive Latched Status Register 3**
 Register Address: **092h + (200h x (n - 1)) : where n = 1 to 8**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|-------|---|---------|-------|-------|---|---------|-------|
| Name | LORCC | — | V52LNKC | RDMAC | LORCD | — | V52LNKD | RDMAD |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Note: All bits in this register are latched and can create interrupts. See [RLS3](#) for T1 Mode.

Bit 7: Loss of Receive Clock Clear (LORCC). Change of state indication. Set when an LORC condition has cleared (falling edge detect of LORC).

Bit 5: V5.2 Link Detected Clear (V52LNKC). Change of state indication. Set when a V52LNK condition has cleared (falling edge detect of V52LNK).

Bit 4: Receive Distant MF Alarm Clear (RDMAC). Change of state indication. Set when an RDMA condition has cleared (falling edge detect of RDMA).

Bit 3: Loss of Receive Clock Detect (LORCD). Change of state indication. Set when the RCLKn pin has not transitioned for one channel time (rising edge detect of LORC).

Bit 1: V5.2 Link Detect (V52LNKD). Change of state indication. Set on detection of a V5.2 link identification signal (G.965). This is the rising edge detect of V52LNK.

Bit 0: Receive Distant MF Alarm Detect (RDMAD). Change of state indication. Set when bit 6 of time slot 16 in frame 0 has been set for two consecutive multiframes. This alarm is not disabled in the CCS signaling mode. This is the rising edge detect of RDMA.

Register Name: **RLS4**
 Register Description: **Receive Latched Status Register 4**
 Register Address: **093h + (200h x (n - 1)) : where n = 1 to 8**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|------|-------|-------|---|-------|------|-------|-----|
| Name | RESF | RESEM | RSLIP | — | RSCOS | 1SEC | TIMER | RMF |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Note: All bits in this register are latched and can create interrupts.

Bit 7: Receive Elastic Store Full Event (RESF). Set when the receive elastic store buffer fills and a frame is deleted.

Bit 6: Receive Elastic Store Empty Event (RESEM). Set when the receive elastic store buffer empties and a frame is repeated.

Bit 5: Receive Elastic Store Slip Occurrence Event (RSLIP). Set when the receive elastic store has either repeated or deleted a frame.

Bit 3: Receive Signaling Change of State Event (RSCOS). Set when any channel selected by the Receive Signaling Change of State Interrupt Enable registers ([RSCSE1](#) through RSCSE3) changes signaling state.

Bit 2: One-Second Timer (1SEC). Set on every one-second interval based on RCLKn.

Bit 1: Timer Event (TIMER). This status bit indicates that the performance monitor counters have been updated and are available to be read by the host. The error counter update interval as determined by the settings in the Error Counter Configuration Register ([ERCNT](#)).

T1: Set on increments of 1 second or 42ms based on RCLKn, or a manual latch event.

E1: Set on increments of 1 second or 62.5ms based on RCLKn, or a manual latch event.

Bit 0: Receive Multiframe Event (RMF)

T1 Mode: Set every 1.5ms on D4 MF boundaries or every 3ms on ESF MF boundaries.

E1 Mode: Set every 2.0ms on receive CAS multiframe boundaries to alert host the signaling data is available. Continues to set on an arbitrary 2.0ms boundary when CAS signaling is not enabled.

Register Name: **RLS5**
 Register Description: **Receive Latched Status Register 5 (HDLC-64)**
 Register Address: **094h + (200h x (n - 1)) : where n = 1 to 8**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|---|------|-------|-----|-----|-------|------|
| Name | — | — | ROVR | RHOBT | RPE | RPS | RHWMS | RNES |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Note: All bits in this register are latched and can cause interrupts.

Bit 5: Receive FIFO Overrun (ROVR). Set when the receive HDLC-64 controller has terminated packet reception because the FIFO buffer is full.

Bit 4: Receive HDLC-64 Opening Byte Event (RHOBT). Set when the next byte available in the receive FIFO is the first byte of a message.

Bit 3: Receive Packet End Event (RPE). Set when the HDLC-64 controller detects either the finish of a valid message (i.e., CRC check complete) or when the controller has experienced a message fault such as a CRC checking error, or an overrun condition, or an abort has been seen. This is a latched bit and will be cleared when read.

Bit 2: Receive Packet Start Event (RPS). Set when the HDLC-64 controller detects an opening byte. This is a latched bit and will be cleared when read.

Bit 1: Receive FIFO Above High Watermark Set Event (RHWMS). Set when the receive 64-byte FIFO crosses the high watermark as defined by the Receive HDLC-64 FIFO Control Register ([RHFC](#)). Rising edge detect of RHWM.

Bit 0: Receive FIFO Not Empty Set Event (RNES). Set when the receive FIFO has transitioned from “empty” to “not empty” (at least one byte has been put into the FIFO). Rising edge detect of RNE.

Register Name: **RLS7 (T1 Mode)**
 Register Description: **Receive Latched Status Register 7**
 Register Address: **096h + (200h x (n - 1)) : where n = 1 to 8**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|---|---------|---------|--------|-------|----|----|
| Name | — | — | RRAI-CI | RAIS-CI | RSLC96 | RFDLF | BC | BD |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Note: All bits in this register are latched and can create interrupts. See [RLS7](#) for E1 Mode.

Bit 5: Receive RAI-CI Detect (RRAI-CI). Set when an RAI-CI pattern has been detected by the receiver. This bit is active in ESF framing mode only, and will set only if an RAI condition is being detected ([RRTS1.3](#)). When the host reads (and clears) this bit, it will set again each time the RAI-CI pattern is detected (approximately every 1.1 seconds).

Bit 4: Receive AIS-CI Detect (RAIS-CI). Set when an AIS-CI pattern has been detected by the receiver. This bit will set only if an AIS condition is being detected ([RRTS1.2](#)). This is a latched bit that must be cleared by the host, and will set again each time the AIS-CI pattern is detected (approximately every 1.2 seconds).

Bit 3: Receive SLC-96 Alignment Event (RSLC96). Set when a valid SLC-96 alignment pattern is detected in the Fs bit stream, and the [T1RSLC1–3](#) registers have data available for retrieval. See Section [9.9.4.4](#) for more information.

Bit 2: Receive FDL Register Full Event (RFDLF). Set when the 8-bit [T1RFDL](#) register is full. Useful for SLC-96 operation, or manual extraction of FDL data bits. See Section [9.9.5.4](#) for more information.

Bit 1: BOC Clear Event (BC). Set when a valid BOC is no longer detected (with the disintegration filter applied).

Bit 0: BOC Detect Event (BD). Set when a valid BOC has been detected (with the BOC filter applied).

Register Name: **RLS7 (E1 Mode)**
 Register Description: **Receive Latched Status Register 7**
 Register Address: **096h + (200h x (n - 1)) : where n = 1 to 8**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|---|---|---|---|---|-------|-------|
| Name | — | — | — | — | — | — | Sa6CD | SaXCD |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Note: All bits in this register are latched and can create interrupts. See [RLS7](#) for T1 Mode.

Bit 1: Sa6 Codeword Detect (Sa6CD). Set when a valid codeword (per ETS 300 233) is detected in the Sa6 bit positions.

Bit 0: SaX Bit Change Detect (SaXCD). Set when a bit change is detected in the SaX bit position. The enabled SaX bits are selected by the [E1RS AIMR](#) register.

Register Name: **RSS1, RSS2, RSS3, RSS4**
 Register Description: **Receive-Signaling Status Registers 1 to 4**
 Register Address: **098h, 099h, 09Ah, 09Bh + (200h x (n - 1)) : where n = 1 to 8**

| Bit # Name | (MSB) | | | | (LSB) | | | | |
|---------------|-------|------|------|------|-------|------|------|-------|----------------------------|
| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
| | CH8 | CH7 | CH6 | CH5 | CH4 | CH3 | CH2 | CH1* | RSS1 |
| | CH16 | CH15 | CH14 | CH13 | CH12 | CH11 | CH10 | CH9 | RSS2 |
| | CH24 | CH23 | CH22 | CH21 | CH20 | CH19 | CH18 | CH17* | RSS3 |
| | CH32 | CH31 | CH30 | CH29 | CH28 | CH27 | CH26 | CH25 | RSS4 (E1 Mode Only) |

Note: Status bits in this register are latched.

When a channel's signaling data changes state, the respective bit in registers RSS1–4 will be set and latched. The RSCOS bit ([RLS4.3](#)) will be set if the channel was also enabled by setting the appropriate bit in [RSCSE1–4](#). The $\overline{\text{INTB}}$ signal will go low if enabled by the interrupt mask bit [RIM4.3](#). The bit will remain set until read.

*Note that in E1 CAS mode, the LSB of RSS1 would typically represent the CAS alignment bits, and the LSB of [RSS3](#) represents reserved bits and the distant multiframe alarm.

Register Name: **T1RSCD1 (T1 Mode Only)**
 Register Description: **Receive Spare Code Definition Register 1**
 Register Address: **09Ch + (200h x (n - 1)) : where n = 1 to 8**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|----|----|----|----|----|----|----|----|
| Name | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Note: Writing this register resets the detector's integration period.

Bit 7: Receive Spare Code Definition Bit 7 (C7). First bit of the repeating pattern.

Bit 6: Receive Spare Code Definition Bit 6 (C6). A Don't Care if a 1-bit length is selected.

Bit 5: Receive Spare Code Definition Bit 5 (C5). A Don't Care if a 1- or 2-bit length is selected.

Bit 4: Receive Spare Code Definition Bit 4 (C4). A Don't Care if a 1- to 3-bit length is selected.

Bit 3: Receive Spare Code Definition Bit 3 (C3). A Don't Care if a 1- to 4-bit length is selected.

Bit 2: Receive Spare Code Definition Bit 2 (C2). A Don't Care if a 1- to 5-bit length is selected.

Bit 1: Receive Spare Code Definition Bit 1 (C1). A Don't Care if a 1- to 6-bit length is selected.

Bit 0: Receive Spare Code Definition Bit 0 (C0). A Don't Care if a 1- to 7-bit length is selected.

Register Name: **T1RSCD2 (T1 Mode Only)**
 Register Description: **Receive Spare Code Definition Register 2**
 Register Address: **09Dh + (200h x (n - 1)) : where n = 1 to 8**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|----|----|----|----|----|----|----|----|
| Name | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7: Receive Spare Code Definition Bit 7 (C7). A Don't Care if a 1- to 7-bit length is selected.

Bit 6: Receive Spare Code Definition Bit 6 (C6). A Don't Care if a 1- to 7-bit length is selected.

Bit 5: Receive Spare Code Definition Bit 5 (C5). A Don't Care if a 1- to 7-bit length is selected.

Bit 4: Receive Spare Code Definition Bit 4 (C4). A Don't Care if a 1- to 7-bit length is selected.

Bit 3: Receive Spare Code Definition Bit 3 (C3). A Don't Care if a 1- to 7-bit length is selected.

Bit 2: Receive Spare Code Definition Bit 2 (C2). A Don't Care if a 1- to 7-bit length is selected.

Bit 1: Receive Spare Code Definition Bit 1 (C1). A Don't Care if a 1- to 7-bit length is selected.

Bit 0: Receive Spare Code Definition Bit 0 (C0). A Don't Care if a 1- to 7-bit length is selected.

Register Name: **RIIR**
 Register Description: **Receive Interrupt Information Register**
 Register Address: **9Fh + (200h x (n - 1)) : where n = 1 to 8**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|------|-------|------|------|------|--------|------|
| Name | — | RLS7 | RLS6* | RLS5 | RLS4 | RLS3 | RLS2** | RLS1 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

* RLS6 is reserved for future use.

** Currently RLS2 does not create an interrupt, therefore this bit is not used in T1 mode.

The Receive Interrupt Information Register indicates which of the DS26518 status registers are generating an interrupt. When an interrupt occurs, the host can read RIIR to quickly identify which of the receive status registers is (are) causing the interrupt(s). The Receive Interrupt Information Register bits will clear once the appropriate interrupt has been serviced and cleared, as long as no additional, unmasked interrupt condition is present in the associated status register. Status bits that have been masked via the Receive Interrupt Mask (RIMx) registers will also be masked from the RIIR register.

Register Name: **RIM1**
 Register Description: **Receive Interrupt Mask Register 1**
 Register Address: **0A0h + (200h x (n - 1)) : where n = 1 to 8**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|-------|-------|-------|-------|-------|-------|-------|-------|
| Name | RRAIC | RAISC | RLOSC | RLOFC | RRAID | RAISD | RLOSD | RLOFD |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7: Receive Remote Alarm Indication Condition Clear (RRAIC)

0 = Interrupt masked.
 1 = Interrupt enabled.

Bit 6: Receive Alarm Indication Signal Condition Clear (RAISC)

0 = Interrupt masked.
 1 = Interrupt enabled.

Bit 5: Receive Loss of Signal Condition Clear (RLOSC)

0 = Interrupt masked.
 1 = Interrupt enabled.

Bit 4: Receive Loss of Frame Condition Clear (RLOFC)

0 = Interrupt masked.
 1 = Interrupt enabled.

Bit 3 : Receive Remote Alarm Indication Condition Detect (RRAID)

0 = Interrupt masked.
 1 = Interrupt enabled.

Bit 2: Receive Alarm Indication Signal Condition Detect (RAISD)

0 = Interrupt masked.
 1 = Interrupt enabled.

Bit 1: Receive Loss of Signal Condition Detect (RLOSD)

0 = Interrupt masked.
 1 = Interrupt enabled.

Bit 0: Receive Loss of Frame Condition Detect (RLOFD)

0 = Interrupt masked.
 1 = Interrupt enabled.

Register Name: **RIM2 (E1 Mode Only)**
 Register Description: **E1 Receive Interrupt Mask Register 2**
 Register Address: **0A1h + (200h x (n - 1)) : where n = 1 to 8**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|---|---|---|------|------|------|-----|
| Name | — | — | — | — | RSA1 | RSA0 | RCMF | RAF |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 3: Receive-Signaling All Ones Event (RSA1)

0 = Interrupt masked.
 1 = Interrupt enabled.

Bit 2: Receive-Signaling All Zeros Event (RSA0)

0 = Interrupt masked.
 1 = interrupt enabled.

Bit 1: Receive CRC-4 Multiframe Event (RCMF)

0 = Interrupt masked.
 1 = Interrupt enabled.

Bit 0: Receive Align Frame Event (RAF)

0 = Interrupt masked.
 1 = Interrupt enabled.

Register Name: **RIM3 (T1 Mode)**
 Register Description: **Receive Interrupt Mask Register 3**
 Register Address: **0A2h + (200h x (n - 1)) : where n = 1 to 8**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|-------|------|------|------|-------|------|------|------|
| Name | LORCC | LSPC | LDNC | LUPC | LORCD | LSPD | LDND | LUPD |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Note: See [RIM3](#) for E1 Mode.

Bit 7: Loss of Receive Clock Condition Clear (LORCC)

0 = Interrupt masked.
 1 = Interrupt enabled.

Bit 6: Spare Code Detected Condition Clear (LSPC)

0 = Interrupt masked.
 1 = Interrupt enabled.

Bit 5: Loop-Down Code Detected Condition Clear (LDNC)

0 = Interrupt masked.
 1 = Interrupt enabled.

Bit 4: Loop-Up Code Detected Condition Clear (LUPC)

0 = Interrupt masked.
 1 = Interrupt enabled.

Bit 3: Loss of Receive Clock Condition Detect (LORCD)

0 = Interrupt masked
 1 = Interrupt enabled

Bit 2: Spare Code Detected Condition Detect (LSPD)

0 = Interrupt masked.
 1 = Interrupt enabled.

Bit 1 : Loop-Down Code Detected Condition Detect (LDND)

0 = Interrupt masked.
 1 = Interrupt enabled.

Bit 0: Loop-Up Code Detected Condition Detect (LUPD)

0 = Interrupt masked.
 1 = Interrupt enabled.

Register Name: **RIM3 (E1 Mode)**
 Register Description: **E1 Receive Interrupt Mask Register 3**
 Register Address: **0A2h + (200h x (n - 1)) : where n = 1 to 8**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|-------|---|---------|-------|-------|---|---------|-------|
| Name | LORCC | — | V52LNKC | RDMAC | LORCD | — | V52LNKD | RDMAD |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Note: See [RIM3](#) for T1 Mode.

Bit 7: Loss of Receive Clock Clear (LORCC)

0 = Interrupt masked.
 1 = Interrupt enabled.

Bit 5: V5.2 Link Detected Clear (V52LNKC)

0 = Interrupt masked.
 1 = Interrupt enabled.

Bit 4: Receive Distant MF Alarm Clear (RDMAC)

0 = Interrupt masked.
 1 = Interrupt enabled.

Bit 3: Loss of Receive Clock Detect (LORCD)

0 = Interrupt masked.
 1 = Interrupt enabled.

Bit 1: V5.2 Link Detect (V52LNKD)

0 = Interrupt masked.
 1 = Interrupt enabled.

Bit 0: Receive Distant MF Alarm Detect (RDMAD)

0 = Interrupt masked.
 1 = Interrupt enabled.

Register Name: **RIM4**
 Register Description: **Receive Interrupt Mask Register 4**
 Register Address: **0A3h + (200h x (n - 1)) : where n = 1 to 8**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|------|-------|-------|---|-------|------|-------|-----|
| Name | RESF | RESEM | RSLIP | — | RSCOS | 1SEC | TIMER | RMF |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7: Receive Elastic Store Full Event (RESF)

0 = Interrupt masked.
 1 = Interrupt enabled.

Bit 6: Receive Elastic Store Empty Event (RESEM)

0 = Interrupt masked.
 1 = Interrupt enabled.

Bit 5: Receive Elastic Store Slip Occurrence Event (RSLIP)

0 = Interrupt masked.
 1 = Interrupt enabled.

Bit 3: Receive Signaling Change of State Event (RSCOS)

0 = Interrupt masked.
 1 = Interrupt enabled.

Bit 2: One-Second Timer (1SEC)

0 = Interrupt masked.
 1 = Interrupt enabled.

Bit 1: Timer Event (TIMER)

0 = Interrupt masked.
 1 = Interrupt enabled.

Bit 0: Receive Multiframe Event (RMF)

0 = Interrupt masked.
 1 = Interrupt enabled.

Register Name: **RIM5**
 Register Description: **Receive Interrupt Mask 5 (HDLC-64)**
 Register Address: **0A4h + (200h x (n - 1)) : where n = 1 to 8**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|---|------|-------|-----|-----|-------|------|
| Name | — | — | ROVR | RHOBT | RPE | RPS | RHWMS | RNES |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 5: Receive FIFO Overrun (ROVR)

0 = Interrupt masked.
 1 = Interrupt enabled.

Bit 4: Receive HDLC-64 Opening Byte Event (RHOBT)

0 = Interrupt masked.
 1 = Interrupt enabled.

Bit 3: Receive Packet End Event (RPE)

0 = Interrupt masked.
 1 = Interrupt enabled.

Bit 2: Receive Packet Start Event (RPS)

0 = Interrupt masked.
 1 = Interrupt enabled.

Bit 1: Receive FIFO Above High Watermark Set Event (RHWMS)

0 = Interrupt masked.
 1 = Interrupt enabled.

Bit 0: Receive FIFO Not Empty Set Event (RNES)

0 = Interrupt masked.
 1 = Interrupt enabled.

Register Name: **RIM7 (T1 Mode)**
 Register Description: **Receive Interrupt Mask Register 7 (BOC:FDL)**
 Register Address: **0A6h + (200h x (n - 1)) : where n = 1 to 8**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|---|---------|---------|--------|-------|----|----|
| Name | — | — | RRAI-CI | RAIS-CI | RSLC96 | RFDLF | BC | BD |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Note: See [RIM7](#) for E1 Mode.

Bit 5: Receive RAI-CI (RRAI-CI)

0 = Interrupt masked.
 1 = Interrupt enabled.

Bit 4: Receive AIS-CI (RAIS-CI)

0 = Interrupt masked.
 1 = Interrupt enabled.

Bit 3: Receive SLC-96 (RSLC96)

0 = Interrupt masked.
 1 = Interrupt enabled.

Bit 2: Receive FDL Register Full (RFDLF)

0 = Interrupt masked.
 1 = Interrupt enabled.

Bit 1: BOC Clear Event (BC)

0 = Interrupt masked.
 1 = Interrupt enabled.

Bit 0: BOC Detect Event (BD)

0 = Interrupt masked.
 1 = Interrupt enabled.

Register Name: **RIM7 (E1 Mode)**
 Register Description: **Receive Interrupt Mask Register 7 (BOC:FDL)**
 Register Address: **0A6h + (200h x (n - 1)) : where n = 1 to 8**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|---|---|---|---|---|-------|-------|
| Name | — | — | — | — | — | — | Sa6CD | SaXCD |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Note: See [RIM7](#) for T1 Mode.

Bit 1: Sa6 Codeword Detect (Sa6CD). This bit will enable the interrupt generated when a valid codeword (per ETS 300 233) is detected in the Sa6 bits.

0 = Interrupt masked.
 1 = Interrupt enabled.

Bit 0: SaX Change Detect (SaXCD). This bit will enable the interrupt generated when a change of state is detected in any of the unmasked SaX bit positions. The masked or unmasked SaX bits are selected by the [E1RSAIMR](#) register.

0 = Interrupt masked.
 1 = Interrupt enabled.

Register Name: **RSCSE1, RSCSE2, RSCSE3, RSCSE4**
 Register Description: **Receive-Signaling Change of State Enable Registers 1 to 4**
 Register Address: **0A8h, 0A9h, 0AAh, 0ABh + (200h x (n - 1)) : where n = 1 to 8**

| Bit # Name | (MSB) | | | | | | | (LSB) | |
|---------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|------------------------------|
| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
| | CH8 | CH7 | CH6 | CH5 | CH4 | CH3 | CH2 | CH1 | RSCSE1 |
| | CH16 | CH15 | CH14 | CH13 | CH12 | CH11 | CH10 | CH9 | RSCSE2 |
| | CH24 | CH23 | CH22 | CH21 | CH20 | CH19 | CH18 | CH17 | RSCSE3 |
| | <i>CH32</i> | <i>CH31</i> | <i>CH30</i> | <i>CH29</i> | <i>CH28</i> | <i>CH27</i> | <i>CH26</i> | <i>CH25</i> | RSCSE4 (E1 Mode Only) |

Setting any of the CH[1:32] bits in the RSCSE1 to RSCSE4 registers will cause RSCOS ([RLS4.3](#)) to be set when that channel's signaling data changes state.

Register Name: **T1RUPCD1 (T1 Mode Only)**
 Register Description: **Receive Up Code Definition Register 1**
 Register Address: **0ACh + (200h x (n - 1)) : where n = 1 to 8**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|----|----|----|----|----|----|----|----|
| Name | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Note: Writing this register resets the detector's integration period.

Bit 7: Receive Up Code Definition Bit 7 (C7). First bit of the repeating pattern.

Bit 6: Receive Up Code Definition Bit 6 (C6). A Don't Care if a 1-bit length is selected.

Bit 5: Receive Up Code Definition Bit 5 (C5). A Don't Care if a 1- or 2-bit length is selected.

Bit 4: Receive Up Code Definition Bit 4 (C4). A Don't Care if a 1- to 3-bit length is selected.

Bit 3: Receive Up Code Definition Bit 3 (C3). A Don't Care if a 1- to 4-bit length is selected.

Bit 2: Receive Up Code Definition Bit 2 (C2). A Don't Care if a 1- to 5-bit length is selected.

Bit 1: Receive Up Code Definition Bit 1 (C1). A Don't Care if a 1- to 6-bit length is selected.

Bit 0: Receive Up Code Definition Bit 0 (C0). A Don't Care if a 1- to 7-bit length is selected.

Register Name: **T1RUPCD2 (T1 Mode Only)**
 Register Description: **Receive Up Code Definition Register 2**
 Register Address: **0ADh + (200h x (n - 1)) : where n = 1 to 8**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|----|----|----|----|----|----|----|----|
| Name | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7: Receive Up Code Definition Bit 7 (C7). A Don't Care if a 1- to 7-bit length is selected.

Bit 6: Receive Up Code Definition Bit 6 (C6). A Don't Care if a 1- to 7-bit length is selected.

Bit 5: Receive Up Code Definition Bit 5 (C5). A Don't Care if a 1- to 7-bit length is selected.

Bit 4: Receive Up Code Definition Bit 4 (C4). A Don't Care if a 1- to 7-bit length is selected.

Bit 3: Receive Up Code Definition Bit 3 (C3). A Don't Care if a 1- to 7-bit length is selected.

Bit 2: Receive Up Code Definition Bit 2 (C2). A Don't Care if a 1- to 7-bit length is selected.

Bit 1: Receive Up Code Definition Bit 1 (C1). A Don't Care if a 1- to 7-bit length is selected.

Bit 0: Receive Up Code Definition Bit 0 (C0). A Don't Care if a 1- to 7-bit length is selected.

Register Name: **T1RDNCD1 (T1 Mode Only)**
 Register Description: **Receive Down Code Definition Register 1**
 Register Address: **0AEh + (200h x (n - 1)) : where n = 1 to 8**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|----|----|----|----|----|----|----|----|
| Name | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Note: Writing this register resets the detector's integration period.

Bit 7: Receive Down Code Definition Bit 7 (C7). First bit of the repeating pattern.

Bit 6: Receive Down Code Definition Bit 6 (C6). A Don't Care if a 1-bit length is selected.

Bit 5: Receive Down Code Definition Bit 5 (C5). A Don't Care if a 1- or 2-bit length is selected.

Bit 4: Receive Down Code Definition Bit 4 (C4). A Don't Care if a 1- to 3-bit length is selected.

Bit 3: Receive Down Code Definition Bit 3 (C3). A Don't Care if a 1- to 4-bit length is selected.

Bit 2: Receive Down Code Definition Bit 2 (C2). A Don't Care if a 1- to 5-bit length is selected.

Bit 1: Receive Down Code Definition Bit 1 (C1). A Don't Care if a 1- to 6-bit length is selected.

Bit 0: Receive Down Code Definition Bit 0 (C0). A Don't Care if a 1- to 7-bit length is selected.

Register Name: **T1RDNCD2 (T1 Mode Only)**
 Register Description: **Receive Down Code Definition Register 2**
 Register Address: **0AFh + (200h x (n - 1)) : where n = 1 to 8**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|----|----|----|----|----|----|----|----|
| Name | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7: Receive Down Code Definition Bit 7 (C7). A Don't Care if a 1- to 7-bit length is selected.

Bit 6: Receive Down Code Definition Bit 6 (C6). A Don't Care if a 1- to 7-bit length is selected.

Bit 5: Receive Down Code Definition Bit 5 (C5). A Don't Care if a 1- to 7-bit length is selected.

Bit 4: Receive Down Code Definition Bit 4 (C4). A Don't Care if a 1- to 7-bit length is selected.

Bit 3: Receive Down Code Definition Bit 3 (C3). A Don't Care if a 1- to 7-bit length is selected.

Bit 2: Receive Down Code Definition Bit 2 (C2). A Don't Care if a 1- to 7-bit length is selected.

Bit 1: Receive Down Code Definition Bit 1 (C1). A Don't Care if a 1- to 7-bit length is selected.

Bit 0: Receive Down Code Definition Bit 0 (C0). A Don't Care if a 1- to 7-bit length is selected.

Register Name: **RRTS1**
 Register Description: **Receive Real-Time Status Register 1**
 Register Address: **0B0h + (200h x (n - 1)) : where n = 1 to 8**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|---|---|---|------|------|------|------|
| Name | — | — | — | — | RRAI | RAIS | RLOS | RLOF |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Note: All bits in this register are real-time (not latched).

Bit 3: Receive Remote Alarm Indication Condition (RRAI). Set when a remote alarm is received at RRINGn and RTIPn.

Bit 2: Receive Alarm Indication Signal Condition (RAIS). Set when an unframed all-ones code is received at RRINGn and RTIPn.

Bit 1: Receive Loss of Signal Condition (RLOS). Set when 192 consecutive zeros have been detected at RRINGn and RTIPn.

Bit 0: Receive Loss of Frame Condition (RLOF). Set when the DS26518 is not synchronized to the received data stream.

Register Name: **RRTS3 (T1 Mode)**
 Register Description: **Receive Real-Time Status Register 3**
 Register Address: **0B2h + (200h x (n - 1)) : where n = 1 to 8**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|---|---|---|------|-----|-----|-----|
| Name | — | — | — | — | LORC | LSP | LDN | LUP |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Note: All bits in this register are real-time (not latched). See [RRTS3](#) for E1 Mode.

Bit 3: Loss of Receive Clock Condition (LORC). Set when the RCLKn pin has not transitioned for one channel time.

Bit 2: Spare Code Detected Condition (LSP). Set when the spare code as defined in the [T1RSCD1:T1RSCD2](#) registers is being received.

Bit 1: Loop-Down Code Detected Condition (LDN). Set when the loop-down code as defined in the [T1RDNC1:T1RDNC2](#) register is being received.

Bit 0: Loop-Up Code Detected Condition (LUP). Set when the loop-up code as defined in the [T1RUPC1:T1RUPC2](#) register is being received.

Register Name: **RRTS3 (E1 Mode)**
 Register Description: **Receive Real-Time Status Register 3**
 Register Address: **0B2h + (200h x (n - 1)) : where n = 1 to 8**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|---|---|---|------|---|--------|------|
| Name | — | — | — | — | LORC | — | V52LNK | RDMA |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Note: All bits in this register are real-time (not latched). See [RRTS3](#) for T1 Mode.

Bit 3: Loss of Receive Clock Condition (LORC). Set when the RCLKn pin has not transitioned for one channel time.

Bit 1: V5.2 Link Detected Condition (V52LNK). Set on detection of a V5.2 link identification signal (G.965).

Bit 0: Receive Distant MF Alarm Condition (RDMA). Set when bit 6 of time slot 16 in frame 0 has been set for two consecutive multiframes. This alarm is not disabled in the CCS signaling mode.

Register Name: **RRTS5**
 Register Description: **Receive Real-Time Status Register 5 (HDLC-64)**
 Register Address: **0B4h + (200h x (n - 1)) : where n = 1 to 8**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|-----|-----|-----|---|---|------|-----|
| Name | — | PS2 | PS1 | PS0 | — | — | RHWM | RNE |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Note: All bits in this register are real time.

Bits 6 to 4: Receive Packet Status (PS[2:0]). These are real-time bits indicating the status as of the last read of the receive FIFO.

| PS2 | PS1 | PS0 | PACKET STATUS |
|-----|-----|-----|---|
| 0 | 0 | 0 | In Progress: End of message has not yet been reached. |
| 0 | 0 | 1 | Packet OK: Packet ended with correct CRC codeword. |
| 0 | 1 | 0 | CRC Error: A closing flag was detected, preceded by a corrupt CRC codeword. |
| 0 | 1 | 1 | Abort: Packet ended because an abort signal was detected (7 or more ones in a row). |
| 1 | 0 | 0 | Overrun: HDLC-64 controller terminated reception of packet because receive FIFO is full. |

Bit 1: Receive FIFO Above High Watermark Condition (RHWM). Set when the receive 64-byte FIFO fills beyond the high watermark as defined by the Receive HDLC-64 FIFO Control Register ([RHFC](#)). This is a real-time bit.

Bit 0: Receive FIFO Not Empty Condition (RNE). Set when the receive 64-byte FIFO has at least one byte available for a read. This is a real-time bit.

Register Name: **RHPBA**
 Register Description: **Receive HDLC-64 Packet Bytes Available Register**
 Register Address: **0B5h + (200h x (n - 1)) : where n = 1 to 8**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|----|-------|-------|-------|-------|-------|-------|-------|
| Name | MS | RPBA6 | RPBA5 | RPBA4 | RPBA3 | RPBA2 | RPBA1 | RPBA0 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7: Message Status (MS)

0 = Bytes indicated by RPBA0 through RPBA6 are the end of a message. Host must check the HDLC-64 status register for details.

1 = Bytes indicated by RPBA0 through RPBA6 are the beginning or continuation of a message. The host does not need to check the HDLC-64 status. The MS bit returns to a value of 1 when the Rx HDLC-64 FIFO is empty.

Bits 6 to 0: Receive FIFO Packet Bytes Available Count (RPBA[6:0]). RPBA0 is the LSB.

Register Name: **RHF**
 Register Description: **Receive HDLC-64 FIFO Register**
 Register Address: **0B6h + (200h x (n - 1)) : where n = 1 to 8**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|------|------|------|------|------|------|------|------|
| Name | RHD7 | RHD6 | RHD5 | RHD4 | RHD3 | RHD2 | RHD1 | RHD0 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7: Receive HDLC-64 Data Bit 7 (RHD7). MSB of an HDLC packet data byte.

Bit 6: Receive HDLC-64 Data Bit 6 (RHD6)

Bit 5: Receive HDLC-64 Data Bit 5 (RHD5)

Bit 4: Receive HDLC-64 Data Bit 4 (RHD4)

Bit 3: Receive HDLC-64 Data Bit 3 (RHD3)

Bit 2: Receive HDLC-64 Data Bit 2 (RHD2)

Bit 1: Receive HDLC-64 Data Bit 1 (RHD1)

Bit 0: Receive HDLC-64 Data Bit 0 (RHD0). LSB of an HDLC-64 packet data byte.

Register Name: **RBCS1, RBCS2, RBCS3, RBCS4**
 Register Description: **Receive Blank Channel Select Registers 1 to 4**
 Register Address: **0C0h, 0C1h, 0C2h, 0C3h + (200h x (n - 1)) : where n = 1 to 8**

| Bit # | (MSB) | | | | | | | (LSB) | |
|-------|-------|------|------|------|------|------|------|-------|-----------------------------|
| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
| Name | CH8 | CH7 | CH6 | CH5 | CH4 | CH3 | CH2 | CH1 | RBCS1 |
| | CH16 | CH15 | CH14 | CH13 | CH12 | CH11 | CH10 | CH9 | RBCS2 |
| | CH24 | CH23 | CH22 | CH21 | CH20 | CH19 | CH18 | CH17 | RBCS3 |
| | CH32 | CH31 | CH30 | CH29 | CH28 | CH27 | CH26 | CH25 | RBCS4 (E1 Mode Only) |

Bits 7 to 0: Receive Blank Channel Select for Channels 1 to 32 (CH[1:32])

0 = Do not blank this channel (channel data is available on RSERn).

1 = Data on RSERn is forced to all ones for this channel.

Note that when two or more sequential channels are chosen to be blanked, the receive-slip zone select bit should be set to zero. If the blank channels are distributed (such as 1, 5, 9, 13, 17, 21, 25, 29), then the RSZS bit can be set to one, which may provide a lower occurrence of slips in certain applications.

Register Name: **RCBR1, RCBR2, RCBR3, RCBR4**
 Register Description: **Receive Channel Blocking Registers 1 to 4**
 Register Address: **0C4h, 0C5h, 0C6h, 0C7h + (200h x (n - 1)) : where n = 1 to 8**

| Bit # | (MSB) | | | | | | | (LSB) | |
|-------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|---------------------|------------------------------|
| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
| Name | CH8 | CH7 | CH6 | CH5 | CH4 | CH3 | CH2 | CH1 | RCBR1 |
| | CH16 | CH15 | CH14 | CH13 | CH12 | CH11 | CH10 | CH9 | RCBR2 |
| | CH24 | CH23 | CH22 | CH21 | CH20 | CH19 | CH18 | CH17 | RCBR3 |
| | <i>CH32</i> | <i>CH31</i> | <i>CH30</i> | <i>CH29</i> | <i>CH28</i> | <i>CH27</i> | <i>CH26</i> | <i>CH25 (F-bit)</i> | RCBR4 (E1 Mode Only)* |

Bits 7 to 0: Channel Blocking Control Bits for Receive Channels 1 to 32 (CH[1:32])

0 = Force the RCHBLK_n pin to remain low during this channel time.

1 = Force the RCHBLK_n pin high during this channel time.

***Note that RCBR4 has two functions:**

When 2.048MHz backplane mode is selected, this register allows the user to enable the channel blocking signal for any of the 32 possible backplane channels.

When 1.544MHz backplane mode is selected, the LSB of this register determines whether or not the RCHBLK_n signal will pulse high during the F-bit time. In this mode RCBR4.1 to RCBR4.7 should be set to 0.

RCBR4.0 = 0, do not pulse RCHBLK_n during the F-bit.

RCBR4.0 = 1, pulse RCHBLK_n during the F-bit.

Register Name: **RSI1, RSI2, RSI3, RSI4**
 Register Description: **Receive-Signaling Reinsertion Enable Registers 1 to 4**
 Register Address: **0C8h, 0C9h, 0CAh, 0CBh + (200h x (n - 1)) : where n = 1 to 8**

| Bit # | (MSB) | | | | | | | (LSB) | |
|-------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|----------------------------|
| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
| Name | CH8 | CH7 | CH6 | CH5 | CH4 | CH3 | CH2 | CH1 | RSI1 |
| | CH16 | CH15 | CH14 | CH13 | CH12 | CH11 | CH10 | CH9 | RSI2 |
| | CH24 | CH23 | CH22 | CH21 | CH20 | CH19 | CH18 | CH17 | RSI3 |
| | <i>CH32</i> | <i>CH31</i> | <i>CH30</i> | <i>CH29</i> | <i>CH28</i> | <i>CH27</i> | <i>CH26</i> | <i>CH25</i> | RSI4 (E1 Mode Only) |

Setting any of the CH[1:24] bits in the RSI1 through RSI4 registers will cause signaling data to be reinserted for the associated channel. RSI4 is used for 2.048MHz backplane operation.

Register Name: **RGCCS1, RGCCS2, RGCCS3, RGCCS4**
 Register Description: **Receive Gapped Clock Channel Select Registers 1 to 4**
 Register Address: **0CCh, 0CDh, 0CEh, 0CFh + (200h x (n - 1)) : where n = 1 to 8**

| Bit # | (MSB) | | | | | | | (LSB) | |
|-------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|---------------------|-------------------------------|
| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
| Name | CH8 | CH7 | CH6 | CH5 | CH4 | CH3 | CH2 | CH1 | RGCCS1 |
| | CH16 | CH15 | CH14 | CH13 | CH12 | CH11 | CH10 | CH9 | RGCCS2 |
| | CH24 | CH23 | CH22 | CH21 | CH20 | CH19 | CH18 | CH17 | RGCCS3 |
| | <i>CH32</i> | <i>CH31</i> | <i>CH30</i> | <i>CH29</i> | <i>CH28</i> | <i>CH27</i> | <i>CH26</i> | <i>CH25 (F-bit)</i> | RGCCS4 (E1 Mode Only)* |

Bits 7 to 0: Gapped Clock Channel Select Bits for Receive Channels 1 to 32(CH[1:32])

0 = No clock is present on RCHCLKn during this channel time.

1 = Force a clock on RCHCLKn during this channel time. The clock will be synchronous with RCLKn if the elastic store is disabled, and synchronous with RSYCLKn if the elastic store is enabled.

*** Note that RGCCS4 has two functions:**

When 2.048MHz backplane mode is selected, this register allows the user to enable the gapped clock on RCHCLKn for any of the 32 possible backplane channels.

When 1.544MHz backplane mode is selected, the LSB of this register determines whether or not a clock is generated on RCHCLKn during the F-bit time:

RGCCS4.0 = 0, do not generate a clock during the F-bit.

RGCCS4.0 = 1, generate a clock during the F-bit.

In this mode RGCCS4.1 to RGCCS4.7 should be set to 0.

Register Name: **RCICE1, RCICE2, RCICE3, RCICE4**
 Register Description: **Receive Channel Idle Code Enable Registers 1 to 4**
 Register Address: **0D0h, 0D1h, 0D2h, 0D3h + (200h x (n - 1)) : where n = 1 to 8**

| Bit # | (MSB) | | | | | | | (LSB) | |
|-------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|------------------------------|
| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
| Name | CH8 | CH7 | CH6 | CH5 | CH4 | CH3 | CH2 | CH1 | RCICE1 |
| | CH16 | CH15 | CH14 | CH13 | CH12 | CH11 | CH10 | CH9 | RCICE2 |
| | CH24 | CH23 | CH22 | CH21 | CH20 | CH19 | CH18 | CH17 | RCICE3 |
| | <i>CH32</i> | <i>CH31</i> | <i>CH30</i> | <i>CH29</i> | <i>CH28</i> | <i>CH27</i> | <i>CH26</i> | <i>CH25</i> | RCICE4 (E1 Mode Only) |

Bits 7 to 0: Receive Channels 1 to 32 Code Insertion Control Bits (CH[1:32])

0 = Do not insert data from the Idle Code Array into the receive data stream.

1 = Insert data from the Idle Code Array into the receive data stream.

Register Name: **RBPCS1, RBPCS2, RBPCS3, RBPCS4**
 Register Description: **Receive BERT Port Channel Select Registers 1 to 4**
 Register Address: **0D4h, 0D5h, 0D6h, 0D7h + (200h x (n - 1)) : where n = 1 to 8**

| Bit # Name | (MSB) | | | | (LSB) | | | | |
|---------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|------------------------------|
| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
| | CH8 | CH7 | CH6 | CH5 | CH4 | CH3 | CH2 | CH1 | RBPCS1 |
| | CH16 | CH15 | CH14 | CH13 | CH12 | CH11 | CH10 | CH9 | RBPCS2 |
| | CH24 | CH23 | CH22 | CH21 | CH20 | CH19 | CH18 | CH17 | RBPCS3 |
| | <i>CH32</i> | <i>CH31</i> | <i>CH30</i> | <i>CH29</i> | <i>CH28</i> | <i>CH27</i> | <i>CH26</i> | <i>CH25</i> | RBPCS4 (E1 Mode Only) |

Bits 7 to 0: BERT Port Channel Select Receive Channels 1 to 32 (CH[1:32])

0 = Do not enable the receive BERT clock for the associated channel time, or map the selected channel data out of the receive BERT port.

1 = Enable receive BERT clock for the associated channel time, and allow mapping of the selected channel data out of the receive BERT port. Multiple or all channels may be selected simultaneously.

Register Name: **RHCS1, RHCS2, RHCS3, RHCS4**
 Register Description: **Receive HDLC-256 Channel Select Registers 1 to 4**
 Register Address: **0DCh, 0DDh, 0DEh, 0DFh + (200h x (n - 1)) : where n = 1 to 8**

| Bit # Name | (MSB) | | | | (LSB) | | | | |
|---------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-----------------------------|
| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
| | CH8 | CH7 | CH6 | CH5 | CH4 | CH3 | CH2 | CH1 | RHCS1 |
| | CH16 | CH15 | CH14 | CH13 | CH12 | CH11 | CH10 | CH9 | RHCS2 |
| | CH24 | CH23 | CH22 | CH21 | CH20 | CH19 | CH18 | CH17 | RHCS3 |
| | <i>CH32</i> | <i>CH31</i> | <i>CH30</i> | <i>CH29</i> | <i>CH28</i> | <i>CH27</i> | <i>CH26</i> | <i>CH25</i> | RHCS4 (E1 Mode Only) |

Setting any of the CH[1:32] bits in the RHCS1 to RHCS4 registers enables the receive HDLC-256 clock for the associated channel time, and allows mapping of the selected channel data into the HDLC-256 port. Multiple or all channels may be selected simultaneously.

10.4.2 Transmit Register Descriptions

Register Name: **THC1**
 Register Description: **Transmit HDLC-64 Control Register 1**
 Register Address: **110h + (200h x (n - 1)) : where n = 1 to 8**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|------|-------|-----|------|-----|------|------|-------|
| Name | NOFS | TEOML | THR | THMS | TFS | TEOM | TZSD | TCRCD |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7: Number of Flags Select (NOFS)

- 0 = Send one flag between consecutive messages.
- 1 = Send two flags between consecutive messages.

Bit 6: Transmit End of Message and Loop (TEOML). To loop on a message, should be set to a one just before the last data byte of an HDLC-64 packet is written into the transmit FIFO. The message will repeat until the user clears this bit or a new message is written to the transmit FIFO. If the host clears the bit, the looping message will complete then flags will be transmitted until new message is written to the FIFO. If the host terminates the loop by writing a new message to the FIFO the loop will terminate, one or two flags will be transmitted and the new message will start. If not disabled via TCRCD, the transmitter will automatically append a two-byte CRC code to the end of all messages.

Bit 5: Transmit HDLC-64 Reset (THR). Will reset the transmit HDLC-64 controller and flush the transmit FIFO. An abort followed by 7Eh or FFh flags/idle will be transmitted until a new packet is initiated by writing new data into the FIFO. This is an acknowledged reset, that is, the host need only to set the bit and the DS26518 will clear it once the reset operation is complete. Total time for the reset is less than 250µs.

- 0 = Normal operation.
- 1 = Reset transmit HDLC-64 controller and flush the transmit FIFO.

Bit 4: Transmit HDLC-64 Mapping Select (THMS)

- 0 = Transmit HDLC-64 assigned to channels.
- 1 = Transmit HDLC-64 assigned to FDL (T1 mode), Sa bits (E1 mode). This mode must be enabled with [T1.TCR2.7](#).

Bit 3: Transmit Flag/Idle Select (TFS). This bit selects the intermessage fill character after the closing and before the opening flags (7Eh).

- 0 = 7Eh
- 1 = FFh

Bit 2: Transmit End of Message (TEOM). Should be set to a one just before the last data byte of an HDLC-64 packet is written into the transmit FIFO at THF. If not disabled via TCRCD, the transmitter will automatically append a two-byte CRC code to the end of the message.

Bit 1: Transmit Zero Stuffer Defeat (TZSD). The zero stuffer function automatically inserts a zero in the message field (between the flags) after five consecutive ones to prevent the emulation of a flag or abort sequence by the data pattern. The receiver automatically removes (destuffs) any zero after five ones in the message field.

- 0 = Enable the zero stuffer (normal operation).
- 1 = Disable the zero stuffer.

Bit 0: Transmit CRC Defeat (TCRCD). A two-byte CRC code is automatically appended to the outbound message. This bit can be used to disable the CRC function.

- 0 = Enable CRC generation (normal operation).
- 1 = Disable CRC generation.

Register Name: **THBSE**
 Register Description: **Transmit HDLC-64 Bit Suppress**
 Register Address: **111h + (200h x (n - 1)) : where n = 1 to 8**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|-------|-------|-------|-------|-------|-------|-------|-------|
| Name | TBSE8 | TBSE7 | TBSE6 | TBSE5 | TBSE4 | TBSE3 | TBSE2 | TBSE1 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7: Transmit Bit 8 Suppress (TBSE8). MSB of the channel. Set to one to stop this bit from being used.

Bit 6: Transmit Bit 7 Suppress (TBSE7). Set to one to stop this bit from being used.

Bit 5: Transmit Bit 6 Suppress (TBSE6). Set to one to stop this bit from being used.

Bit 4: Transmit Bit 5 Suppress (TBSE5). Set to one to stop this bit from being used.

Bit 3: Transmit Bit 4 Suppress (TBSE4). Set to one to stop this bit from being used.

Bit 2: Transmit Bit 3 Suppress (TBSE3). Set to one to stop this bit from being used.

Bit 1: Transmit Bit 2 Suppress (TBSE2). Set to one to stop this bit from being used.

Bit 0: Transmit Bit 1 Suppress (TBSE1). LSB of the channel. Set to one to stop this bit from being used.

Register Name: **THC2**
 Register Description: **Transmit HDLC-64 Control Register 2**
 Register Address: **113h + (200h x (n - 1)) : where n = 1 to 8**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|------|------|-------|-------|-------|-------|-------|-------|
| Name | TABT | SBOC | THCEN | THCS4 | THCS3 | THCS2 | THCS1 | THCS0 |
| Default | TABT | — | THCEN | THCS4 | THCS3 | THCS2 | THCS1 | THCS0 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7: Transmit Abort (TABT). A 0-to-1 transition will cause the FIFO contents to be dumped and one FEh abort to be sent followed by 7Eh or FFh flags/idle until a new packet is initiated by writing new data into the FIFO. Must be cleared and set again for a subsequent abort to be sent.

Bit 6: Send BOC (SBOC) (T1 Mode Only). Set = 1 to transmit the BOC code placed in bits 0 to 5 of the [T1TBOC](#) register.

Bit 5: Transmit HDLC-64 Controller Enable (THCEN)
 0 = Transmit HDLC-64 controller is not enabled.
 1 = Transmit HDLC-64 controller is enabled.

Bits 4 to 0: Transmit HDLC-64 Channel Select (THCS[4:0]). Determines which DSO channel will carry the HDLC-64 message if enabled. Changes to this value are acknowledged only upon a transmit HDLC-64 controller reset (THR at [THC1.5](#)).

Register Name: **E1TSACR**
 Register Description: **E1 Transmit Sa-Bit Control Register**
 Register Address: **114h + (200h x (n - 1)) : where n = 1 to 8, for Ports 1 to 8**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|------|-------|----|-----|-----|-----|-----|-----|
| Name | SiAF | SiNAF | RA | Sa4 | Sa5 | Sa6 | Sa7 | Sa8 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7: International Bit in Align Frame Insertion Control Bit (SiAF)

0 = Do not insert data from the [E1TSiAF](#) register into the transmit data stream.
 1 = Insert data from the [E1TSiAF](#) register into the transmit data stream.

Bit 6: International Bit in Non-Align Frame Insertion Control Bit (SiNAF)

0 = Do not insert data from the [E1TSiNAF](#) register into the transmit data stream.
 1 = Insert data from the [E1TSiNAF](#) register into the transmit data stream.

Bit 5: Remote Alarm Insertion Control Bit (RA)

0 = Do not insert data from the [E1TRA](#) register into the transmit data stream.
 1 = Insert data from the [E1TRA](#) register into the transmit data stream.

Bit 4: Additional Bit 4 Insertion Control Bit (Sa4)

0 = Do not insert data from the [E1TSa4](#) register into the transmit data stream.
 1 = Insert data from the [E1TSa4](#) register into the transmit data stream.

Bit 3: Additional Bit 5 Insertion Control Bit (Sa5)

0 = Do not insert data from the [E1TSa5](#) register into the transmit data stream.
 1 = Insert data from the [E1TSa5](#) register into the transmit data stream.

Bit 2: Additional Bit 6 Insertion Control Bit (Sa6)

0 = Do not insert data from the [E1TSa6](#) register into the transmit data stream.
 1 = Insert data from the [E1TSa6](#) register into the transmit data stream.

Bit 1: Additional Bit 7 Insertion Control Bit (Sa7)

0 = Do not insert data from the [E1TSa7](#) register into the transmit data stream.
 1 = Insert data from the [E1TSa7](#) register into the transmit data stream.

Bit 0: Additional Bit 8 Insertion Control Bit (Sa8)

0 = Do not insert data from the [E1TSa8](#) register into the transmit data stream.
 1 = Insert data from the [E1TSa8](#) register into the transmit data stream.

Register Name: **SSIE1, SSIE2, SSIE3, SSIE4**
 Register Description: **Software-Signaling Insertion Enable Registers 1 to 4**
 Register Address: **118h, 119h, 11Ah, 11Bh + (200h x (n - 1)) : where n = 1 to 8**

| Bit # Name | (MSB) | | | | (LSB) | | | | |
|---------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-----------------------------|
| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
| | CH8 | CH7 | CH6 | CH5 | CH4 | CH3 | CH2 | CH1 | SSIE1 |
| | CH16 | CH15 | CH14 | CH13 | CH12 | CH11 | CH10 | CH9 | SSIE2 |
| | CH24 | CH23 | CH22 | CH21 | CH20 | CH19 | CH18 | CH17 | SSIE3 |
| | <i>CH32</i> | <i>CH31</i> | <i>CH30</i> | <i>CH29</i> | <i>CH28</i> | <i>CH27</i> | <i>CH26</i> | <i>CH25</i> | SSIE4 (E1 Mode Only) |

Bits 7 to 0: Software-Signaling Insertion Enable for Channels 1 to 32 (CH[1:32]). These bits determine which channels are to have signaling inserted from the Transmit Signaling registers.

0 = Do not source signaling data from the TS registers for this channel.

1 = Source signaling data from the TS registers for this channel.

Register Name: **TIDR1 to TIDR32**
 Register Description: **Transmit Idle Code Definition Registers 1 to 32**
 Register Address: **120h to 13Fh + (200h x (n - 1)) : where n = 1 to 8**

| Bit # Name | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------------|----|----|----|----|----|----|----|----|
| | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 7 to 0: Per-Channel Idle Code Bits (C[7:0]). C0 is the LSB of the code (this bit is transmitted last). Address 120h is for channel 1, address 13Fh is for channel 32. TIDR25:TIDR32 are E1 mode.

Register Name: **TS1 to TS16**
 Register Description: **Transmit-Signaling Registers**
 Register Address: **140h to 14Fh + (200h x (n - 1)) : where n = 1 to 8**

T1 Mode:

| Bit # Name | (MSB) | | | | (LSB) | | | | |
|---------------|--------|--------|--------|--------|--------|--------|--------|-------------|--|
| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
| CH1-A | CH1-B | CH1-C | CH1-D | CH13-A | CH13-B | CH13-C | CH13-D | TS1 | |
| CH2-A | CH2-B | CH2-C | CH2-D | CH14-A | CH14-B | CH14-C | CH14-D | TS2 | |
| CH3-A | CH3-B | CH3-C | CH3-D | CH15-A | CH15-B | CH15-C | CH15-D | TS3 | |
| CH4-A | CH4-B | CH4-C | CH4-D | CH16-A | CH16-B | CH16-C | CH16-D | TS4 | |
| CH5-A | CH5-B | CH5-C | CH5-D | CH17-A | CH17-B | CH17-C | CH17-D | TS5 | |
| CH6-A | CH6-B | CH6-C | CH6-D | CH18-A | CH18-B | CH18-C | CH18-D | TS6 | |
| CH7-A | CH7-B | CH7-C | CH7-D | CH19-A | CH19-B | CH19-C | CH19-D | TS7 | |
| CH8-A | CH8-B | CH8-C | CH8-D | CH20-A | CH20-B | CH20-C | CH20-D | TS8 | |
| CH9-A | CH9-B | CH9-C | CH9-D | CH21-A | CH21-B | CH21-C | CH21-D | TS9 | |
| CH10-A | CH10-B | CH10-C | CH10-D | CH22-A | CH22-B | CH22-C | CH22-D | TS10 | |
| CH11-A | CH11-B | CH11-C | CH11-D | CH23-A | CH23-B | CH23-C | CH23-D | TS11 | |
| CH12-A | CH12-B | CH12-C | CH12-D | CH24-A | CH24-B | CH24-C | CH24-D | TS12 | |

Note: In D4 framing mode, the C and D bits are not used.

E1 Mode:

| Bit # Name | (MSB) | | | | (LSB) | | | | |
|---------------|--------|--------|--------|--------|--------|--------|--------|-------------|------------|
| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
| | 0 | 0 | 0 | 0 | X | Y | X | X | TS1 |
| CH1-A | CH1-B | CH1-C | CH1-D | CH16-A | CH16-B | CH16-C | CH16-D | TS2 | |
| CH2-A | CH2-B | CH2-C | CH2-D | CH17-A | CH17-B | CH17-C | CH17-D | TS3 | |
| CH3-A | CH3-B | CH3-C | CH3-D | CH18-A | CH18-B | CH18-C | CH18-D | TS4 | |
| CH4-A | CH4-B | CH4-C | CH4-D | CH19-A | CH19-B | CH19-C | CH19-D | TS5 | |
| CH5-A | CH5-B | CH5-C | CH5-D | CH20-A | CH20-B | CH20-C | CH20-D | TS6 | |
| CH6-A | CH6-B | CH6-C | CH6-D | CH21-A | CH21-B | CH21-C | CH21-D | TS7 | |
| CH7-A | CH7-B | CH7-C | CH7-D | CH22-A | CH22-B | CH22-C | CH22-D | TS8 | |
| CH8-A | CH8-B | CH8-C | CH8-D | CH23-A | CH23-B | CH23-C | CH23-D | TS9 | |
| CH9-A | CH9-B | CH9-C | CH9-D | CH24-A | CH24-B | CH24-C | CH24-D | TS10 | |
| CH10-A | CH10-B | CH10-C | CH10-D | CH25-A | CH25-B | CH25-C | CH25-D | TS11 | |
| CH11-A | CH11-B | CH11-C | CH11-D | CH26-A | CH26-B | CH26-C | CH26-D | TS12 | |
| CH12-A | CH12-B | CH12-C | CH12-D | CH27-A | CH27-B | CH27-C | CH27-D | TS13 | |
| CH13-A | CH13-B | CH13-C | CH13-D | CH28-A | CH28-B | CH28-C | CH28-D | TS14 | |
| CH14-A | CH14-B | CH14-C | CH14-D | CH29-A | CH29-B | CH29-C | CH29-D | TS15 | |
| CH15-A | CH15-B | CH15-C | CH15-D | CH30-A | CH30-B | CH30-C | CH30-D | TS16 | |

Register Name: **TCICE1, TCICE2, TCICE3, TCICE4**
 Register Description: **Transmit Channel Idle Code Enable Registers 1 to 4**
 Register Address: **150h, 151h, 152h, 153h + (200h x (n - 1)) : where n = 1 to 8**

| Bit # | (MSB) | | | | | | | (LSB) | |
|-------|-------|------|------|------|------|------|------|-------|------------------------------|
| Name | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
| | CH8 | CH7 | CH6 | CH5 | CH4 | CH3 | CH2 | CH1 | TCICE1 |
| | CH16 | CH15 | CH14 | CH13 | CH12 | CH11 | CH10 | CH9 | TCICE2 |
| | CH24 | CH23 | CH22 | CH21 | CH20 | CH19 | CH18 | CH17 | TCICE3 |
| | CH32 | CH31 | CH30 | CH29 | CH28 | CH27 | CH26 | CH25 | TCICE4 (E1 Mode Only) |

The Transmit Channel Idle Code Enable Registers (TCICE1–4) are used to determine which of the 24 T1 channels (or 32 E1 channels) from the backplane should be overwritten with the code placed in the Transmit Idle Code Definition Register ([TIDR1–32](#)).

Bits 7 to 0: Transmit Channels 1 to 32 Code Insertion Control Bits (CH[1:32])

- 0 = Do not insert data from the Idle Code Array into the transmit data stream.
- 1 = Insert data from the Idle Code Array into the transmit data stream.

Register Name: **TJBE1, TJBE2, TJBE3, TJBE4**
 Register Description: **Transmit Jammed Bit Eight Stuffing Registers 1 to 4**
 Register Address: **104h, 105h, 106h, 107h + (200h x (n - 1)) : where n = 1 to 8**

| Bit # | (MSB) | | | | | | | (LSB) | |
|-------|-------|------|------|------|------|------|------|-------|--------------|
| Name | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
| | CH8 | CH7 | CH6 | CH5 | CH4 | CH3 | CH2 | CH1 | TJBE1 |
| | CH16 | CH15 | CH14 | CH13 | CH12 | CH11 | CH10 | CH9 | TJBE2 |
| | CH24 | CH23 | CH22 | CH21 | CH20 | CH19 | CH18 | CH17 | TJBE3 |
| | CH32 | CH31 | CH30 | CH29 | CH28 | CH27 | CH26 | CH25 | TJBE4 |

The Transmit Jammed Bit Eight Stuffing Registers (TJBE1–4) select which of the 24 T1 channels (or 32 E1 Channels) to insert jammed bit eight stuffing. These registers are enabled by [TCR4.TJBEN](#).

Bits 7 to 0: Transmit Channels 1 to 32 Jammed Bit Eight Stuffing Control Bits (CH[1:32])

- 0 = Do not affect data in this channel.
- 1 = Replace the channel with TJBES if the channel is all zeros.

Register Name: **TDDS1, TDDS2, TDDS3**
 Register Description: **Transmit DDS Zero Code Registers 1 to 3**
 Register Address: **108h, 109h, 10Ah + (200h x (n - 1)) : where n = 1 to 8**

| (MSB) | | | | | | | (LSB) | |
|-------|------|------|------|------|------|------|-------|--------------|
| CH8 | CH7 | CH6 | CH5 | CH4 | CH3 | CH2 | CH1 | TDDS1 |
| CH16 | CH15 | CH14 | CH13 | CH12 | CH11 | CH10 | CH9 | TDDS2 |
| CH24 | CH23 | CH22 | CH21 | CH20 | CH19 | CH18 | CH17 | TDDS3 |

The Transmit DDS Zero Code Registers (TDDS1–3) select which of the 24 T1 channels to insert DDS zero code stuffing. These registers are enabled by [T1.TCR2.TDDSEN](#).

Bits 7 to 0: Transmit Channels 1 to 24 DDS Zero Code Control Bits (CH[1:32])

- 0 = Do not affect data in this channel.
- 1 = Replace the channel with DDS Zero Code stuffing if the channel is all zeros.

Register Name: **T1TFDL**
 Register Description: **Transmit FDL Register**
 Register Address: **162h + (200h x (n - 1)) : where n = 1 to 8**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|-------|-------|-------|-------|-------|-------|-------|-------|
| Name | TFDL7 | TFDL6 | TFDL5 | TFDL4 | TFDL3 | TFDL2 | TFDL1 | TFDL0 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Note: Also used to insert *Fs* framing pattern in D4 framing mode.

The Transmit FDL Register (T1TFDL) contains the Facility Data Link (FDL) information that is to be inserted on a byte basis into the outgoing T1 data stream. The LSB is transmitted first. In D4 mode, only the lower six bits are used.

Bit 7: Transmit FDL Bit 7 (TFDL7). MSB of the Transmit FDL Code.

Bit 6: Transmit FDL Bit 6 (TFDL6)

Bit 5: Transmit FDL Bit 5 (TFDL5)

Bit 4: Transmit FDL Bit 4 (TFDL4)

Bit 3: Transmit FDL Bit 3 (TFDL3)

Bit 2: Transmit FDL Bit 2 (TFDL2)

Bit 1: Transmit FDL Bit 1 (TFDL1)

Bit 0: Transmit FDL Bit 0 (TFDL0). LSB of the Transmit FDL Code.

Register Name: **T1TBOC**
 Register Description: **Transmit BOC Register**
 Register Address: **163h + (200h x (n - 1)) : where n = 1 to 8**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|---|-------|-------|-------|-------|-------|-------|
| Name | — | — | TBOC5 | TBOC4 | TBOC3 | TBOC2 | TBOC1 | TBOC0 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 5: Transmit BOC Bit 5 (TBOC5). MSB of the transmit BOC code.

Bit 4: Transmit BOC Bit 4 (TBOC4)

Bit 3: Transmit BOC Bit 3 (TBOC3)

Bit 2: Transmit BOC Bit 2 (TBOC2)

Bit 1: Transmit BOC Bit 1 (TBOC1)

Bit 0: Transmit BOC Bit 0 (TBOC0). LSB of the transmit BOC code.

Register Name: **T1TSLC1, T1TSLC2, T1TSLC3 (T1 Mode)**
 Register Description: **Transmit SLC-96 Data Link Registers 1 to 3**
 Register Address: **164h, 165h, 166h + (200h x (n - 1)) : where n = 1 to 8**

| Bit # | (MSB) | | | | (LSB) | | | | |
|-------|-------|----|-----|-----|-------|-----|-----|----|----------------|
| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
| Name | C8 | C7 | C6 | C5 | C4 | C3 | C2 | C1 | T1TSLC1 |
| | M2 | M1 | S=0 | S=1 | S=0 | C11 | C10 | C9 | T1TSLC2 |
| | S=1 | S4 | S3 | S2 | S1 | A2 | A1 | M3 | T1TSLC3 |

Note: See [E1TAF](#), [E1TNAF](#), and [E1TSIAF](#) for E1 Mode.

Register Name: **E1TAF (E1 Mode)**
 Register Description: **Transmit Align Frame Register**
 Register Address: **164h + (200h x (n - 1)) : where n = 1 to 8**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|----|---|---|---|---|---|---|---|
| Name | Si | 0 | 0 | 1 | 1 | 0 | 1 | 1 |
| Default | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 |

Bit 7: International Bit (Si)

Bit 6: Frame Alignment Signal Bit (0)

Bit 5: Frame Alignment Signal Bit (0)

Bit 4: Frame Alignment Signal Bit (1)

Bit 3: Frame Alignment Signal Bit (1)

Bit 2: Frame Alignment Signal Bit (0)

Bit 1: Frame Alignment Signal Bit (1)

Bit 0: Frame Alignment Signal Bit (1)

Register Name: **E1TNAF (E1 Mode)**
 Register Description: **Transmit Non-Align Frame Register**
 Register Address: **165h + (200h x (n - 1)) : where n = 1 to 8**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|----|---|---|-----|-----|-----|-----|-----|
| Name | Si | 1 | A | Sa4 | Sa5 | Sa6 | Sa7 | Sa8 |
| Default | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7: International Bit (Si)

Bit 6: Frame Non-Alignment Signal Bit (1)

Bit 5: Remote Alarm (Used to Transmit the Alarm) (A)

Bit 4: Additional Bit 4 (Sa4)

Bit 3: Additional Bit 5 (Sa5)

Bit 2: Additional Bit 6 (Sa6)

Bit 1: Additional Bit 7 (Sa7)

Bit 0: Additional Bit 8 (Sa8)

Register Name: **E1TSiAF (E1 Mode)**
 Register Description: **Transmit Si Bits of the Align Frame Register**
 Register Address: **166h + (200h x (n - 1)) : where n = 1 to 8**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|--------|--------|--------|-------|-------|-------|-------|-------|
| Name | TSiF14 | TSiF12 | TSiF10 | TSiF8 | TSiF6 | TSiF4 | TSiF2 | TSiF0 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7: Si Bit of Frame 14 (TSiF14)

Bit 6: Si Bit of Frame 12 (TSiF12)

Bit 5: Si Bit of Frame 10 (TSiF10)

Bit 4: Si Bit of Frame 8 (TSiF8)

Bit 3: Si Bit of Frame 6 (TSiF6)

Bit 2: Si Bit of Frame 4 (TSiF4)

Bit 1: Si Bit of Frame 2 (TSiF2)

Bit 0: Si Bit of Frame 0 (TSiF0)

Register Name: **E1TSiNAF (E1 Mode Only)**
 Register Description: **Transmit Si Bits of the Non-Align Frame Register**
 Register Address: **167h + (200h x (n - 1)) : where n = 1 to 8**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|--------|--------|--------|-------|-------|-------|-------|-------|
| Name | TSiF15 | TSiF13 | TSiF11 | TSiF9 | TSiF7 | TSiF5 | TSiF3 | TSiF1 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7: Si Bit of Frame 15 (TSiF15)

Bit 6: Si Bit of Frame 13 (TSiF13)

Bit 5: Si Bit of Frame 11 (TSiF11)

Bit 4: Si Bit of Frame 9 (TSiF9)

Bit 3: Si Bit of Frame 7 (TSiF7)

Bit 2: Si Bit of Frame 5 (TSiF5)

Bit 1: Si Bit of Frame 3 (TSiF3)

Bit 0: Si Bit of Frame 1 (TSiF1)

Register Name: **E1TRA (E1 Mode Only)**
 Register Description: **Transmit Remote Alarm Register**
 Register Address: **168h + (200h x (n - 1)) : where n = 1 to 8**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|--------|--------|--------|-------|-------|-------|-------|-------|
| Name | TRAF15 | TRAF13 | TRAF11 | TRAF9 | TRAF7 | TRAF5 | TRAF3 | TRAF1 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7: Remote Alarm Bit of Frame 15 (TRAF15)

Bit 6: Remote Alarm Bit of Frame 13 (TRAF13)

Bit 5: Remote Alarm Bit of Frame 11 (TRAF11)

Bit 4: Remote Alarm Bit of Frame 9 (TRAF9)

Bit 3: Remote Alarm Bit of Frame 7 (TRAF7)

Bit 2: Remote Alarm Bit of Frame 5 (TRAF5)

Bit 1: Remote Alarm Bit of Frame 3 (TRAF3)

Bit 0: Remote Alarm Bit of Frame 1 (TRAF1)

Register Name: **E1TSa4 (E1 Mode Only)**
 Register Description: **Transmit Sa4 Bits Register**
 Register Address: **169h + (200h x (n - 1)) : where n = 1 to 8**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---------|---------|---------|--------|--------|--------|--------|--------|
| Name | TSa4F15 | TSa4F13 | TSa4F11 | TSa4F9 | TSa4F7 | TSa4F5 | TSa4F3 | TSa4F1 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7: Sa4 Bit of Frame 15 (TSa4F15)

Bit 6: Sa4 Bit of Frame 13 (TSa4F13)

Bit 5: Sa4 Bit of Frame 11 (TSa4F11)

Bit 4: Sa4 Bit of Frame 9 (TSa4F9)

Bit 3: Sa4 Bit of Frame 7 (TSa4F7)

Bit 2: Sa4 Bit of Frame 5 (TSa4F5)

Bit 1: Sa4 Bit of Frame 3 (TSa4F3)

Bit 0: Sa4 Bit of Frame 1 (TSa4F1)

Register Name: **E1TSa5 (E1 Mode Only)**
 Register Description: **Transmit Sa5 Bits Register**
 Register Address: **16Ah + (200h x (n - 1)) : where n = 1 to 8**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---------|---------|---------|--------|--------|--------|--------|--------|
| Name | TSa5F15 | TSa5F13 | TSa5F11 | TSa5F9 | TSa5F7 | TSa5F5 | TSa5F3 | TSa5F1 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7: Sa5 Bit of Frame 15 (TSa5F15)

Bit 6: Sa5 Bit of Frame 13 (TSa5F13)

Bit 5: Sa5 Bit of Frame 11 (TSa5F11)

Bit 4: Sa5 Bit of Frame 9 (TSa5F9)

Bit 3: Sa5 Bit of Frame 7 (TSa5F7)

Bit 2: Sa5 Bit of Frame 5 (TSa5F5)

Bit 1: Sa5 Bit of Frame 3 (TSa5F3)

Bit 0: Sa5 Bit of Frame 1 (TSa5F1)

Register Name: **E1TSa6 (E1 Mode Only)**
 Register Description: **Transmit Sa6 Bits Register**
 Register Address: **16Bh + (200h x (n - 1)) : where n = 1 to 8**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---------|---------|---------|--------|--------|--------|--------|--------|
| Name | TSa6F15 | TSa6F13 | TSa6F11 | TSa6F9 | TSa6F7 | TSa6F5 | TSa6F3 | TSa6F1 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7: Sa6 Bit of Frame 15 (TSa6F15)

Bit 6: Sa6 Bit of Frame 13 (TSa6F13)

Bit 5: Sa6 Bit of Frame 11 (TSa6F11)

Bit 4: Sa6 Bit of Frame 9 (TSa6F9)

Bit 3: Sa6 Bit of Frame 7 (TSa6F7)

Bit 2: Sa6 Bit of Frame 5 (TSa6F5)

Bit 1: Sa6 Bit of Frame 3 (TSa6F3)

Bit 0: Sa6 Bit of Frame 1 (TSa6F1)

Register Name: **E1TSa7 (E1 Mode Only)**
 Register Description: **Transmit Sa7 Bits Register**
 Register Address: **16Ch + (200h x (n - 1)) : where n = 1 to 8**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---------|---------|---------|--------|--------|--------|--------|--------|
| Name | TSa7F15 | TSa7F13 | TSa7F11 | TSa7F9 | TSa7F7 | TSa7F5 | TSa7F3 | TSa7F1 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7: Sa7 Bit of Frame 15 (TSa4F15)

Bit 6: Sa7 Bit of Frame 13 (TSa7F13)

Bit 5: Sa7 Bit of Frame 11 (TSa7F11)

Bit 4: Sa7 Bit of Frame 9 (TSa7F9)

Bit 3: Sa7 Bit of Frame 7 (TSa7F7)

Bit 2: Sa7 Bit of Frame 5 (TSa7F5)

Bit 1: Sa7 Bit of Frame 3 (TSa7F3)

Bit 0: Sa7 Bit of Frame 1 (TSa7F1)

Register Name: **E1TSa8 (E1 Mode Only)**
 Register Description: **Transmit Sa8 Bits Register**
 Register Address: **16Dh + (200h x (n - 1)) : where n = 1 to 8**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---------|---------|---------|--------|--------|--------|--------|--------|
| Name | TSa8F15 | TSa8F13 | TSa8F11 | TSa8F9 | TSa8F7 | TSa8F5 | TSa8F3 | TSa8F1 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7: Sa8 Bit of Frame 15 (TSa8F15)

Bit 6: Sa8 Bit of Frame 13 (TSa8F13)

Bit 5: Sa8 Bit of Frame 11 (TSa8F11)

Bit 4: Sa8 Bit of Frame 9 (TSa8F9)

Bit 3: Sa8 Bit of Frame 7 (TSa8F7)

Bit 2: Sa8 Bit of Frame 5 (TSa8F5)

Bit 1: Sa8 Bit of Frame 3 (TSa8F3)

Bit 0: Sa8 Bit of Frame 1 (TSa8F1)

Register Name: **TMMR**
 Register Description: **Transmit Master Mode Register**
 Register Address: **180h + (200h x (n - 1)) : where n = 1 to 8**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|--------|-----------|---|---|---|---|--------|-------|
| Name | FRM_EN | INIT_DONE | — | — | — | — | SFTRST | T1/E1 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7: Framer Enable (FRM_EN). This bit must be set to the desired state before writing INIT_DONE.
 0 = Framer disabled—held in low-power state.
 1 = Framer enabled—all features active.

Bit 6: Initialization Done (INIT_DONE). The user must set this bit once he has written the configuration registers. The host is required to write or clear all device registers prior to setting this bit. Once INIT_DONE is set, the DS26518 will check the FRM_EN bit and, if enabled, will begin operation based on the initial configuration.

Bit 1: Soft Reset (SFTRST). Level sensitive “soft” reset. Should be taken high, then low to reset the transceiver.
 0 = Normal operation.
 1 = Reset the transceiver.

Note: This reset does not clear the registers.

Bit 0: Transmitter T1/E1 Mode Select (T1/E1). Sets operating mode for transmitter only! This bit must be written with the desired value prior to setting INIT_DONE.
 0 = T1 operation.
 1 = E1 operation.

Register Name: **TCR1 (T1 Mode)**
 Register Description: **Transmit Control Register 1**
 Register Address: **181h + (200h x (n - 1)) : where n = 1 to 8**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|-----|------|------|------|------|-------|------|------|
| Name | TJC | TFPT | TCPT | TSSE | GB7S | TB8ZS | TAIS | TRAI |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Note: See [TCR1](#) for E1 Mode.

Bit 7: Transmit Japanese CRC-6 Enable (TJC)

- 0 = Use ANSI/AT&T:ITU-T CRC-6 calculation (normal operation).
- 1 = Use Japanese standard JT-G704 CRC-6 calculation.

Bit 6: Transmit F-Bit Pass Through (TFPT)

- 0 = F bits sourced internally.
- 1 = F bits sampled at TSErN ([T1.TCR2.7](#) TFDLS must be programmed to 0).

Bit 5: Transmit CRC Pass Through (TCPT)

- 0 = Source CRC-6 bits internally.
- 1 = CRC-6 bits sampled at TSErN during F-bit time.

Bit 4: Transmit Software Signaling Enable (TSSE). This function is enabled by TB7ZS ([T1.TCR2.0](#)).

- 0 = Do not source signaling data from the [TS1](#)–16 registers regardless of the [SSIE1](#)–4 registers. The [SSIE1](#)–4 registers still define which channels are to have B7 stuffing performed.
- 1 = Source signaling data as enabled by the [SSIE1](#)–4 registers.

Bit 3: Global Bit 7 Stuffing (GB7S). This function is enabled by TB7ZS ([T1.TCR2.0](#)).

- 0 = Allow the [SSIE1](#)–4 registers to determine which channels containing all zeros are to be bit 7 stuffed.
- 1 = Force bit 7 stuffing in all zero byte channels of that port, regardless of how the [SSIE1](#)–4 registers are programmed.

Bit 2: Transmit B8ZS Enable (TB8ZS)

- 0 = B8ZS disabled.
- 1 = B8ZS enabled.

Bit 1: Transmit Alarm Indication Signal (TAIS)

- 0 = Transmit data normally.
- 1 = Transmit an unframed all-ones code at TTIPn and TRINGn.

Bit 0: Transmit Remote Alarm Indication (TRAI)

- 0 = Do not transmit remote alarm.
- 1 = Transmit remote alarm.

Register Name: **TCR1 (E1 Mode)**
 Register Description: **Transmit Control Register 1**
 Register Address: **181h + (200h x (n - 1)) : where n = 1 to 8**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|------|------|-------|------|------|-------|------|-------|
| Name | TTPT | T16S | TG802 | TSiS | TSA1 | THDB3 | TAIS | TCRC4 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Note: See [TCR1](#) for T1 Mode.

Bit 7: Transmit Time Slot 0 Pass Through (TTPT)

0 = FAS bits/Sa bits/Remote Alarm sourced internally from the [E1TAF](#) and [E1TNAF](#) registers.
 1 = FAS bits/Sa bits/Remote Alarm sourced from TSERn.

Bit 6: Transmit Time Slot 16 Data Select (T16S). See Section [9.9.4](#) on software signaling.

0 = Time slot 16 determined by the [SSIE1](#)–4 and [THSCS1](#)–4 registers.
 1 = Source time slot 16 from [TS1](#)–16 registers.

Bit 5: Transmit G.802 Enable (TG802). See Section [11.4](#).

0 = Do not force TCHBLKn high during bit 1 of time slot 26.
 1 = Force TCHBLKn high during bit 1 of time slot 26.

Bit 4: Transmit International Bit Select (TSiS)

0 = Sample Si bits at TSERn pin.
 1 = Source Si bits from [E1TAF](#) and [E1TNAF](#) registers (in this mode, [TCR1.7](#) must be set to 0).

Bit 3: Transmit Signaling All Ones (TSA1)

0 = Normal operation.
 1 = Force time slot 16 in every frame to all ones.

Bit 2: Transmit HDB3 Enable (THDB3)

0 = HDB3 disabled.
 1 = HDB3 enabled.

Bit 1: Transmit AIS (TAIS)

0 = Transmit data normally.
 1 = Transmit an unframed all-ones code at TTIPn and TRINGn.

Bit 0: Transmit CRC-4 Enable (TCRC4)

0 = CRC-4 disabled.
 1 = CRC-4 enabled.

Register Name: **T1.TCR2 (T1 Mode)**
 Register Description: **Transmit Control Register 2**
 Register Address: **182h + (200h x (n - 1)) : where n = 1 to 8**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|-------|--------|--------|-------|-------|-------|---|-------|
| Name | TFDLS | TSLC96 | TDDSEN | FBCT2 | FBCT1 | TRAIS | — | TB7ZS |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Note: See [E1.TCR2](#) for E1 Mode.

Bit 7: TFDL Register Select (TFDLS)

- 0 = Source FDL or Fs bits from the internal TFDL register or the SLC-96 data formatter ([T1.TCR2.6](#)).
- 1 = Source FDL or Fs bits from the internal HDLC-64 controller.

Bit 6: Transmit SLC-96 (TSLC96). Set this bit to a one in SLC-96 framing applications. Must be set to source the SLC-96 alignment pattern and data from the [T1TSLC1–3](#) registers. See Section [9.9.4.3](#) for details.

- 0 = SLC-96 insertion disabled.
- 1 = SLC-96 insertion enabled.

Bit 5: Transmit DDS Zero Suppression Enable (TDDSEN)

- 0 = No DDS stuffing.
- 1 = DDS stuffing enabled. Force zero code 10011000 in all zero byte channels based on the channel select registers [TDDSD1–3](#).

Bit 4: F-Bit Corruption Type 2 (FBCT2). Setting this bit high enables the corruption of one Ft (D4 framing mode) or FPS (ESF framing mode) bit in every 128 Ft or FPS bits as long as the bit remains set.

Bit 3: F-Bit Corruption Type 1 (FBCT1). A low-to-high transition of this bit causes the next three consecutive Ft (D4 framing mode) or FPS (ESF framing mode) bits to be corrupted causing the remote end to experience a loss of synchronization.

Bit 2: Transmit RAI Select (TRAIS)

- 0 = Transmit RAI is T1.
 - D4—Zeros in bit 2 of all channels.
 - ESF—00FF pattern in the FDL.
- 1 = Transmit RAI is J1.
 - D4—A one in the S-bit position of frame 12.
 - ESF—All ones in FDL.

Note: This bit only selects the type of remote alarm to send. To enable transmission of remote alarm, set [TCR1.TRAI](#).

Bit 0: Transmit-Side Bit 7 Zero Suppression Enable (TB7ZS)

- 0 = No stuffing occurs.
- 1 = Force bit 7 to a one as determined by the GB7S bit at [TCR1.3](#).

Register Name: **E1.TCR2 (E1 Mode)**
 Register Description: **Transmit Control Register 2**
 Register Address: **182h + (200h x (n - 1)) : where n = 1 to 8**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|------|------|-----|---|---|---|---|---|
| Name | AEBE | AAIS | ARA | — | — | — | — | — |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Note: See [T1.TCR2](#) for T1 Mode.

Bit 7: Automatic E-Bit Enable (AEBE)

- 0 = E-bits not automatically set in the transmit direction.
- 1 = E-bits automatically set in the transmit direction.

Bit 6: Automatic AIS Generation (AAIS)

- 0 = Disabled
- 1 = Enabled

Bit 5: Automatic Remote Alarm Generation (ARA)

- 0 = Disabled
- 1 = Enabled

Register Name: **TCR3**
 Register Description: **Transmit Control Register 3**
 Register Address: **183h + (200h x (n - 1)) : where n = 1 to 8**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|---|--------------|--------------|-------------|-----|-------------|-------------|
| Name | — | — | TCSS1 | TCSS0 | MFRS | TFM | IBPV | TLOOP |
| | — | — | <i>TCSS1</i> | <i>TCSS0</i> | <i>MFRS</i> | — | <i>IBPV</i> | <i>CRC4</i> |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 5 and 4 : Transmit Clock Source Select 1 and 0 (TCSS[1:0])

| TCSS1 | TCSS0 | Transmit Clock Source |
|-------|-------|---|
| 0 | 0 | The TCLKn pin is always the source of transmit clock. |
| 0 | 1 | Switch to the clock present at RCLKn when the signal at the TCLKn pin fails to transition after 1 channel time. |
| 1 | 0 | Reserved. |
| 1 | 1 | Use the signal present at RCLKn as the transmit clock. The TCLKn pin is ignored (loop time). |

Bit 3: Multiframe Reference Select (MFRS). This bit selects the source for the transmit formatter multiframe boundary.

0 = Normal operation. Transmit multiframe boundary is determined by 'line-side' counters referenced to TSYNCn when TSYNCn is an input. Free-running when TSYNCn is an output.

1 = Pass-forward operation. Tx multiframe boundary determined by 'system-side' counters referenced to TSSYNClOn (input mode3), which is then passed forward to the line side clock domain. This mode can only be used when the transmit elastic store is enabled with a synchronous backplane (i.e., no frame slips allowed). This mode must be used to allow Tx hardware signaling insertion while the Tx elastic store is enabled.

Bit 2: Transmit Frame Mode Select (TFM) (T1 Mode Only)

0 = ESF framing mode.

1 = D4 framing mode.

Bit 1: Insert BPV (IBPV). A 0-to-1 transition on this bit will cause a single Bipolar Violation (BPV) to be inserted into the transmit data stream. Once this bit has been toggled from a 0 to a 1, the device waits for the next occurrence of three consecutive ones to insert the BPV. This bit must be cleared and set again for a subsequent error to be inserted.

Bit 0 (T1 Mode): Transmit Loop Code Enable (TLOOP). See Section [9.9.15](#) for details.

0 = Transmit data normally.

1 = Replace normal transmitted data with repeating code as defined in registers [T1TCD1](#) and [T1TCD2](#).

Bit 0 (E1 Mode): CRC-4 Recalculate (CRC4R)

0 = Transmit CRC-4 generation and insertion operates in normal mode.

1 = Transmit CRC-4 generation operates according to G.706 Intermediate Path Recalculation method.

Register Name: **TIOCR**
 Register Description: **Transmit I/O Configuration Register**
 Register Address: **184h + (200h x (n - 1)) : where n = 1 to 8**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|----------------|-----------------|------------------|---------------|-------------|-------------|------|------------|
| Name | TCLKINV | TSYNCINV | TSSYNCINV | TSCLKM | TSSM | TSIO | TSDW | TSM |
| | <i>TCLKINV</i> | <i>TSYNCINV</i> | <i>TSSYNCINV</i> | <i>TSCLKM</i> | <i>TSSM</i> | <i>TSIO</i> | — | <i>TSM</i> |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7: TCLKn Invert (TCLKINV)

0 = No inversion.
 1 = Invert.

Bit 6: TSYNCn Invert (TSYNCINV)

0 = No inversion.
 1 = Invert.

Bit 5: TSSYNCn (Input Mode Only) Invert (TSSYNCINV)

0 = No inversion.
 1 = Invert.

Bit 4: TSYCLKn Mode Select (TSCLKM)

0 = If TSYCLKn is 1.544MHz.
 1 = If TSYCLKn is 2.048/4.096/8.192MHz or IBO enabled (see Section [9.8.2](#) for details on IBO function).

Bit 3: TSSYNCn Mode Select (TSSM). Selects frame or multiframe mode for the TSSYNCn pin.

0 = Frame mode.
 1 = Multiframe mode.

Bit 2: TSYNCn I/O Select (TSIO)

0 = TSYNCn is an input.
 1 = TSYNCn is an output.

Bit 1: TSYNCn Double-Wide (TSDW) (T1 Mode Only) (Note: This bit must be set to zero when TSM = 1 or when TSIO = 0.)

0 = Do not pulse double-wide in signaling frames.
 1 = Do pulse double-wide in signaling frames.

Bit 0: TSYNCn Mode Select (TSM). Selects frame or multiframe mode for the TSYNCn pin.

0 = Frame mode.
 1 = Multiframe mode.

Register Name: **TESCR**
 Register Description: **Transmit Elastic Store Control Register**
 Register Address: **185h + (200h x (n - 1)) : where n = 1 to 8**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---------|---------|---|------|---------|------|--------|------|
| Name | TDATFMT | TGCLKEN | — | TSZS | TESALGN | TESR | TESMDM | TESE |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Note: Bits 6 and 7 are used for fractional backplane support. See Section [9.8.5](#).

Bit 7: Transmit Channel Data Format (TDATFMT)

- 0 = 64kbps (data contained in all 8 bits).
- 1 = 56kbps (data contained in 7 out of the 8 bits).

Bit 6: Transmit Gapped Clock Enable (TGCLKEN)

- 0 = TCHCLK functions normally.
- 1 = Enable gapped bit clock output on TCHCLKn.

Bit 4: Transmit Slip Zone Select (TSZS). This bit determines the minimum distance allowed between the elastic store read and write pointers before forcing a controlled slip. This bit is only applies during T1 to E1 or E1 to T1 conversion applications.

- 0 = Force a slip at 9 bytes or less of separation (used for clustered blank channels).
- 1 = Force a slip at 2 bytes or less of separation (used for distributed blank channels).

Bit 3: Transmit Elastic Store Align (TESALGN). Setting this bit from a zero to a one will force the transmit elastic store's write/read pointers to a minimum separation of half a frame. No action will be taken if the pointer separation is already greater or equal to half a frame. If pointer separation is less than half a frame, the command will be executed and the data will be disrupted. Should be toggled after TSYCLKn has been applied and is stable. Must be cleared and set again for a subsequent align.

Bit 2: Transmit Elastic Store Reset (TESR). Setting this bit from a zero to a one will force the read pointer into the same frame that the write pointer is exiting, minimizing the delay through the elastic store. If this command should place the pointers within the slip zone (see bit 4), then an immediate slip will occur and the pointers will move back to opposite frames. Should be toggled after TSYCLKn has been applied and is stable. Do not leave this bit set high.

Bit 1: Transmit Elastic Store Minimum Delay Mode (TESMDM)

- 0 = Elastic stores operate at full two-frame depth.
- 1 = Elastic stores operate at 32-bit depth.

Bit 0: Transmit Elastic Store Enable (TESE)

- 0 = Elastic store is bypassed.
- 1 = Elastic store is enabled.

Register Name: **TCR4**
 Register Description: **Transmit Control Register 4**
 Register Address: **186h + (200h x (n - 1)) : where n = 1 to 8**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|--------------|--------------|--------------|--------------|-------|-------|-----|-----|
| Name | uALAW | BINV1 | BINV0 | TJBEN | TRAIM | TAISM | TC1 | TC0 |
| | <i>uALAW</i> | <i>BINV1</i> | <i>BINV0</i> | <i>TJBEN</i> | — | — | — | — |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7: u-Law or A-Law Digital Milliwatt Code Select (uALAW)

0 = u-law code is inserted based on TDMWEx registers.
 1 = A-law code is inserted based on TDMWEx registers.

Bits 6 and 5: Transmit Bit Inversion (BINV[1:0])

00 = No inversion.
 01 = Invert framing.
 10 = Invert signaling.
 11 = Invert payload.

Bit 4: Transmit Jammed Bit 8 Suppression Enable (TJBEN)

0 = No stuffing enabled.
 1 = Jammed Bit 8 Suppression enabled. This forces bit 8 to a one as determined by [TJBE1](#)–4 registers and bit 7 to a one in T1 signaling frames.

Bits 3: Transmit RAI Mode (TRAIM) (T1 Mode Only). Determines the pattern sent when TRAI ([TCR1.0](#)) is activated in ESF frame mode only.

0 = Transmit normal RAI when [TCR1.RAI](#) = 1
 1 = If T1 ESF mode, transmit RAI-CI (T1.403) when [TCR1.RAI](#) = 1

Bits 2 : Transmit AIS Mode (TAISM) (T1 Mode Only). Determines the pattern sent when TAIS ([TCR1.1](#)) is activated.

0 = Transmit normal AIS (unframed all ones) upon activation with [TCR1.1](#).
 1 = Transmit AIS-CI (T1.403) upon activation with [TCR1.1](#).

Bits 1 and 0 : Transmit Code Length Definition Bits (TC[1:0]) (T1 Mode Only)

| TC1 | TC0 | Length Selected (Bits) |
|-----|-----|------------------------|
| 0 | 0 | 5 |
| 0 | 1 | 6 : 3 |
| 1 | 0 | 7 |
| 1 | 1 | 16 : 8 : 4 : 2 : 1 |

Register Name: **THFC**
 Register Description: **Transmit HDLC-64 FIFO Control Register**
 Register Address: **187h + (200h x (n - 1)) : where n = 1 to 8**

| | | | | | | | | |
|---------|---|---|---|---|---|---|--------|--------|
| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | — | — | — | — | — | — | TFLWM1 | TFLWM0 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 1 and 0: Transmit HDLC-64 FIFO Low Watermark Select (TFLWM[1:0])

| TFLWM1 | TFLWM0 | Transmit FIFO Watermark (Bytes) |
|--------|--------|---------------------------------|
| 0 | 0 | 4 |
| 0 | 1 | 16 |
| 1 | 0 | 32 |
| 1 | 1 | 48 |

Register Name: **TIBOC**
 Register Description: **Transmit Interleave Bus Operation Control Register**
 Register Address: **188h + (200h x (n - 1)) : where n = 1 to 8**

| | | | | | | | | |
|---------|---|---|---|--------|-------|---|---|---|
| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | — | — | — | IBOSEL | IBOEN | — | — | — |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 4: Interleave Bus Operation Select (IBOSEL). This bit selects channel or frame interleave mode.
 0 = Channel Interleave.
 1 = Frame Interleave.

Bit 3: Interleave Bus Operation Enable (IBOEN)

0 = Interleave Bus Operation disabled.
 1 = Interleave Bus Operation enabled.

Register Name: **TDS0SEL**
 Register Description: **Transmit DS0 Channel Monitor Select Register**
 Register Address: **189h + (200h x (n - 1)) : where n = 1 to 8**

| | | | | | | | | |
|---------|---|---|---|------|------|------|------|------|
| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | — | — | — | TCM4 | TCM3 | TCM2 | TCM1 | TCM0 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 4 to 0: Transmit Channel Monitor Bits (TCM[4:0]). TCM0 is the LSB of a 5-bit channel select that determines which transmit channel data will appear in the [TDS0M](#) register. Channels 1 through 32 are represented by a 5-bit BCD code from 0 to 31. TCM[0:4] = all 0s selects channel 1, TCM[0:4] = 11111 selects channel 32.

Register Name: **TXPC**
 Register Description: **Transmit Expansion Port Control Register**
 Register Address: **18Ah + (200h x (n - 1)) : where n = 1 to 8**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|-------------|-------------|---|---|---|---------------|--------|--------------|
| Name | THMS | THEN | — | — | — | TBPDIR | TBPFUS | TBPEN |
| | <i>THMS</i> | <i>THEN</i> | — | — | — | <i>TBPDIR</i> | — | <i>TBPEN</i> |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7 (T1 Mode): Transmit HDLC-256 Mode Select (THMS)

0 = Transmit HDLC-256 assigned to time slots.
 1 = Transmit HDLC-256 assigned to FDL bits.

Bit 7 (E1 Mode): Transmit HDLC-256 Mode Select (THMS)

0 = Transmit HDLC-256 assigned to time slots.
 1 = Transmit HDLC-256 assigned to the Sa bits.

Bit 6: Transmit HDLC-256 Enable (THEN)

0 = Transmit HDLC-256 is not active.
 1 = Transmit HDLC-256 is active.

Bit 2: Transmit BERT Port Direction Control (TBPDIR)

0 = Normal (line) operation. Transmit BERT port sources data into the transmit path.
 1 = System (backplane) operation. Transmit BERT port sources data into the receive path (RSERn). In this mode, the data from the BERT is muxed into the receive path.

Bit 1: Transmit BERT Port Framed/Unframed Select (TBPFUS) (T1 Mode Only)

0 = The DS26518's transmit BERT will *not* clock data into the F-bit position (framed).
 1 = The DS26518's transmit BERT will clock data into the F-bit position (unframed).

Bit 0: Transmit BERT Port Enable (TBPEN)

0 = Transmit BERT port is not active.
 1 = Transmit BERT port is active.

Register Name: **TBPBS**
 Register Description: **Transmit BERT Port Bit Suppress Register**
 Register Address: **18Bh + (200h x (n - 1)) : where n = 1 to 8**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|--------|--------|--------|--------|--------|--------|--------|--------|
| Name | BPBSE8 | BPBSE7 | BPBSE6 | BPBSE5 | BPBSE4 | BPBSE3 | BPBSE2 | BPBSE1 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7: Transmit Channel Bit 8 Suppress (BPBSE8). MSB of the channel. Set to one to stop this bit from being used.

Bit 6: Transmit Channel Bit 7 Suppress (BPBSE7). Set to one to stop this bit from being used.

Bit 5: Transmit Channel Bit 6 Suppress (BPBSE6). Set to one to stop this bit from being used.

Bit 4: Transmit Channel Bit 5 Suppress (BPBSE5). Set to one to stop this bit from being used.

Bit 3: Transmit Channel Bit 4 Suppress (BPBSE4). Set to one to stop this bit from being used.

Bit 2: Transmit Channel Bit 3 Suppress (BPBSE3). Set to one to stop this bit from being used.

Bit 1: Transmit Channel Bit 2 Suppress (BPBSE2). Set to one to stop this bit from being used.

Bit 0: Transmit Channel Bit 1 Suppress (BPBSE1). LSB of the channel. Set to one to stop this bit from being used.

Register Name: **THBS**
 Register Description: **Transmit HDLC-256 Bit Suppress Register**
 Register Address: **18Dh + (200h x (n - 1)) : where n = 1 to 8**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|--------|--------|--------|--------|--------|--------|--------|--------|
| Name | THBSE8 | THBSE7 | THBSE6 | THBSE5 | THBSE4 | THBSE3 | THBSE2 | THBSE1 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7: Transmit Channel Bit 8 Suppress (THBSE8). MSB of the channel. Set to one to stop this bit from being used.

Bit 6: Transmit Channel Bit 7 Suppress (THBSE7). Set to one to stop this bit from being used.

Bit 5: Transmit Channel Bit 6 Suppress (THBSE6). Set to one to stop this bit from being used.

Bit 4: Transmit Channel Bit 5 Suppress/Sa4 Bit Suppress (THBSE5). Set to one to stop this bit from being used.

Bit 3: Transmit Channel Bit 4 Suppress/Sa5 Bit Suppress (THBSE4). Set to one to stop this bit from being used.

Bit 2: Transmit Channel Bit 3 Suppress/Sa6 Bit Suppress (THBSE3). Set to one to stop this bit from being used.

Bit 1: Transmit Channel Bit 2 Suppress/Sa7 Bit Suppress (THBSE2). Set to one to stop this bit from being used.

Bit 0: Transmit Channel Bit 1 Suppress/Sa8 Bit Suppress (THBSE1). LSB of the channel. Set to one to stop this bit from being used.

Register Name: **TSYNCC**
 Register Description: **Transmit Synchronizer Control Register**
 Register Address: **18Eh + (200h x (n - 1)) : where n = 1 to 8**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|---|---|---|-------------|-------------|--------------|---------------|
| Name | — | — | — | — | — | TSEN | SYNCE | RESYNC |
| | — | — | — | — | <i>CRC4</i> | <i>TSEN</i> | <i>SYNCE</i> | <i>RESYNC</i> |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 3: CRC-4 Enable (CRC4) (E1 Mode Only)

0 = Do not search for the CRC-4 multiframe word.
 1 = Search for the CRC-4 multiframe word.

Bit 2: Transmit Synchronizer Enable (TSEN)

0 = Transmit synchronizer disabled.
 1 = Transmit synchronizer enabled.

Bit 1: Sync Enable (SYNCE)

0 = Auto resync enabled.
 1 = Auto resync disabled.

Bit 0: Resynchronize (RESYNC). When toggled from low to high, a resynchronization of the transmit-side framer is initiated. Must be cleared and set again for a subsequent resync.

Register Name: **TLS1**
 Register Description: **Transmit Latched Status Register 1**
 Register Address: **190h + (200h x (n - 1)) : where n = 1 to 8**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|-------------|--------------|--------------|--------|------------|------------|--------------|--------------|
| Name | TESF | TESEM | TSLIP | TSLC96 | — | TMF | LOTCC | LOTCC |
| | <i>TESF</i> | <i>TESEM</i> | <i>TSLIP</i> | — | <i>TAF</i> | <i>TMF</i> | <i>LOTCC</i> | <i>LOTCC</i> |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Note: All bits in this register are latched and can cause interrupts.

Bit 7: Transmit Elastic Store Full Event (TESF). Set when the transmit elastic store buffer fills and a frame is deleted.

Bit 6: Transmit Elastic Store Empty Event (TESEM). Set when the transmit elastic store buffer empties and a frame is repeated.

Bit 5: Transmit Elastic Store Slip Occurrence Event (TSLIP). Set when the transmit elastic store has either repeated or deleted a frame.

Bit 4: Transmit SLC-96 Multiframe Event (TSLC96) (T1 Mode Only). When enabled by [T1.TCR2.6](#), this bit will set once per SLC-96 multiframe (72 frames) to alert the host that new data may be written to the [T1TSLC1–3](#) registers. See Section [9.9.4.3](#) for more information.

Bit 3: Transmit Align Frame Event (TAF) (E1 Mode Only). Set every 250µs to alert the host that the [E1TAF](#) and [E1TNAF](#) registers need to be updated.

Bit 2: Transmit Multiframe Event (TMF). In T1 mode, this bit is set every 1.5ms on D4 MF boundaries or every 3ms on ESF MF boundaries. In E1 operation, this bit is set every 2ms (regardless if CRC-4 is enabled) on transmit multiframe boundaries. Used to alert the host that signaling data needs to be updated.

Bit 1: Loss of Transmit Clock Condition Clear (LOTCC). Set when the LOTC condition has cleared (a clock has been sensed at the TCLKn pin).

Bit 0: Loss of Transmit Clock Condition (LOTCC). Set when the TCLKn pin has not transitioned for approximately 3 clock periods. Will force the LOTC pin high if enabled. This bit can be cleared by the host even if the condition is still present. The LOTC pin will remain high while the condition exists, even if the host has cleared the status bit. If enabled by [TIM1.0](#), the [INTB](#) pin will transition low when this bit is set, and transition high when this bit is cleared (if no other unmasked interrupt conditions exist).

Register Name: **TLS2**
 Register Description: **Transmit Latched Status Register 2 (HDLC-64)**
 Register Address: **191h + (200h x (n - 1)) : where n = 1 to 8**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|---|---|-------|------|-------|-------|------|
| Name | — | — | — | TFDLE | TUDR | TMEND | TLWMS | TNFS |
| | — | — | — | — | TUDR | TMEND | TLWMS | TNFS |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Note: All bits in this register are latched and can create interrupts.

Bit 4: Transmit FDL Register Empty (TFDLE) (T1 Mode Only). Set when the TFDL register has shifted out all 8 bits. Useful if the user wants to manually use the TFDL register to send messages, instead of using the HDLC-64 or BOC controller circuits.

Bit 3: Transmit FIFO Underrun Event (TUDR). Set when the transmit FIFO empties out without having seen the TMEND bit set. An abort is automatically sent.

Bit 2: Transmit Message End Event (TMEND). Set when the transmit HDLC-64 controller has finished sending a message.

Bit 1: Transmit FIFO Below Low Watermark Set Condition (TLWMS). Set when the transmit 64-byte FIFO empties beyond the low watermark as defined by the transmit low watermark bits (TLWM), rising edge detect of TLWM.

Bit 0: Transmit FIFO Not Full Set Condition (TNFS). Set when the transmit 64-byte FIFO has at least one empty byte available for write. Rising edge detect of TNF. Indicates change of state from full to not full.

Register Name: **TLS3**
 Register Description: **Transmit Latched Status Register 3 (Synchronizer)**
 Register Address: **192h + (200h x (n - 1)) : where n = 1 to 8**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|---|---|---|---|---|-----|------|
| Name | — | — | — | — | — | — | LOF | LOFD |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Note: Some bits in this register are latched and can create interrupts.

Bit 1: Loss of Frame (LOF). A real-time bit that indicates that the transmit synchronizer is searching for the sync pattern in the incoming data stream.

Bit 0: Loss Of Frame Synchronization Detect (LOFD). This latched bit is set when the transmit synchronizer is searching for the sync pattern in the incoming data stream.

Register Name: **TIIR**
 Register Description: **Transmit Interrupt Information Register**
 Register Address: **19Fh + (200h x (n - 1)) : where n = 1 to 8**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|---|---|---|---|------|------|------|
| Name | — | — | — | — | — | TLS3 | TLS2 | TLS1 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

The interrupt information register provides an indication of which status registers are generating an interrupt. When an interrupt occurs, the host can read TIIR to quickly identify which of the transmit status registers are causing the interrupt(s). These are real-time registers in that the bits will clear once the appropriate interrupt has been serviced and cleared.

Bit 2: Transmit Latched Status Register 3 Interrupt Status (TLS3)

0 = No interrupt pending.

1 = Interrupt pending.

Bit 1: Transmit Latched Status Register 2 Interrupt Status (TLS2)

0 = No interrupt pending.

1 = Interrupt pending.

Bit 0: Transmit Latched Status Register 1 Interrupt Status (TLS1)

0 = No interrupt pending.

1 = Interrupt pending.

Register Name: **TIM1**
 Register Description: **Transmit Interrupt Mask Register 1**
 Register Address: **1A0h + (200h x (n - 1)) : where n = 1 to 8**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|-------------|--------------|--------------|--------|------------|------------|--------------|--------------|
| Name | TESF | TESEM | TSLIP | TSLC96 | — | TMF | LOTCC | LOTCC |
| | <i>TESF</i> | <i>TESEM</i> | <i>TSLIP</i> | — | <i>TAF</i> | <i>TMF</i> | <i>LOTCC</i> | <i>LOTCC</i> |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7: Transmit Elastic Store Full Event (TESF)

0 = Interrupt masked.
 1 = Interrupt enabled.

Bit 6: Transmit Elastic Store Empty Event (TESEM)

0 = Interrupt masked.
 1 = Interrupt enabled.

Bit 5: Transmit Elastic Store Slip Occurrence Event (TSLIP)

0 = Interrupt masked.
 1 = Interrupt enabled.

Bit 4: Transmit SLC96 Multiframe Event (TSLC96) (T1 Mode Only)

0 = Interrupt masked.
 1 = Interrupt enabled.

Bit 3: Transmit Align Frame Event (TAF) (E1 Mode Only)

0 = Interrupt masked.
 1 = Interrupt enabled.

Bit 2: Transmit Multiframe Event (TMF)

0 = Interrupt masked.
 1 = Interrupt enabled.

Bit 1: Loss of Transmit Clock Clear Condition (LOTCC)

0 = Interrupt masked.
 1 = Interrupt enabled.

Bit 0: Loss of Transmit Clock Condition (LOTCC)

0 = Interrupt masked.
 1 = Interrupt enabled.

Register Name: **TIM2**
 Register Description: **Transmit Interrupt Mask Register 2 (HDLC-64)**
 Register Address: **1A1h + (200h x (n - 1)) : where n = 1 to 8**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|---|---|-------|-------------|--------------|--------------|-------------|
| Name | — | — | — | TFDLE | TUDR | TMEND | TLWMS | TNFS |
| | — | — | — | — | <i>TUDR</i> | <i>TMEND</i> | <i>TLWMS</i> | <i>TNFS</i> |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 4: Transmit FDL Register Empty (TFDLE) (T1 Mode Only)

0 = Interrupt masked.
 1 = Interrupt enabled.

Bit 3: Transmit FIFO Underrun Event (TUDR)

0 = Interrupt masked.
 1 = Interrupt enabled.

Bit 2: Transmit Message End Event (TMEND)

0 = Interrupt masked.
 1 = Interrupt enabled.

Bit 1: Transmit FIFO Below Low Watermark Set Condition (TLWMS)

0 = Interrupt masked.
 1 = Interrupt enabled.

Bit 0: Transmit FIFO Not Full Set Condition (TNFS)

0 = Interrupt masked.
 1 = Interrupt enabled.

Register Name: **TIM3**
 Register Description: **Transmit Interrupt Mask Register 3 (Synchronizer)**
 Register Address: **1A2h + (200h x (n - 1)) : where n = 1 to 8**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|---|---|---|---|---|---|------|
| Name | — | — | — | — | — | — | — | LOFD |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 0: Loss of Frame Synchronization Detect (LOFD)

0 = Interrupt masked.
 1 = Interrupt enabled.

Register Name: **T1TCD1 (T1 Mode Only)**
 Register Description: **Transmit Code Definition Register 1**
 Register Address: **1ACh + (200h x (n - 1)) : where n = 1 to 8**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|----|----|----|----|----|----|----|----|
| Name | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7: Transmit Code Definition Bit 7 (C7). First bit of the repeating pattern.

Bit 6: Transmit Code Definition Bit 6 (C6)

Bit 5: Transmit Code Definition Bit 5 (C5)

Bit 4: Transmit Code Definition Bit 4 (C4)

Bit 3: Transmit Code Definition Bit 3 (C3)

Bit 2: Transmit Code Definition Bit 2 (C2). A Don't Care if a 5-bit length is selected.

Bit 1: Transmit Code Definition Bit 1 (C1). A Don't Care if a 5- or 6-bit length is selected.

Bit 0: Transmit Code Definition Bit 0 (C0). A Don't Care if a 5-, 6-, or 7-bit length is selected.

Register Name: **T1TCD2 (T1 Mode Only)**
 Register Description: **Transmit Code Definition Register 2**
 Register Address: **1ADh + (200h x (n - 1)) : where n = 1 to 8**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|----|----|----|----|----|----|----|----|
| Name | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7: Transmit Code Definition Bit 7 (C7). A Don't Care if a 5-, 6-, or 7-bit length is selected.

Bit 6: Transmit Code Definition Bit 6 (C6). A Don't Care if a 5-, 6-, or 7-bit length is selected.

Bit 5: Transmit Code Definition Bit 5 (C5). A Don't Care if a 5-, 6-, or 7-bit length is selected.

Bit 4: Transmit Code Definition Bit 4 (C4). A Don't Care if a 5-, 6-, or 7-bit length is selected.

Bit 3: Transmit Code Definition Bit 3 (C3). A Don't Care if a 5-, 6-, or 7-bit length is selected.

Bit 2: Transmit Code Definition Bit 2 (C2). A Don't Care if a 5-, 6-, or 7-bit length is selected.

Bit 1: Transmit Code Definition Bit 1 (C1). A Don't Care if a 5-, 6-, or 7-bit length is selected.

Bit 0: Transmit Code Definition Bit 0 (C0). A Don't Care if a 5-, 6-, or 7-bit length is selected.

Register Name: **TRTS2**
 Register Description: **Transmit Real-Time Status Register 2 (HDLC-64)**
 Register Address: **1B1h + (200h x (n - 1)) : where n = 1 to 8**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|---|---|---|-------|-------|------|-----|
| Name | — | — | — | — | EMPTY | TFULL | TLWM | TNF |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Note: All bits in this register are real time.

Bit 3: Transmit FIFO Empty (EMPTY). A real-time bit that is set high when the FIFO is empty.

Bit 2: Transmit FIFO Full (TFULL). A real-time bit that is set high when the FIFO is full.

Bit 1: Transmit FIFO Below Low Watermark Condition (TLWM). Set when the transmit 64-byte FIFO empties beyond the low watermark as defined by the transmit low watermark bits (TLWM).

Bit 0: Transmit FIFO Not Full Condition (TNF). Set when the transmit 64-byte FIFO has at least one byte available.

Register Name: **TFBA**
 Register Description: **Transmit HDLC-64 FIFO Buffer Available Register**
 Register Address: **1B3h + (200h x (n - 1)) : where n = 1 to 8**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|-------|-------|-------|-------|-------|-------|-------|-------|
| Name | TFBA7 | TFBA6 | TFBA5 | TFBA4 | TFBA3 | TFBA2 | TFBA1 | TFBA0 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 6 to 0: Transmit FIFO Bytes Available (TFBA6 to TFBA0). TFBA0 is the LSB.

Register Name: **THF**
 Register Description: **Transmit HDLC-64 FIFO Register**
 Register Address: **1B4h + (200h x (n - 1)) : where n = 1 to 8**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|------|------|------|------|------|------|------|------|
| Name | THD7 | THD6 | THD5 | THD4 | THD3 | THD2 | THD1 | THD0 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7: Transmit HDLC-64 Data Bit 7 (THD7). MSB of an HDLC-64 packet data byte.

Bit 6: Transmit HDLC-64 Data Bit 6 (THD6)

Bit 5: Transmit HDLC-64 Data Bit 5 (THD5)

Bit 4: Transmit HDLC-64 Data Bit 4 (THD4)

Bit 3: Transmit HDLC-64 Data Bit 3 (THD3)

Bit 2: Transmit HDLC-64 Data Bit 2 (THD2)

Bit 1: Transmit HDLC-64 Data Bit 1 (THD1)

Bit 0: Transmit HDLC-64 Data Bit 0 (THD0). LSB of an HDLC-64 packet data byte.

Register Name: **TDS0M**
 Register Description: **Transmit DS0 Monitor Register**
 Register Address: **1BBh + (200h x (n - 1)) : where n = 1 to 8**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|----|----|----|----|----|----|----|----|
| Name | B1 | B2 | B3 | B4 | B5 | B6 | B7 | B8 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 7 to 0: Transmit DS0 Channel Bits (B[1:8]). Transmit channel data that has been selected by the [TDS0SEL](#) register. B8 is the LSB of the DS0 channel (last bit to be transmitted).

Register Name: **TBCS1, TBCS2, TBCS3, TBCS4**
 Register Description: **Transmit Blank Channel Select Registers 1 to 4**
 Register Address: **1C0h, 1C1h, 1C2h, 1C3h + (200h x (n - 1)) : where n = 1 to 8**

| Bit # | (MSB) | | | | | | | (LSB) | |
|-------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|---------------------------------|
| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
| Named | CH8 | CH7 | CH6 | CH5 | CH4 | CH3 | CH2 | CH1 | TBCS1 |
| | CH16 | CH15 | CH14 | CH13 | CH12 | CH11 | CH10 | CH9 | TBCS2 |
| | CH24 | CH23 | CH22 | CH21 | CH20 | CH19 | CH18 | CH17 | TBCS3 |
| | <i>CH32</i> | <i>CH31</i> | <i>CH30</i> | <i>CH29</i> | <i>CH28</i> | <i>CH27</i> | <i>CH26</i> | <i>CH25</i> | TBCS4 (E1 Mode Only) |

Bits 7 to 0: Transmit Blank Channel Select for Channels 1 to 32 (CH[1:32])

0 = Transmit TSERn data from this channel.

1 = Ignore TSERn data from this channel.

Note that when two or more sequential channels are chosen to be ignored, the receive slip zone select bit should be set to zero. If the ignore channels are distributed (such as 1, 5, 9, 13, 17, 21, 25, 29) then the RSZS bit can be set to one, which may provide a lower occurrence of slips in certain applications.

Register Name: **TCBR1, TCBR2, TCBR3, TCBR4**
 Register Description: **Transmit Channel Blocking Registers 1 to 4**
 Register Address: **1C4h, 1C5h, 1C6h, 1C7h + (200h x (n - 1)) : where n = 1 to 8**

| Bit # Name | (MSB) | | | | | | | (LSB) | |
|---------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|---------------------|------------------------------|
| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
| | CH8 | CH7 | CH6 | CH5 | CH4 | CH3 | CH2 | CH1 | TCBR1 |
| | CH16 | CH15 | CH14 | CH13 | CH12 | CH11 | CH10 | CH9 | TCBR2 |
| | CH24 | CH23 | CH22 | CH21 | CH20 | CH19 | CH18 | CH17 | TCBR3 |
| | <i>CH32</i> | <i>CH31</i> | <i>CH30</i> | <i>CH29</i> | <i>CH28</i> | <i>CH27</i> | <i>CH26</i> | <i>CH25 (F-bit)</i> | TCBR4 (E1 Mode Only)* |

Bits 7 to 0: Transmit Channels 1 to 32 Channel Blocking Control Bits (CH[1:32]).

0 = Force the TCHBLKn pin to remain low during this channel time.
 1 = Force the TCHBLKn pin high during this channel time.

*** Note that TCBR4 has two functions:**

When 2.048MHz backplane mode is selected, this register allows the user to enable the channel blocking signal for any of the 32 possible backplane channels.

When 1.544MHz backplane mode is selected, the LSB of this register determines whether or not the TCHBLKn signal will pulse high during the F-bit time:

TCBR4.0 = 0, do not pulse TCHBLKn during the F-bit.
 TCBR4.0 = 1, pulse TCHBLKn during the F-bit.

In this mode TCBR4.1 to TCBR4.7 should be set to 0.

Register Name: **THSCS1, THSCS2, THSCS3, THSCS4**
 Register Description: **Transmit Hardware-Signaling Channel Select Registers 1 to 4**
 Register Address: **1C8h, 1C9h, 1CAh, 1CBh + (200h x (n - 1)) : where n = 1 to 8**

| Bit # Name | (MSB) | | | | | | | (LSB) | |
|---------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------------------------|
| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
| | CH8 | CH7 | CH6 | CH5 | CH4 | CH3 | CH2 | CH1 | THSCS1 |
| | CH16 | CH15 | CH14 | CH13 | CH12 | CH11 | CH10 | CH9 | THSCS2 |
| | CH24 | CH23 | CH22 | CH21 | CH20 | CH19 | CH18 | CH17 | THSCS3 |
| | <i>CH32</i> | <i>CH31</i> | <i>CH30</i> | <i>CH29</i> | <i>CH28</i> | <i>CH27</i> | <i>CH26</i> | <i>CH25</i> | THSCS4 (E1 Mode Only)* |

Bits 7 to 0: Transmit Hardware-Signaling Channel Select for Channels 1 to 32 (CH[1:32]). These bits determine which channels have signaling data inserted from the TSiGn pin into the TSErN PCM data.

0 = Do not source signaling data from the TSiGn pin for this channel.
 1 = Source signaling data from the TSiGn pin for this channel.

*** Note that THSCS4 is only used in 2.048MHz backplane applications.**

Register Name: **TGCCS1, TGCCS2, TGCCS3, TGCCS4**
 Register Description: **Transmit Gapped Clock Channel Select Registers 1 to 4**
 Register Address: **1CCh, 1CDh, 1CEh, 1CFh + (200h x (n - 1)) : where n = 1 to 8**

| Bit # Name | (MSB) | | | | | | | (LSB) | |
|---------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|------------------------|-------------------------------|
| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
| | CH8 | CH7 | CH6 | CH5 | CH4 | CH3 | CH2 | CH1 | TGCCS1 |
| | CH16 | CH15 | CH14 | CH13 | CH12 | CH11 | CH10 | CH9 | TGCCS2 |
| | CH24 | CH23 | CH22 | CH21 | CH20 | CH19 | CH18 | CH17 | TGCCS3 |
| | <i>CH32</i> | <i>CH31</i> | <i>CH30</i> | <i>CH29</i> | <i>CH28</i> | <i>CH27</i> | <i>CH26</i> | <i>CH25</i> (F-bit) | TGCCS4 (E1 Mode Only)* |

Bits 7 to 0: Transmit Channels 1 to 32 Gapped Clock Channel Select Bits (CH[1:32])

0 = no clock is present on TCHCLK during this channel time

1 = force a clock on TCHCLK during this channel time. The clock will be synchronous with TCLKn if the elastic store is disabled, and synchronous with TSYCLKn if the elastic store is enabled.

*** Note that TGCCS4 has two functions:**

When 2.048MHz backplane mode is selected, this register allows the user to enable the gapped clock on TCHCLK for any of the 32 possible backplane channels.

When 1.544MHz backplane mode is selected, the LSB of this register determines whether or not a clock is generated on TCHCLK during the F-bit time:

TGCCS4.0 = 0, do not generate a clock during the F-bit.

TGCCS4.0 = 1, generate a clock during the F-bit.

In this mode TGCCS4.1 to TGCCS4.7 should be set to 0.

Register Name: **PCL1, PCL2, PCL3, PCL4**
 Register Description: **Per-Channel Loopback Enable Registers 1 to 4**
 Register Address: **1D0h, 1D1h, 1D2h, 1D3h + (200h x (n - 1)) : where n = 1 to 8**

| Bit # Name | (MSB) | | | | | | | (LSB) | |
|---------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|----------------------------|
| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
| | CH8 | CH7 | CH6 | CH5 | CH4 | CH3 | CH2 | CH1 | PCL1 |
| | CH16 | CH15 | CH14 | CH13 | CH12 | CH11 | CH10 | CH9 | PCL2 |
| | CH24 | CH23 | CH22 | CH21 | CH20 | CH19 | CH18 | CH17 | PCL3 |
| | <i>CH32</i> | <i>CH31</i> | <i>CH30</i> | <i>CH29</i> | <i>CH28</i> | <i>CH27</i> | <i>CH26</i> | <i>CH25</i> | PCL4 (E1 Mode Only) |

Bits 7 to 0: Per-Channel Loopback Enable for Channels 1 to 32 (CH[1:32])

0 = Loopback disabled.

1 = Enable loopback. Source data from the corresponding receive channel.

Register Name: **TBPCS1, TBPCS2, TBPCS3, TBPCS4**
 Register Description: **Transmit BERT Port Channel Select Registers**
 Register Address: **1D4h, 1D5h, 1D6h, 1D7h + (200h x (n - 1)) : where n = 1 to 8**

| Bit # Name | (MSB) | | | | (LSB) | | | | |
|---------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|----------------------------------|
| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
| | CH8 | CH7 | CH6 | CH5 | CH4 | CH3 | CH2 | CH1 | TBPCS1 |
| | CH16 | CH15 | CH14 | CH13 | CH12 | CH11 | CH10 | CH9 | TBPCS2 |
| | CH24 | CH23 | CH22 | CH21 | CH20 | CH19 | CH18 | CH17 | TBPCS3 |
| | <i>CH32</i> | <i>CH31</i> | <i>CH30</i> | <i>CH29</i> | <i>CH28</i> | <i>CH27</i> | <i>CH26</i> | <i>CH25</i> | TBPCS4 (E1 Mode Only) |

Setting any of the CH[1:32] bits in the TBPCS1 to TBPCS4 registers will enable the transmit BERT clock for the associated channel time, and allow mapping of the selected channel data out of the receive BERT port. Multiple or all channels may be selected simultaneously.

Register Name: **THCS1, THCS2, THCS3, THCS4**
 Register Description: **Transmit HDLC-256 Channel Select Registers 1 to 4**
 Register Address: **1DCh, 1DDh, 1DEh, 1DFh + (200h x (n - 1)) : where n = 1 to 8**

| Bit # Name | (MSB) | | | | (LSB) | | | | |
|---------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|---------------------------------|
| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
| | CH8 | CH7 | CH6 | CH5 | CH4 | CH3 | CH2 | CH1 | THCS1 |
| | CH16 | CH15 | CH14 | CH13 | CH12 | CH11 | CH10 | CH9 | THCS2 |
| | CH24 | CH23 | CH22 | CH21 | CH20 | CH19 | CH18 | CH17 | THCS3 |
| | <i>CH32</i> | <i>CH31</i> | <i>CH30</i> | <i>CH29</i> | <i>CH28</i> | <i>CH27</i> | <i>CH26</i> | <i>CH25</i> | THCS4 (E1 Mode Only) |

Setting any of the CH[1:32] bits in the THCS1 to THCS4 registers will enable the transmit HDLC-256 clock for the associated channel time, and allow mapping of the selected channel data out of the HDLC-256 FIFO. Multiple or all channels may be selected simultaneously.

10.5 LIU Register Definitions

Table 10-17. LIU Register Set

| ADDRESS | NAME | DESCRIPTION | R/W |
|-------------|------------------------|---|-----|
| 1000h | LTRCR | LIU Transmit Receive Control Register | R/W |
| 1001h | LTIPSR | LIU Transmit Impedance and Pulse Shape Selection Register | R/W |
| 1002h | LMCR | LIU Maintenance Control Register | R/W |
| 1003h | LRSR | LIU Real Status Register | R |
| 1004h | LSIMR | LIU Status Interrupt Mask Register | R/W |
| 1005h | LLSR | LIU Latched Status Register | R/W |
| 1006h | LRSL | LIU Receive Signal Level Register | R |
| 1007h | LRISMR | LIU Receive Impedance and Sensitivity Monitor Register | R/W |
| 1008h | LRCR | LIU Receive Control Register | R/W |
| 1009h–101Fh | — | Reserved | — |

Note: Reserved registers should only be written with all zeros.

Register Name: **LTRCR**
 Register Description: **LIU Transmit Receive Control Register**
 Register Addresses: **1000h + (20h x (n - 1)) : where n = 1 to 8**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|------|-------|-------|-------|-------|---------|-----|
| Name | — | RHPM | JADS1 | JADS0 | JAPS1 | JAPS0 | T1J1E1S | LSC |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 6: Receive Hitless Protection Mode (RHPM)

- 0 = Normal operation using software for hitless protection (RIMPON).
- 1 = Hitless protection switching mode using TXENABLE pin.

If the TXENABLE pin is low and this bit is set to one, the receive LIU will present a high impedance to the line, overriding the receive impedance selection register bits [LRISMR.RIMPON\[2:0\]](#).

Bits 5 and 4 : Jitter Attenuator Depth Select (JADS[1:0])

| JADS1 | JADS0 | FUNCTION |
|-------|-------|---|
| 0 | 0 | Jitter attenuator FIFO depth 128 bits. |
| 0 | 1 | Jitter attenuator FIFO depth 64 bits. |
| 1 | 0 | Jitter attenuator FIFO depth 32 bits. |
| 1 | 1 | Jitter attenuator FIFO depth 16 bits (used for delay-sensitive applications). |

Bits 3 and 2: Jitter Attenuator Position Select (JAPS[1:0]). These bits are used to select the position of the jitter attenuator.

| JAPS1 | JAPS0 | FUNCTION |
|-------|-------|---|
| 0 | 0 | Jitter attenuator in the receive path. |
| 0 | 1 | Jitter attenuator in the transmit path. |
| 1 | 0 | Jitter attenuator disabled. |
| 1 | 1 | Jitter attenuator disabled. |

Bit 1: T1J1E1 Selection (T1J1E1S). This bit configures the LIU for E1 or T1/J1 operation.

- 0 = E1
- 1 = T1 or J1

Bit 0: LOS Selection Criteria (LSC). This bit is used for LIU LOS selection criteria.

- E1 Mode**
- 0 = G.775
 - 1 = ETS 300 233

- T1/J1 Mode**
- 0 = T1.231
 - 1 = T1.231

Register Name: **LTIPSR**
 Register Description: **LIU Transmit Impedance and Pulse Shape Selection Register**
 Register Address: **1001h + (20h x (n - 1)) : where n = 1 to 8**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|-------|---------|--------|--------|---|----|----|----|
| Name | TG703 | TIMPTON | TIMPL1 | TIMPL0 | — | L2 | L1 | L0 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7: Transmit G.703 Synchronization Clock (TG703)

0 = Normal transmitter mode.

1 = G.703 2.048MHz clock transmitted on TTIPn and TRINGn.

Bit 6: Transmit Impedance On (TIMPTON)

0 = Disable transmit terminating impedance.

1 = Enable transmit terminating impedance.

Bits 5 and 4: Transmit Load Impedance 1 and 0 (TIMPL[1:0]). These bits are used to select the transmit load impedance. These must be set to match the cable impedance. Even if the Internal load impedance is turned off (via TIMPTOFF); the external cable impedance has to be specified for optimum operation. For J1 applications, use 110Ω. See [Table 10-18](#).

Bits 2 to 0: Line Build-Out Select 2 to 0 (L[2:0]). Used to select the transmit waveshape. The waveshape has a voltage level and load impedance associated with it once the T1/J1 or E1 selection is made by settings in the LTRCR register. See [Table 10-19](#).

Table 10-18. Transmit Load Impedance Selection

| TIMPL1 | TIMPLO | IMPEDANCE SELECTION |
|--------|--------|---------------------|
| 0 | 0 | 75Ω |
| 0 | 1 | 100Ω |
| 1 | 0 | 110Ω |
| 1 | 1 | 120Ω |

Table 10-19. Transmit Pulse Shape Selection

| L2 | L1 | L0 | MODE | IMPEDANCE | NOMINAL VOLTAGE |
|----|----|----|------|-----------|-----------------|
| 0 | 0 | 0 | E1 | 75Ω | 2.37V |
| 0 | 0 | 1 | E1 | 120Ω | 3.0V |

| L2 | L1 | L0 | MODE | CABLE LENGTH | MAX ALLOWED CABLE LOSS |
|----|----|----|-------|------------------------------------|------------------------|
| 0 | 0 | 0 | T1/J1 | DSX-1/0dB CSU, 0ft–133ft ABAM 100Ω | 0.6dB |
| 0 | 0 | 1 | T1/J1 | DSX-1, 133ft–266ft ABAM 100Ω | 1.2dB |
| 0 | 1 | 0 | T1/J1 | DSX-1, 266ft–399ft ABAM 100Ω | 1.8dB |
| 0 | 1 | 1 | T1/J1 | DSX-1, 399ft–533ft ABAM 100Ω | 2.4dB |
| 1 | 0 | 0 | T1/J1 | DSX-1, 533ft–655ft ABAM 100Ω | 3.0dB |
| 1 | 0 | 1 | T1/J1 | -7.5dB CSU | — |
| 1 | 1 | 0 | T1/J1 | -15dB CSU | — |
| 1 | 1 | 1 | T1/J1 | -22.5dB CSU | — |

Register Name: **LMCR**
 Register Description: **LIU Maintenance Control Register**
 Register Address: **1002h + (20h x (n - 1)) : where n = 1 to 8**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|------|-------|-----|-----|-----|------|------|----|
| Name | TAIS | ATAIS | LB2 | LB1 | LB0 | TPDE | RPDE | TE |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7: Manual Transmit AIS (TAIS). Alarm Indication Signal (AIS) is sent using MCLK as the reference clock. The transmit data coming from the framer is ignored.

0 = TAIS is disabled.

1 = Output an unframed all-ones pattern (AIS) at TTIPn and TRINGn.

Bit 6: Automatic Transmit AIS (ATAIS)

0 = ATAIS is disabled.

1 = Automatically transmit AIS on the occurrence of an LIU LOS.

Bits 5 to 3: Loopback Selection (LB[2:0]). See [Figure 9-28](#) for more details on each loopback.

| LB2 | LB1 | LB0 | Loopback Selection |
|-----|-----|-----|--|
| 0 | 0 | 0 | No loopback selected |
| 0 | 0 | 1 | Remote Loopback 2 (includes jitter attenuator) |
| 0 | 1 | 0 | Analog Loopback |
| 0 | 1 | 1 | Remote Loopback 1 (no jitter attenuator) |
| 1 | 0 | 0 | Local Loopback (includes jitter attenuator) |
| 1 | 0 | 1 | Dual Loopback—Remote Loopback 1 and Local Loopback (jitter attenuator is included in Local Loopback) |
| 1 | 1 | 0 | Reserved |
| 1 | 1 | 1 | Reserved |

Bit 2: Transmit Power-Down Enable (TPDE)

0 = Transmitter power enabled.

1 = Transmitter powered down. TTIPn/TRINGn outputs are high impedance.

Bit 1: Receiver Power-Down Enable (RPDE)

0 = Receiver power enabled.

1 = Receiver powered down.

Bit 0: Transmit Enable (TE). This function is overridden by the TXENABLE pin.

0 = TTIPn/TRINGn outputs are high impedance.

1 = TTIPn/TRINGn outputs enabled.

Register Name: **LRSR**
 Register Description: **LIU Real Status Register**
 Register Address: **1003h + (20h x (n - 1)) : where n = 1 to 8**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|---|-----|-----|------|------|-----|------|
| Name | — | — | OEQ | UEQ | RSCS | TSCS | OCS | LOSS |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 5: Over Equalized (OEQ). The equalizer is over equalized. This can happen if there very large unexpected resistive loss. This could result if monitor mode is used and the device is not placed in monitor mode. This indicator provides more qualitative information to the receive loss indicators.

Bit 4: Under Equalized (UEQ). The equalizer is under equalized. A signal with a very high resistive gain is being applied. This indicator provides more qualitative information to the receive loss indicators.

Bit 3: Receive Short-Circuit Status (RSCS). A real-time bit set when the LIU detects that the RTIPn and RRINGn inputs are short-circuited. The load resistance has to be 25Ω (typically) or less for short circuit detection.

Bit 2: Transmit Short-Circuit Status (TSCS). A real-time bit set when the LIU detects that the TTIPn and TRINGn outputs are short-circuited. The load resistance has to be 25Ω (typically) or less for short circuit detection.

Bit 1: Open-Circuit Status (OCS). A real-time bit that is set when the LIU detects that the TTIPn and TRINGn outputs are open-circuited.

Bit 0: Loss of Signal Status (LOSS). A real-time bit that is set when the LIU detects an LOS condition at RTIPn and RRINGn.

Register Name: **LSIMR**
 Register Description: **LIU Status Interrupt Mask Register**
 Register Address: **1004h + (20h x (n - 1)) : where n = 1 to 8**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---------|-------|-------|--------|---------|-------|-------|--------|
| Name | JALTCIM | OCCIM | SCCIM | LOSCIM | JALTSIM | OCDIM | SCDIM | LOSDIM |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7: Jitter Attenuator Limit Trip Clear Interrupt Mask (JALTCIM)

0 = Interrupt masked.
 1 = Interrupt enabled.

Bit 6: Open-Circuit Clear Interrupt Mask (OCCIM)

0 = Interrupt masked.
 1 = Interrupt enabled.

Bit 5: Short-Circuit Clear Interrupt Mask (SCCIM)

0 = Interrupt masked.
 1 = Interrupt enabled.

Bit 4: Loss of Signal Clear Interrupt Mask (LOSCIM)

0 = Interrupt masked.
 1 = Interrupt enabled.

Bit 3: Jitter Attenuator Limit Trip Set Interrupt Mask (JALTSIM)

0 = Interrupt masked.
 1 = Interrupt enabled.

Bit 2: Open-Circuit Detect Interrupt Mask (OCDIM)

0 = Interrupt masked.
 1 = Interrupt enabled.

Bit 1: Short-Circuit Detect Interrupt Mask (SCDIM)

0 = Interrupt masked.
 1 = Interrupt enabled.

Bit 0 : Loss of Signal Detect Interrupt Mask (LOSDIM)

0 = Interrupt masked.
 1 = Interrupt enabled.

Register Name: **LLSR**
 Register Description: **LIU Latched Status Register**
 Register Address: **1005h + (20h x (n - 1)) : where n = 1 to 8**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|-------|-----|-----|------|-------|-----|-----|------|
| Name | JALTC | OCC | SCC | LOSC | JALTS | OCD | SCD | LOSD |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Note: All bits in this register are latched and can create interrupts.

Bit 7: Jitter Attenuator Limit Trip Clear (JALTC). This latched bit is set when a JA limit trip condition was detected and then removed.

Bit 6: Open-Circuit Clear (OCC). This latched bit is set when an open circuit condition was detected at TTIPn and TRINGn and then removed.

Bit 5: Short-Circuit Clear (SCC). This latched bit is set when a short circuit condition was detected at TTIPn and TRINGn and then removed.

Bit 4: Loss of Signal Clear (LOSC). This latched bit is set when a loss of signal condition was detected at RTIPn and RRINGn and then removed.

Bit 3: Jitter Attenuator Limit Trip Set (JALTS). This latched bit is set when the jitter attenuator trip condition is detected.

Bit 2: Open-Circuit Detect (OCD). This latched bit is set when open-circuit condition is detected at TTIPn and TRINGn. This bit is not functional in T1 CSU operating modes (T1 LBO 5, LBO 6, and LBO 7).

Bit 1: Short-Circuit Detect (SCD). This latched bit is set when short-circuit condition is detected at TTIPn and TRINGn. This bit is not functional in T1 CSU operating modes (T1 LBO 5, LBO 6, and LBO 7).

Bit 0: Loss of Signal Detect (LOSD). This latched bit is set when an LOS condition is detected at RTIPn and RRINGn.

Register Name: **LRSL**
 Register Description: **LIU Receive Signal Level Register**
 Register Address: **1006h + (20h x (n - 1)) : where n = 1 to 8**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|------|------|------|------|---|---|---|---|
| Name | RSL3 | RSL2 | RLS1 | RLS0 | — | — | — | — |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 7 to 4: Receiver Signal Level 3 to 0 (RSL[3:0]). Real-time receive signal level as shown in [Table 10-20](#). Note that the range of signal levels reported the RSL[3:0] is limited by the Equalizer Gain Limit (EGL) in short-haul applications.

Table 10-20. Receive Level Indication

| RSL3 | RSL2 | RSL1 | RSL0 | RECEIVE LEVEL DS1/E1 (dB) |
|------|------|------|------|------------------------------|
| 0 | 0 | 0 | 0 | > -2.5 |
| 0 | 0 | 0 | 1 | -2.5 to -5 |
| 0 | 0 | 1 | 0 | -5 to -7.5 |
| 0 | 0 | 1 | 1 | -7.5 to -10 |
| 0 | 1 | 0 | 0 | -10 to -12.5 |
| 0 | 1 | 0 | 1 | -12.5 to -15 |
| 0 | 1 | 1 | 0 | -15 to -17.5 |
| 0 | 1 | 1 | 1 | -17.5 to -20 |
| 1 | 0 | 0 | 0 | -20 to -22.5 |
| 1 | 0 | 0 | 1 | -22.5 to 25 |
| 1 | 0 | 1 | 0 | -25 to -27.5 |
| 1 | 0 | 1 | 1 | -27.5 to -30 |
| 1 | 1 | 0 | 0 | -30 to -32.5 |
| 1 | 1 | 0 | 1 | -32.5 to -35 |
| 1 | 1 | 1 | 0 | -35 to -37.5 |
| 1 | 1 | 1 | 1 | < -37.5 |

Register Name: **LRISMR**
 Register Description: **LIU Receive Impedance and Sensitivity Monitor Register**
 Register Address: **1007h + (20h x (n - 1)) : where n = 1 to 8**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|--------|---|---|---|--------|--------|--------|
| Name | — | RIMPON | — | — | — | RIMPM2 | RIMPM1 | RIMPM0 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 6: Receive Internal Impedance Match On (RIMPON)

0 = Receive internal impedance termination is disabled (high impedance).

1 = Receive internal impedance termination is enabled.

Bits 2 to 0: Receive Impedance Selection (RIMPM[2:0]). These bits are used to select the receive impedance termination. They must be set according to the cable impedance even if internal termination resistance is disabled (RIMPON = 0). See [Table 10-21](#).

Table 10-21. Receive Impedance Selection

| RIMPON | RIMPRM[2:0] | RECEIVE IMPEDANCE SELECTED (Ω) |
|--------|-------------|--|
| 0 | x00 | 75 Ω external termination (<i>no internal impedance match</i>) |
| 0 | x01 | 100 Ω external termination (<i>no internal impedance match</i>) |
| 0 | x10 | 110 Ω external termination (<i>no internal impedance match</i>) |
| 0 | x11 | 120 Ω external termination (<i>no internal impedance match</i>) |
| 1 | 000 | 75 Ω , with external 120 Ω resistor |
| 1 | 001 | 100 Ω , with external 120 Ω resistor |
| 1 | 010 | 110 Ω , with external 120 Ω resistor |
| 1 | 011 | 120 Ω , with external 120 Ω resistor |
| 1 | 100 | 75 Ω internal termination |
| 1 | 101 | 100 Ω internal termination |
| 1 | 110 | 110 Ω internal termination |
| 1 | 111 | 120 Ω internal termination |

Register Name: **LRCR**
 Register Description: **LIU Receive Control Register**
 Register Address: **1008h + (20h x (n - 1)) : where n = 1 to 8**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|-------|---|---|---|-----|--------|-------|-------|
| Name | RG703 | — | — | — | RTR | RMONEN | RSMS1 | RSMS0 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7: Receive G.703 Clock (RG703). If this bit is set, the receiver expects a 2.048MHz or 1.544MHz clock from the RTIPn/RRINGn, based on the selection of T1 (1.544) or E1 (2.048) mode in the [LTRCR](#) register.

Bit 3: Receiver Turns Ratio (RTR)

0 = Receive transformer turns ratio is 1:1.

1 = Receive transformer turns ratio is 2:1. This option should only be used in short-haul applications.

Note: Internal impedance match is not available for this mode.

Bit 2: Receiver Monitor Mode Enable (RMONEN)

0 = Disable receive monitor mode.

1 = Enable receive monitor mode. Resistive gain is added with the maximum sensitivity. The receiver sensitivity is determined by RSMS1 and RSMS0.

Bits 1 and 0: Receiver Sensitivity/Monitor Gain Select (RSMS[1:0]). These bits are used to select the receiver sensitivity level and additional gain in monitoring applications. The monitor mode (RMONEN) adds resistive gain to compensate for the signal loss caused by the isolation resistors. See [Table 10-22](#) and [Table 10-23](#).

Table 10-22. Receiver Sensitivity Selection with Monitor Mode Disabled

| RMONEN | RSMS[1:0] | RECEIVER MONITOR MODE GAIN (dB) | RECEIVER SENSITIVITY (MAX CABLE LOSS ALLOWED) (dB) |
|--------|-----------|---------------------------------|--|
| 0 | 00 | 0 | 12 |
| 0 | 01 | 0 | 20 |
| 0 | 10 | 0 | 30 |
| 0 | 11 | 0 | 36 for T1; 43 for E1 |

Table 10-23. Receiver Sensitivity Selection with Monitor Mode Enabled

| RMONEN | RSMS[1:0] | RECEIVER MONITOR MODE GAIN (dB) | RECEIVER SENSITIVITY (MAX CABLE LOSS ALLOWED) (dB) |
|--------|-----------|---------------------------------|--|
| 1 | 00 | 14 | 30 |
| 1 | 01 | 20 | 22.5 |
| 1 | 10 | 26 | 17.5 |
| 1 | 11 | 32 | 12 |

10.6 BERT Register Definitions

Table 10-24. BERT Register Set

| ADDRESS | NAME | DESCRIPTION | R/W |
|---------|----------------------|---|-----|
| 1100h | BAWC | BERT Alternating Word Count Rate Register | R |
| 1101h | BRP1 | BERT Repetitive Pattern Set Register 1 | R/W |
| 1102h | BRP2 | BERT Repetitive Pattern Set Register 2 | R/W |
| 1103h | BRP3 | BERT Repetitive Pattern Set Register 3 | R/W |
| 1104h | BRP4 | BERT Repetitive Pattern Set Register 4 | R/W |
| 1105h | BC1 | BERT Control Register 1 | R/W |
| 1106h | BC2 | BERT Control Register 2 | R/W |
| 1107h | BBC1 | BERT Bit Count Register 1 | R |
| 1108h | BBC2 | BERT Bit Count Register 2 | R |
| 1109h | BBC3 | BERT Bit Count Register 3 | R |
| 110Ah | BBC4 | BERT Bit Count Register 4 | R |
| 110Bh | BEC1 | BERT Error Count Register 1 | R |
| 110Ch | BEC2 | BERT Error Count Register 2 | R |
| 110Dh | BEC3 | BERT Error Count Register 3 | R |
| 110Eh | BSR | BERT Status Register | R |
| 110Fh | BSIM | BERT Status Interrupt Mask Register | R/W |

Register Name: **BAWC**
 Register Description: **BERT Alternating Word Count Rate Register**
 Register Address: **1100h + (10h x (n - 1)) : where n = 1 to 8**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|-------|-------|-------|-------|-------|-------|-------|-------|
| Name | ACNT7 | ACNT6 | ACNT5 | ACNT4 | ACNT3 | ACNT2 | ACNT1 | ACNT0 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 7 to 0: Alternating Word Count Rate Bits 7 to 0 (ACNT[7:0]). When the BERT is programmed in the alternating word mode, the words will repeat for the count loaded into this register then flip to the other word and again repeat for the number of times loaded into this register. ACNT0 is the LSB of the 8-bit alternating word count rate counter.

Register Name: **BRP1**
 Register Description: **BERT Repetitive Pattern Set Register 1**
 Register Address: **1101h + (10h x (n - 1)) : where n = 1 to 8**

| | | | | | | | | |
|---------|-------|-------|-------|-------|-------|-------|-------|-------|
| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | RPAT7 | RPAT6 | RPAT5 | RPAT4 | RPAT3 | RPAT2 | RPAT1 | RPAT0 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 7 to 0: BERT Repetitive Pattern Set Bits 7 to 0 (RPAT[7:0]). RPAT0 is the LSB of the 32-bit repetitive pattern.

Register Name: **BRP2**
 Register Description: **BERT Repetitive Pattern Set Register 2**
 Register Address: **1102h + (10h x (n - 1)) : where n = 1 to 8**

| | | | | | | | | |
|---------|--------|--------|--------|--------|--------|--------|-------|-------|
| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | RPAT15 | RPAT14 | RPAT13 | RPAT12 | RPAT11 | RPAT10 | RPAT9 | RPAT8 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 7 to 0: BERT Repetitive Pattern Set Bits 15 to 8 (RPAT[15:8])

Register Name: **BRP3**
 Register Description: **BERT Repetitive Pattern Set Register 3**
 Register Address: **1103h + (10h x (n - 1)) : where n = 1 to 8**

| | | | | | | | | |
|---------|--------|--------|--------|--------|--------|--------|--------|--------|
| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | RPAT23 | RPAT22 | RPAT21 | RPAT20 | RPAT19 | RPAT18 | RPAT17 | RPAT16 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 7 to 0: BERT Repetitive Pattern Set Bits 23 to 16 (RPAT[23:16])

Register Name: **BRP4**
 Register Description: **BERT Repetitive Pattern Set Register 4**
 Register Address: **1104h + (10h x (n - 1)) : where n = 1 to 8**

| | | | | | | | | |
|---------|--------|--------|--------|--------|--------|--------|--------|--------|
| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | RPAT31 | RPAT30 | RPAT29 | RPAT28 | RPAT27 | RPAT26 | RPAT25 | RPAT24 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 7 to 0: BERT Repetitive Pattern Set Bits 31 to 24 (RPAT[31:24]). RPAT31 is the MSB of the 32-bit repetitive pattern.

Register Name: **BC1**
 Register Description: **BERT Control Register 1**
 Register Address: **1105h + (10h x (n - 1)) : where n = 1 to 8**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|----|------|------|-----|-----|-----|----|--------|
| Name | TC | TINV | RINV | PS2 | PS1 | PS0 | LC | RESYNC |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7: Transmit Pattern Load (TC). A low-to-high transition loads the pattern generator with the pattern that is to be generated. This bit should be toggled from low to high whenever the host wishes to load a new pattern. Must be cleared and set again for a subsequent loads.

Bit 6: Transmit Invert Data Enable (TINV)

- 0 = Do not invert the outgoing data stream.
- 1 = Invert the outgoing data stream.

Bit 5: Receive Invert Data Enable (RINV).

- 0 = Do not invert the incoming data stream.
- 1 = Invert the incoming data stream.

Bits 4 to 2: Pattern Select Bits 2 to 0 (PS[2:0]). These bits select data pattern used by the transmit and receive circuits. See [Table 10-25](#).

Table 10-25. BERT Pattern Select

| PS2 | PS1 | PS0 | PATTERN DEFINITION |
|-----|-----|-----|---|
| 0 | 0 | 0 | Pseudorandom 2E7-1. |
| 0 | 0 | 1 | Pseudorandom 2E11-1. |
| 0 | 1 | 0 | Pseudorandom 2E15-1. |
| 0 | 1 | 1 | Pseudorandom Pattern QRSS. A $2^{20} - 1$ pattern with 14 consecutive zero restriction. |
| 1 | 0 | 0 | Repetitive Pattern. |
| 1 | 0 | 1 | Alternating Word Pattern. |
| 1 | 1 | 0 | Modified 55 Octet (Daly) Pattern. The Daly pattern is a repeating 55 Octet pattern that is byte-aligned into the active DS0 time slots. The pattern is defined in an ATIS (Alliance for Telecommunications Industry Solutions) Committee T1 Technical Report Number 25 (November 1993). |
| 1 | 1 | 1 | Pseudorandom 2E-9-1. |

Bit 1: Load Bit and Error Counters (LC). A low-to-high transition latches the current bit and error counts into the registers BBC1, BBC2, BBC3, BBC4 and BEC1, BEC2, BEC3 and clears the internal count. This bit should be toggled from low to high whenever the host wishes to begin a new acquisition period. Must be cleared and set again for a subsequent loads.

Bit 0: Force Resynchronization (RESYNC). A low-to-high transition will force the receive BERT synchronizer to resynchronize to the incoming data stream. This bit should be toggled from low to high whenever the host wishes to acquire synchronization on a new pattern. Must be cleared and set again for a subsequent resynchronization.

Register Name: **BC2**
 Register Description: **BERT Control Register 2**
 Register Address: **1106h + (10h x (n - 1)) : where n = 1 to 8**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|------|------|------|-----|------|------|------|------|
| Name | EIB2 | EIB1 | EIB0 | SBE | RPL3 | RPL2 | RPL1 | RPL0 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 7 to 5: Error Insert Bits 2 to 0 (EIB[2:0]). Will automatically insert bit errors at the prescribed rate into the generated data pattern. Can be used for verifying error detection features. See [Table 10-26](#).

Table 10-26. BERT Error Insertion Rate

| EIB2 | EIB1 | EIB0 | ERROR RATE INSERTED |
|------|------|------|----------------------------------|
| 0 | 0 | 0 | No errors automatically inserted |
| 0 | 0 | 1 | 10E-1 |
| 0 | 1 | 0 | 10E-2 |
| 0 | 1 | 1 | 10E-3 |
| 1 | 0 | 0 | 10E-4 |
| 1 | 0 | 1 | 10E-5 |
| 1 | 1 | 0 | 10E-6 |
| 1 | 1 | 1 | 10E-7 |

Bit 4: Single Bit Error Insert (SBE). A low-to-high transition will create a single bit error. Must be cleared and set again for a subsequent bit error to be inserted.

Bits 3 to 0: Repetitive Pattern Length Select 3 to 0 (RPL[3:0]). RPL0 is the LSB and RPL3 is the MSB of a nibble that describes the how long the repetitive pattern is. The valid range is 17 (0000) to 32 (1111). These bits are ignored if the receive BERT is programmed for a pseudorandom pattern. To create repetitive patterns fewer than 17 bits in length, the user must set the length to an integer number of the desired length that is less than or equal to 32. For example, to create a 6-bit pattern, the user can set the length to 18 (0001) or to 24 (0111) or to 30 (1101). See [Table 10-27](#).

Table 10-27. BERT Repetitive Pattern Length Select

| LENGTH (BITS) | RPL3 | RPL2 | RPL1 | RPL0 |
|---------------|------|------|------|------|
| 17 | 0 | 0 | 0 | 0 |
| 18 | 0 | 0 | 0 | 1 |
| 19 | 0 | 0 | 1 | 0 |
| 20 | 0 | 0 | 1 | 1 |
| 21 | 0 | 1 | 0 | 0 |
| 22 | 0 | 1 | 0 | 1 |
| 23 | 0 | 1 | 1 | 0 |
| 24 | 0 | 1 | 1 | 1 |
| 25 | 1 | 0 | 0 | 0 |
| 26 | 1 | 0 | 0 | 1 |
| 27 | 1 | 0 | 1 | 0 |
| 28 | 1 | 0 | 1 | 1 |
| 29 | 1 | 1 | 0 | 0 |
| 30 | 1 | 1 | 0 | 1 |
| 31 | 1 | 1 | 1 | 0 |
| 32 | 1 | 1 | 1 | 1 |

Register Name: **BBC1**
 Register Description: **BERT Bit Count Register 1**
 Register Address: **$1107h + (10h \times (n - 1))$: where $n = 1$ to 8**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|------|------|------|------|------|------|------|------|
| Name | BBC7 | BBC6 | BBC5 | BBC4 | BBC3 | BBC2 | BBC1 | BBC0 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 7 to 0: BERT Bit Counter Bits 7 to 0 (BBC[7:0]). BBC0 is the LSB of the 32-bit counter.

Register Name: **BBC2**
 Register Description: **BERT Bit Count Register 2**
 Register Address: **$1108h + (10h \times (n - 1))$: where $n = 1$ to 8**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|-------|-------|-------|-------|-------|-------|------|------|
| Name | BBC15 | BBC14 | BBC13 | BBC12 | BBC11 | BBC10 | BBC9 | BBC8 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 7 to 0: BERT Bit Counter Bits 15 to 8 (BBC[15:8]).

Register Name: **BBC3**
 Register Description: **BERT Bit Count Register 3**
 Register Address: **$1109h + (10h \times (n - 1))$: where $n = 1$ to 8**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|-------|-------|-------|-------|-------|-------|-------|-------|
| Name | BBC23 | BBC22 | BBC21 | BBC20 | BBC19 | BBC18 | BBC17 | BBC16 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 7 to 0: BERT Bit Counter Bits 23 to 16 (BBC[23:16]).

Register Name: **BBC4**
 Register Description: **BERT Bit Count Register 4**
 Register Address: **$110Ah + (10h \times (n - 1))$: where $n = 1$ to 8**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|-------|-------|-------|-------|-------|-------|-------|-------|
| Name | BBC31 | BBC30 | BBC29 | BBC28 | BBC27 | BBC26 | BBC25 | BBC24 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 7 to 0: BERT Bit Counter Bits 31 to 24 (BBC[31:24]). BBC31 is the MSB of the 32-bit counter.

Register Name: **BEC1**
 Register Description: **BERT Error Count Register 1**
 Register Address: **110Bh + (10h x (n - 1)) : where n = 1 to 8**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|-----|-----|-----|-----|-----|-----|-----|-----|
| Name | EC7 | EC6 | EC5 | EC4 | EC3 | EC2 | EC1 | EC0 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 7 to 0: Error Counter Bits 7 to 0 (EC[7:0]). EC0 is the LSB of the 24-bit counter.

Register Name: **BEC2**
 Register Description: **BERT Error Count Register 2**
 Register Address: **110Ch + (10h x (n - 1)) : where n = 1 to 8**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|------|------|------|------|------|------|-----|-----|
| Name | EC15 | EC14 | EC13 | EC12 | EC11 | EC10 | EC9 | EC8 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 7 to 0: Error Counter Bits 15 to 8 (EC[15:8])

Register Name: **BEC3**
 Register Description: **BERT Error Count Register 3**
 Register Address: **110Dh + (10h x (n - 1)) : where n = 1 to 8**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|------|------|------|------|------|------|------|------|
| Name | EC23 | EC22 | EC21 | EC20 | EC19 | EC18 | EC17 | EC16 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 7 to 0: Error Counter Bits 23 to 16 (EC[23:16]). EC23 is the MSB of the 24-bit counter.

Register Name: **BSR**
 Register Description: **BERT Status Register**
 Register Address: **110Eh + (10h x (n - 1)) : where n = 1 to 8**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|------|-------|-------|------|------|-------|-------|
| Name | — | BBED | RBA01 | RSYNC | BRA1 | BRA0 | BRLOS | BSYNC |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Note: All latched bits in this register can create interrupts.

Bit 6: BERT Bit Error Detected Event (BBED). A latched bit that is set when a bit error is detected. The receive BERT must be in synchronization for it to detect bit errors.

Bit 5: Real-Time BERT All Zeros or All Ones (RBA01). ORed real-time status of all-zeros detection and all-ones detection.

Bit 4: Real-Time Sync (RSYNC). Real-time sync status. A zero indicates not synchronized; a one indicates synchronization state.

Bit 3: BERT Receive All-Ones Condition (BRA1). A latched bit that is set when 32 consecutive ones are received.

Bit 2: BERT Receive All-Zeros Condition (BRA0). A latched bit that is set when 32 consecutive zeros are received.

Bit 1: BERT Receive Loss of Synchronization Condition (BRLOS). A latched bit that is set whenever the receive BERT begins searching for a pattern.

Bit 0: BERT in Synchronization Condition (BSYNC). A latched bit that is set when the incoming pattern matches for 32 consecutive bit positions.

Register Name: **BSIM**
 Register Description: **BERT Status Interrupt Mask Register**
 Register Address: **110Fh + (10h x (n - 1)) : where n = 1 to 8**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|------|---|---|------|------|-------|-------|
| Name | — | BBED | — | — | BRA1 | BRA0 | BRLOS | BSYNC |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 6: BERT Bit Error Detected Event (BBED)

0 = Interrupt masked.
 1 = Interrupt enabled.

Bit 3: BERT Receive All-Ones Condition (BRA1)

0 = Interrupt masked.
 1 = Interrupt enabled—interrupts on rising and falling edges.

Bit 2: BERT Receive All-Zeros Condition (BRA0)

0 = Interrupt masked.
 1 = Interrupt enabled—interrupts on rising and falling edges.

Bit 1: BERT Receive Loss of Synchronization Condition (BRLOS)

0 = Interrupt masked.
 1 = Interrupt enabled—interrupts on rising and falling edges.

Bit 0: BERT in Synchronization Condition (BSYNC)

0 = Interrupt masked.
 1 = Interrupt enabled—interrupts on rising and falling edges.

10.6.1 Extended BERT Register Definitions

Table 10-28. Extended BERT Register Set

| ADDRESS | NAME | DESCRIPTION | R/W |
|---------|-----------------------|---------------------------------------|-----|
| 1400h | BC3 | BERT Control Register 3 | R/W |
| 1401h | BRSR | BERT Real-Time Status Register | R |
| 1402h | BLSR1 | BERT Latched Status Register 1 | R/W |
| 1403h | BSIM1 | BERT Status Interrupt Mask Register 1 | R/W |
| 1404h | BLSR2 | BERT Latched Status Register 2 | R/W |
| 1405h | BSIM2 | BERT Status Interrupt Mask Register 2 | R/W |

Register Name: **BC3**
 Register Description: **BERT Control Register 3**
 Register Address: **1400h + (10h x (n - 1)) : where n = 1 to 8**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|---|---|---|---|---|-------|--------|
| Name | — | — | — | — | — | — | 55OCT | BALIGN |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 1: 55 Octet Pattern (55OCT). This bit selects data pattern used by the transmit and receive circuits.
 0 = 55 Octet pattern disabled.
 1 = 55 Octet pattern enabled, when modified 55 Octet (Daly) pattern is selected by [BC1](#).PSn register bits.

Bit 0: Byte Alignment to DS0 Boundary (BALIGN). A low-to-high transition causes the transmit BERT pattern to be byte-aligned to the DS0 boundary. This bit should be toggled from low to high when a pattern load is executed ([BC1](#).TC).

Register Name: **BRSR**
 Register Description: **BERT Real-Time Status Register**
 Register Address: **1401h + (10h x (n - 1)) : where n = 1 to 8**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|---|---|---|------|------|-------|-------|
| Name | — | — | — | — | BRA1 | BRA0 | BRLOS | BSYNC |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 3: BERT Receive All-Ones Condition (BRA1). This bit is set when 32 consecutive ones are received and clears when at least one “zero” is received.

Bit 2: BERT Receive All-Zeros Condition (BRA0). This bit is set when 32 consecutive zeros are received and clears when at least one “one” is received.

Bit 1: BERT Receive Loss of Synchronization Condition (BRLOS). This bit is set whenever the receive BERT begins searching for a pattern and clears when BERT enters SYNC condition.

Bit 0: BERT in Synchronization Condition (BSYNC). This bit is set when the incoming pattern matches for 32 consecutive bit positions and remains set until the BERT enters loss of synchronization condition.

Register Name: **BLSR1**
 Register Description: **BERT Latched Status Register 1**
 Register Address: **1402h + (10h x (n - 1)) : where n = 1 to 8**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|-------|-------|--------|--------|-------|-------|--------|--------|
| Name | BRA1C | BRA0C | BRLOSC | BSYNCC | BRA1D | BRA0D | BRLOSD | BSYNCD |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Note: All latched bits in this register can create interrupts.

Bit 7: BERT Receive All-Ones Condition Clear (BRA1C). A latched bit that is set when the BERT transitions out of all-ones condition.

Bit 6: BERT Receive All-Zeros Condition Clear (BRA0C). A latched bit that is set when the BERT transitions out of all-zeros condition.

Bit 5: BERT Receive Loss of Synchronization Condition Clear (BRLOSC). A latched bit that is set when the BERT transitions out of loss of synchronization condition.

Bit 4: BERT in Synchronization Condition Clear (BSYNCC). A latched bit that is set when the BERT transitions out of synchronization condition.

Bit 3: BERT Receive All-Ones Condition Detect (BRA1D). A latched bit that is set when 32 consecutive ones are received.

Bit 2: BERT Receive All-Zeros Condition Detect (BRA0D). A latched bit that is set when 32 consecutive zeros are received.

Bit 1: BERT Receive Loss of Synchronization Condition Detect (BRLOSD). A latched bit that is set whenever the receive BERT begins searching for a pattern.

Bit 0: BERT in Synchronization Condition Detect (BSYNCD). A latched bit that is set when the incoming pattern matches for 32 consecutive bit positions.

Register Name: **BSIM1**
 Register Description: **BERT Status Interrupt Mask Register 1**
 Register Address: **1403h + (10h x (n - 1)) : where n = 1 to 8**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|-------|-------|--------|--------|-------|-------|--------|--------|
| Name | BRA1C | BRA0C | BRLOSC | BSYNCC | BRA1D | BRA0D | BRLOSD | BSYNCD |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7: Receive All-Ones Condition Clear (BRA1C)

0 = interrupt masked
 1 = interrupt enabled

Bit 6: Receive All-Zeros Condition Clear (BRA0C)

0 = interrupt masked
 1 = interrupt enabled

Bit 5: Receive Loss of Synchronization Condition Clear (BRLOSC)

0 = interrupt masked
 1 = interrupt enabled

Bit 4: BERT in Synchronization Condition Clear (BSYNCC)

0 = interrupt masked
 1 = interrupt enabled

Bit 3: Receive All-Ones Condition Detect (BRA1D)

0 = interrupt masked
 1 = interrupt enabled

Bit 2: Receive All-Zeros Condition Detect (BRA0D)

0 = interrupt masked
 1 = interrupt enabled

Bit 1: Receive Loss of Synchronization Condition Detect (BRLOSD)

0 = interrupt masked
 1 = interrupt enabled

Bit 0 : BERT in Synchronization Condition Detect (BSYNCD)

0 = interrupt masked
 1 = interrupt enabled

Register Name: **BLSR2**
 Register Description: **BERT Latched Status Register 2**
 Register Address: **1404h + (10h x (n - 1)) : where n = 1 to 8**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|---|---|---|---|-----|------|------|
| Name | — | — | — | — | — | BED | BBCO | BECO |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Note: All latched bits in this register can create interrupts.

Bit 2: BERT Bit Error Detected Event (BED). A latched bit that is set when a bit error is detected. The receive BERT must be in synchronization for it to detect bit errors.

Bit 1: BERT Bit Counter Overflow Event (BBCO). A latched bit that is set when the 32-bit BERT bit counter (BBC) overflows.

Bit 0: BERT Error Counter Overflow Event (BECO). A latched bit that is set when the 24-bit BERT error counter (BEC) overflows.

Register Name: **BSIM2**
 Register Description: **BERT Status Interrupt Mask Register 2**
 Register Address: **1405h + (10h x (n - 1)) : where n = 1 to 8**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|---|---|---|---|-----|------|------|
| Name | — | — | — | — | — | BED | BBCO | BECO |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 2: Bit Error Detected Event (BED)

0 = interrupt masked
 1 = interrupt enabled

Bit 1: BERT Bit Counter Overflow Event (BBCO)

0 = interrupt masked
 1 = interrupt enabled

Bit 0: BERT Error Counter Overflow Event (BECO)

0 = interrupt masked
 1 = interrupt enabled

10.7 HDLC-256 Register Definitions

10.7.1 Transmit HDLC-256 Register Definitions

Table 10-29. Transmit-Side HDLC-256 Register Set

| ADDRESS | NAME | DESCRIPTION | R/W |
|---------|---------------------------|--|-----|
| 1500h | TH256CR1 | Transmit HDLC-256 Control Register 1 | R/W |
| 1501h | TH256CR2 | Transmit HDLC-256 Control Register 2 | R/W |
| 1502h | TH256FDR1 | Transmit HDLC-256 FIFO Data Register 1 | R/W |
| 1503h | TH256FDR2 | Transmit HDLC-256 FIFO Data Register 2 | R/W |
| 1504h | TH256SR1 | Transmit HDLC-256 Status Register 1 | R |
| 1505h | TH256SR2 | Transmit HDLC-256 Status Register 2 | R |
| 1506h | TH256SRL | Transmit HDLC-256 Status Register Latched | R/W |
| 1507h | — | Reserved | — |
| 1508h | TH256SRIE | Transmit HDLC-256 Status Register Interrupt Enable | R/W |
| 1509h | — | Reserved | — |
| 150Ah | — | Reserved | — |
| 150Bh | — | Reserved | — |
| 150Ch | — | Reserved | — |
| 150Dh | — | Reserved | — |
| 150Eh | — | Reserved | — |
| 150Fh | — | Reserved | — |

Register Name: **TH256CR1**
 Register Description: **Transmit HDLC-256 Control Register 1**
 Register Address: **1500h + (20h x (n - 1)) : where n = 1 to 8**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|------|------|------|------|------|------|-------|
| Name | — | TPSD | TFEI | TIFV | TBRE | TDIE | TFPD | TFRST |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 6: Transmit Packet Start Disable (TPSD). When 0, the transmit packet processor continues sending packets after the current packet end. When 1, the transmit packet processor stops sending packets after the current packet end.

Bit 5: Transmit FCS Error Insertion (TFEI). When 0, the calculated FCS (inverted CRC-16) is appended to the packet. When 1, the inverse of the calculated FCS (noninverted CRC-16) is appended to the packet causing a FCS error. This bit is ignored if transmit FCS processing is disabled (TFPD = 1).

Bit 4: Transmit Interframe Fill Value (TIFV). When 0, interframe fill is done with the flag sequence (7Eh). When 1, interframe fill is done with all ones.

Bit 3: Transmit Bit Reordering Enable (TBRE). When 0, bit reordering is disabled. (The first bit transmitted is the LSB of the transmit FIFO data byte TFD[0]). When 1, bit reordering is enabled. (The first bit transmitted is the MSB of the transmit FIFO data byte TFD[7]).

Bit 2: Transmit Data Inversion Enable (TDIE). When 0, the outgoing data is directly output from packet processing. When 1, the outgoing data is inverted before being output from packet processing.

Bit 1: Transmit FCS Processing Disable (TFPD). This bit controls whether a FCS is calculated and appended to the end of each packet. When 0, the calculated FCS bytes are appended to the end of the packet. When 1, the packet is transmitted without a FCS.

Bit 0: Transmit FIFO Reset (TFRST). When 0, the transmit FIFO resumes normal operations, however, data is discarded until a start of packet is received after RAM power-up is completed. When 1, the transmit FIFO is emptied, any transfer in progress is halted, the FIFO RAM is powered down, and all incoming data is discarded (all TFDR register writes are ignored).

Register Name: **TH256CR2**
 Register Description: **Transmit HDLC-256 Control Register 2**
 Register Address: **1501h + (20h x (n - 1)) : where n = 1 to 8**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|---|---|-------|-------|-------|-------|-------|
| Name | — | — | — | TDAL4 | TDAL3 | TDAL2 | TDAL1 | TDAL0 |
| Default | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |

Bits 4 to 0: Transmit HDLC-256 Data Storage Available Level (TDAL[4:0]). These five bits indicate the minimum number of bytes ($[TDAL \times 8] + 1$) that must be available for storage (do not contain data) in the transmit FIFO for HDLC-256 data storage to be available. For example, a value of 21 (15h) results in HDLC-256 data storage being available (THDA = 1) when the transmit FIFO has 169 (A9h) bytes or more available for storage, and HDLC-256 data storage not being available (THDA = 0) when the transmit FIFO has 168 (A8h) bytes or less available for storage. Default value (after reset) is 128 bytes minimum available.

Register Name: **TH256FDR1**
 Register Description: **Transmit HDLC-256 FIFO Data Register 1**
 Register Address: **1502h + (20h x (n - 1)) : where n = 1 to 8**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|---|---|---|---|---|---|------|
| Name | — | — | — | — | — | — | — | TDPE |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 0: Transmit FIFO Data Packet End (TDPE). When 0, the transmit FIFO data is not a packet end. When 1, the transmit FIFO data is a packet end. This bit should be written before the last byte of the packet is written into TH256FDR2.

Register Name: **TH256FDR2**
 Register Description: **Transmit HDLC-256 FIFO Data Register 2**
 Register Address: **1503h + (20h x (n - 1)) : where n = 1 to 8**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|------|------|------|------|------|------|------|------|
| Name | TFD7 | TFD6 | TFD5 | TFD4 | TFD3 | TFD2 | TFD1 | TFD0 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Note: When read, the value of these bits is always zero.

Bits 7 to 0: Transmit FIFO Data (TFD[7:0]). These eight bits are the packet data to be stored in the transmit FIFO. TFD[7] is the MSB, and TFD[0] is the LSB. If bit reordering is disabled, TFD[0] is the first bit transmitted, and TFD[7] is the last bit transmitted. If bit reordering is enabled, TFD[7] is the first bit transmitted, and TFD[0] is the last bit transmitted.

Register Name: **TH256SR1**
 Register Description: **Transmit HDLC-256 Status Register 1**
 Register Address: **1504h + (20h x (n - 1)) : where n = 1 to 8**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|---|---|---|---|-----|-----|------|
| Name | — | — | — | — | — | TFF | TFE | THDA |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 2: Transmit FIFO Full (TFF). When 0, the transmit FIFO contains 255 or less bytes of data. When 1, the transmit FIFO is full.

Bit 1: Transmit FIFO Empty (TFE). When 0, the transmit FIFO contains at least one byte of data. When 1, the transmit FIFO is empty.

Bit 0: Transmit HDLC-256 Data Storage Available (THDA). When 0, the transmit FIFO has less storage space available in the transmit FIFO than the transmit HDLC-256 data storage available level (TDAL[4:0]). When 1, the transmit FIFO has the same or more storage space available than the transmit FIFO HDLC-256 data storage available level.

Register Name: **TH256SR2**
 Register Description: **Transmit HDLC-256 Status Register 2**
 Register Address: **1505h + (20h x (n - 1)) : where n = 1 to 8**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|---|-------|-------|-------|-------|-------|-------|
| Name | — | — | TFFL5 | TFFL4 | TFFL3 | TFFL2 | TFFL1 | TFFL0 |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 5 to 0: Transmit FIFO Fill Level (TFFL[5:0]). These six bits indicate the number of eight byte groups available for storage (do not contain data) in the transmit FIFO, e.g., a value of 21 (15h) indicates the FIFO has 168 (A8h) to 175 (AFh) bytes are available for storage.

Register Name: **TH256SRL**
 Register Description: **Transmit HDLC-256 Status Register Latched**
 Register Address: **1506h + (20h x (n - 1)) : where n = 1 to 8**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|---|------|------|------|---|------|-------|
| Name | — | — | TFOL | TFUL | TPEL | — | TFEL | THDAL |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 5: Transmit FIFO Overflow Latched (TFOL). This bit is set when a transmit FIFO overflow condition occurs.

Bit 4: Transmit FIFO Underflow Latched (TFUL). This bit is set when a transmit FIFO underflow condition occurs. An underflow condition results in a loss of data.

Bit 3: Transmit Packet End Latched (TPEL). This bit is set when an end of packet is read from the transmit FIFO.

Bit 1: Transmit FIFO Empty Latched (TFEL). This bit is set when the TFE bit transitions from 0 to 1. **Note:** This bit is also set when TH256CR1.TFRST is deasserted.

Bit 0: Transmit HDLC-256 Data Available Latched (THDAL). This bit is set when the THDA bit transitions from 0 to 1. **Note:** This bit is also set when TH256CR1.TFRST is deasserted.

Register Name: **TH256SRIE**
 Register Description: **Transmit HDLC-256 Status Register Interrupt Enable**
 Register Address: **1508h + (20h x (n-1)) : where n = 1 to 8**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|---|-------|-------|-------|---|-------|--------|
| Name | — | — | TFOIE | TFUIE | TPEIE | — | TFEIE | THDAIE |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 5: Transmit FIFO Overflow Interrupt Enable (TFOIE). This bit enables an interrupt if the TFOL bit is set.

0 = interrupt disabled

1 = interrupt enabled

Bit 4: Transmit FIFO Underflow Interrupt Enable (TFUIE). This bit enables an interrupt if the TFUL bit is set.

0 = interrupt disabled

1 = interrupt enabled

Bit 3: Transmit Packet End Interrupt Enable (TPEIE). This bit enables an interrupt if the TPEL bit is set.

0 = interrupt disabled

1 = interrupt enabled

Bit 1: Transmit FIFO Empty Interrupt Enable (TFEIE). This bit enables an interrupt if the TFEL bit is set.

0 = interrupt disabled

1 = interrupt enabled

Bit 0: Transmit HDLC-256 Data Available Interrupt Enable (THDAIE). This bit enables an interrupt if the THDAL bit is set.

0 = interrupt disabled

1 = interrupt enabled

10.7.2 Receive HDLC-256 Register Definitions

Table 10-30. Receive-Side HDLC-256 Register Set

| ADDRESS | NAME | DESCRIPTION | R/W |
|---------|---------------------------|---|-----|
| 1510h | RH256CR1 | Receive HDLC-256 Control Register 1 | R/W |
| 1511h | RH256CR2 | Receive HDLC-256 Control Register 2 | R/W |
| 1512h | — | Reserved | — |
| 1513h | — | Reserved | — |
| 1514h | RH256SR | Receive HDLC-256 Status Register | R |
| 1515h | — | Reserved | — |
| 1516h | RH256SRL | Receive HDLC-256 Status Register Latched | R/W |
| 1517h | — | Reserved | — |
| 1518h | RH256SRIE | Receive HDLC-256 Status Register Interrupt Enable | R/W |
| 1519h | — | Reserved | — |
| 151Ah | — | Reserved | — |
| 151Bh | — | Reserved | — |
| 151Ch | RH256FDR1 | Receive HDLC-256 FIFO Data Register 1 | R |
| 151Dh | RH256FDR2 | Receive HDLC-256 FIFO Data Register 2 | R |
| 151Eh | — | Reserved | — |
| 151Fh | — | Reserved | — |

Register Name: **RH256CR1**
 Register Description: **Receive HDLC-256 Control Register 1**
 Register Address: **1510h + (20h x (n - 1)) : where n = 1 to 8**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|---|---|---|------|------|------|-------|
| Name | — | — | — | — | RBRE | RDIE | RFPD | RFRST |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 3: Receive Bit Reordering Enable (RBRE). When 0, bit reordering is disabled. (The first bit received is in the LSB of the receive FIFO data byte RFD[0].) When 1, bit reordering is enabled. (The first bit received is in the MSB of the receive FIFO Data byte RFD[7].)

Bit 2: Receive Data Inversion Enable (RDIE). When 0, the incoming data is directly passed on for packet processing. When 1, the incoming data is inverted before being passed on for packet processing.

Bit 1: Receive FCS Processing Disable (RFPD). When 0, FCS processing is performed (the packets have a FCS appended). When 1, FCS processing is disabled (the packets do not have a FCS appended).

Bit 0: Receive FIFO Reset (RFRST). When 0, the receive FIFO resumes normal operations, however, data is discarded until a start of packet is received after RAM power-up is completed. When 1, the receive FIFO is emptied, any transfer in progress is halted, the FIFO RAM is powered down, the RHDA bit is forced low, and all incoming data is discarded.

Register Name: **RH256CR2**
 Register Description: **Receive HDLC-256 Control Register 2**
 Register Address: **1511h+ (20h x (n - 1)) : where n = 1 to 8**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|---|---|-------|-------|-------|-------|-------|
| Name | — | — | — | RDAL4 | RDAL3 | RDAL2 | RDAL1 | RDAL0 |
| Default | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |

Bits 4 to 0: Receive HDLC-256 Data Available Level (RDAL[4:0]). These five bits indicate the minimum number of eight byte groups that must be stored (contain data) in the receive FIFO before HDLC-256 data is considered to be available (RHDA = 1). For example, a value of 21 (15h) results in HDLC-256 data being available when the receive FIFO contains 168 (A8h) bytes or more.

Register Name: **RH256SR**
 Register Description: **Receive HDLC-256 Status Register**
 Register Address: **1514h+ (20h x (n - 1)) : where n = 1 to 8**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|---|---|---|---|-----|-----|------|
| Name | — | — | — | — | — | RFF | RFE | RHDA |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 2: Receive FIFO Full (RFF). When 0, the receive FIFO contains 255 or less bytes of data. When 1, the receive FIFO is full.

Bit 1: Receive FIFO Empty (RFE). When 0, the receive FIFO contains at least one byte of data. When 1, the receive FIFO is empty.

Bit 0: Receive HDLC-256 Data Available (RHDA). When 0, the receive FIFO contains less data than the receive HDLC-256 data available level (RDAL[4:0]). When 1, the receive FIFO contains the same or more data than the receive HDLC-145 data available level.

Register Name: **RH256SRL**
 Register Description: **Receive HDLC-256 Status Register Latched**
 Register Address: **1516h + (20h x (n - 1)) : where n = 1 to 8**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|------|---|---|------|------|------|---|-------|
| Name | RFOL | — | — | RPEL | RPSL | RFFL | — | RHDAL |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7: Receive FIFO Overflow Latched (RFOL). This bit is set when a receive FIFO overflow condition occurs. An overflow condition results in a loss of data.

Bit 4: Receive Packet End Latched (RPEL). This bit is set when an end of packet is stored in the receive FIFO.

Bit 3: Receive Packet Start Latched (RPSL). This bit is set when a start of packet is stored in the receive FIFO.

Bit 2: Receive FIFO Full Latched (RFFL). This bit is set when the RFF bit transitions from 0 to 1.

Bit 0: Receive HDLC-256 Data Available Latched (RHDAL). This bit is set when the RHDA bit transitions from 0 to 1.

Register Name: **RH256SRIE**
 Register Description: **Receive HDLC-256 Status Register Interrupt Enable**
 Register Address: **1518h + (20h x (n - 1)) : where n = 1 to 8**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|-------|---|---|-------|-------|-------|---|--------|
| Name | RFOIE | — | — | RPEIE | RPSIE | RFFIE | — | RHDAIE |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 7: Receive FIFO Overflow Interrupt Enable (RFOIE). This bit enables an interrupt if the RFOL bit is set.
 0 = interrupt disabled
 1 = interrupt enabled

Bit 4: Receive Packet End Interrupt Enable (RPEIE). This bit enables an interrupt if the RPEL bit is set.
 0 = interrupt disabled
 1 = interrupt enabled

Bit 3: Receive Packet Start Interrupt Enable (RPSIE). This bit enables an interrupt if the RPSL bit is set.
 0 = interrupt disabled
 1 = interrupt enabled

Bit 2: Receive FIFO Full Interrupt Enable (RFFIE). This bit enables an interrupt if the RFFL bit is set.
 0 = interrupt disabled
 1 = interrupt enabled

Bit 0: Receive HDLC-256 Data Available Interrupt Enable (RHDAIE). This bit enables an interrupt if the RHDAL bit is set and.
 0 = interrupt disabled
 1 = interrupt enabled

Register Name: **RH256FDR1**
 Register Description: **Receive HDLC-256 FIFO Data Register 1**
 Register Address: **151Ch + (20h x (n - 1)) : where n = 1 to 8**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|---|---|---|------|------|------|------|
| Name | — | — | — | — | RPS2 | RPS1 | RPS0 | RFDV |
| Default | 0 | 0 | 0 | 0 | X | X | X | 0 |

Note: The FIFO data and status are updated when the receive FIFO data (RH256FDR2.RFD[7:0]) is read. Reading this register reflects the status of the next read of RH256FDR2.

Bits 3 to 1: Receive Packet Status (RPS[2:0]). These three bits indicate the status of the received packet and packet data.

- 000 = packet middle
- 001 = packet start
- 010 = reserved
- 011 = reserved
- 100 = packet end: good packet
- 101 = packet end: FCS errored packet
- 110 = packet end: invalid packet (a noninteger number of bytes)
- 111 = packet end: aborted packet

Bit 0: Receive FIFO Data Valid (RFDV). When 0, the receive FIFO data (RFD[7:0]) is invalid (the receive FIFO is empty). When 1, the receive FIFO data (RFD[7:0]) is valid.

Register Name: **RH256FDR2**
 Register Description: **Receive HDLC-256 FIFO Data Register 2**
 Register Address: **151Dh + (20h x (n - 1)) : where n = 1 to 8**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|------|------|------|------|------|------|------|------|
| Name | RFD7 | RFD6 | RFD5 | RFD4 | RFD3 | RFD2 | RFD1 | RFD0 |
| Default | X | X | X | X | X | X | X | X |

Note: Reading this register when RH256FDR1.RFDV = 0 can result in a loss of data.

Bits 7 to 0: Receive FIFO Data (RFD[7:0]). These eight bits are the packet data stored in the receive FIFO. RFD[7] is the MSB, and RFD[0] is the LSB. If bit reordering is disabled, RFD[0] is the first bit received, and RFD[7] is the last bit received. If bit reordering is enabled, RFD[7] is the first bit received, and RFD[0] is the last bit received.

11. FUNCTIONAL TIMING

11.1 T1 Receiver Functional Timing Diagrams

Figure 11-1. T1 Receive-Side D4 Timing



Figure 11-2. T1 Receive-Side ESF Timing

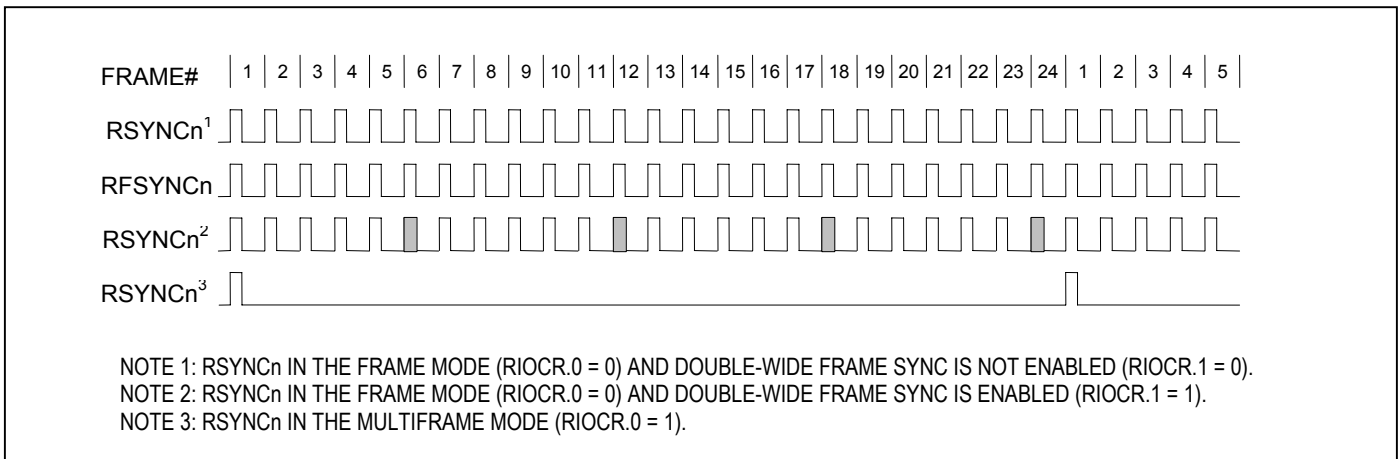


Figure 11-3. T1 Receive-Side Boundary Timing (Elastic Store Disabled)

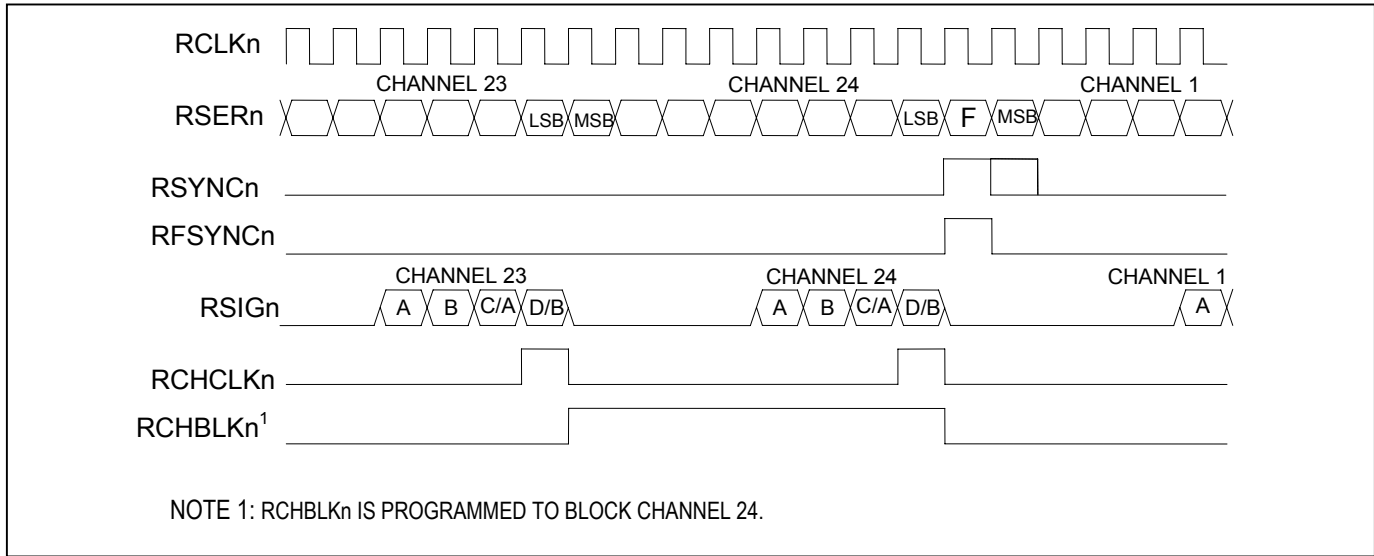


Figure 11-4. T1 Receive-Side 1.544MHz Boundary Timing (Elastic Store Enabled)



Figure 11-5. T1 Receive-Side 2.048MHz Boundary Timing (Elastic Store Enabled)

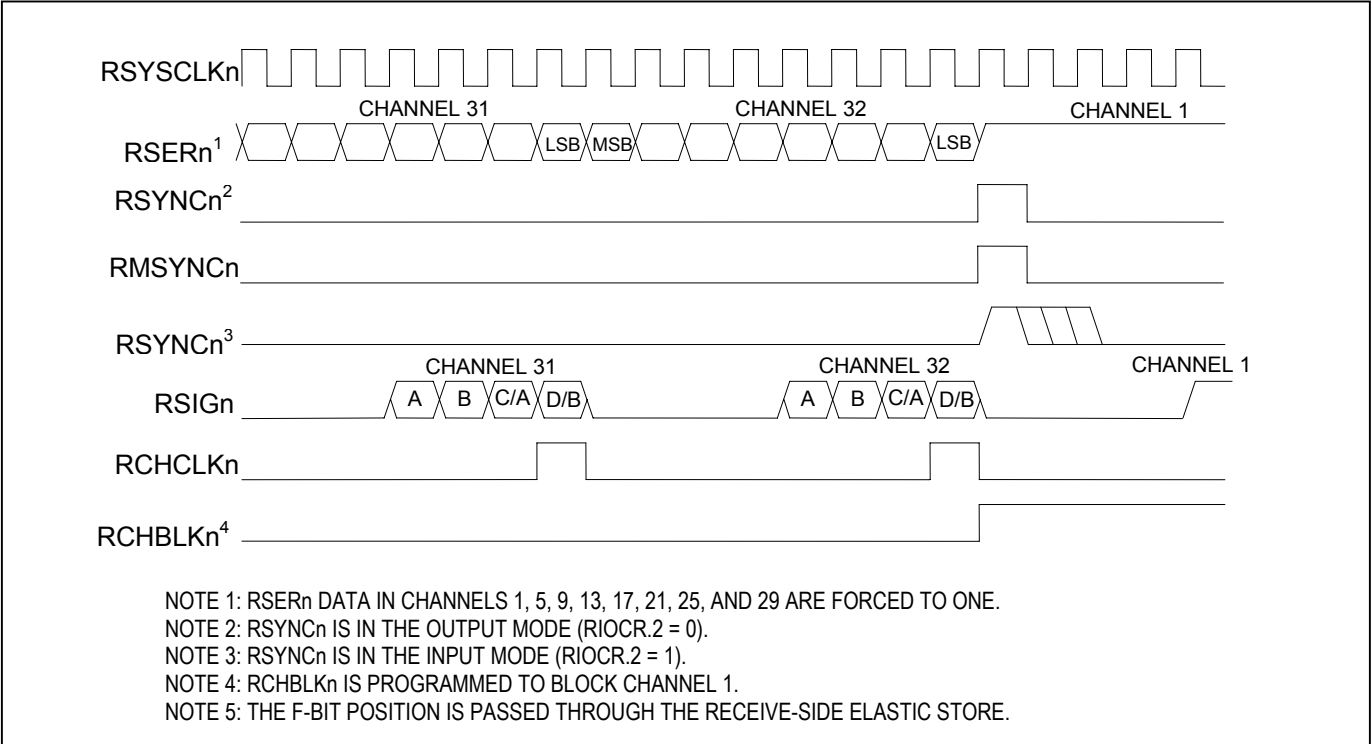


Figure 11-6. T1 Receive-Side Interleave Bus Operation—BYTE Mode



Figure 11-7. T1 Receive-Side Interleave Bus Operation—FRAME Mode

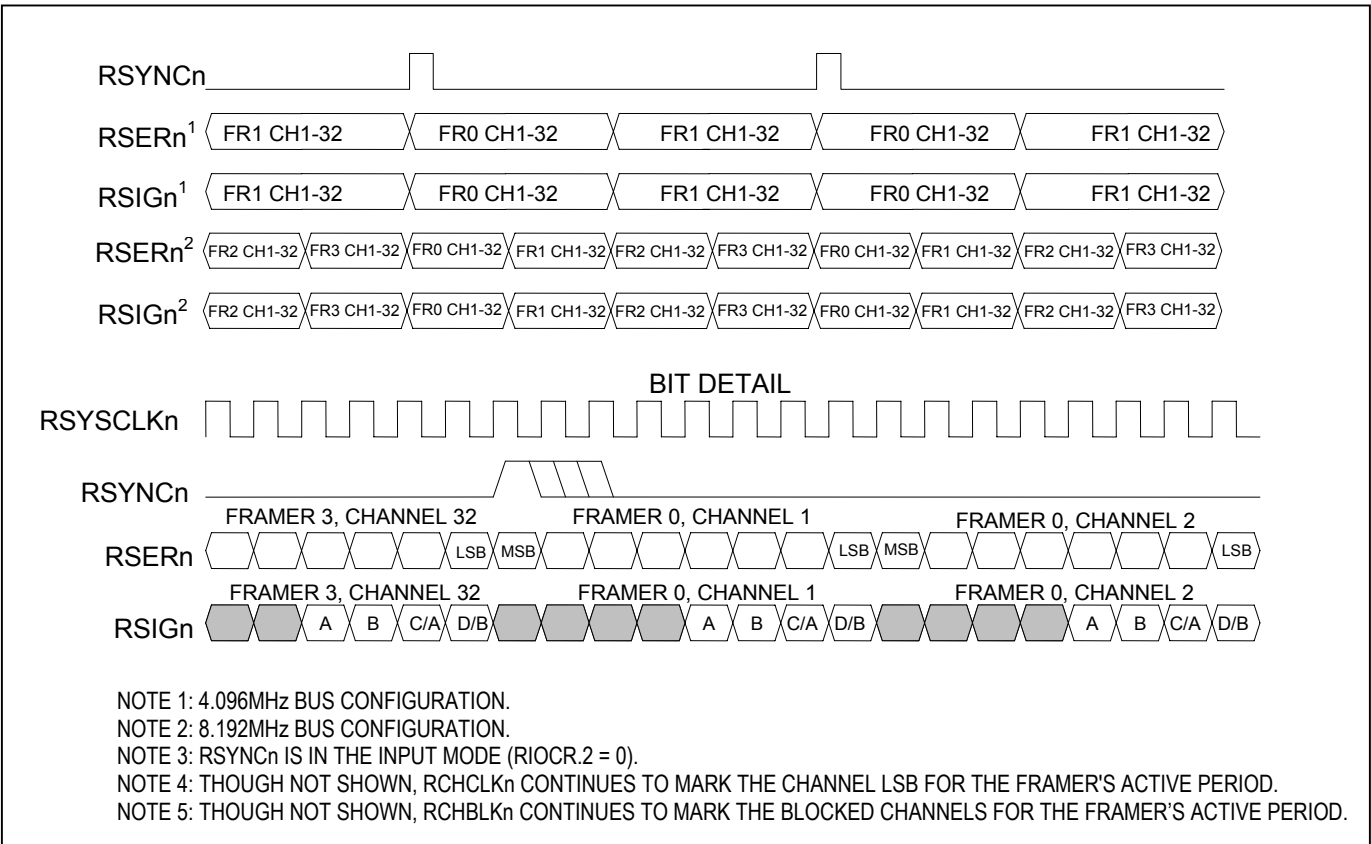


Figure 11-8. T1 Receive-Side RCHCLKn Gapped Mode During F-Bit



11.2 T1 Transmitter Functional Timing Diagrams

Figure 11-9. T1 Transmit-Side D4 Timing

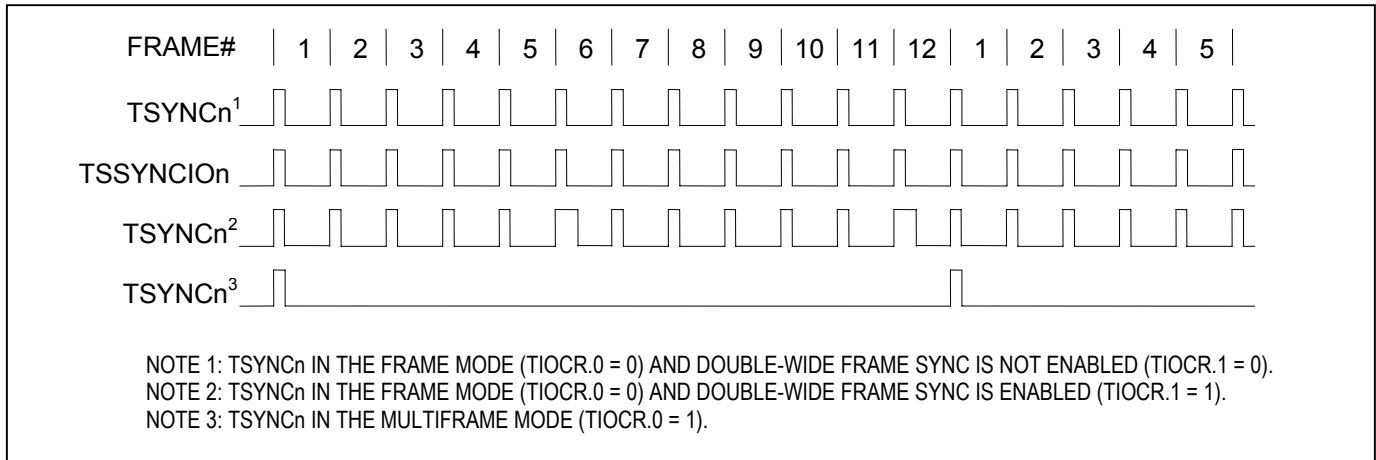


Figure 11-10. T1 Transmit-Side ESF Timing

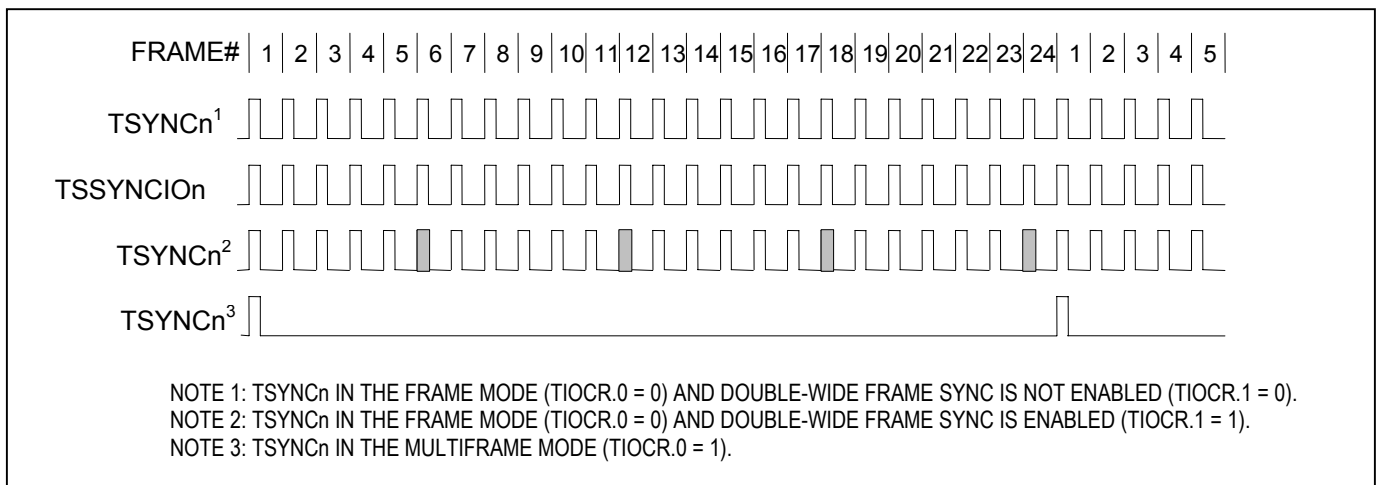


Figure 11-11. T1 Transmit-Side Boundary Timing (Elastic Store Disabled)

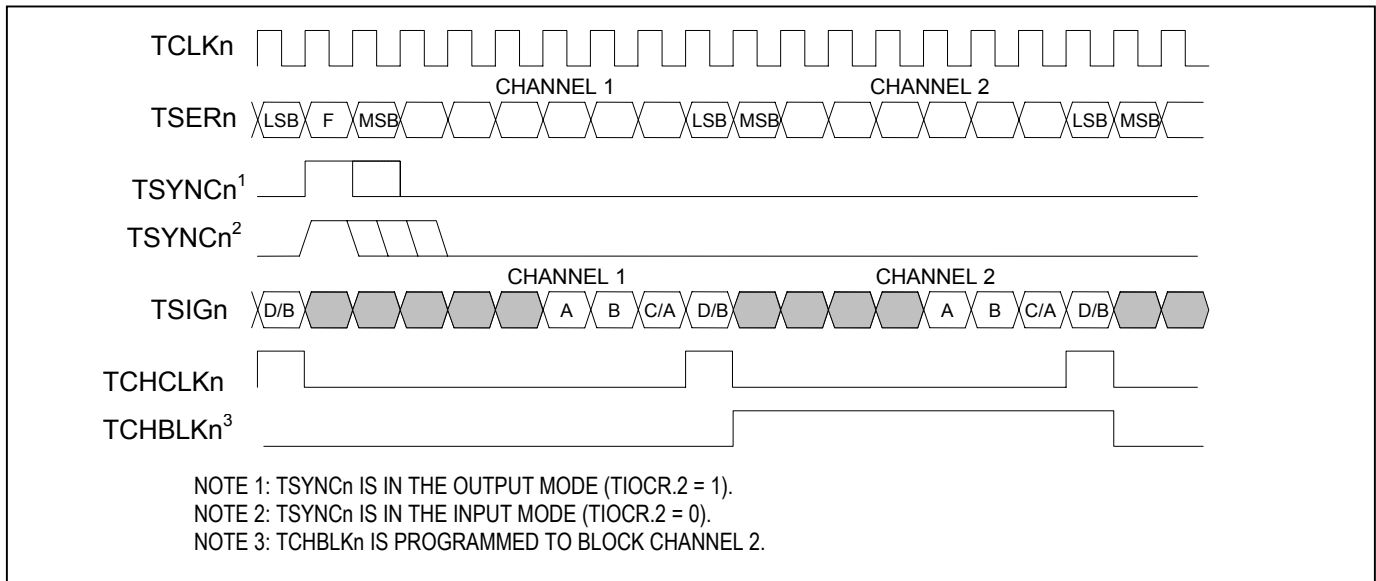


Figure 11-12. T1 Transmit-Side 1.544MHz Boundary Timing (Elastic Store Enabled)

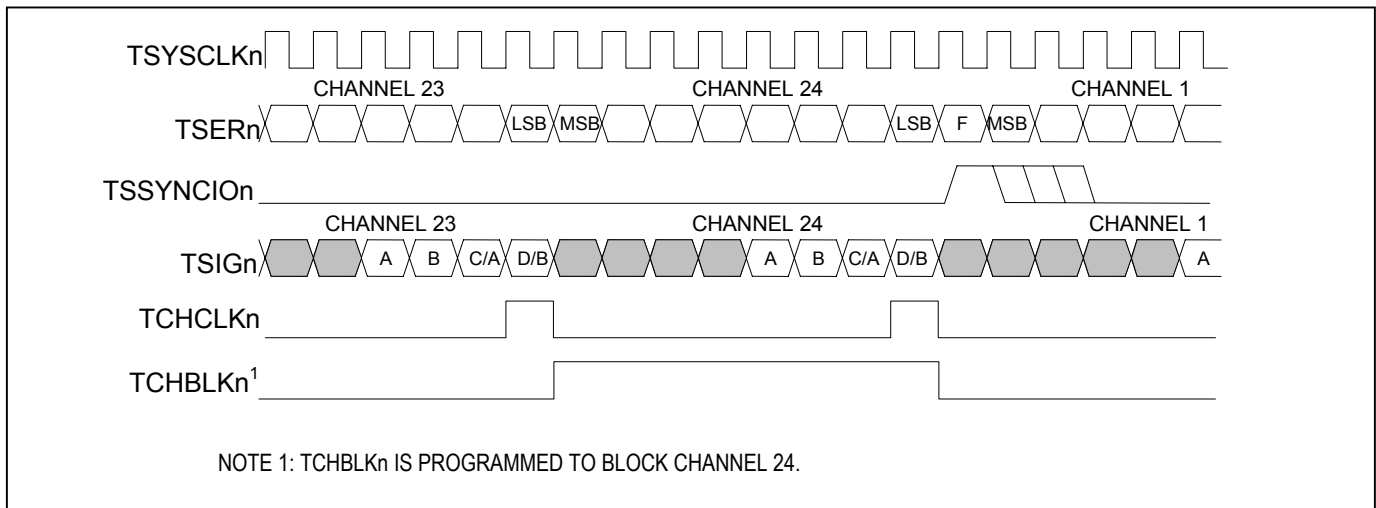


Figure 11-13. T1 Transmit-Side 2.048MHz Boundary Timing (Elastic Store Enabled)

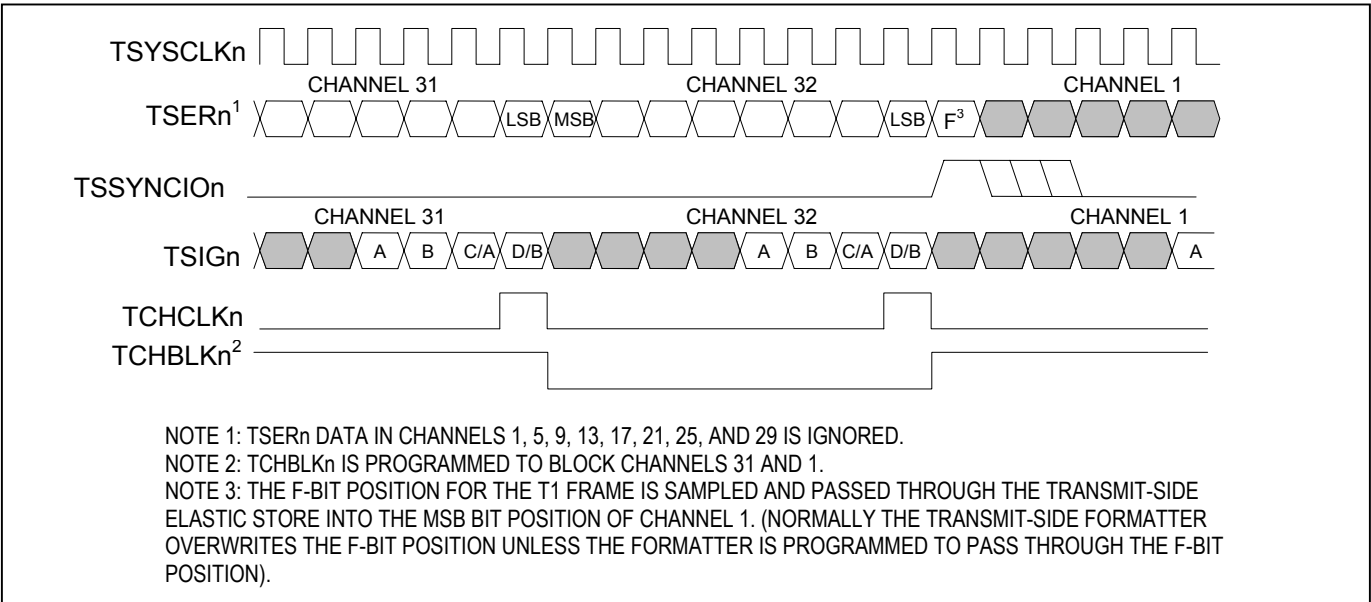


Figure 11-14. T1 Transmit-Side Interleave Bus Operation—BYTE Mode



Figure 11-15. T1 Transmit-Side Interleave Bus Operation—FRAME Mode

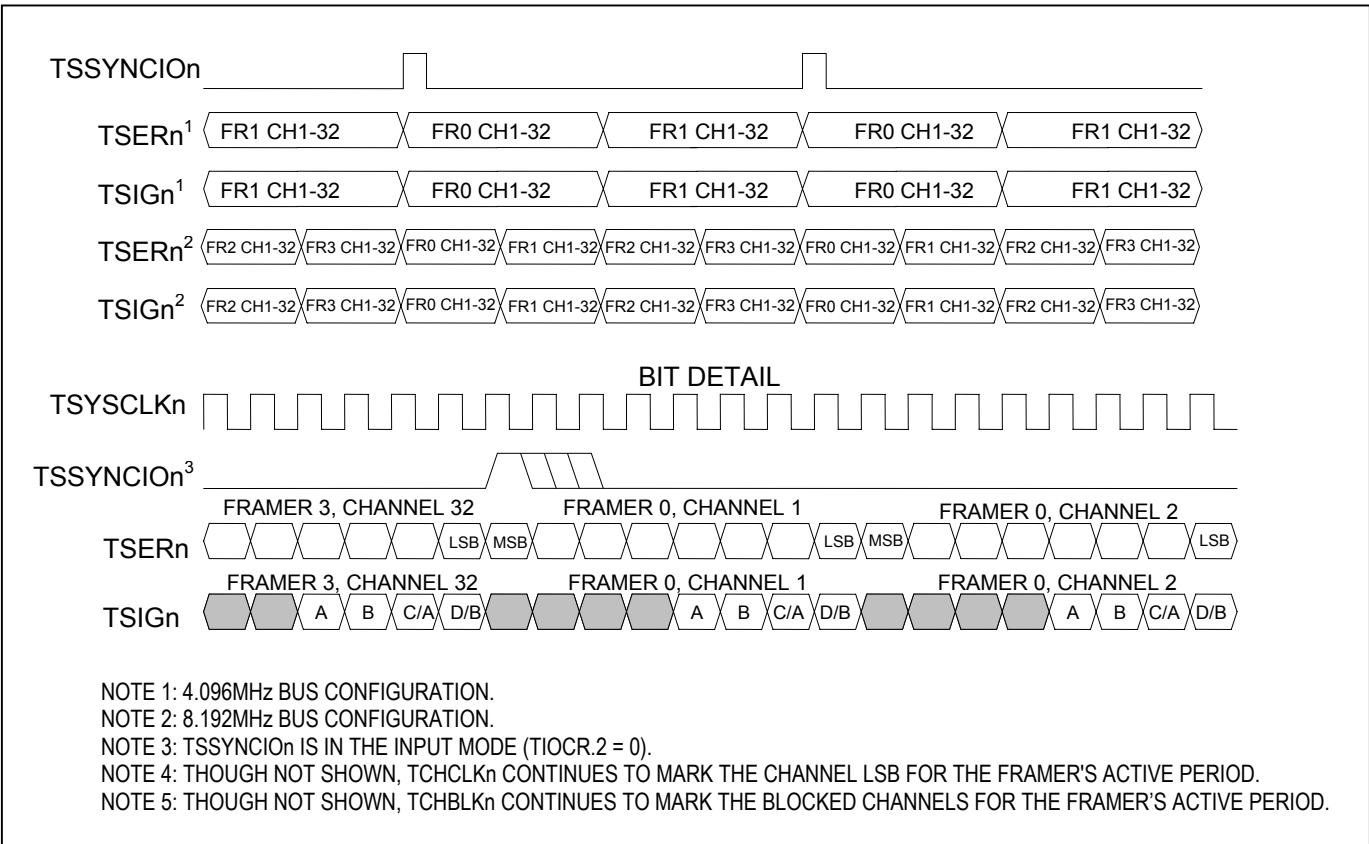


Figure 11-16. T1 Transmit-Side TCHCLKn Gapped Mode During F-Bit



11.3 E1 Receiver Functional Timing Diagrams

Figure 11-17. E1 Receive-Side Timing

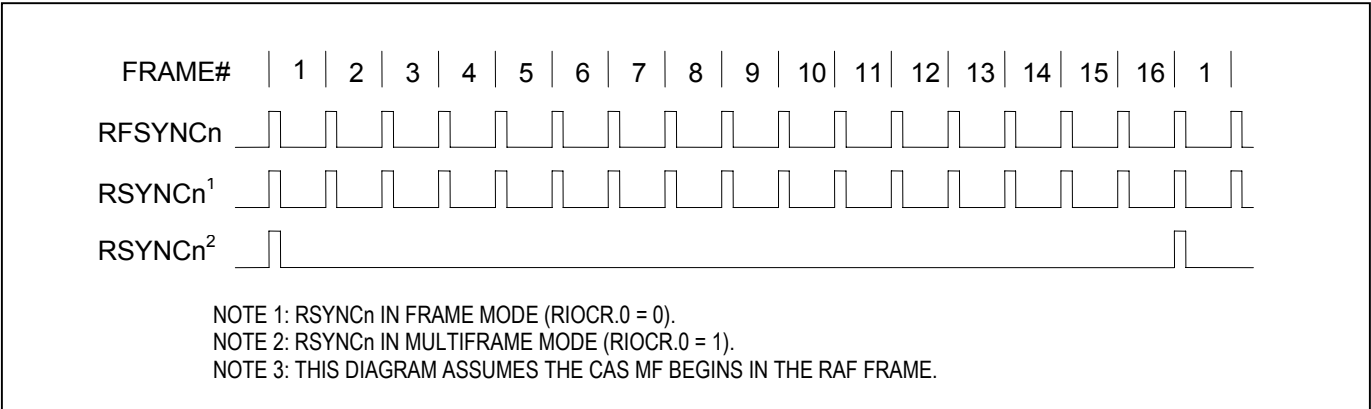


Figure 11-18. E1 Receive-Side Boundary Timing (Elastic Store Disabled)

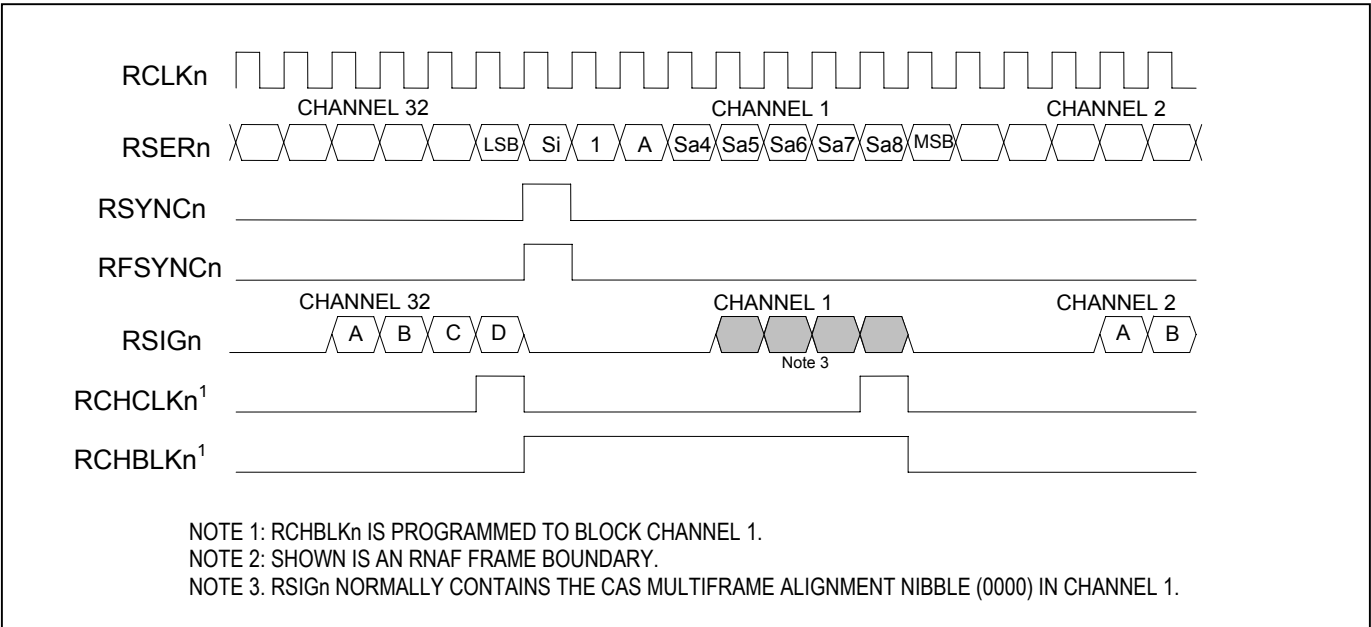


Figure 11-19. E1 Receive-Side 1.544MHz Boundary Timing (Elastic Store Enabled)



Figure 11-20. E1 Receive-Side 2.048MHz Boundary Timing (Elastic Store Enabled)



Figure 11-21. E1 Receive-Side Interleave Bus Operation—BYTE Mode

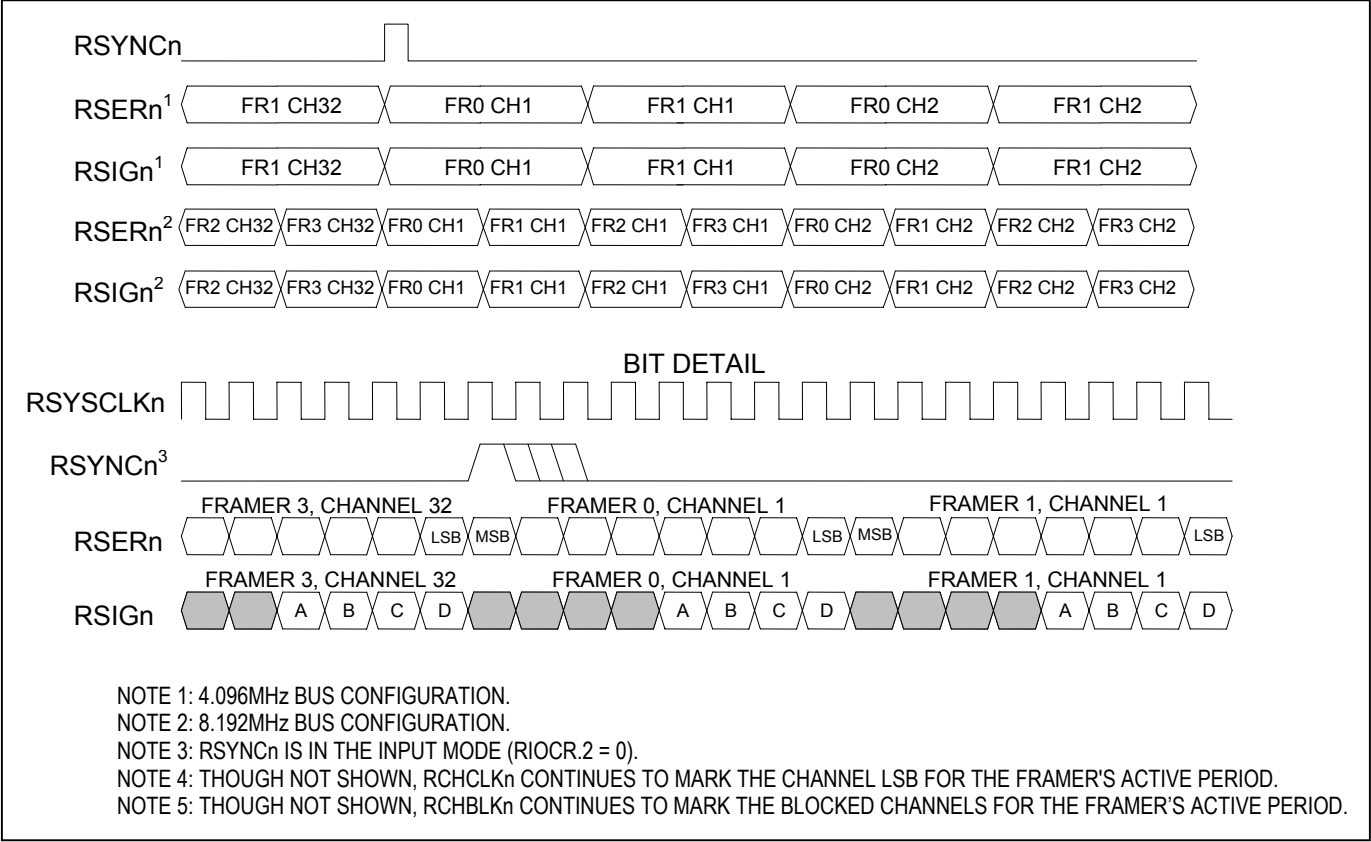


Figure 11-22. E1 Receive-Side Interleave Bus Operation—FRAME Mode

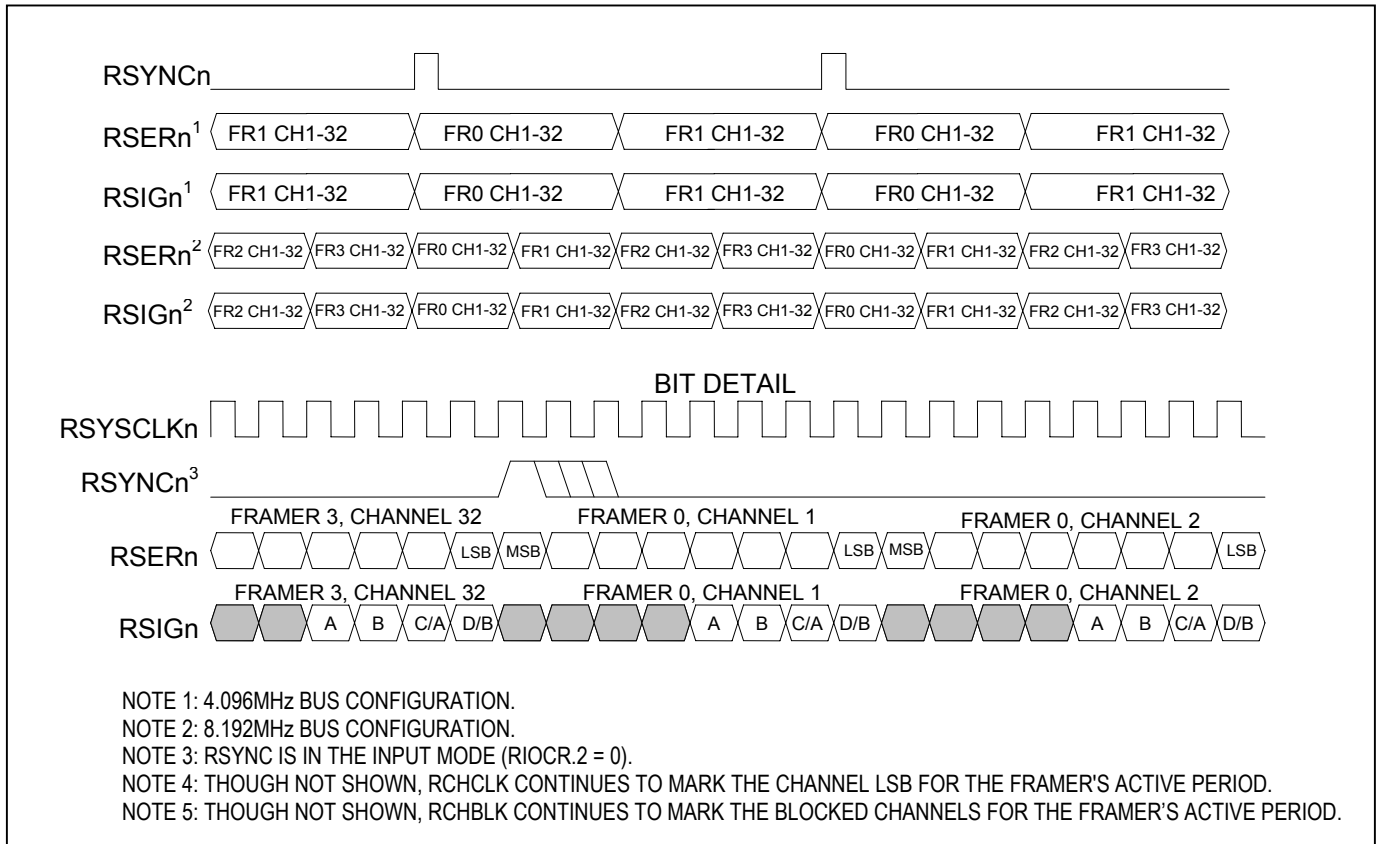
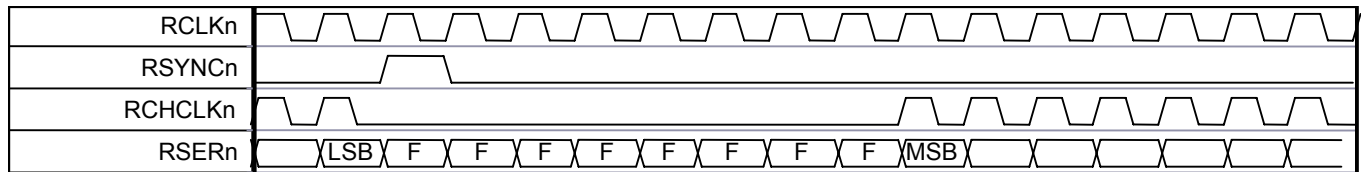


Figure 11-23. E1 Receive-Side RCHCLKn Gapped Mode During Channel 1



11.4 E1 Transmitter Functional Timing Diagrams

Figure 11-24. E1 Transmit-Side Timing



Figure 11-25. E1 Transmit-Side Boundary Timing (Elastic Store Disabled)



Figure 11-26. E1 Transmit-Side 1.544MHz Boundary Timing (Elastic Store Enabled)

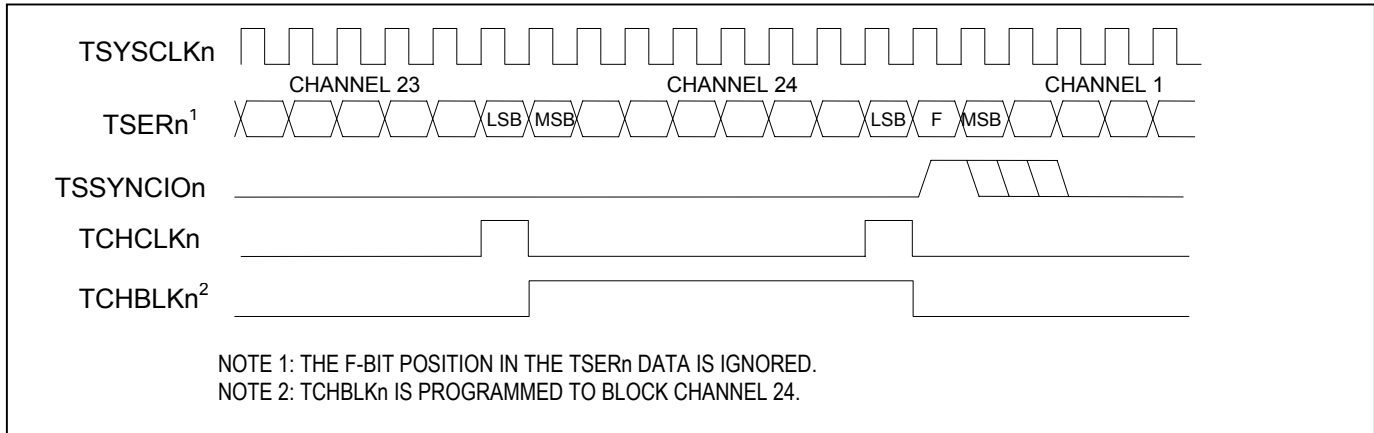


Figure 11-27. E1 Transmit-Side 2.048MHz Boundary Timing (Elastic Store Enabled)

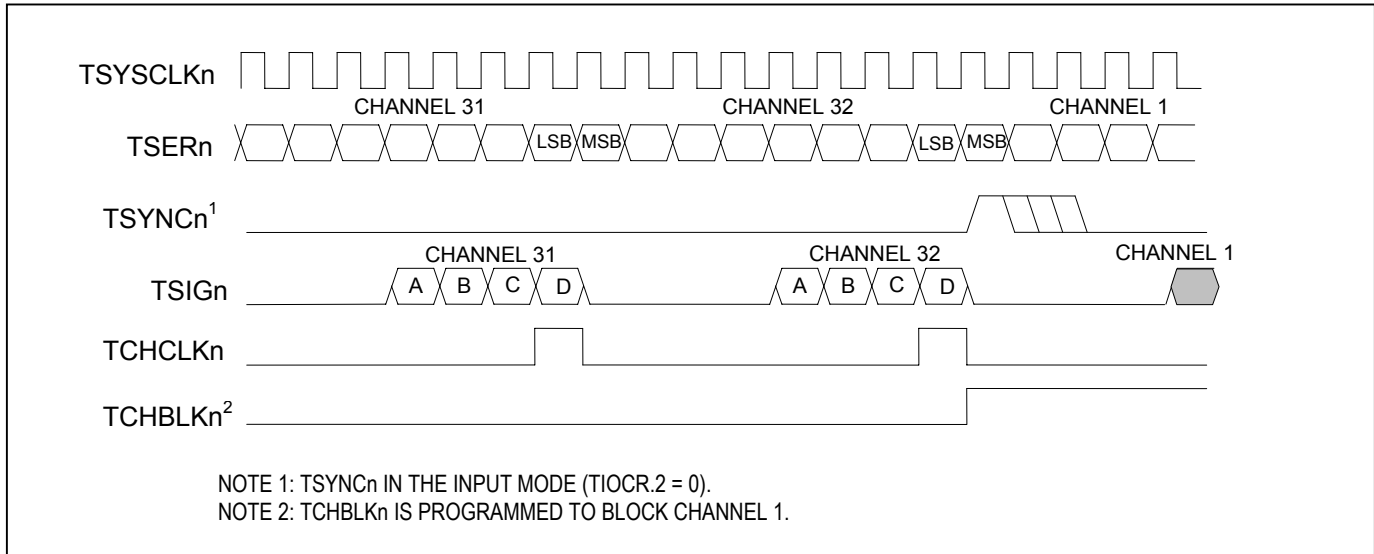


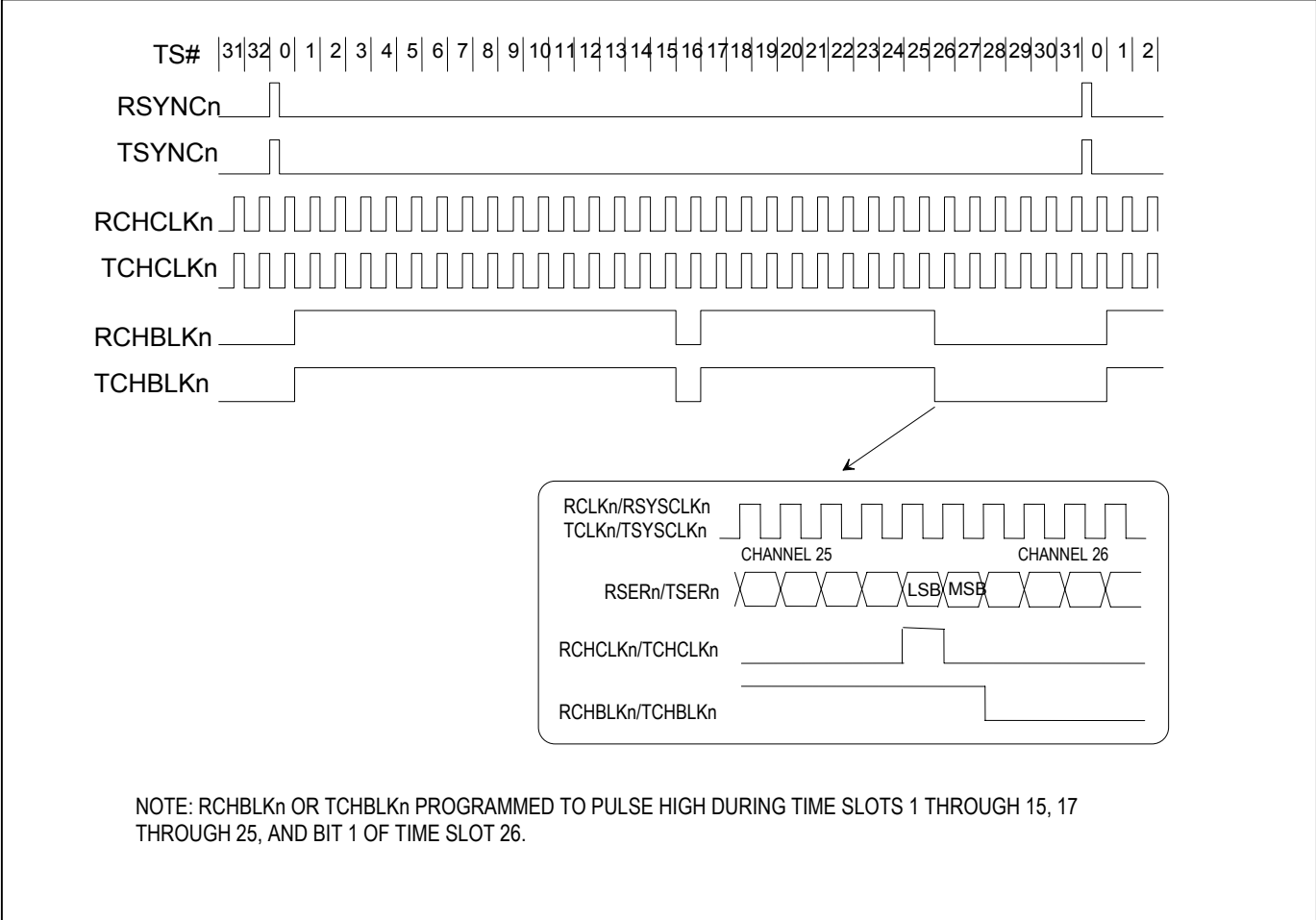
Figure 11-28. E1 Transmit-Side Interleave Bus Operation—BYTE Mode



Figure 11-29. E1 Transmit-Side Interleave Bus Operation—FRAME Mode



Figure 11-30. E1 G.802 Timing



NOTE: RCHBLKn OR TCHBLKn PROGRAMMED TO PULSE HIGH DURING TIME SLOTS 1 THROUGH 15, 17 THROUGH 25, AND BIT 1 OF TIME SLOT 26.

Figure 11-31. E1 Transmit-Side TCHCLKn Gapped Mode During Channel 1



12. OPERATING PARAMETERS

ABSOLUTE MAXIMUM RATINGS

| | |
|---|---------------------------------------|
| Voltage Range on Any Lead with Respect to V_{SS} (except V_{DD}) | -0.3V to +5.5V |
| Supply Voltage (V_{DD}) Range with Respect to V_{SS} | -0.3V to +3.63V |
| Operating Temperature Range | -40°C to +85°C (Note 1) |
| Storage Temperature Range | -55°C to +125°C |
| Soldering Temperature | See IPC/JEDEC J-STD-020 Specification |

This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

Note 1: Specifications to -40°C are guaranteed by design (GBD) and not production tested.

Table 12-1. Recommended DC Operating Conditions

($T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|-------------|---------------|------------|-------|-----|-------|-------|
| Logic 1 | V_{IH} | | 2.0 | | 5.5 | V |
| Logic 0 | V_{IL} | | -0.3 | | +0.8 | V |
| I/O Supply | V_{DD} | | 3.135 | 3.3 | 3.465 | V |
| Core Supply | $V_{DD-CORE}$ | | 1.71 | 1.8 | 1.89 | V |

Table 12-2. Capacitance

($T_A = +25^\circ\text{C}$)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|--------------------|-----------|------------|-----|-----|-----|-------|
| Input Capacitance | C_{IN} | | | 7 | | pF |
| Output Capacitance | C_{OUT} | | | 7 | | pF |

Table 12-3. Recommended DC Operating Conditions

($V_{DD} = 3.135\text{V}$ to 3.465V , $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---------------|--------------|-------|-----|-------|---------------|
| 3.3V Supply Current | I_{DD} | (Notes 1, 2) | | 300 | 450 | mA |
| 1.8V Core Supply Current | $I_{DD-CORE}$ | (Notes 1, 2) | | 75 | 120 | mA |
| Input Leakage | I_{IL} | | -10.0 | | +10.0 | μA |
| Pullup Pin Input Leakage | I_{ILP} | (Note 3) | -85.0 | | +10.0 | μA |
| Pulldown Pin Input Leakage | I_{ILP} | (Note 3) | -10.0 | | +85.0 | μA |
| Tri-State Output Leakage | I_{OL} | | -10.0 | | +10.0 | μA |
| Output Voltage ($I_{OH} = -4\text{mA}$) | V_{OH} | | 2.4 | | | V |
| Output Voltage ($I_{OL} = +4\text{mA}$) | V_{OL} | | | | 0.4 | V |

Note 1: RCLK1-n = TCLK1-n = 2.048MHz, digital outputs without load.

Note 2: Max power consumed is measured with all ports transmitting an all-ones data pattern with a transmitter load of 100 Ω .

Note 3: Pullup/pulldown pins include SPI_SEL, TSYCLK[2:8], RSYCLK[2:8], DIGIOEN, $\overline{\text{JTRST}}$, JTMS, and JTDI.

12.1 Thermal Characteristics

Table 12-4. Thermal Characteristics

| PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS |
|--|------------|-----|-------|------|-------|
| Ambient Temperature | (Note 1) | -40 | | +85 | °C |
| Junction Temperature | | | | +125 | °C |
| Theta-JA (θ_{JA}) in Still Air for 256-Pin TE-CSBGA | (Note 2) | | +17.5 | | °C/W |

Note 1: The package is mounted on a four-layer JEDEC standard test board.

Note 2: Theta-JA (θ_{JA}) is the junction-to-ambient thermal resistance, when the package is mounted on a four-layer JEDEC standard test board.

12.2 Line Interface Characteristics

Table 12-5. Transmitter Characteristics

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|--|--------|-----------------|------|------|------|-------|
| Output Mark Amplitude | V_m | E1 75 Ω | 2.13 | 2.37 | 2.61 | V |
| | | E1 120 Ω | 2.70 | 3.00 | 3.30 | |
| | | T1 100 Ω | 2.40 | 3.00 | 3.60 | |
| | | J1 110 Ω | 2.40 | 3.00 | 3.60 | |
| Output Zero Amplitude | V_s | (Note 1) | -0.3 | | +0.3 | V |
| Transmit Amplitude Variation with Supply | | | -1 | | +1 | % |

Table 12-6. Receiver Characteristics

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|--------|------------|-----|------|-----|-------|
| Cable Attenuation | Attn | | | | 43 | dB |
| Allowable Zeros Before Loss (Note 1) | | | | 192 | | |
| | | | | 192 | | |
| | | | | 2048 | | |
| Allowable Ones Before Loss (Note 2) | | | | 24 | | |
| | | | | 192 | | |
| | | | | 192 | | |

Note 1: 192 zeros for T1 and T1.231 Specification Compliance. 192 zeros for E1 and G.775 Specification Compliance. 2048 zeros for ETS 300 233 compliance.

Note 2: 24 ones in 192-bit period for T1.231; 192 ones for G.775; 192 ones for ETS 300 233.

13. AC TIMING CHARACTERISTICS

Unless otherwise noted, all timing numbers assume 20pF test load on output signals, 40pF test load on bus signals.

13.1 Microprocessor Bus AC Characteristics

13.1.1 SPI Bus Mode

Table 13-1. SPI Bus Mode Timing

(See [Figure 13-1.](#))

| SYMBOL (Note 1) | CHARACTERISTIC (Note 2) | SYMBOL | MIN | MAX | UNITS |
|--------------------|--|---------------|-----|-----|-------|
| | Operating Frequency Slave | $f_{BUS(S)}$ | | 5 | MHz |
| t1 | Cycle Time: Slave | $t_{CYC(S)}$ | 200 | | ns |
| t2 | Enable Lead Time | $t_{LEAD(S)}$ | 15 | | ns |
| t3 | Enable Lag Time | $t_{LAG(S)}$ | 15 | | ns |
| t4, t5 | Clock (CLK) Duty Cycle Slave (t4/t1 or t5/t1) | $t_{CLKH(S)}$ | 80 | | ns |
| t6 | Data Setup Time (Inputs) Slave | $t_{SU(S)}$ | 5 | | ns |
| t7 | Data Hold Time (Inputs) Slave | $t_{H(S)}$ | 15 | | ns |
| t8 | Disable Time, Slave (Note 3) | $t_{DIS(S)}$ | | 25 | ns |
| t9 | Data Valid Time, After Enable Edge Slave (Note 4) | $t_{V(S)}$ | | 40 | ns |
| t10 | Data Hold Time, Outputs, After Enable Edge Slave | $t_{HD(S)}$ | 5 | | ns |

Note 1: Symbols refer to dimensions in [Figure 13-1.](#)

Note 2: 100pF load on all SPI pins.

Note 3: Hold time to high-impedance state.

Note 4: With 100pF on all SPI pins.

Figure 13-1. SPI Interface Timing Diagram



Table 13-2. AC Characteristics—Microprocessor Bus Timing(V_{DD} = 3.3V ±5%, T_A = -40°C to +85°C.) (See [Figure 13-2](#), [Figure 13-3](#), [Figure 13-4](#), and [Figure 13-5](#).)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|--------|------------|-----|-----|-----|-------|
| Setup Time for A[12:0] Valid to $\overline{\text{CSB}}$ Active | t1 | | 0 | | | ns |
| Setup Time for $\overline{\text{CSB}}$ Active to Either $\overline{\text{RDB}}$, or $\overline{\text{WRB}}$ Active | t2 | | 0 | | | ns |
| Delay Time from Either $\overline{\text{RDB}}$ or $\overline{\text{DSB}}$ Active to D[7:0] Valid | t3 | (Note 1) | | | 175 | ns |
| Hold Time from Either $\overline{\text{RDB}}$ or $\overline{\text{WRB}}$ Inactive to $\overline{\text{CSB}}$ Inactive | t4 | | 0 | | | ns |
| Hold Time from $\overline{\text{CSB}}$ or $\overline{\text{RDB}}$ or $\overline{\text{DSB}}$ Inactive to D[7:0] Tri-State | t5 | | 5 | | 20 | ns |
| Wait Time from $\overline{\text{WRB}}$ Active to Latch Data | t6 | | 40 | | | ns |
| Data Setup Time to $\overline{\text{WRB}}$ Inactive | t7 | | 10 | | | ns |
| Data Hold Time from $\overline{\text{WRB}}$ Inactive | t8 | | 2 | | | ns |
| Address Hold from $\overline{\text{WRB}}$ Inactive | t9 | | 0 | | | ns |
| Write Access to Subsequent Write/Read Access Delay Time | t10 | (Note 1) | 30 | | | ns |

Note 1: If supplying a 1.544MHz MCLK, the FREQSEL bit must be set to meet this timing.

Figure 13-2. Intel Bus Read Timing (BTS = 0)

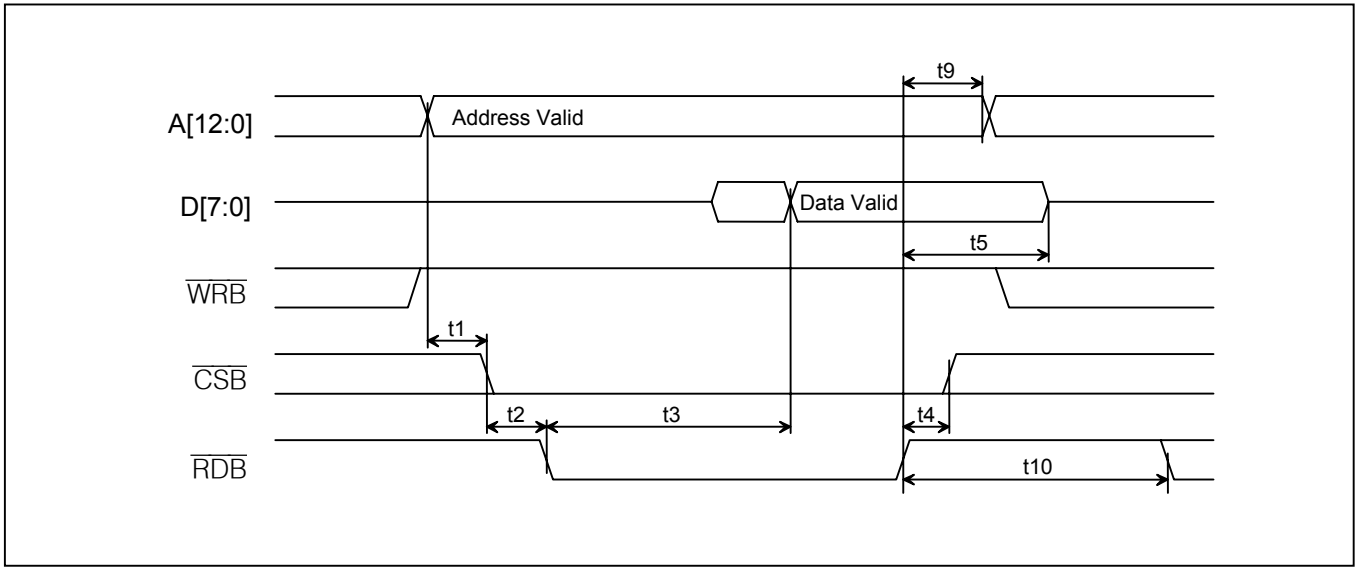


Figure 13-3. Intel Bus Write Timing (BTS = 0)

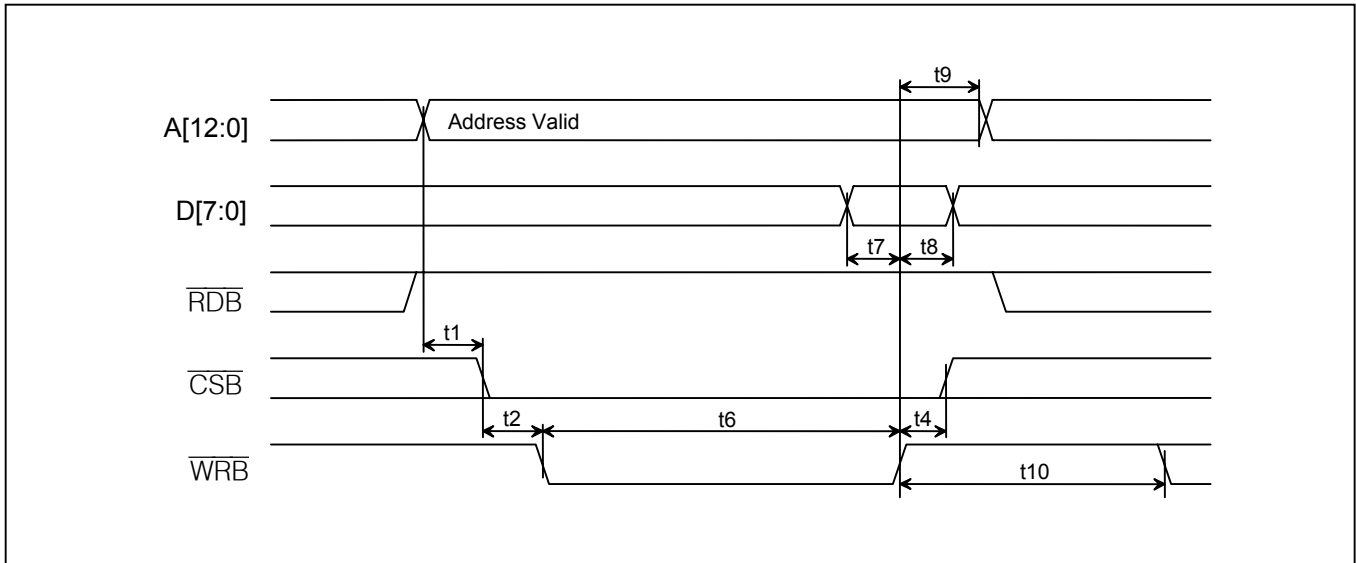


Figure 13-4. Motorola Bus Read Timing (BTS = 1)

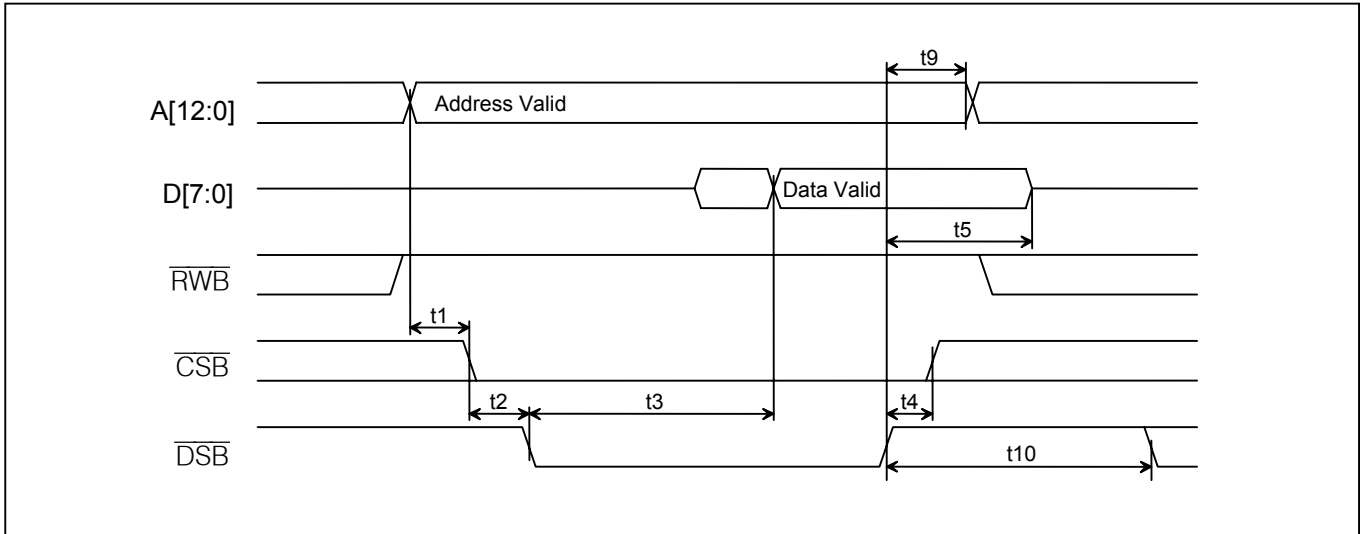


Figure 13-5 Motorola Bus Write Timing (BTS = 1)



Table 13-3. Receiver AC Characteristics(V_{DD} = 3.3V ±5%, T_A = -40°C to +85°C.) (See [Figure 13-6](#) and [Figure 13-7](#).)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|--|-----------------|------------|-----|-----|-----|-------|
| RCLKn Period | t _{CP} | (Note 1) | | 648 | | ns |
| | | (Note 2) | | 488 | | |
| RCLKn Pulse Width | t _{CH} | | 125 | | | ns |
| | t _{CL} | | 125 | | | |
| RSYSCLKn Period | t _{SP} | (Note 3) | 60 | | | ns |
| | | (Note 4) | 60 | | | |
| RSYSCLKn Pulse Width | t _{SH} | | 30 | | | ns |
| | t _{SL} | | 30 | | | |
| RSYNCn Setup to RSYCLKn Falling | t _{SU} | | 10 | | | ns |
| RSYNCn Pulse Width | t _{PW} | | 50 | | | ns |
| Delay RCLKn to RSERn, RSIGn Valid | t _{D1} | | | | 10 | ns |
| Delay RCLKn to RCHCLKn, RSYNCn, RCHBLKn, RFSYNCn | t _{D2} | | | | 20 | ns |
| Delay RSYCLKn to RSERn, RSIGn Valid | t _{D3} | | | | 20 | ns |
| Delay RSYCLKn to RCHCLKn, RCHBLKn, RMSYNCn, RSYNCn | t _{D4} | | | | 20 | ns |

Note 1: T1 Mode.**Note 2:** E1 Mode.**Note 3:** RSYCLKn = 1.544MHz.**Note 4:** RSYCLKn = 2.048MHz.

Figure 13-6. Receive Framer Timing—Backplane (T1 Mode)

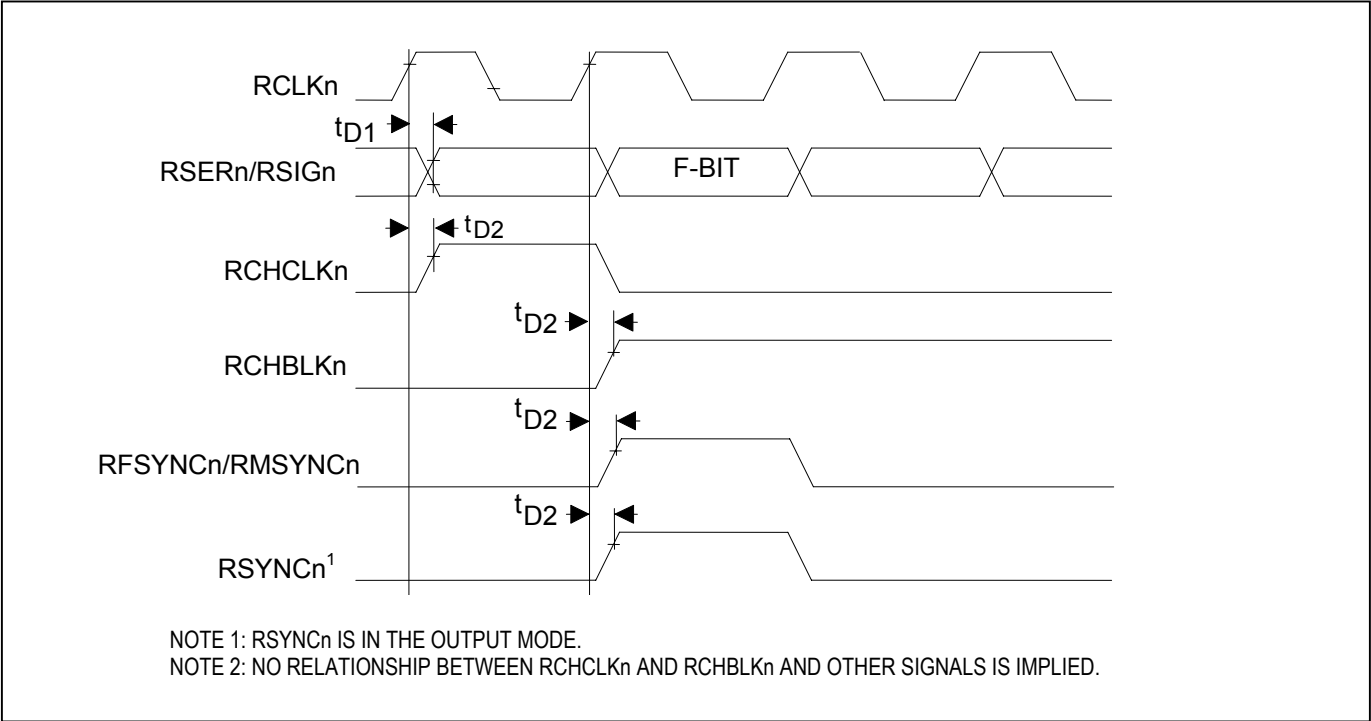


Figure 13-7. Receive-Side Timing—Elastic Store Enabled (T1 Mode)

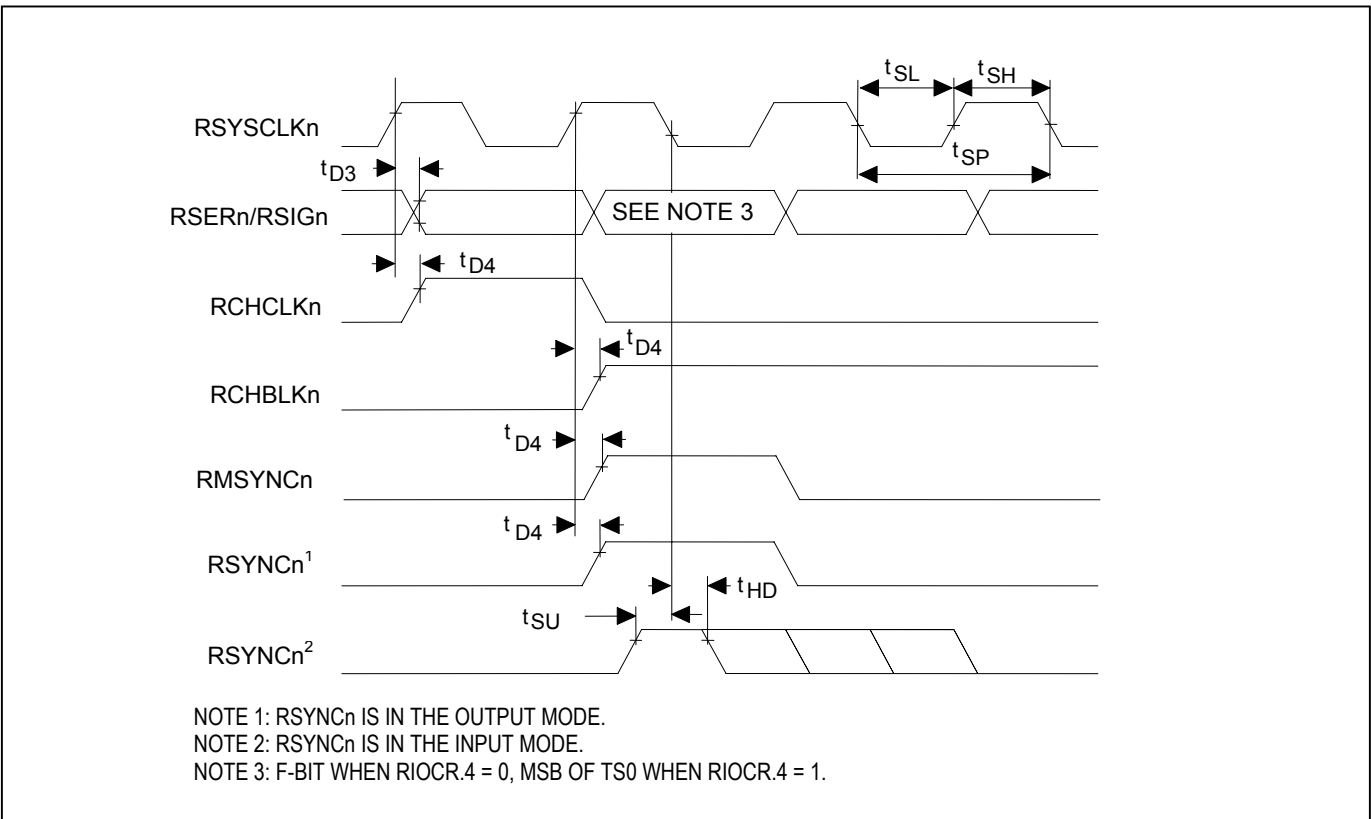


Table 13-4. Transmit AC Characteristics(V_{DD} = 3.3V ±5%, T_A = -40°C to +85°C.) (See [Figure 13-8](#), [Figure 13-9](#), and [Figure 13-10](#).)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|--|-----------------|------------|-----|-----|-----|-------|
| TCLKn Period | t _{CP} | (Note 1) | | 648 | | ns |
| | | (Note 2) | | 488 | | |
| TCLKn Pulse Width | t _{CH} | | 125 | | | ns |
| | t _{CL} | | 125 | | | |
| TSYSCLKn Period | t _{SP} | (Note 3) | 60 | | | ns |
| | | (Note 4) | 60 | | | |
| TSYSCLKn Pulse Width | t _{SH} | | 30 | | | ns |
| | t _{SL} | | 30 | | | |
| TSYNCn or TSSYNClOn Setup to TCLKn or TSYSCLKn Falling | t _{SU} | | 10 | | | ns |
| TSYNCn or TSSYNClOn Pulse Width | t _{PW} | (Note 5) | 50 | | | ns |
| TSSYNClOn Pulse Width (Notes 6, 7) | t _{PW} | | | 488 | | ns |
| | | | | 244 | | |
| | | | | 122 | | |
| | | | | 61 | | |
| TSERn, TSIgn Setup to TCLKn, TSYSCLKn Falling | t _{SU} | | 10 | | | ns |
| TSERn, TSIgn Hold from TCLKn, TSYSCLKn Falling | t _{HD} | | 10 | | | ns |
| Delay TCLKn to TCHBLKn, TCHCLKn, TSYNCn | t _{D2} | | | | 20 | ns |
| Delay TSYSCLKn to TCHCLKn, TCHBLKn | t _{D3} | | | | 20 | ns |
| Delay BPCLK1 to TSSYNClOn | t _{D5} | (Note 6) | | | 5 | ns |

Note 1: T1 Mode.**Note 2:** E1 Mode.**Note 3:** RSYSCLKn = 1.544MHz.**Note 4:** RSYSCLKn = 2.048MHz.**Note 5:** TSSYNClOn configured as an input ([GTCR3.1](#) = 0).**Note 6:** TSSYNClOn configured as an output ([GTCR3.1](#) = 1).**Note 7:** Varies depending on the frequency of BPCLK1.

Figure 13-8. Transmit Formatter Timing—Backplane



NOTE 1: TSYNCn IS IN THE OUTPUT MODE.

NOTE 2: TSYNCn IS IN THE INPUT MODE.

NOTE 3: TSERn IS SAMPLED ON THE FALLING EDGE OF TCLK WHEN THE TRANSMIT-SIDE ELASTIC STORE IS DISABLED.

NOTE 4: TCHCLKn AND TCHBLKn ARE SYNCHRONOUS WITH TCLK WHEN THE TRANSMIT-SIDE ELASTIC STORE IS DISABLED.

NOTE 5: NO RELATIONSHIP BETWEEN TCHCLKn AND TCHBLKn AND THE OTHER SIGNALS IS IMPLIED.

Figure 13-9. Transmit Formatter Timing—Elastic Store Enabled



Figure 13-10. BPCLK1 Timing



13.2 JTAG Interface Timing

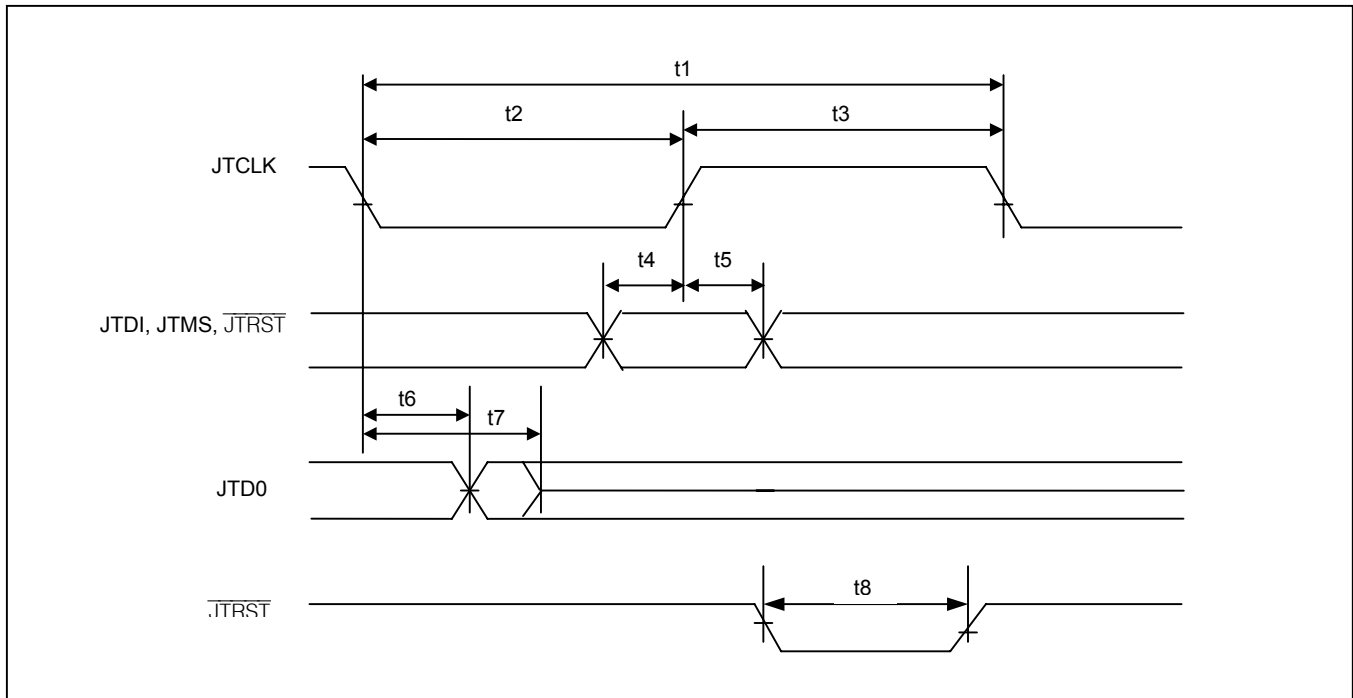
Table 13-5. JTAG Interface Timing

($V_{DD} = 3.3V \pm 5\%$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$.) (See [Figure 13-11](#).)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|--|--------|------------|-----|------|-----|-------|
| JTCLK Clock Period | t1 | | | 1000 | | ns |
| JTCLK Clock High:Low Time | t2:t3 | (Note 1) | 50 | 500 | | ns |
| JTCLK to JTDI, JTMS Setup Time | t4 | | 5 | | | ns |
| JTCLK to JTDI, JTMS Hold Time | t5 | | 2 | | | ns |
| JTCLK to JTDO Delay | t6 | | 2 | | 50 | ns |
| JTCLK to JTDO High-Impedance Delay | t7 | | 2 | | 50 | ns |
| $\overline{\text{JTRST}}$ Width Low Time | t8 | | 100 | | | ns |

Note 1: Clock can be stopped high or low.

Figure 13-11. JTAG Interface Timing Diagram



14. JTAG BOUNDARY SCAN AND TEST ACCESS PORT

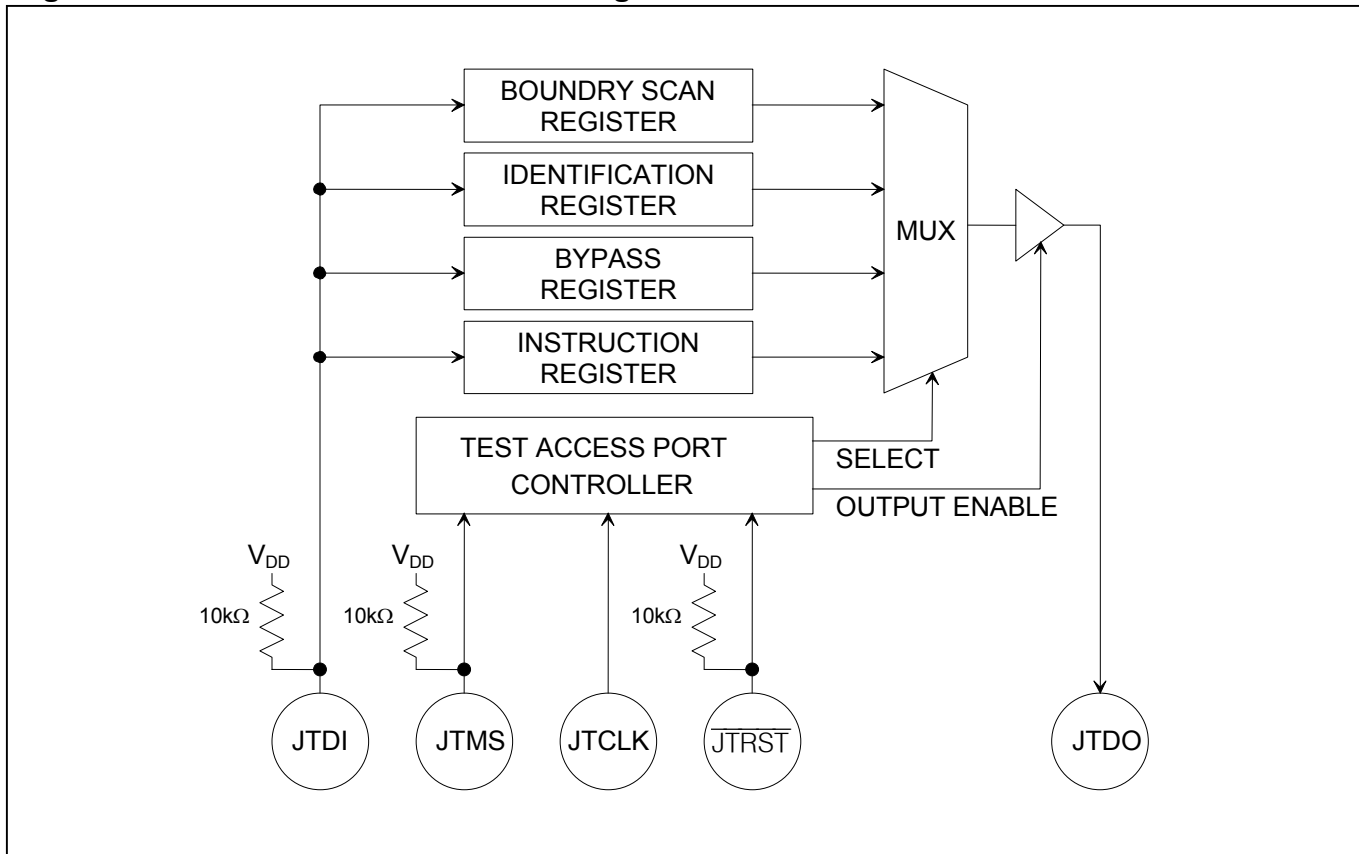
The DS26518 IEEE 1149.1 design supports the standard instruction codes SAMPLE:PRELOAD, BYPASS, and EXTEST. Optional public instructions included are HIGHZ, CLAMP, and IDCODE. See [Table 14-1](#). The DS26518 contains the following as required by IEEE 1149.1 Standard Test Access Port and Boundary Scan Architecture.

Test Access Port (TAP)
TAP Controller
Instruction Register

Bypass Register
Boundary Scan Register
Device Identification Register

The Test Access Port has the necessary interface pins: $\overline{\text{JTRST}}$, JTCLK, JTMS, JTDI, and JTDO. See the pin descriptions for details.

Figure 14-1. JTAG Functional Block Diagram



14.1 TAP Controller State Machine

The TAP controller is a finite state machine that responds to the logic level at JTMS on the rising edge of JTCLK. See [Figure 14-2](#).

14.1.1 Test-Logic-Reset

Upon power-up, the TAP Controller will be in the Test-Logic-Reset state. The instruction register will contain the IDCODE instruction. All system logic of the device will operate normally.

14.1.2 Run-Test-Idle

The Run-Test-Idle is used between scan operations or during specific tests. The Instruction Register and test registers will remain idle.

14.1.3 Select-DR-Scan

All test registers retain their previous state. With JTMS LOW, a rising edge of JTCLK moves the controller into the Capture-DR state and will initiate a scan sequence. JTMS HIGH during a rising edge on JTCLK moves the controller to the Select-IR-Scan state.

14.1.4 Capture-DR

Data may be parallel-loaded into the test data registers selected by the current instruction. If the instruction does not call for a parallel load or the selected register does not allow parallel loads, the Test Register remains at its current value. On the rising edge of JTCLK, the controller goes to the Shift-DR state if JTMS is LOW or it goes to the Exit1-DR state if JTMS is HIGH.

14.1.5 Shift-DR

The test data register selected by the current instruction is connected between JTDI and JTDO and will shift data one stage towards its serial output on each rising edge of JTCLK. If a test register selected by the current instruction is not placed in the serial path, it maintains its previous state.

14.1.6 Exit1-DR

While in this state, a rising edge on JTCLK puts the controller in the Update-DR state, which terminates the scanning process if JTMS is HIGH. A rising edge on JTCLK with JTMS LOW puts the controller in the Pause-DR state.

14.1.7 Pause-DR

Shifting of the test registers is halted while in this state. All test registers selected by the current instruction retain their previous state. The controller remains in this state while JTMS is LOW. A rising edge on JTCLK with JTMS HIGH puts the controller in the Exit2-DR state.

14.1.8 Exit2-DR

A rising edge on JTCLK with JTMS HIGH while in this state puts the controller in the Update-DR state and terminates the scanning process. A rising edge on JTCLK with JTMS LOW enters the Shift-DR state.

14.1.9 Update-DR

A falling edge on JTCLK while in the Update-DR state latches the data from the shift register path of the test registers into the data output latches. This prevents changes at the parallel output due to changes in the shift register.

14.1.10 Select-IR-Scan

All test registers retain their previous state. The instruction register remains unchanged during this state. With JTMS LOW, a rising edge on JTCLK moves the controller into the Capture-IR state and initiates a scan sequence

for the instruction register. JTMS HIGH during a rising edge on JTCLK puts the controller back into the Test-Logic-Reset state.

14.1.11 Capture-IR

The Capture-IR state is used to load the shift register in the instruction register with a fixed value. This value is loaded on the rising edge of JTCLK. If JTMS is HIGH on the rising edge of JTCLK, the controller enters the Exit1-IR state. If JTMS is LOW on the rising edge of JTCLK, the controller enters the Shift-IR state.

14.1.12 Shift-IR

In this state, the shift register in the instruction register is connected between JTDI and JTDO and shifts data one stage for every rising edge of JTCLK towards the serial output. The parallel register, as well as all test registers, remains at their previous states. A rising edge on JTCLK with JTMS HIGH moves the controller to the Exit1-IR state. A rising edge on JTCLK with JTMS LOW keeps the controller in the Shift-IR state while moving data one stage through the instruction shift register.

14.1.13 Exit1-IR

A rising edge on JTCLK with JTMS LOW puts the controller in the Pause-IR state. If JTMS is HIGH on the rising edge of JTCLK, the controller enters the Update-IR state and terminates the scanning process.

14.1.14 Pause-IR

Shifting of the instruction shift register is halted temporarily. With JTMS HIGH, a rising edge on JTCLK puts the controller in the Exit2-IR state. The controller remains in the Pause-IR state if JTMS is LOW during a rising edge on JTCLK.

14.1.15 Exit2-IR

A rising edge on JTCLK with JTMS LOW puts the controller in the Update-IR state. The controller loops back to Shift-IR if JTMS is HIGH during a rising edge of JTCLK in this state.

14.1.16 Update-IR

The instruction code shifted into the instruction shift register is latched into the parallel output on the falling edge of JTCLK as the controller enters this state. Once latched, this instruction becomes the current instruction. A rising edge on JTCLK with JTMS LOW puts the controller in the Run-Test-Idle state. With JTMS HIGH, the controller enters the Select-DR-Scan state.

Figure 14-2. TAP Controller State Diagram



14.2 Instruction Register

The instruction register contains a shift register as well as a latched parallel output and is 3 bits in length. When the TAP controller enters the Shift-IR state, the instruction shift register is connected between JTDI and JTDO. While in the Shift-IR state, a rising edge on JTCLK with JTMS LOW shifts the data one stage towards the serial output at JTDO. A rising edge on JTCLK in the Exit1-IR state or the Exit2-IR state with JTMS HIGH moves the controller to the Update-IR state. The falling edge of that same JTCLK will latch the data in the instruction shift register to the instruction parallel output. Instructions supported by the DS26518 and its respective operational binary codes are shown in [Table 14-1](#).

Table 14-1. Instruction Codes for IEEE 1149.1 Architecture

| INSTRUCTION | SELECTED REGISTER | INSTRUCTION CODES |
|----------------|-----------------------|-------------------|
| SAMPLE:PRELOAD | Boundary Scan | 010 |
| BYPASS | Bypass | 111 |
| EXTEST | Boundary Scan | 000 |
| CLAMP | Bypass | 011 |
| HIGHZ | Bypass | 100 |
| IDCODE | Device Identification | 001 |

14.2.1 SAMPLE:PRELOAD

This is a mandatory instruction for the IEEE 1149.1 specification. This instruction supports two functions. The digital I/Os of the device can be sampled at the Boundary Scan Register without interfering with the normal operation of the device by using the Capture-DR state. SAMPLE:PRELOAD also allows the device to shift data into the boundary scan register via JTDI using the Shift-DR state.

14.2.2 BYPASS

When the BYPASS instruction is latched into the parallel instruction register, JTDI connects to JTDO through the one-bit Bypass Test Register. This allows data to pass from JTDI to JTDO without affecting the device's normal operation.

14.2.3 EXTEST

This allows testing of all interconnections to the device. When the EXTEST instruction is latched in the instruction register, the following actions occur. Once enabled via the Update-IR state, the parallel outputs of all digital output pins will be driven. The Boundary Scan Register will be connected between JTDI and JTDO. The Capture-DR will sample all digital inputs into the Boundary Scan Register.

14.2.4 CLAMP

All digital outputs of the device will output data from the boundary scan parallel output while connecting the Bypass Register between JTDI and JTDO. The outputs will not change during the CLAMP instruction.

14.2.5 HIGHZ

All digital outputs of the device will be placed in a high-impedance state. The Bypass Register will be connected between JTDI and JTDO.

14.2.6 IDCODE

When the IDCODE instruction is latched into the parallel instruction register, the identification test register is selected. The device identification code will be loaded into the identification register on the rising edge of JTCLK following entry into the Capture-DR state. Shift-DR can be used to shift the identification code out serially via JTDO. During Test-Logic-Reset, the identification code is forced into the instruction register's parallel output. The ID code will always have a "1" in the LSB position. The next 11 bits identify the manufacturer's JEDEC number and number of continuation bytes followed by 16 bits for the device and 4 bits for the version.

14.3 JTAG ID Codes

Table 14-2. ID Code Structure

| DEVICE | REVISION ID[31:28] | DEVICE CODE ID[27:12] | MANUFACTURER'S CODE ID[11:1] | REQUIRED ID[0] |
|---------|--------------------|-----------------------|------------------------------|----------------|
| DS26519 | Consult factory | 0000000010001011 | 00010100001 | 1 |
| DS26518 | Consult factory | 0000000010001010 | 00010100001 | 1 |
| DS26514 | Consult factory | 0000000010001100 | 00010100001 | 1 |

14.4 Test Registers

IEEE 1149.1 requires a minimum of two test registers: the Bypass Register and the Boundary Scan Register. An optional test register, the Identification Register, has been included with the DS26518 design. The Identification Register is used in conjunction with the IDCODE instruction and the Test-Logic-Reset state of the TAP controller.

14.4.1 Boundary Scan Register

This register contains both a shift register path and a latched parallel output for all control cells and digital I/O cells, and is n bits in length.

14.4.2 Bypass Register

This register is a single one-bit shift register used in conjunction with the BYPASS, CLAMP, and HIGHZ instructions, providing a short path between JTDI and JTDO.

14.4.3 Identification Register

The Identification Register contains a 32-bit shift register and a 32-bit latched parallel output. This register is selected during the IDCODE instruction and when the TAP controller is in the Test-Logic-Reset state.

15. PIN CONFIGURATION

15.1 Pin Configuration—256-Ball TE-CSBGA

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | | |
|----------|----------|----------|--------------------------------|-----------------------|---------------------|-----------------------|-----------------------|-----------------|---------------------|-----------------------|-----------------------|-----------------------|----------------------|--------------------------------|-----------|-----------|----------|----------|
| A | TTIP1 | TTIP1 | TRING1 | RSYNC1 | TCHBLK1/ TCHCLK1 | TSIG2 | REFCLKIO | A11 | A7 | A1 | TSIG7 | RSIG7 | TSYNC8/ TSSYNClO8 | TRING8 | TTIP8 | TTIP8 | A | |
| B | ATVDD | ATVSS | TRING1 | TSYNCl1/ TSSYNClO1 | RCHBLK2/ RCHCLK2 | RSYNCl2 | MCLK | A10 | A8 | A2 | TSYNCl7/ TSSYNClO7 | RSER7 | TCLK8 | TRING8 | ATVSS | ATVDD | B | |
| C | RTIP1 | RRING1 | SPL_SEL/ AL/RSIG/ FLOS1 | RMSYNCl1/ RFSYNCl1 | TCLK1 | RMSYNCl2/ RFSYNCl2 | TCHBLK2/ TCHCLK2 | A12 | A6 | A0 | RSYNCl7 | RCHBLK7/ RCHCLK7 | TSIG8 | TSYSCLK8/ AL/RSIG/ FLOS8 | RRING8 | RTIP8 | C | |
| D | ARVDD | ARVSS | CLKO/ RLF/LTC1 | RSIG1 | TSIG1 | RSER2 | TCLK2 | DIGIOEN | A5 | TCHBLK7/ TCHCLK7 | RMSYNCl7/ RFSYNCl7 | TSER8 | RSYNCl8 | RSYSCLK8/ RLF/LTC8 | ARVSS | ARVDD | D | |
| E | ARVDD | ARVSS | RSYSCLK2/ RLF/LTC2 | RCHBLK1/ RCHCLK1 | RSER1 | RSIG2 | TSER2 | BPCLK1 | A4 | TCLK7 | TCHBLK8/ TCHCLK8 | RMSYNCl8/ RFSYNCl8 | RCLK8 | RSYSCLK7/ RLF/LTC7 | ARVSS | ARVDD | E | |
| F | RTIP2 | RRING2 | TSYSCLK2/ AL/RSIG/ FLOS2 | RCLK1 | JTCLK | TSER1 | TSYNCl2/ TSSYNClO2 | A9 | A3 | TSER7 | RSER8 | RSIG8 | RCLK7 | TSYSCLK7/ AL/RSIG/ FLOS7 | RRING7 | RTIP7 | F | |
| G | ATVDD | ATVSS | TRING2 | RCLK2 | DVDD33 | DVDD33 | DVDD18 | DVDD18 | DVDD18 | DVDD18 | DVDD33 | DVDD33 | RCHBLK8/ RCHCLK8 | TRING7 | ATVSS | ATVDD | G | |
| H | TTIP2 | TTIP2 | TRING2 | JTDI | DVDD33 | DVDD33 | ACVDD | DVDD33 | DVDD33 | DVDD33 | DVDD33 | DVSS | SCANMODE | TRING7 | TTIP7 | TTIP7 | H | |
| J | TTIP3 | TTIP3 | TRING3 | JTDO | RESREF | DVSS | ACVSS | DVSS | DVSS | DVSS | DVSS | DVSS | RESETB | RCLK6 | TRING6 | TTIP6 | TTIP6 | J |
| K | ATVDD | ATVSS | TRING3 | JTMS | DVSS | DVSS | DVSS | DVSS | DVSS | DVSS | DVSS | DVSS | RCLK5 | TRING6 | ATVSS | ATVDD | K | |
| L | RTIP3 | RRING3 | TSYSCLK3/ AL/RSIG/ FLOS3 | RCLK3 | JTRST | RCHBLK3/ RCHCLK3 | TCHBLK3/ TCHCLK3 | TCLK4 | D1/ SPI_MOSI | TCLK5 | TSER6 | RSYSCLK1 | TXENABLE/ SCAN_EN | TSYSCLK6/ AL/RSIG/ FLOS6 | RRING6 | RTIP6 | L | |
| M | ARVDD | ARVSS | RSYSCLK3/ RLF/LTC3 | RCLK4 | RSIG3 | TSYNCl3/ TSSYNClO3 | TSYNCl4/ TSSYNClO4 | RDB/ DSB | D5/ SPI_SWAP | TSER5 | RSER5 | RSER6 | BTS | RSYSCLK6/ RLF/LTC6 | ARVSS | ARVDD | M | |
| N | ARVDD | ARVSS | RSYSCLK4/ RLF/LTC4 | RSER3 | RSYNCl3 | RSER4 | TSER4 | D0/ SPI_MISO | D6/ SPI_CPHA | TSYNCl5/ TSSYNClO5 | TCLK6 | RMSYNCl6/ RFSYNCl6 | TSSYNClO | RSYSCLK5/ RLF/LTC5 | ARVSS | ARVDD | N | |
| P | RTIP4 | RRING4 | TSYSCLK4/ AL/RSIG/ FLOS4 | RMSYNCl3/ RFSYNCl3 | TCLK3 | RMSYNCl4/ RFSYNCl4 | TCHBLK4/ TCHCLK4 | D2/ SPI_SCLK | TCHBLK5/ TCHCLK5 | RMSYNCl5/ RFSYNCl5 | TCHBLK6/ TCHCLK6 | RSYNCl6 | TSYSCLK1 | TSYSCLK5/ AL/RSIG/ FLOS5 | RRING5 | RTIP5 | P | |
| R | ATVDD | ATVSS | TRING4 | TSER3 | RSIG4 | TSIG4 | WRB/ RWB | D4 | TNTB | RSYNCl5 | RSIG5 | TSIG6 | RSIG6 | TRING5 | ATVSS | ATVDD | R | |
| T | TTIP4 | TTIP4 | TRING4 | TSIG3 | RCHBLK4/ RCHCLK4 | RSYNCl4 | CSB | D3 | D7/ SPI_CPOL | TSIG5 | RCHBLK5/ RCHCLK5 | TSYNCl6/ TSSYNClO6 | RCHBLK6/ RCHCLK6 | TRING5 | TTIP5 | TTIP5 | T | |
| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | | |

16. PACKAGE INFORMATION

For the latest package outline information and land patterns, go to www.maxim-ic.com/packages.

The DS26518 uses a 256-lead thermally enhanced chip scale ball grid array (TE-CSBGA) package. The package dimensions are shown in Maxim document [56-G6028-001](#).

17. DOCUMENT REVISION HISTORY

| REVISION DATE | DESCRIPTION | PAGES CHANGED |
|---------------|--|------------------|
| 022007 | New Product Release. | — |
| 060607 | In the Absolute Maximum Ratings portion of Section 12, added Note 1 stating that specifications to -40°C are guaranteed by design (GBD) and not production tested. | 267 |
| 080607 | Updated data sheet to reflect new features with B1 die revision: HDLC-256 Controller—introduced in Section 9.10 and described in Section 9.10.3. Extended BERT Registers—introduced in Section 9.13 and defined in Section 10.6.1. | 75, 77, 101, 259 |
| 103008 | Removed commercial temperature range product option from the Ordering Information table and Operating Parameters (Section 12). | 1 |
| | Added content to TCLKn pin description (Section 8.1). | 21 |
| | Clarified how Read Bar/Data-Strobe Bar and Write Bar/ Read-Write Bar function in Intel and Motorola bus modes (Section 8.1). | 25 |
| | Added instruction in Step 5 of the Example Device Initialization and Sequence (Section 9.4.1) to increase the frequency of the internally generated clock which is supplied to the framers. | 34 |
| | Added definition for Receive Master Mode Register bit 5 (RMMR.5) which, when set, disables the receive-side synchronizer in the framer. This feature is new with revision B1. | 165 |
| | Replaced package drawing with table providing link to package drawing (Section 16). | 311 |

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