



# VNQ5050AK-E

## Quad channel high side driver with analog current sense for automotive applications

### Features

Parameters	Symbol	Value
Max supply voltage	$V_{CC}$	41 V
Operating voltage range	$V_{CC}$	4.5 to 36 V
Max on-state resistance (per ch.)	$R_{ON}$	50 m $\Omega$
Current limitation (typ)	$I_{LIMH}$	19 A
Off-state supply current	$I_S$	2 $\mu$ A <sup>(1)</sup>

1. Typical value with all loads connected.

#### ■ General features:

- Inrush current active management by power limitation
- Very low standby current
- 3.0V CMOS compatible input
- Optimized electromagnetic emission
- Very low electromagnetic susceptibility
- In compliance with the 2002/95/EC European directive

#### ■ Diagnostic functions:

- Proportional load current sense
- High current sense precision for wide current range
- Current sense disable
- Thermal shutdown indication
- Very low current sense leakage

#### ■ Protection:

- Undervoltage shutdown
- Overvoltage clamp
- Load current limitation
- Self limiting of fast thermal transients
- Protection against loss of ground and loss of  $V_{CC}$
- Thermal shutdown



- Reverse battery protection (see [Figure 25](#))
- Electrostatic discharge protection

### Application

- All types of resistive, inductive and capacitive loads.
- Suitable as LED driver.

### Description

The VNQ5050AK-E is a monolithic device made using STMicroelectronics VIPower M0-5 technology. It is intended for driving resistive or inductive loads with one side connected to ground. Active  $V_{CC}$  pin voltage clamp protects the device against low energy spikes (see ISO7637 transient compatibility table).

This device integrates an analog current sense which delivers a current proportional to the load current (according to a known ratio) when CS\_DIS is driven low or left open. When CS\_DIS is driven high, the CURRENT SENSE pin is in a high impedance condition.

Output current limitation protects the device in overload condition. In case of long overload duration, the device limits the dissipated power to a safe level up to thermal shutdown intervention. Thermal shutdown with automatic restart allows the device to recover normal operation as soon as the fault condition disappears.

Table 1. Device summary

Package	Order codes	
	Tube	Tape and Reel
PowerSSO-24	VNQ5050AK-E	VNQ5050AKTR-E

# Contents

<b>1</b>	<b>Block diagram and pin configuration</b>	<b>5</b>
<b>2</b>	<b>Electrical specifications</b>	<b>7</b>
2.1	Absolute maximum ratings	7
2.2	Thermal data	8
2.3	Electrical characteristics	9
2.4	Electrical characteristics curves	17
<b>3</b>	<b>Application information</b>	<b>20</b>
3.1	GND protection network against reverse battery	20
3.1.1	Solution 1: resistor in the ground line (RGND only)	20
3.1.2	Solution 2: a diode (DGND) in the ground line.	21
3.2	Load dump protection	21
3.3	Microcontroller I/Os protection	21
3.4	Maximum demagnetization energy (VCC = 13.5V)	23
<b>4</b>	<b>Package and PC board thermal data</b>	<b>24</b>
4.1	PowerSSO-24 thermal data	24
<b>5</b>	<b>Package and packing information</b>	<b>27</b>
5.1	ECOPACK® packages	27
5.2	PowerSSO-24™ mechanical data	27
5.3	Packing information	29
<b>6</b>	<b>Revision history</b>	<b>30</b>

## List of tables

Table 1.	Device summary . . . . .	1
Table 2.	Pin functions . . . . .	5
Table 3.	Suggested connections for unused and not connected pins . . . . .	6
Table 4.	Absolute maximum ratings . . . . .	7
Table 5.	Thermal data . . . . .	8
Table 6.	Power section . . . . .	9
Table 7.	Switching ( $V_{CC}=13V$ ) . . . . .	9
Table 8.	Current sense ( $8V < V_{CC} < 16V$ ) . . . . .	10
Table 9.	Protection . . . . .	11
Table 10.	Logic input . . . . .	12
Table 11.	Truth table. . . . .	15
Table 12.	Electrical transient requirements (part 1/3). . . . .	16
Table 13.	Electrical transient requirements (part 2/3). . . . .	16
Table 14.	Electrical transient requirements (part 3/3). . . . .	16
Table 15.	Thermal parameters . . . . .	26
Table 16.	PowerSSO-24™ mechanical data . . . . .	27
Table 17.	Document revision history . . . . .	30

## List of figures

Figure 1.	Block diagram . . . . .	5
Figure 2.	Configuration diagram (top view) . . . . .	6
Figure 3.	Current and voltage conventions . . . . .	7
Figure 4.	Current sense delay characteristics . . . . .	12
Figure 5.	Delay response time between rising edge of output current and rising edge of current sense (CS enabled) . . . . .	13
Figure 6.	Switching characteristics . . . . .	13
Figure 7.	$I_{OUT}/I_{SENSE}$ vs $I_{OUT}$ . . . . .	14
Figure 8.	Maximum current sense ratio drift vs load current . . . . .	14
Figure 9.	Output voltage drop limitation . . . . .	15
Figure 10.	Off-state output current . . . . .	17
Figure 11.	High level input current . . . . .	17
Figure 12.	Input clamp voltage . . . . .	17
Figure 13.	Input low level . . . . .	17
Figure 14.	Input high level . . . . .	17
Figure 15.	Input hysteresis voltage . . . . .	17
Figure 16.	On-state resistance vs $T_{case}$ . . . . .	18
Figure 17.	On-state resistance vs $V_{CC}$ . . . . .	18
Figure 18.	Undervoltage shutdown . . . . .	18
Figure 19.	Turn-on voltage slope . . . . .	18
Figure 20.	$I_{LIMH}$ vs $T_{case}$ . . . . .	18
Figure 21.	Turn-off voltage slope . . . . .	18
Figure 22.	CS_DIS high level voltage . . . . .	19
Figure 23.	CS_DIS clamp voltage . . . . .	19
Figure 24.	CS_DIS low level voltage . . . . .	19
Figure 25.	Application schematic . . . . .	20
Figure 26.	Waveforms . . . . .	22
Figure 27.	Maximum turn-off current versus inductance (for each channel) . . . . .	23
Figure 28.	PowerSSO-24 PC board . . . . .	24
Figure 29.	$R_{thj-amb}$ vs PCB copper area in open box free air condition (one channel on) . . . . .	24
Figure 30.	PowerSSO-24 thermal impedance junction ambient single pulse (one channel on) . . . . .	25
Figure 31.	Thermal fitting model of a double channel HSD in PowerSSO-24 . . . . .	25
Figure 32.	PowerSSO-24™ package dimensions . . . . .	28
Figure 33.	PowerSSO-24 tube shipment (no suffix) . . . . .	29
Figure 34.	PowerSSO-24 tape and reel shipment (suffix "TR") . . . . .	29

# 1 Block diagram and pin configuration

Figure 1. Block diagram

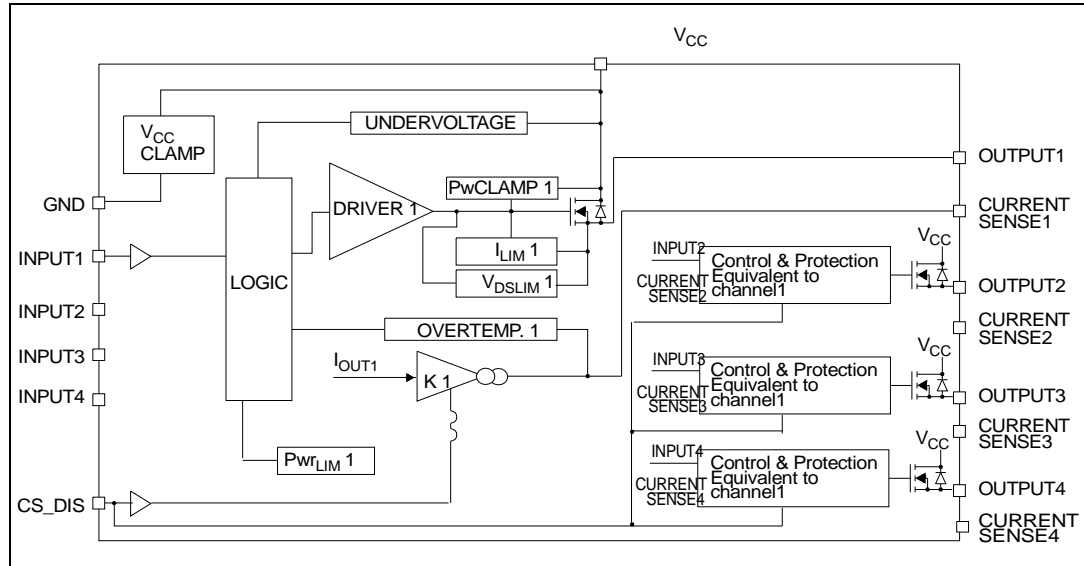


Table 2. Pin functions

Name	Function
V <sub>CC</sub>	Battery connection
OUTPUT <sub>n</sub>	Power output
GND	Ground connection. Must be reverse battery protected by an external diode/resistor network
INPUT <sub>n</sub>	Voltage controlled input pin with hysteresis, CMOS compatible. Controls output switch state
CURRENT SENSE <sub>n</sub>	Analog current sense pin, delivers a current proportional to the load current
CS_DIS	Active high CMOS compatible pin, to disable the current sense pin

Figure 2. Configuration diagram (top view)

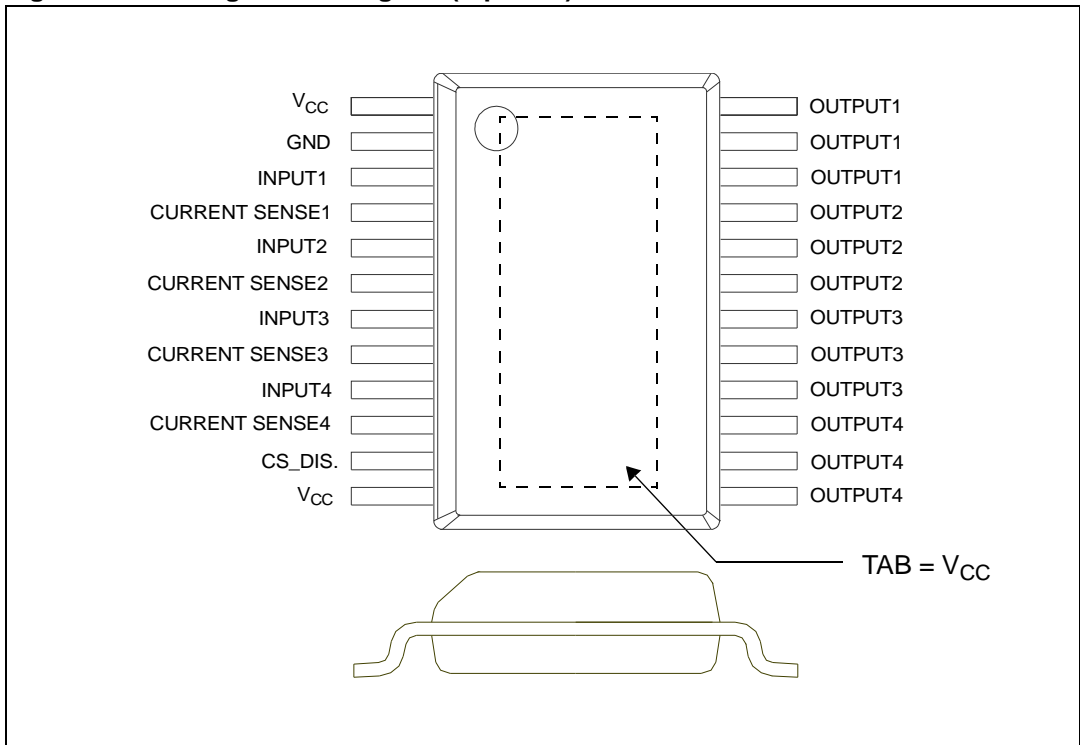


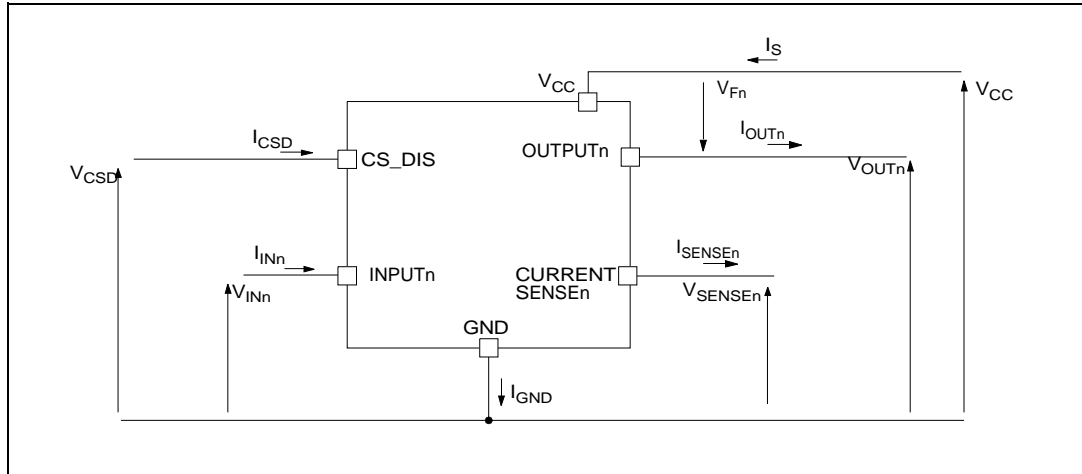
Table 3. Suggested connections for unused and not connected pins

Connection/pin	Current sense	N.C.	Output	Input	CS_DIS
Floating	N.R. <sup>(1)</sup>	X	X	X	X
To ground	Through 1 kΩ resistor	X	N.R.	Through 10 kΩ resistor	Through 10 kΩ resistor

1. Not recommended.

## 2 Electrical specifications

Figure 3. Current and voltage conventions



Note:  $V_{Fn} = V_{OUTn} - V_{CC}$  during reverse battery condition.

### 2.1 Absolute maximum ratings

Stress values that exceed those listed in the “Absolute maximum ratings” table can cause permanent damage to the device. These are stress ratings only, and operation of the device at these, or any other conditions greater than those, indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics sure program and other relevant quality documents.

Table 4. Absolute maximum ratings

Symbol	Parameter	Value	Unit
$V_{CC}$	DC supply voltage	41	V
$-V_{CC}$	Reverse DC supply voltage	0.3	V
$-I_{GND}$	DC reverse ground pin current	200	mA
$I_{OUT}$	DC output current	Internally limited	A
$-I_{OUT}$	Reverse DC output current	20	A
$I_{IN}$	DC input current	-1 to 10	mA
$I_{CSD}$	DC current sense disable input current	-1 to 10	mA
$-I_{CSENSE}$	DC reverse CS pin current	200	mA
$V_{CSENSE}$	Current sense maximum voltage	$V_{CC}-41$ $+V_{CC}$	V V
$E_{MAX}$	Maximum switching energy (single pulse) ( $L=3$ mH; $R_L=0$ $\Omega$ ; $V_{bat}=13.5$ V; $T_{jstart}=150$ $^{\circ}C$ ; $I_{OUT} = I_{limL}(Typ.)$ )	104	mJ

**Table 4. Absolute maximum ratings (continued)**

Symbol	Parameter	Value	Unit
V <sub>ESD</sub>	Electrostatic discharge (human body model: R=1.5KΩ; C=100pF)		
	– Input	4000	V
	– Current sense	2000	V
	– CS_DIS	4000	V
	– Output	5000	V
	– V <sub>CC</sub>	5000	V
V <sub>ESD</sub>	Charge device model (CDM-AEC-Q100-011)	750	V
T <sub>j</sub>	Junction operating temperature	-40 to 150	°C
T <sub>stg</sub>	Storage temperature	-55 to 150	°C

## 2.2 Thermal data

**Table 5. Thermal data**

Symbol	Parameter	Max value	Unit
R <sub>thj-case</sub>	Thermal resistance junction-case (With one channel ON)	2.8	°C/W
R <sub>thj-amb</sub>	Thermal resistance junction-ambient	See <a href="#">Figure 29</a>	°C/W



## 2.3 Electrical characteristics

Values specified in this section are for  $8\text{ V} < V_{CC} < 36\text{ V}$ ,  $-40\text{ °C} < T_j < 150\text{ °C}$ , unless otherwise stated.

**Table 6. Power section**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{CC}$	Operating supply voltage		4.5	13	36	V
$V_{USD}$	Undervoltage shutdown		-	3.5	4.5	V
$V_{USDhyst}$	Undervoltage shutdown hysteresis		-	0.5	-	V
$R_{ON}$	On-state resistance	$I_{OUT}=2\text{ A}$ ; $T_j=25\text{ °C}$ $I_{OUT}=2\text{ A}$ ; $T_j=150\text{ °C}$ $I_{OUT}=2\text{ A}$ ; $V_{CC}=5\text{ V}$ ; $T_j=25\text{ °C}$	-	-	50 100 65	mΩ mΩ mΩ
$V_{clamp}$	Clamp voltage	$I_S=20\text{ mA}$	41	46	52	V
$I_S$	Supply current	Off-State; $V_{CC}=13\text{ V}$ ; $T_j=25\text{ °C}$ ; $V_{IN}=V_{OUT}=V_{SENSE}=V_{CSD}=0\text{ V}$ On-State; $V_{CC}=13\text{ V}$ ; $V_{IN}=5\text{ V}$ ; $I_{OUT}=0\text{ A}$	-	2 <sup>(1)</sup> 8	5 <sup>(1)</sup> 14	μA mA
$I_{L(off)}$	Off-state output current <sup>(2)</sup>	$V_{IN}=V_{OUT}=0\text{ V}$ ; $V_{CC}=13\text{ V}$ ; $T_j=25\text{ °C}$ $V_{IN}=V_{OUT}=0\text{ V}$ ; $V_{CC}=13\text{ V}$ ; $T_j=125\text{ °C}$	0 0	0.01	3 5	μA
$V_F$	Output - $V_{CC}$ diode voltage <sup>(2)</sup>	$-I_{OUT}=2\text{ A}$ ; $T_j=150\text{ °C}$	-	-	0.7	V

1. PowerMOS leakage included.

2. For each channel.

**Table 7. Switching ( $V_{CC}=13\text{V}$ )**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$R_L=6.5\text{ Ω}$ (see <a href="#">Figure 6</a> )	-	20	-	μs
$t_{d(off)}$	Turn-off delay time	$R_L=6.5\text{ Ω}$ (see <a href="#">Figure 6</a> )	-	45	-	μs
$(dV_{OUT}/dt)_{on}$	Turn-on voltage slope	$R_L=6.5\text{ Ω}$	-	See <a href="#">Figure 19</a>	-	V/μs
$(dV_{OUT}/dt)_{off}$	Turn-off voltage slope	$R_L=6.5\text{ Ω}$	-	See <a href="#">Figure 21</a>	-	V/μs
$W_{ON}$	Switching energy losses during $t_{won}$	$R_L=6.5\text{ Ω}$ (see <a href="#">Figure 6</a> )	-	0.15	-	mJ
$W_{OFF}$	Switching energy losses during $t_{woff}$	$R_L=6.5\text{ Ω}$ (see <a href="#">Figure 6</a> )	-	0.3	-	mJ

Table 8. Current sense ( $8V < V_{CC} < 16V$ )

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$K_0$	$I_{OUT}/I_{SENSE}$	$I_{OUT} = 0.05 A$ ; $V_{SENSE} = 0.5 V$ ; $V_{CSD} = 0 V$ ; $T_j = -40\text{ }^\circ\text{C} \dots 150\text{ }^\circ\text{C}$	1340	2420	3460	
$K_1$	$I_{OUT}/I_{SENSE}$	$I_{OUT} = 1 A$ ; $V_{SENSE} = 0.5 V$ ; $V_{CSD} = 0 V$ ; $T_j = -40\text{ }^\circ\text{C} \dots 150\text{ }^\circ\text{C}$ $T_j = 25\text{ }^\circ\text{C} \dots 150\text{ }^\circ\text{C}$	1370 1510	1860 1860	2510 2210	
$dK_1/K_1^{(1)}$	Current sense ratio drift	$I_{OUT} = 1 A$ ; $V_{SENSE} = 0.5 V$ ; $V_{CSD} = 0 V$ ; $T_j = -40\text{ }^\circ\text{C}$ to $150\text{ }^\circ\text{C}$	-10	-	10	%
$K_2$	$I_{OUT}/I_{SENSE}$	$I_{OUT} = 2 A$ ; $V_{SENSE} = 4 V$ ; $V_{CSD} = 0 V$ ; $T_j = -40\text{ }^\circ\text{C} \dots 150\text{ }^\circ\text{C}$ $T_j = 25\text{ }^\circ\text{C} \dots 150\text{ }^\circ\text{C}$	1590 1600	1760 1760	2140 1930	
$dK_2/K_2^{(1)}$	Current sense ratio drift	$I_{OUT} = 2 A$ ; $V_{SENSE} = 4 V$ ; $V_{CSD} = 0 V$ ; $T_j = -40\text{ }^\circ\text{C}$ to $150\text{ }^\circ\text{C}$	-8	-	8	%
$K_3$	$I_{OUT}/I_{SENSE}$	$I_{OUT} = 4 A$ ; $V_{SENSE} = 4 V$ ; $V_{CSD} = 0 V$ ; $T_j = -40\text{ }^\circ\text{C} \dots 150\text{ }^\circ\text{C}$ $T_j = 25\text{ }^\circ\text{C} \dots 150\text{ }^\circ\text{C}$	1650 1650	1740 1740	1950 1830	-
$dK_3/K_3^{(1)}$	Current sense ratio drift	$I_{OUT} = 4 A$ ; $V_{SENSE} = 4 V$ ; $V_{CSD} = 0 V$ ; $T_j = -40\text{ }^\circ\text{C}$ to $150\text{ }^\circ\text{C}$	-5	-	5	%
$I_{SENSE0}$	Analog sense leakage current	$I_{OUT} = 0 A$ ; $V_{SENSE} = 0 V$ ; $V_{CSD} = 5 V$ ; $V_{IN} = 0 V$ ; $T_j = -40\text{ }^\circ\text{C} \dots 150\text{ }^\circ\text{C}$	0	-	1	$\mu A$
		$V_{CSD} = 0 V$ ; $V_{IN} = 5 V$ ; $T_j = -40\text{ }^\circ\text{C} \dots 150\text{ }^\circ\text{C}$	0	-	2	$\mu A$
		$I_{OUT} = 2 A$ ; $V_{SENSE} = 0 V$ ; $V_{CSD} = 5 V$ ; $V_{IN} = 5 V$ ; $T_j = -40\text{ }^\circ\text{C} \dots 150\text{ }^\circ\text{C}$	0	-	1	$\mu A$
$I_{OL}$	Openload ON state current detection threshold	$V_{IN} = 5 V$ , $I_{SENSE} = 5\text{ } \mu A$	4	-	20	mA
$V_{SENSE}$	Max analog sense output voltage	$I_{OUT} = 4 A$ ; $V_{CSD} = 0 V$	5	-	-	V
$V_{SENSEH}$	Analog sense output voltage in over temperature condition	$V_{CC} = 13 V$ ; $R_{SENSE} = 10\text{ } K\Omega$	-	9	-	V

**Table 8. Current sense (8V<V<sub>CC</sub><16V) (continued)**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I <sub>SENSEH</sub>	Analog sense output current in over temperature condition	V <sub>CC</sub> = 13 V; V <sub>SENSE</sub> = 5 V	-	8	-	mA
t <sub>DSENSE1H</sub>	Delay response time from falling edge of CS_DIS pin	V <sub>SENSE</sub> <4 V, 0.5 A<I <sub>out</sub> <4 A I <sub>SENSE</sub> = 90 % of I <sub>SENSE max</sub> (see <a href="#">Figure 4</a> )	-	50	100	μs
t <sub>DSENSE1L</sub>	Delay response time from rising edge of CS_DIS pin	V <sub>SENSE</sub> <4 V, 0.5 A<I <sub>out</sub> <4 A I <sub>SENSE</sub> =10 % of I <sub>SENSE max</sub> (see <a href="#">Figure 4</a> )	-	5	20	μs
t <sub>DSENSE2H</sub>	Delay response time from rising edge of INPUT pin	V <sub>SENSE</sub> <4 V, 0.5 A<I <sub>out</sub> <4 A I <sub>SENSE</sub> =90 % of I <sub>SENSE max</sub> (see <a href="#">Figure 4</a> )	-	80	250	μs
Δt <sub>DSENSE2H</sub>	Delay response time between rising edge of output current and rising edge of current sense	V <sub>SENSE</sub> <4 V, I <sub>SENSE</sub> =90 % of I <sub>SENSEMAX</sub> , I <sub>OUT</sub> =90 % of I <sub>OUTMAX</sub> I <sub>OUTMAX</sub> =2 A (see <a href="#">Figure 5</a> )	-	-	65	μs
t <sub>DSENSE2L</sub>	Delay response time from falling edge of INPUT pin	V <sub>SENSE</sub> <4 V, 0.5 A<I <sub>out</sub> <4 A I <sub>SENSE</sub> =10 % of I <sub>SENSE max</sub> (see <a href="#">Figure 4</a> )	-	100	250	μs

1. Parameter guaranteed by design; it is not tested.

**Table 9. Protection<sup>(1)</sup>**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I <sub>limH</sub>	DC short circuit current	V <sub>CC</sub> =13 V 5 V<V <sub>CC</sub> <36 V	13.5	19	26.5 26.5	A A
I <sub>limL</sub>	Short circuit current during thermal cycling	V <sub>CC</sub> =13 V; T <sub>R</sub> <T <sub>j</sub> <T <sub>TSD</sub>	-	7	-	A
T <sub>TSD</sub>	Shutdown temperature		150	175	200	°C
T <sub>R</sub>	Reset temperature		T <sub>RS</sub> + 1	T <sub>RS</sub> + 5	-	°C
T <sub>RS</sub>	Thermal reset of STATUS		135	-	-	°C
T <sub>HYST</sub>	Thermal hysteresis (T <sub>TSD</sub> -T <sub>R</sub> )		-	7	-	°C
V <sub>DEMAG</sub>	Turn-off output voltage clamp	I <sub>OUT</sub> =2 A; V <sub>IN</sub> =0; L=6 mH	V <sub>CC</sub> -41	V <sub>CC</sub> -46	V <sub>CC</sub> -52	V
V <sub>ON</sub>	Output voltage drop limitation	I <sub>OUT</sub> =0.1 A; T <sub>j</sub> =-40 °C...150 °C (see <a href="#">Figure 9</a> )	-	25	-	mV

1. To ensure long term reliability under heavy overload or short circuit conditions, protection and related diagnostic signals must be used together with a proper software strategy. If the device is subjected to abnormal conditions, this software must limit the duration and number of activation cycles.

**Table 10. Logic input**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{IL}$	Input low level voltage		-	-	0.9	V
$I_{IL}$	Low level input current	$V_{IN} = 0.9\text{ V}$	1	-	-	$\mu\text{A}$
$V_{IH}$	Input high level voltage		2.1	-	-	V
$I_{IH}$	High level input current	$V_{IN} = 2.1\text{ V}$	-	-	10	$\mu\text{A}$
$V_{I(hyst)}$	Input hysteresis voltage		0.25	-	-	V
$V_{ICL}$	Input clamp voltage	$I_{IN} = 1\text{ mA}$ $I_{IN} = -1\text{ mA}$	5.5	-0.7	7	V V
$V_{CSDL}$	CS_DIS low level voltage		-	-	0.9	V
$I_{CSDL}$	Low level CS_DIS current	$V_{CSD} = 0.9\text{ V}$	1	-	-	$\mu\text{A}$
$V_{CSDH}$	CS_DIS high level voltage		2.1	-	-	V
$I_{CSDH}$	High level CS_DIS current	$V_{CSD} = 2.1\text{ V}$	-	-	10	$\mu\text{A}$
$V_{CSD(hyst)}$	CS_DIS hysteresis voltage		0.25	-	-	V
$V_{CSCL}$	CS_DIS clamp voltage	$I_{CSD} = 1\text{ mA}$ $I_{CSD} = -1\text{ mA}$	5.5	-0.7	7	V V

**Figure 4. Current sense delay characteristics**

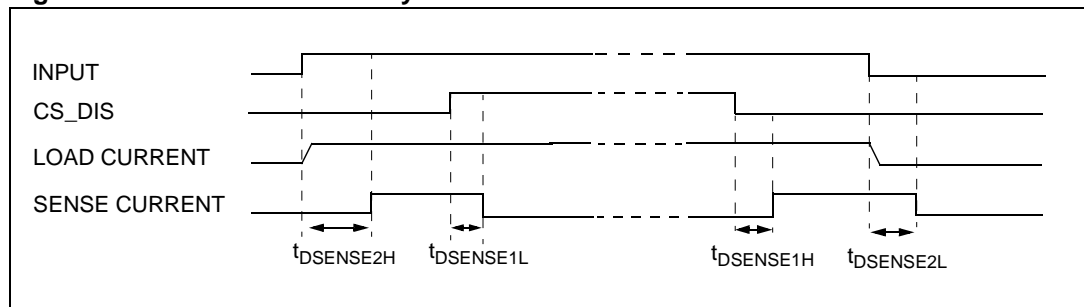


Figure 5. Delay response time between rising edge of output current and rising edge of current sense (CS enabled)

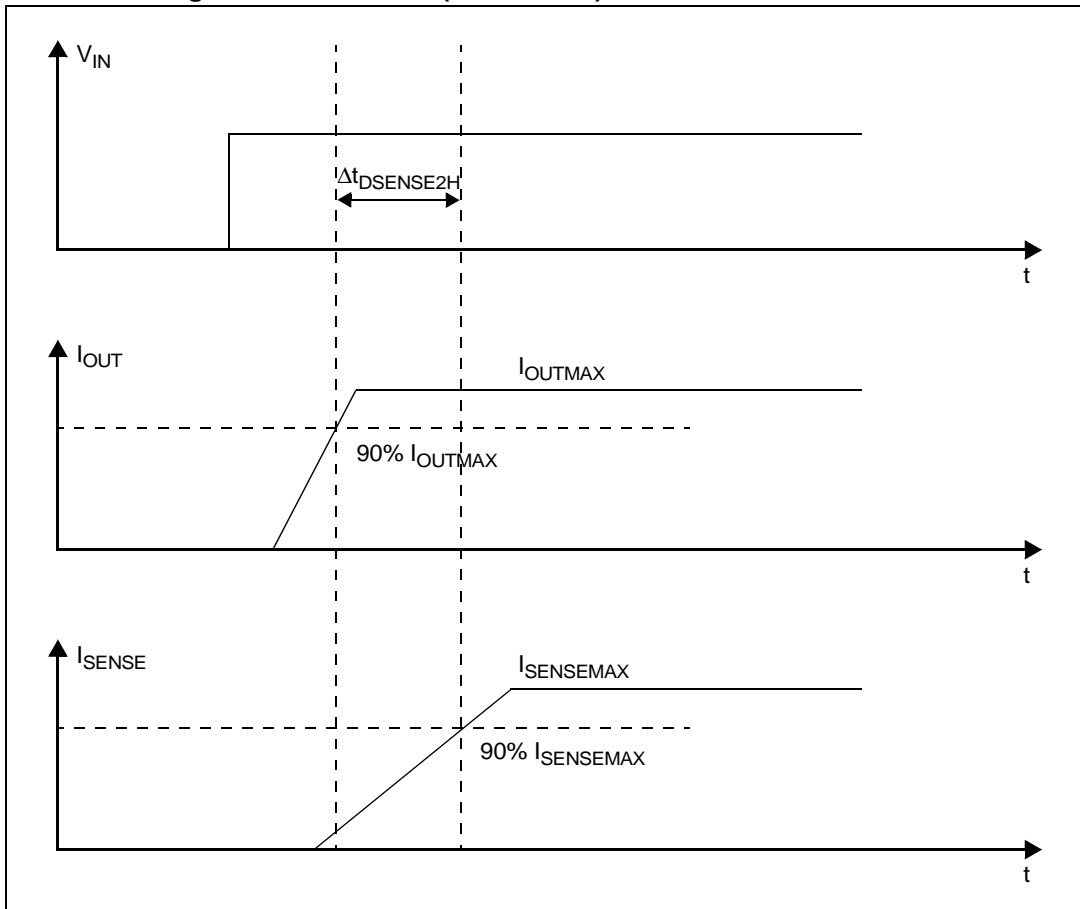


Figure 6. Switching characteristics

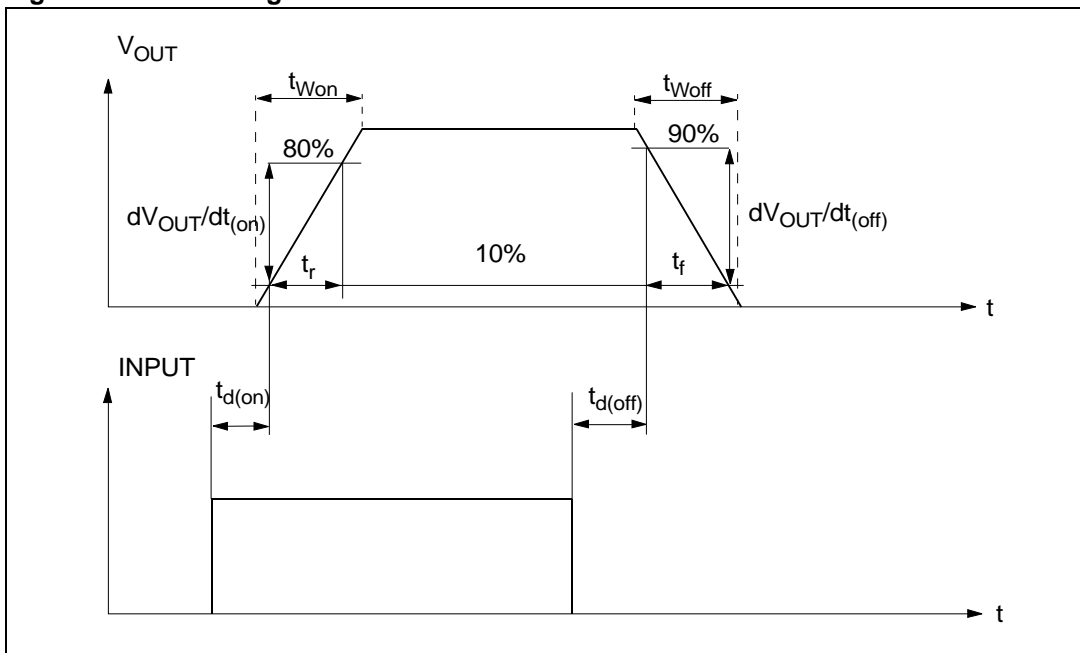


Figure 7.  $I_{OUT}/I_{SENSE}$  vs  $I_{OUT}$

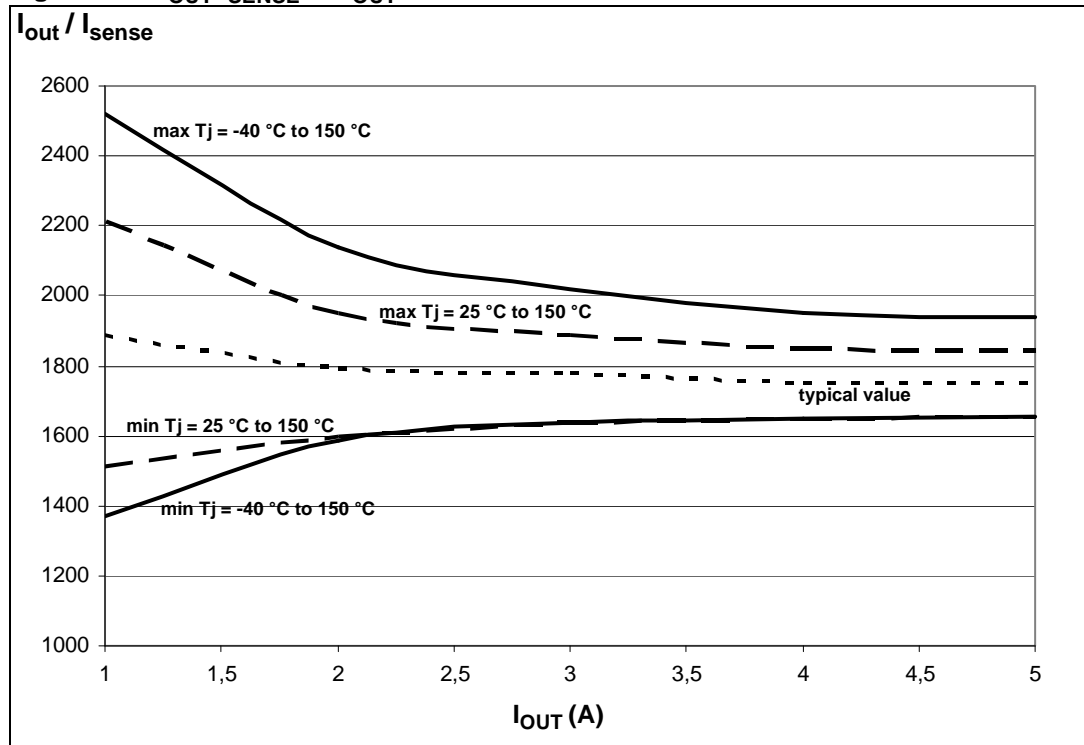
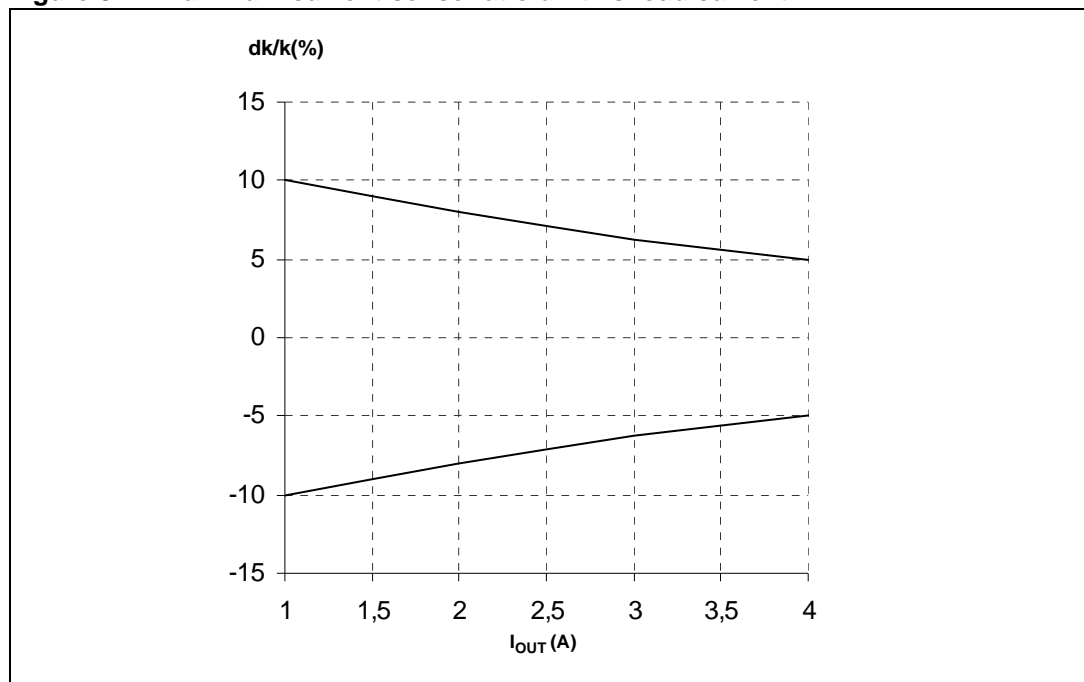


Figure 8. Maximum current sense ratio drift vs load current



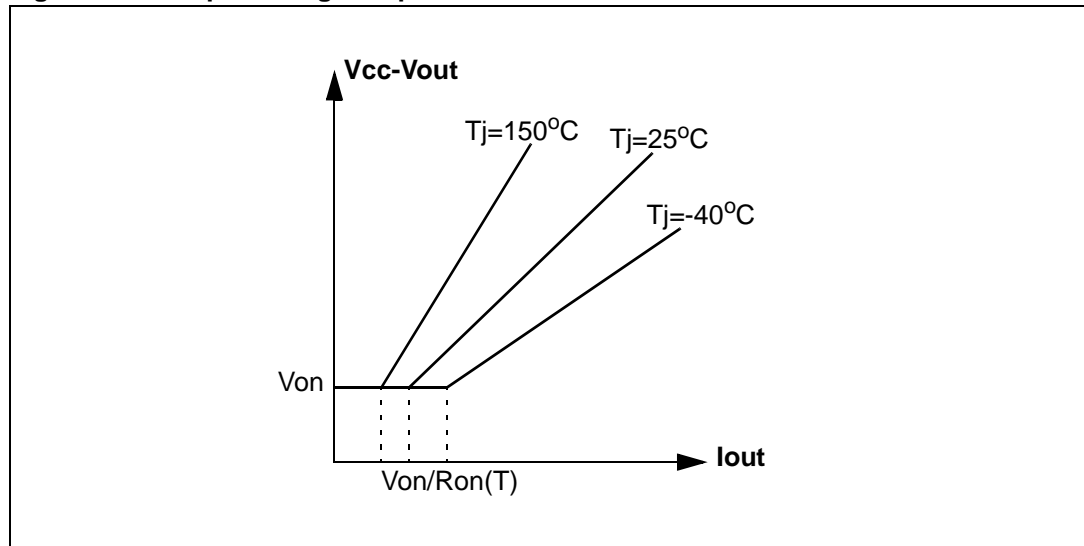
Note: Parameter guaranteed by design; it is not tested.

**Table 11. Truth table**

Conditions	Input	Output	Sense ( $V_{CSD}=0\text{ V}$ ) <sup>(1)</sup>
Normal operation	L	L	0
	H	H	Nominal
Over temperature	L	L	0
	H	L	$V_{SENSEH}$
Undervoltage	L	L	0
	H	L	0
Short circuit to GND ( $R_{sc} \leq 10\text{ m}\Omega$ )	L	L	0
	H	L	0 if $T_j < T_{TSD}$
	H	L	$V_{SENSEH}$ if $T_j > T_{TSD}$
Short circuit to $V_{CC}$	L	H	0
	H	H	< Nominal
Negative output voltage clamp	L	L	0

1. If the  $V_{CSD}$  is high, the SENSE output is at a high impedance, its potential depends on leakage currents and external circuit.

**Figure 9. Output voltage drop limitation**



**Table 12. Electrical transient requirements (part 1/3)**

ISO 7637-2: 2004(E) test pulse	Test levels		Number of pulses or test times	Burst cycle/pulse repetition time		Delays and Impedance
	III	IV				
1	-75 V	-100 V	5000 pulses	0.5 s	5 s	2 ms, 10 Ω
2a	+37 V	+50 V	5000 pulses	0.2 s	5 s	50 μs, 2 Ω
3a	-100 V	-150 V	1h	90 ms	100 ms	0.1 μs, 50 Ω
3b	+75 V	+100 V	1h	90 ms	100 ms	0.1 μs, 50 Ω
4	-6 V	-7 V	1 pulse	-		100 ms, 0.01 Ω
5b <sup>(2)</sup>	+65 V	+87 V	1 pulse	-		400 ms, 2 Ω

**Table 13. Electrical transient requirements (part 2/3)**

ISO 7637-2: 2004(E) test pulse	Test level results <sup>(1)</sup>	
	III	IV
1	C	C
2a	C	C
3a	C	C
3b	C	C
4	C	C
5b <sup>(2)</sup>	C	C

1. The above test levels must be considered referred to Vcc = 13.5V except for pulse 5b.
2. Valid in case of external load dump clamp: 40V maximum referred to ground.

**Table 14. Electrical transient requirements (part 3/3)**

Class	Contents
C	All functions of the device are performed as designed after exposure to disturbance.
E	One or more functions of the device are not performed as designed after exposure to disturbance and cannot be returned to proper operation without replacing the device.



## 2.4 Electrical characteristics curves

Figure 10. Off-state output current

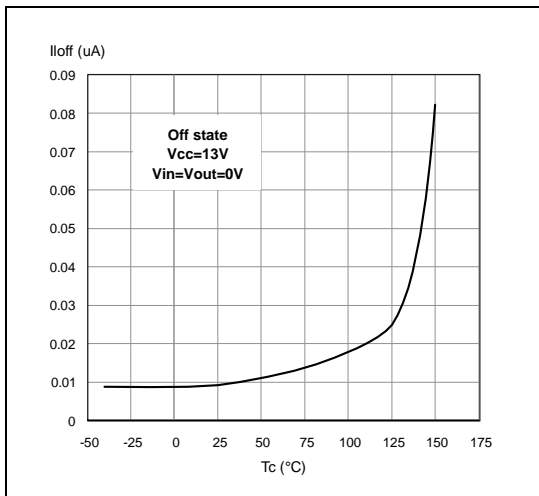


Figure 11. High level input current

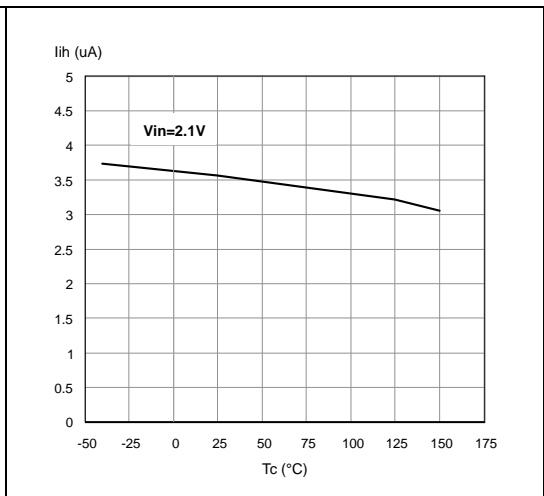


Figure 12. Input clamp voltage

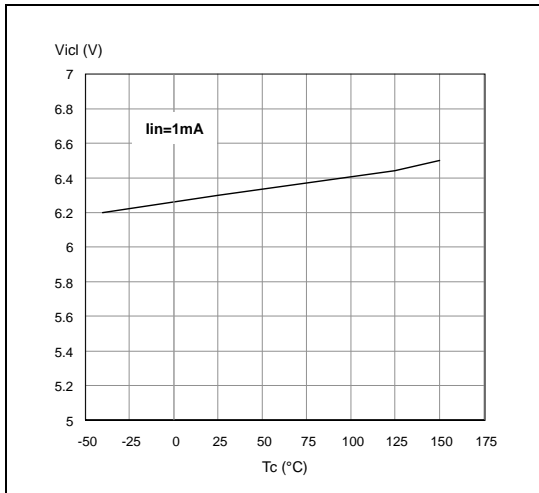


Figure 13. Input low level

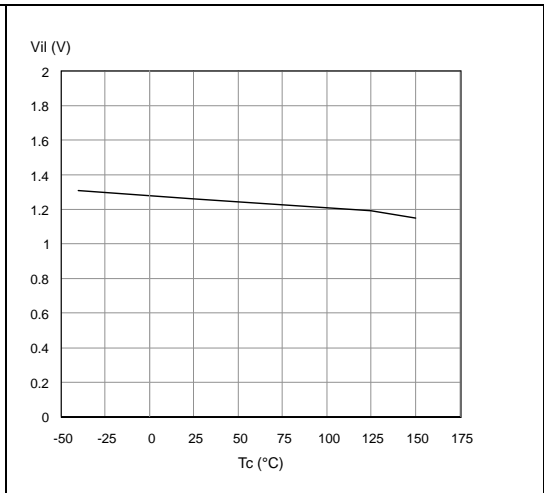


Figure 14. Input high level

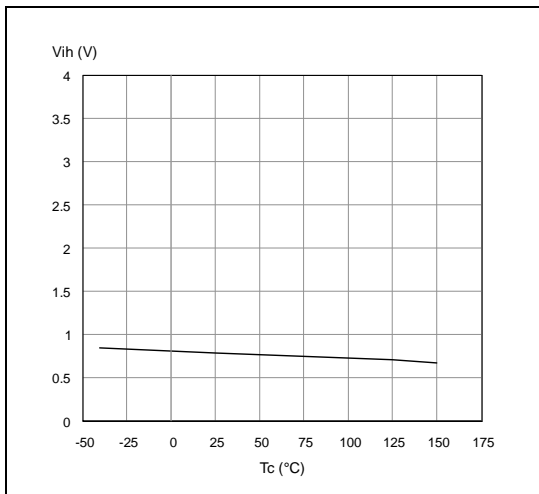


Figure 15. Input hysteresis voltage

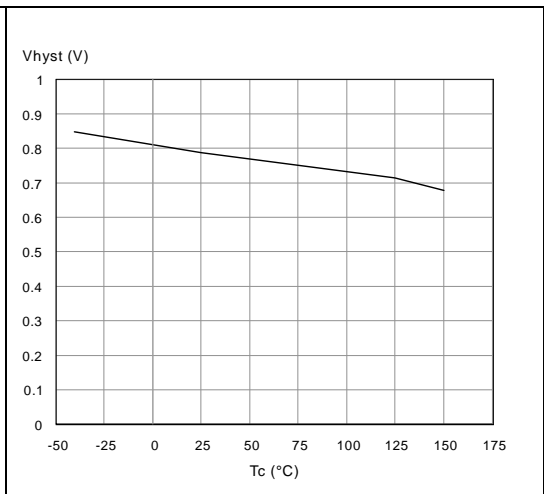


Figure 16. On-state resistance vs  $T_{case}$

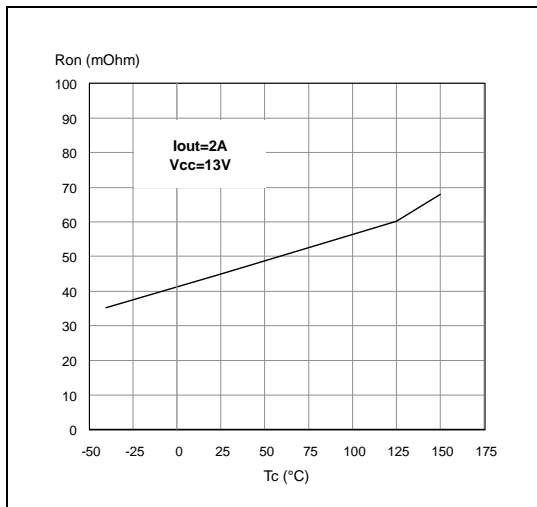


Figure 17. On-state resistance vs  $V_{CC}$

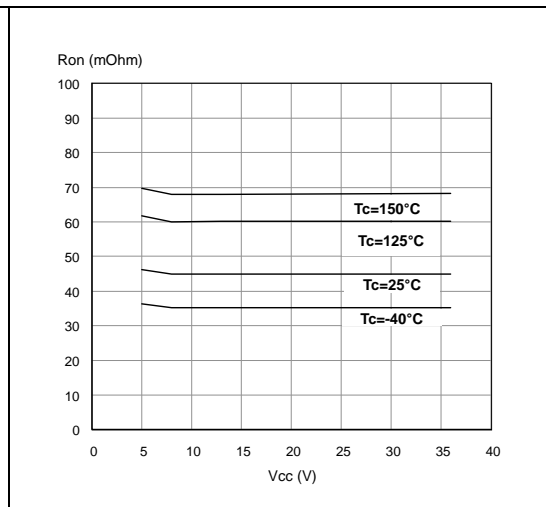


Figure 18. Undervoltage shutdown

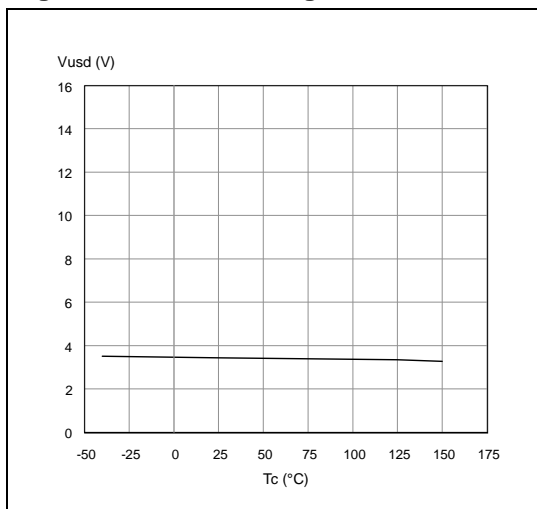


Figure 19. Turn-on voltage slope

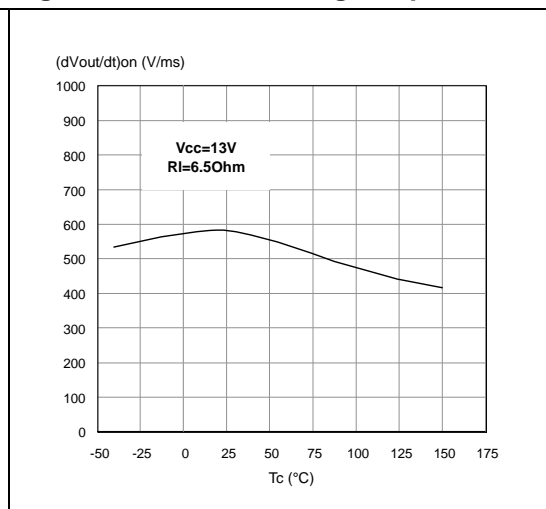


Figure 20.  $I_{LIMH}$  vs  $T_{case}$

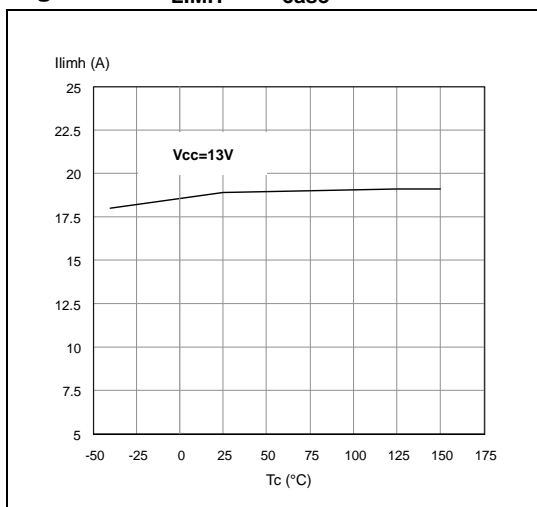


Figure 21. Turn-off voltage slope

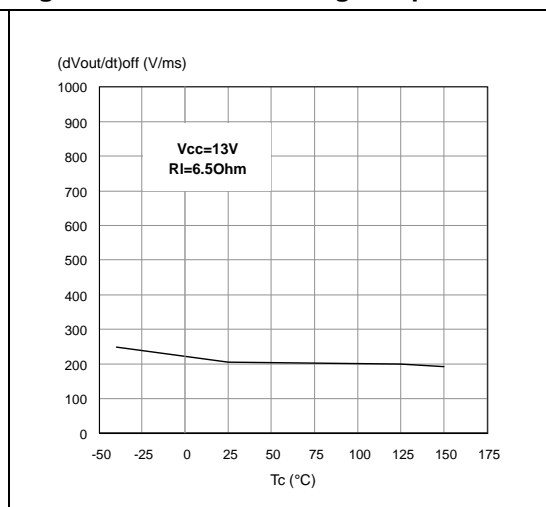


Figure 22. CS\_DIS high level voltage

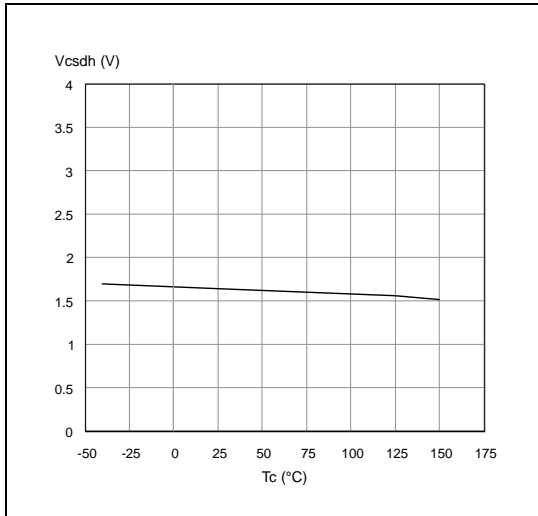


Figure 23. CS\_DIS clamp voltage

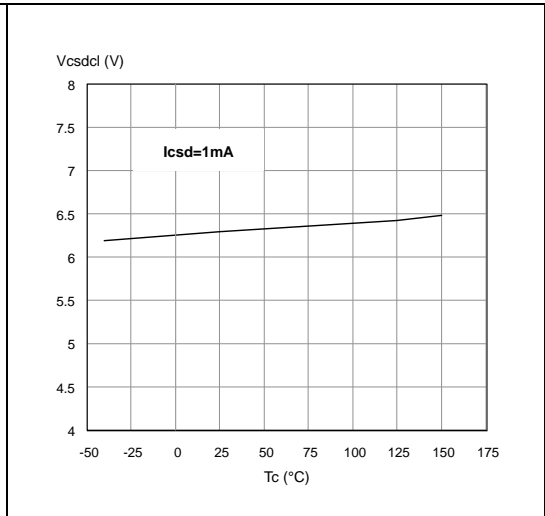
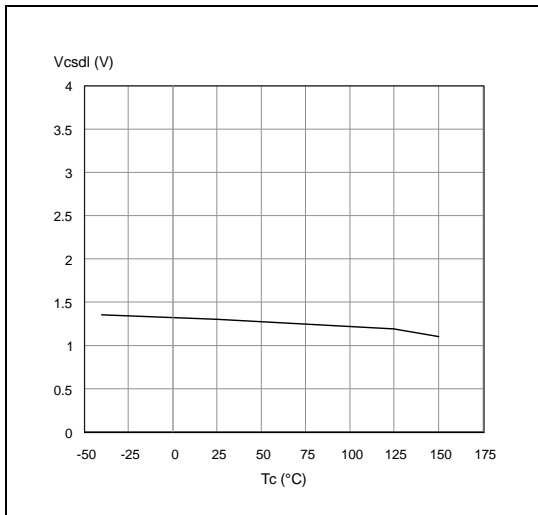
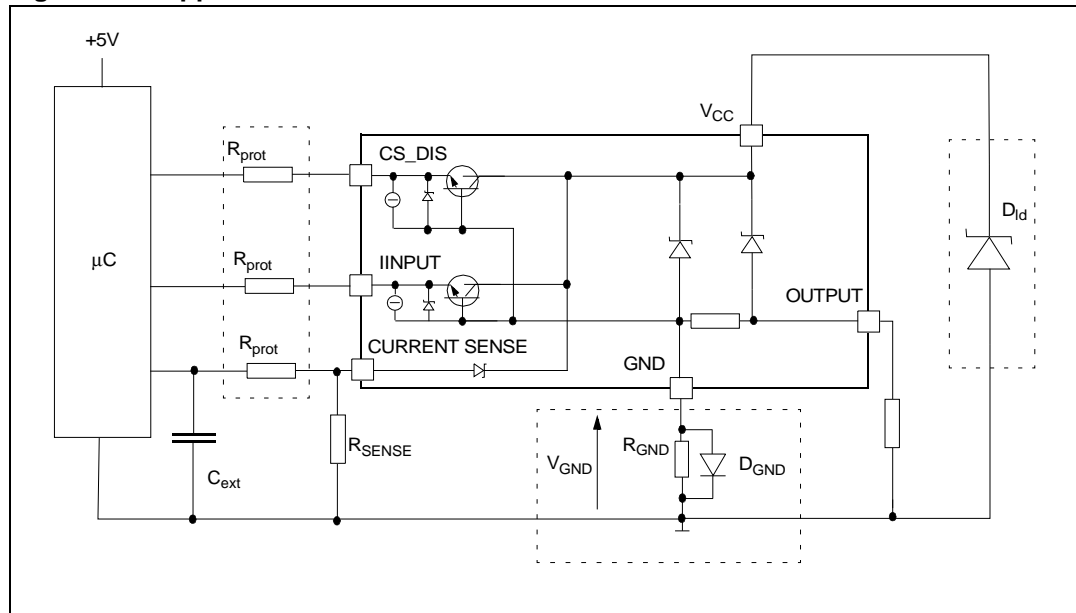


Figure 24. CS\_DIS low level voltage



### 3 Application information

Figure 25. Application schematic



Note: Channel 2, 3, 4 have the same internal circuit as channel 1.

### 3.1 GND protection network against reverse battery

#### 3.1.1 Solution 1: resistor in the ground line (R\_GND only)

This can be used with any type of load.

The following is an indication on how to dimension the R\_GND resistor.

1.  $R_{GND} \leq 600 \text{ mV} / (I_{S(on)max})$ .
2.  $R_{GND} \geq (-V_{CC}) / (-I_{GND})$

where  $-I_{GND}$  is the DC reverse ground pin current and can be found in the absolute maximum rating section of the device datasheet.

Power Dissipation in R\_GND (when  $V_{CC} < 0$ : during reverse battery situations) is:

$$P_D = (-V_{CC})^2 / R_{GND}$$

This resistor can be shared amongst several different HSDs. Please note that the value of this resistor should be calculated with formula (1) where  $I_{S(on)max}$  becomes the sum of the maximum on-state currents of the different devices.

Please note that if the microprocessor ground is not shared by the device ground then the R\_GND will produce a shift ( $I_{S(on)max} * R_{GND}$ ) in the input thresholds and the status output values. This shift will vary depending on how many devices are ON in the case of several high side drivers sharing the same R\_GND.

If the calculated power dissipation leads to a large resistor or several devices have to share the same resistor then ST suggests to utilize Solution 2 (see below).

### 3.1.2 Solution 2: a diode ( $D_{GND}$ ) in the ground line.

A resistor ( $R_{GND} = 1 \text{ k}\Omega$ ) should be inserted in parallel to  $D_{GND}$  if the device drives an inductive load.

This small signal diode can be safely shared amongst several different HSDs. Also in this case, the presence of the ground network will produce a shift ( $\approx 600\text{mV}$ ) in the input threshold and in the status output values if the microprocessor ground is not common to the device ground. This shift will not vary if more than one HSD shares the same diode/resistor network.

## 3.2 Load dump protection

$D_{ld}$  is necessary (Voltage Transient Suppressor) if the load dump peak voltage exceeds the  $V_{CC}$  max DC rating. The same applies if the device is subject to transients on the  $V_{CC}$  line that are greater than the ones shown in the ISO T/R 7637/1 table.

## 3.3 Microcontroller I/Os protection

If a ground protection network is used and negative transients are present on the  $V_{CC}$  line, the control pins will be pulled negative. ST suggests to insert a resistor ( $R_{prot}$ ) in line to prevent the  $\mu\text{C}$  I/Os pins to latch-up.

The value of these resistors is a compromise between the leakage current of  $\mu\text{C}$  and the current required by the HSD I/Os (Input levels compatibility) with the latch-up limit of  $\mu\text{C}$  I/Os.

$$-V_{CCpeak}/I_{latchup} \leq R_{prot} \leq (V_{OH\mu C} - V_{IH} - V_{GND}) / I_{IHmax}$$

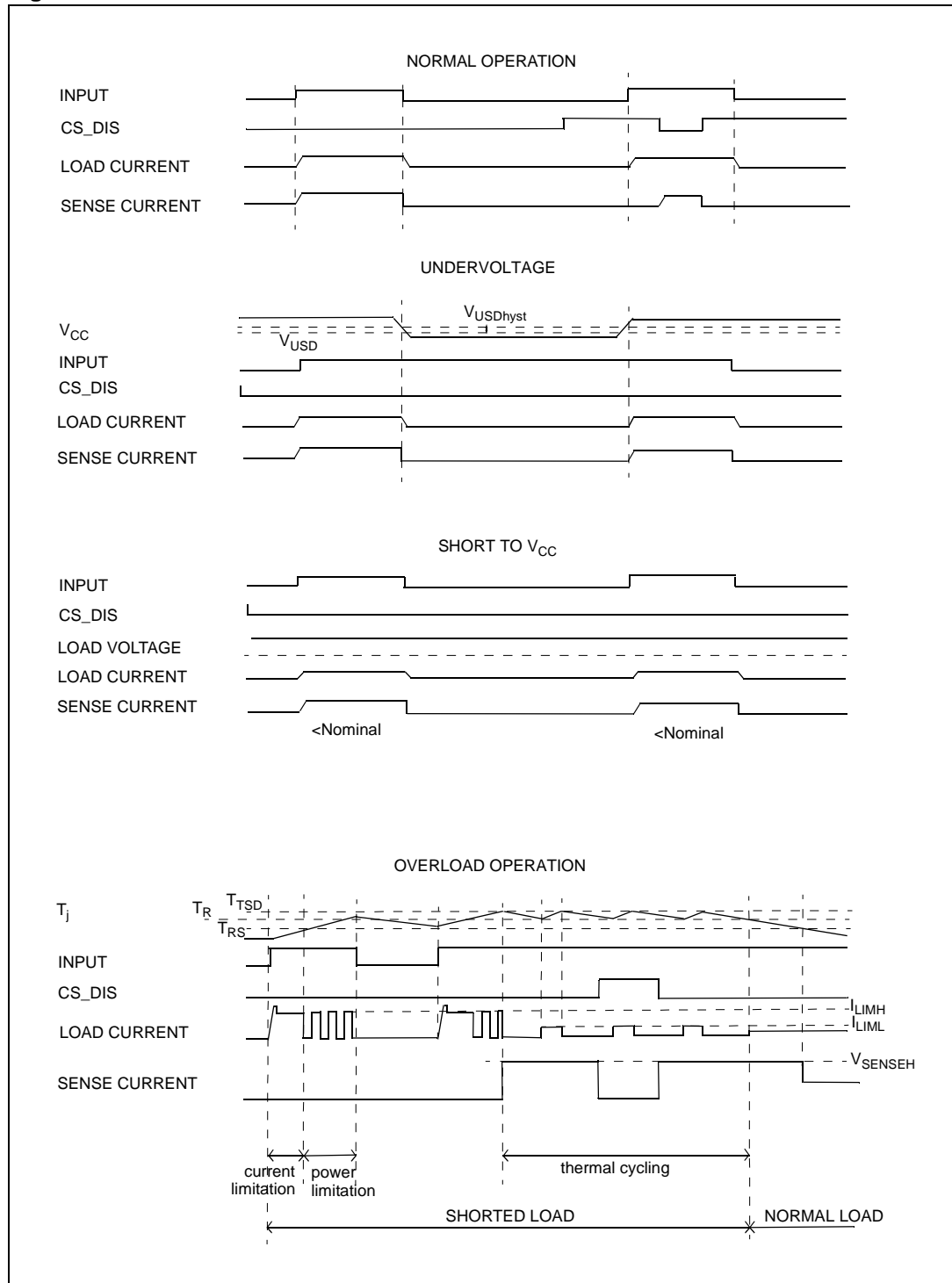
Calculation example:

For  $V_{CCpeak} = -100 \text{ V}$  and  $I_{latchup} \geq 20 \text{ mA}$ ;  $V_{OH\mu C} \geq 4.5 \text{ V}$

$$5 \text{ k}\Omega \leq R_{prot} \leq 180 \text{ k}\Omega.$$

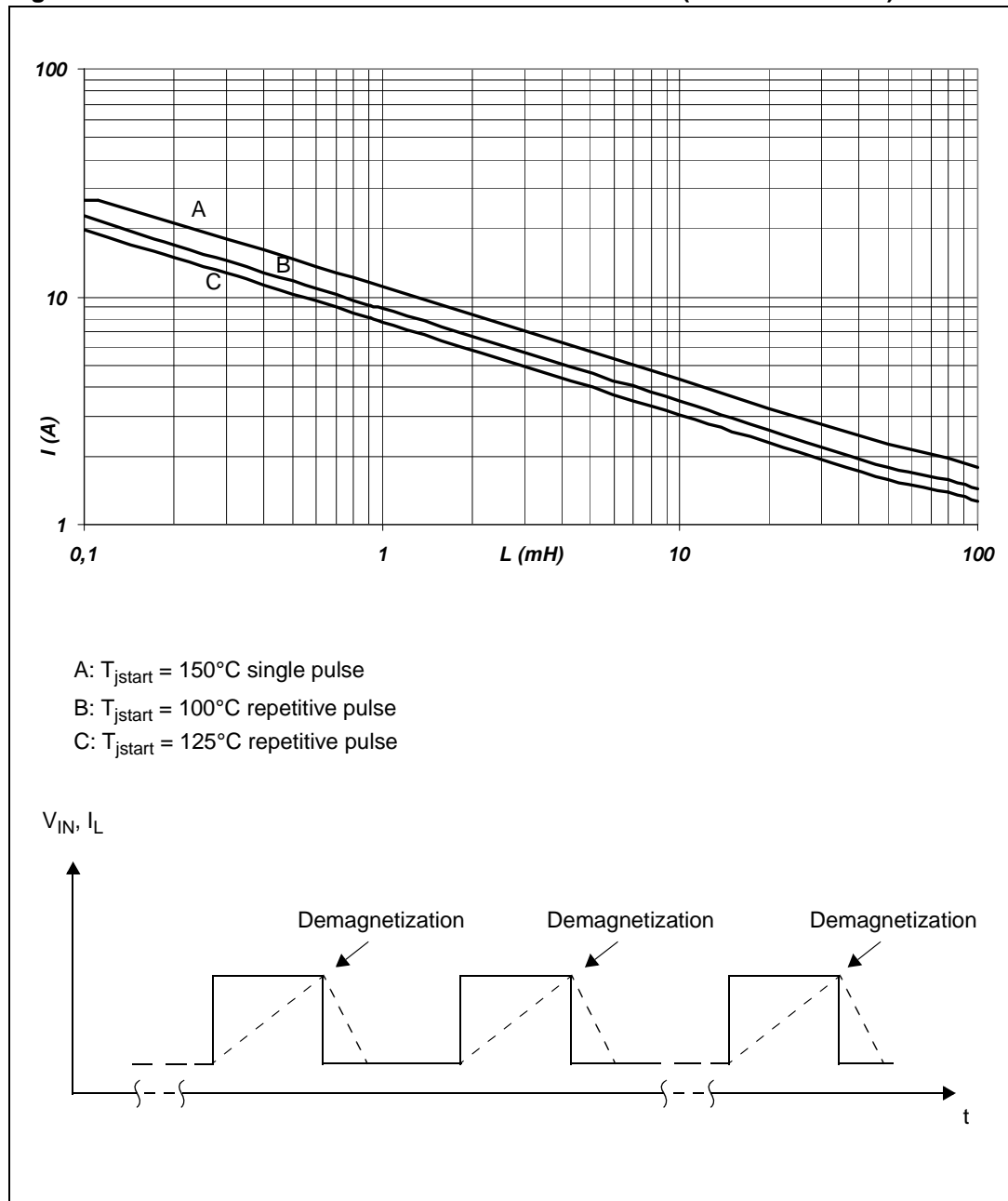
Recommended values:  $R_{prot} = 10 \text{ k}\Omega$ ,  $C_{EXT} = 10 \text{ nF}$ .

Figure 26. Waveforms



### 3.4 Maximum demagnetization energy ( $V_{CC} = 13.5V$ )

Figure 27. Maximum turn-off current versus inductance (for each channel)

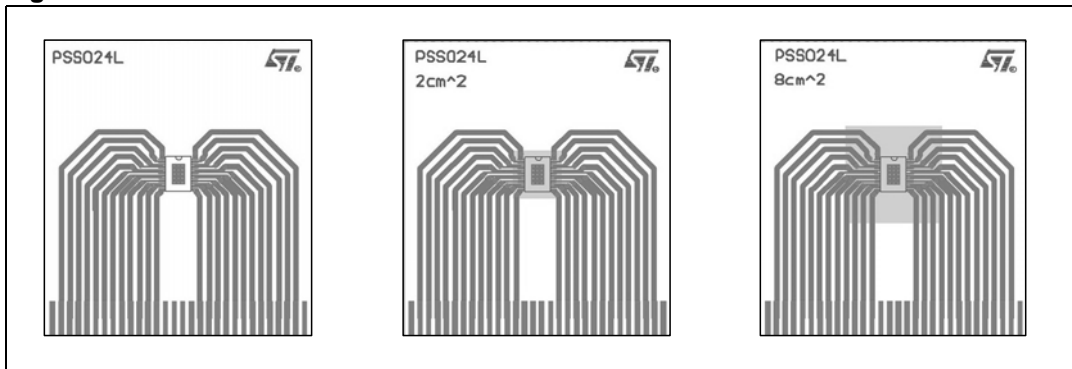


Note: Values are generated with  $R_L = 0 \Omega$ .  
 In case of repetitive pulses,  $T_{jstart}$  (at beginning of each demagnetization) of every pulse must not exceed the temperature specified above for curves A and B.

## 4 Package and PC board thermal data

### 4.1 PowerSSO-24 thermal data

Figure 28. PowerSSO-24 PC board



Note: Layout condition of  $R_{th}$  and  $Z_{th}$  measurements (PCB: Double layer, Thermal Vias, FR4 area= 77 mm x 86 mm, PCB thickness=1.6mm, Cu thickness=70  $\mu$ m (front and back side), Copper areas: from minimum pad lay-out to 8 cm<sup>2</sup>).

Figure 29.  $R_{thj-amb}$  vs PCB copper area in open box free air condition (one channel on)

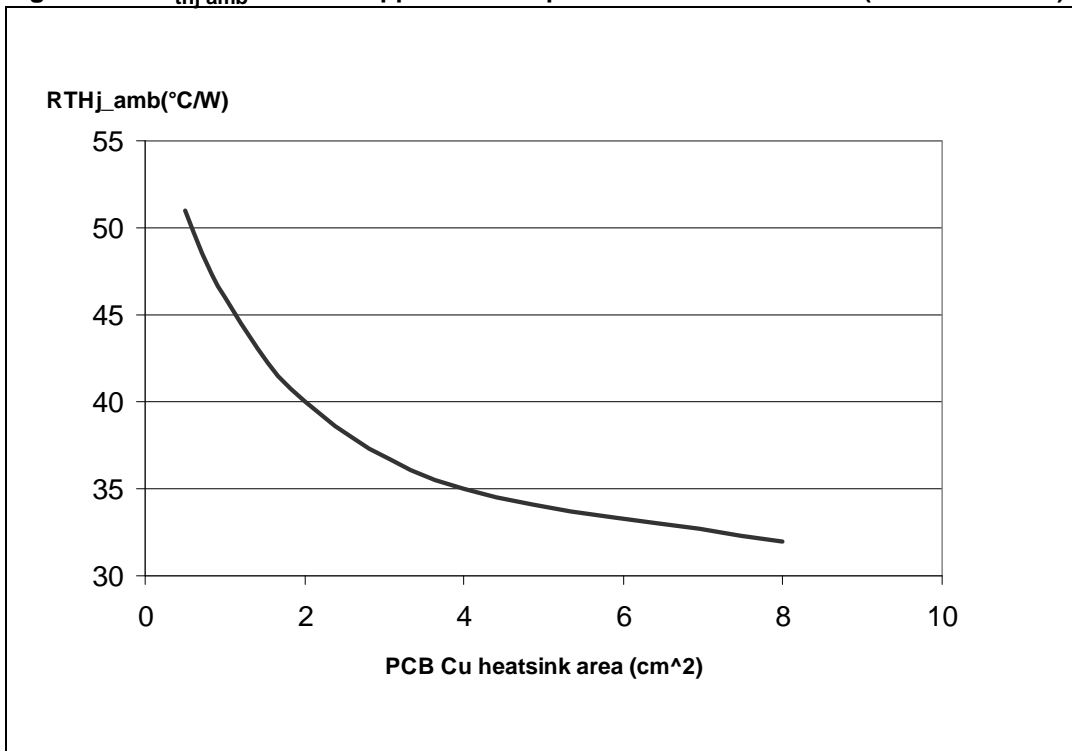




Figure 30. PowerSSO-24 thermal impedance junction ambient single pulse (one channel on)

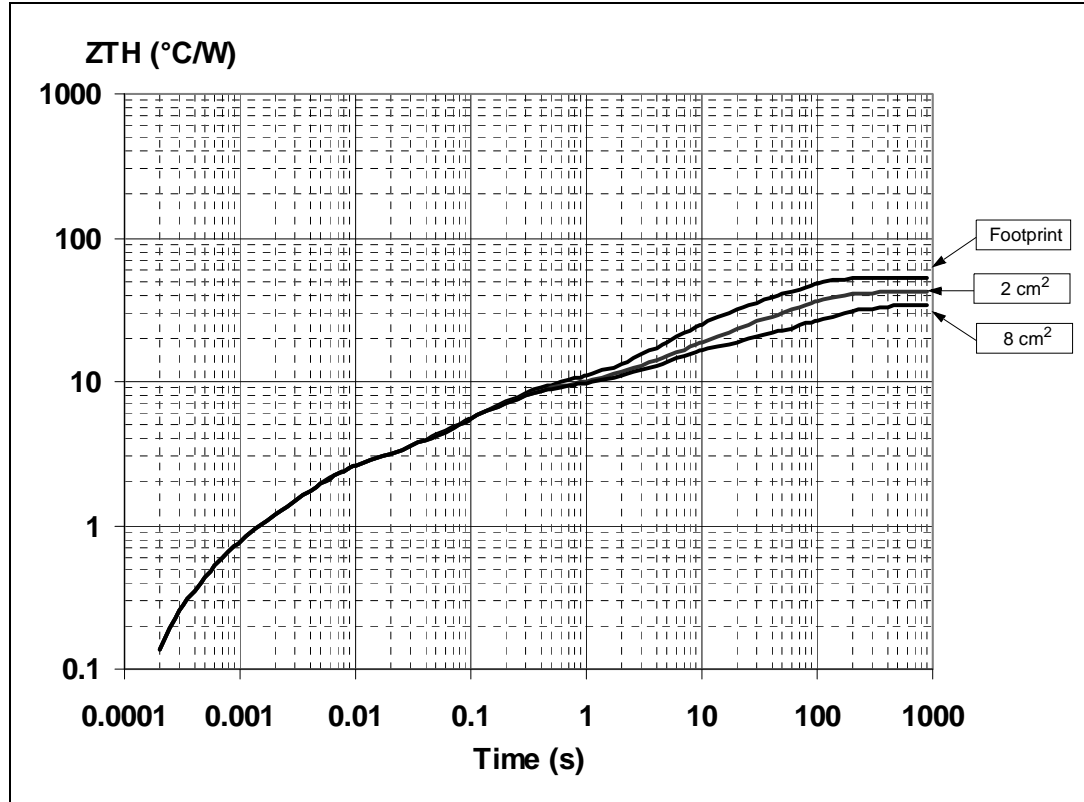
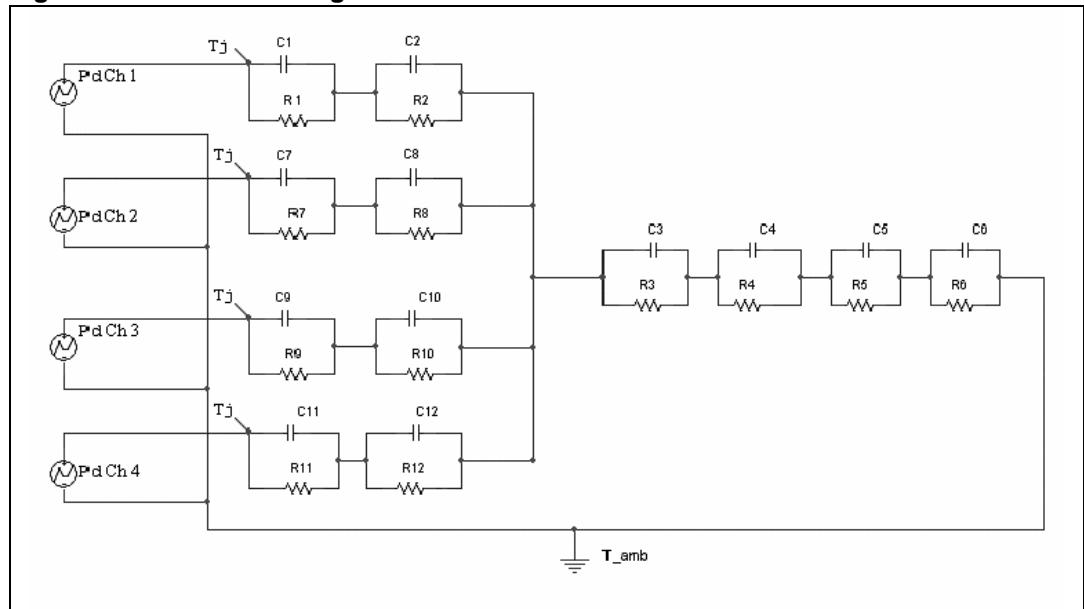


Figure 31. Thermal fitting model of a double channel HSD in PowerSSO-24<sup>(a)</sup>



a. The fitting model is a simplified thermal tool and is valid for transient evolutions where the embedded protections (power limitation or thermal cycling during thermal shutdown) are not triggered.

**Equation 1: pulse calculation formula**

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where  $\delta = t_p/T$

**Table 15. Thermal parameters**

Area/island (cm <sup>2</sup> )	Footprint	2	8
R1=R7=R9=R11 (°C/W)	0.4	-	-
R2=R8=R10=R12 (°C/W)	2	-	-
R3 (°C/W)	6	-	-
R4 (°C/W)	7.7	-	-
R5 (°C/W)	9	9	8
R6 (°C/W)	28	17	10
C1=C7=C9=C11 (W.s/°C)	0.001	-	-
C2=C8=C10=C12 (W.s/°C)	0.0022	-	-
C3 (W.s/°C)	0.025	-	-
C4 (W.s/°C)	0.75	-	-
C5 (W.s/°C)	1	4	9
C6 (W.s/°C)	2.2	5	17

## 5 Package and packing information

### 5.1 ECOPACK® packages

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com).

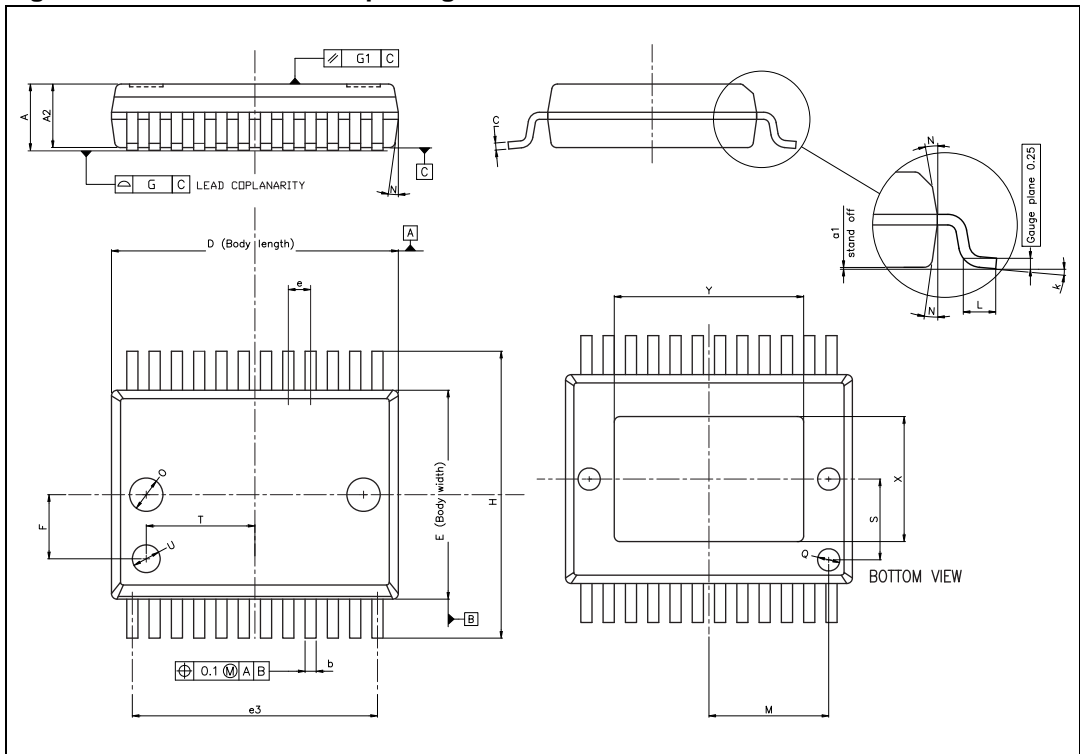
ECOPACK® is an ST trademark.

### 5.2 PowerSSO-24™ mechanical data

Table 16. PowerSSO-24™ mechanical data

Symbol	Millimeters		
	Min.	Typ.	Max.
A	-	-	2.45
A2	2.15	-	2.35
a1	0	-	0.10
b	0.33	-	0.51
c	0.23	-	0.32
D	10.10	-	10.50
E	7.4	-	7.6
e	-	0.8	-
e3	-	8.8	-
G	-	-	0.1
G1	-	-	0.06
H	10.1	-	10.5
h	-	-	0.4
k	0°	-	8°
L	0.55	-	0.85
N	-	-	10°
X	4.1	-	4.7
Y	6.5	-	7.1

Figure 32. PowerSSO-24™ package dimensions



### 5.3 Packing information

Figure 33. PowerSSO-24 tube shipment (no suffix)

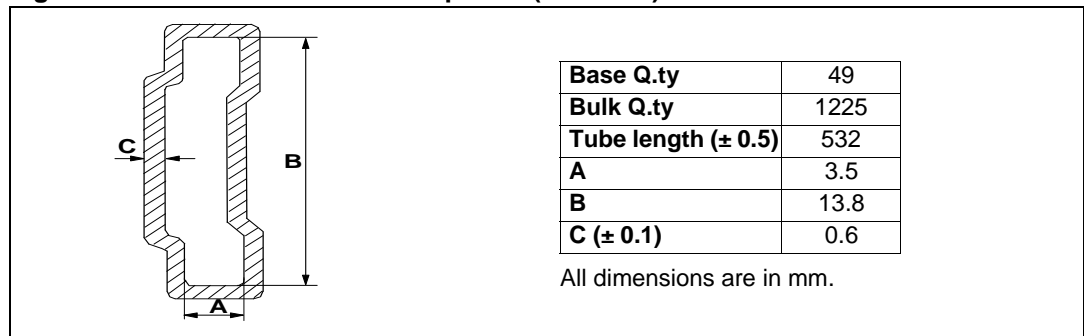
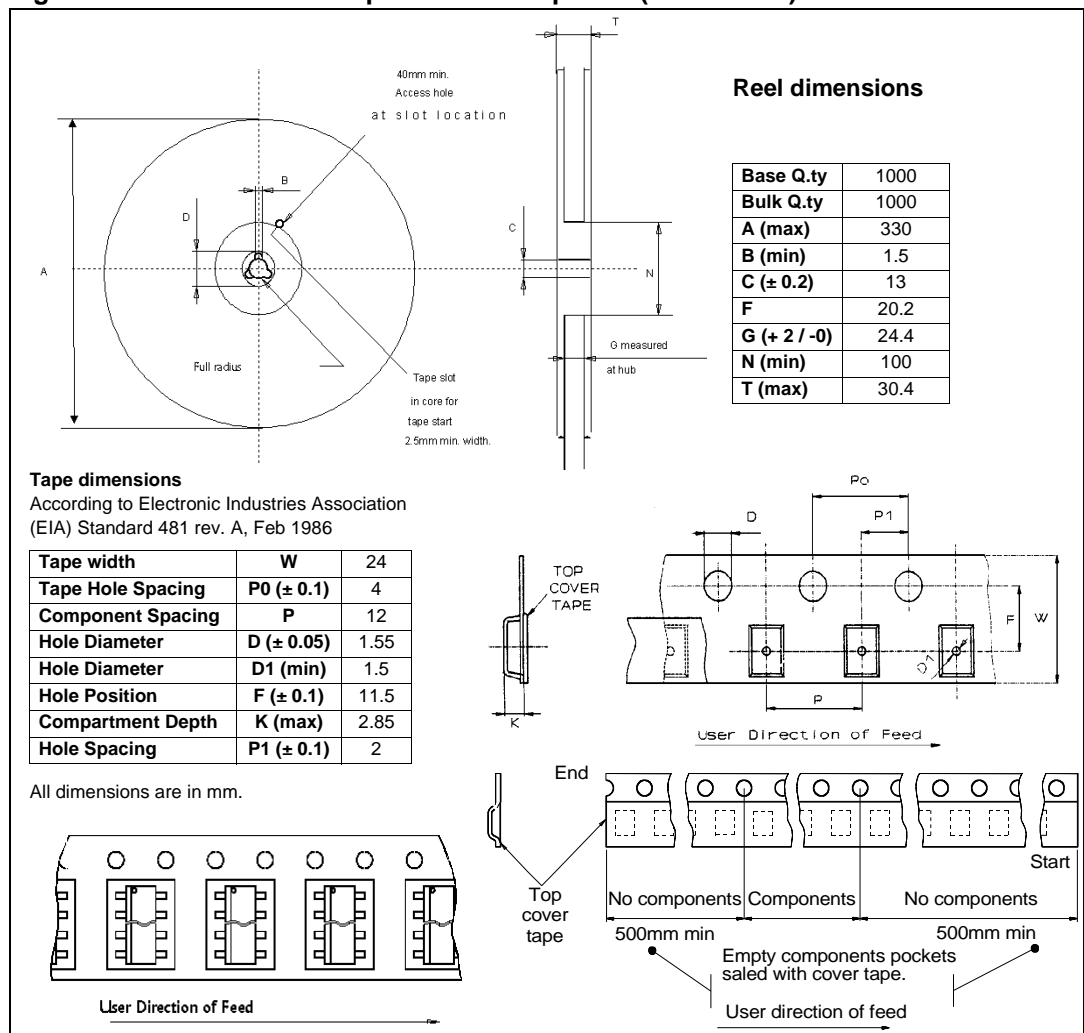


Figure 34. PowerSSO-24 tape and reel shipment (suffix "TR")



## 6 Revision history

**Table 17. Document revision history**

Date	Revision	Changes
14-Sep-2004	1	Initial release.
12-Jan-2006	2	Major general update.
9-Mar-2007	3	Reformatted and restructured. Added contents, lists of tables and list of figures. Added <a href="#">Section 3.4: Maximum demagnetization energy (VCC = 13.5V)</a> . Added <a href="#">ECOPACK® packages</a> information. Added new disclaimer.
22-Aug-2007	4	<a href="#">Figure 14: Input high level</a> and <a href="#">Figure 15: Input hysteresis voltage</a> corrected.
01-Oct-2007	5	<a href="#">Table 4: Absolute maximum ratings</a> : changed E <sub>MAX</sub> value from 51 to 104 mJ. <a href="#">Table 8: Current sense (8V &lt; V<sub>CC</sub> &lt; 16V)</a> : added dk1/k1, dk2/k2, dk3/k3, Δt <sub>DSENSE2H</sub> . Added <a href="#">Figure 5: Delay response time between rising edge of output current and rising edge of current sense (CS enabled)</a> . Updated <a href="#">Figure 7: I<sub>OUT</sub>/I<sub>SENSE</sub> vs I<sub>OUT</sub></a> . Added <a href="#">Figure 8: Maximum current sense ratio drift vs load current</a> . <a href="#">Table 12: Electrical transient requirements (part 1/3)</a> : added notes. <a href="#">Figure 31: Thermal fitting model of a double channel HSD in PowerSSO-24</a> , added note.
04-Dec-2007	6	Updated <a href="#">Table 8: Current sense (8V &lt; V<sub>CC</sub> &lt; 16V)</a> : – changed t <sub>DSENSE2H</sub> max value from 300 μs to 250 μs. – added I <sub>OL</sub> parameter.
12-Feb-2008	7	Corrected typing error in <a href="#">Table 8: Current sense (8V &lt; V<sub>CC</sub> &lt; 16V)</a> : changed I <sub>OL</sub> test condition from V <sub>IN</sub> = 0V to V <sub>IN</sub> = 5V.
14-May-2009	8	<a href="#">Table 16: PowerSSO-24™ mechanical data</a> : – Updated a1 (max) from 0.075 to 0.10.
29-May-2009	9	<a href="#">Table 16: PowerSSO-24™ mechanical data</a> : – Updated A (min) from 2.15 to - and A (max) from 2.47 to 2.45 – Updated A2 (max) from 2.40 to 2.35 – Updated k (min) from - to 0°, k (typ) from 5° to - and k (max) from - to 8°
22-Sep-2013	10	Updated Disclaimer.

**Please Read Carefully:**

Information in this document is provided solely in connection with ST products. STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, modifications or improvements, to this document, and the products and services described herein at any time, without notice.

All ST products are sold pursuant to ST's terms and conditions of sale.

Purchasers are solely responsible for the choice, selection and use of the ST products and services described herein, and ST assumes no liability whatsoever relating to the choice, selection or use of the ST products and services described herein.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted under this document. If any part of this document refers to any third party products or services it shall not be deemed a license grant by ST for the use of such third party products or services, or any intellectual property contained therein or considered as a warranty covering the use in any manner whatsoever of such third party products or services or any intellectual property contained therein.

**UNLESS OTHERWISE SET FORTH IN ST'S TERMS AND CONDITIONS OF SALE ST DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY WITH RESPECT TO THE USE AND/OR SALE OF ST PRODUCTS INCLUDING WITHOUT LIMITATION IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE (AND THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION), OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.**

**ST PRODUCTS ARE NOT DESIGNED OR AUTHORIZED FOR USE IN: (A) SAFETY CRITICAL APPLICATIONS SUCH AS LIFE SUPPORTING, ACTIVE IMPLANTED DEVICES OR SYSTEMS WITH PRODUCT FUNCTIONAL SAFETY REQUIREMENTS; (B) AERONAUTIC APPLICATIONS; (C) AUTOMOTIVE APPLICATIONS OR ENVIRONMENTS, AND/OR (D) AEROSPACE APPLICATIONS OR ENVIRONMENTS. WHERE ST PRODUCTS ARE NOT DESIGNED FOR SUCH USE, THE PURCHASER SHALL USE PRODUCTS AT PURCHASER'S SOLE RISK, EVEN IF ST HAS BEEN INFORMED IN WRITING OF SUCH USAGE, UNLESS A PRODUCT IS EXPRESSLY DESIGNATED BY ST AS BEING INTENDED FOR "AUTOMOTIVE, AUTOMOTIVE SAFETY OR MEDICAL" INDUSTRY DOMAINS ACCORDING TO ST PRODUCT DESIGN SPECIFICATIONS. PRODUCTS FORMALLY ESCC, QML OR JAN QUALIFIED ARE DEEMED SUITABLE FOR USE IN AEROSPACE BY THE CORRESPONDING GOVERNMENTAL AGENCY.**

Resale of ST products with provisions different from the statements and/or technical features set forth in this document shall immediately void any warranty granted by ST for the ST product or service described herein and shall not create or extend in any manner whatsoever, any liability of ST.

ST and the ST logo are trademarks or registered trademarks of ST in various countries.

Information in this document supersedes and replaces all information previously supplied.

The ST logo is a registered trademark of STMicroelectronics. All other names are the property of their respective owners.

© 2013 STMicroelectronics - All rights reserved

STMicroelectronics group of companies

Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco - Philippines - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States of America

[www.st.com](http://www.st.com)

## Данный компонент на территории Российской Федерации

### Вы можете приобрести в компании MosChip.

Для оперативного оформления запроса Вам необходимо перейти по данной ссылке:

<http://moschip.ru/get-element>

Вы можете разместить у нас заказ для любого Вашего проекта, будь то серийное производство или разработка единичного прибора.

В нашем ассортименте представлены ведущие мировые производители активных и пассивных электронных компонентов.

Нашей специализацией является поставка электронной компонентной базы двойного назначения, продукции таких производителей как XILINX, Intel (ex.ALTERA), Vicor, Microchip, Texas Instruments, Analog Devices, Mini-Circuits, Amphenol, Glenair.

Сотрудничество с глобальными дистрибьюторами электронных компонентов, предоставляет возможность заказывать и получать с международных складов практически любой перечень компонентов в оптимальные для Вас сроки.

На всех этапах разработки и производства наши партнеры могут получить квалифицированную поддержку опытных инженеров.

Система менеджмента качества компании отвечает требованиям в соответствии с ГОСТ Р ИСО 9001, ГОСТ РВ 0015-002 и ЭС РД 009

### Офис по работе с юридическими лицами:

105318, г.Москва, ул.Щербаковская д.3, офис 1107, 1118, ДЦ «Щербаковский»

Телефон: +7 495 668-12-70 (многоканальный)

Факс: +7 495 668-12-70 (доб.304)

E-mail: [info@moschip.ru](mailto:info@moschip.ru)

Skype отдела продаж:

moschip.ru

moschip.ru\_4

moschip.ru\_6

moschip.ru\_9