



# 16-Bit, 135ksps, Single-Supply ADCs with Bipolar Analog Input Range

## General Description

The MAX1178/MAX1188 16-bit, low-power, successive-approximation analog-to-digital converters (ADCs) feature automatic power-down, a factory-trimmed internal clock, and a byte-wide parallel interface. The devices operate from a single +4.75V to +5.25V analog supply and feature a separate digital supply input for direct interface with a +2.7V to +5.25V digital logic.

The MAX1188 accepts a bipolar analog input voltage range of  $\pm 10V$ , while the MAX1178 accepts a bipolar analog input voltage range of  $\pm 5V$ . All devices consume no more than 26.5mW at a sampling rate of 135ksps when using an external reference, and 31mW when using the internal +4.096V reference. AutoShutdown™ reduces supply current to 0.4mA at 10ksps.

The MAX1178/MAX1188 are ideal for high-performance, battery-powered, data-acquisition applications. Excellent AC performance (THD = -100dB) and DC accuracy ( $\pm 2$  LSB INL) make the MAX1178/MAX1188 ideal for industrial process control, instrumentation, and medical applications.

The MAX1178/MAX1188 are available in a 20-pin TSSOP package and are fully specified over the -40°C to +85°C extended temperature range and the 0°C to +70°C commercial temperature range.

## Applications

Temperature Sensing and Monitoring  
Industrial Process Control  
I/O Modules  
Data-Acquisition Systems  
Precision Instrumentation

**Pin Configuration and Functional Diagram appear at end of data sheet.**

AutoShutdown is a trademark of Maxim Integrated Products, Inc.

## Features

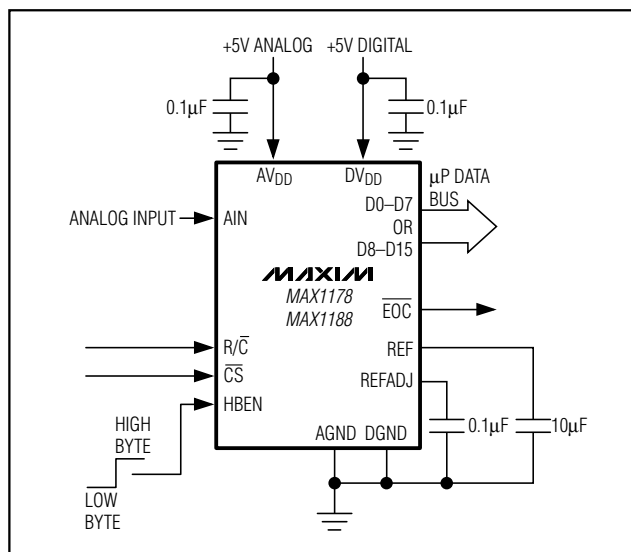
- ◆ Byte-Wide Parallel Interface
- ◆ Analog Input Voltage Range:  $\pm 10V$ ,  $\pm 5V$
- ◆ Single +4.75V to +5.25V Analog Supply Voltage
- ◆ Interface with +2.7V to +5.25V Digital Logic
- ◆  $\pm 2$  LSB INL
- ◆  $\pm 1$  LSB DNL
- ◆ Low Supply Current (max)
  - 2.9mA (External Reference)
  - 3.8mA (Internal Reference)
  - 5µA AutoShutdown Mode
- ◆ Small Footprint
- ◆ 20-Pin TSSOP Package

## Ordering Information

| PART        | TEMP RANGE     | PIN-PACKAGE | INPUT VOLTAGE RANGE (V) |
|-------------|----------------|-------------|-------------------------|
| MAX1178ACUP | 0°C to +70°C   | 20 TSSOP    | $\pm 5$                 |
| MAX1178BCUP | 0°C to +70°C   | 20 TSSOP    | $\pm 5$                 |
| MAX1178CCUP | 0°C to +70°C   | 20 TSSOP    | $\pm 5$                 |
| MAX1178AEUP | -40°C to +85°C | 20 TSSOP    | $\pm 5$                 |
| MAX1178BEUP | -40°C to +85°C | 20 TSSOP    | $\pm 5$                 |
| MAX1178CEUP | -40°C to +85°C | 20 TSSOP    | $\pm 5$                 |

Ordering Information continued at end of data sheet.

## Typical Operating Circuit



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**For pricing, delivery, and ordering information, please contact Maxim/Dallas Direct! at 1-888-629-4642, or visit Maxim's website at [www.maxim-ic.com](http://www.maxim-ic.com).**

MAX1178/MAX1188

# 16-Bit, 135ksps, Single-Supply ADCs with Bipolar Analog Input Range

## ABSOLUTE MAXIMUM RATINGS

|                                               |                                    |                                                       |                 |
|-----------------------------------------------|------------------------------------|-------------------------------------------------------|-----------------|
| AV <sub>DD</sub> to AGND .....                | -0.3V to +6V                       | Continuous Power Dissipation (T <sub>A</sub> = +70°C) |                 |
| DV <sub>DD</sub> to DGND .....                | -0.3V to +6V                       | TSSOP (derate 10.9mW/°C above +70°C) .....            | 879mW           |
| AGND to DGND .....                            | -0.3V to +0.3V                     | Operating Temperature Ranges                          |                 |
| AIN to AGND .....                             | -16.5V to +16.5V                   | MAX11__CUP .....                                      | 0°C to +70°C    |
| REF, REFADJ to AGND .....                     | -0.3V to (AV <sub>DD</sub> + 0.3V) | MAX11__EUP .....                                      | -40°C to +85°C  |
| CS, R/C, HBEN to DGND .....                   | -0.3V to +6V                       | Storage Temperature Range .....                       | -65°C to +150°C |
| D <sub>-</sub> , EOC to DGND .....            | -0.3V to (DV <sub>DD</sub> + 0.3V) | Junction Temperature .....                            | +150°C          |
| Maximum Continuous Current into Any Pin ..... | 50mA                               | Lead Temperature (soldering, 10s) .....               | +300°C          |

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## ELECTRICAL CHARACTERISTICS

(AV<sub>DD</sub> = DV<sub>DD</sub> = +5V ±5%, external reference = +4.096V, C<sub>REF</sub> = 10μF, C<sub>REFADJ</sub> = 0.1μF, V<sub>REFADJ</sub> = AV<sub>DD</sub>, T<sub>A</sub> = T<sub>MIN</sub> to T<sub>MAX</sub>, unless otherwise noted. Typical values are at T<sub>A</sub> = +25°C.)

| PARAMETER                                                                    | SYMBOL           | CONDITIONS                        |                  | MIN  | TYP  | MAX  | UNITS              |
|------------------------------------------------------------------------------|------------------|-----------------------------------|------------------|------|------|------|--------------------|
| DC ACCURACY                                                                  |                  |                                   |                  |      |      |      |                    |
| Resolution                                                                   | RES              |                                   |                  | 16   |      |      | Bits               |
| Differential Nonlinearity                                                    | DNL              | No missing codes over temperature | MAX11_ _A        | -1   | +1   |      | LSB                |
|                                                                              |                  |                                   | MAX11_ _B        | -1.0 | +1.5 |      |                    |
|                                                                              |                  |                                   | MAX11_ _C        | -1   | +2   |      |                    |
| Integral Nonlinearity                                                        | INL              | MAX11_ _A                         |                  | -2   | +2   |      | LSB                |
|                                                                              |                  | MAX11_ _B                         |                  | -2   | +2   |      |                    |
|                                                                              |                  | MAX11_ _C                         |                  | -4   | +4   |      |                    |
| Transition Noise                                                             |                  | RMS noise, external reference     |                  | 0.6  |      |      | LSB <sub>RMS</sub> |
|                                                                              |                  | Internal reference                |                  | 0.75 |      |      |                    |
| Offset Error                                                                 |                  |                                   |                  | -10  | 0    | +10  | mV                 |
| Gain Error                                                                   |                  |                                   |                  |      | 0    | ±0.2 | %FSR               |
| Offset Drift                                                                 |                  |                                   |                  |      | 16   |      | μV/°C              |
| Gain Drift                                                                   |                  |                                   |                  |      | ±1   |      | ppm/°C             |
| AC ACCURACY (f <sub>IN</sub> = 1kHz, V <sub>AIN</sub> = full range, 135ksps) |                  |                                   |                  |      |      |      |                    |
| Signal-to-Noise Plus Distortion                                              | SINAD            |                                   |                  | 86   | 90   |      | dB                 |
| Signal-to-Noise Ratio                                                        | SNR              |                                   |                  | 87   | 91   |      | dB                 |
| Total Harmonic Distortion                                                    | THD              |                                   |                  |      | -100 | -92  | dB                 |
| Spurious-Free Dynamic Range                                                  | SFDR             |                                   |                  | 92   | 103  |      | dB                 |
| ANALOG INPUT                                                                 |                  |                                   |                  |      |      |      |                    |
| Input Range                                                                  | V <sub>AIN</sub> | MAX1178                           |                  | -5   | +5   |      | V                  |
|                                                                              |                  | MAX1188                           |                  | -10  | +10  |      |                    |
| Input Resistance                                                             | R <sub>AIN</sub> | MAX1178                           | Normal operation | 5.3  | 6.9  | 9.2  | kΩ                 |
|                                                                              |                  |                                   | Shutdown mode    | 3.0  |      |      |                    |
|                                                                              |                  | MAX1188                           | Normal operation | 7.8  | 10   | 13.0 |                    |
|                                                                              |                  |                                   | Shutdown mode    | 6.0  |      |      |                    |

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MAX1178/MAX1188

## ELECTRICAL CHARACTERISTICS (continued)

( $AV_{DD} = DV_{DD} = +5V \pm 5\%$ , external reference = +4.096V,  $C_{REF} = 10\mu F$ ,  $C_{REFADJ} = 0.1\mu F$ ,  $V_{REFADJ} = AV_{DD}$ ,  $T_A = T_{MIN}$  to  $T_{MAX}$ , unless otherwise noted. Typical values are at  $T_A = +25^\circ C$ .)

| PARAMETER                          | SYMBOL              | CONDITIONS                                                                                 |                  | MIN                    | TYP   | MAX                    | UNITS  |
|------------------------------------|---------------------|--------------------------------------------------------------------------------------------|------------------|------------------------|-------|------------------------|--------|
| Input Current                      | I <sub>AIN</sub>    | MAX1178,<br>-5V ≤ V <sub>AIN</sub> ≤ +5V                                                   | Normal operation | -1.8                   |       | +0.4                   | mA     |
|                                    |                     |                                                                                            | Shutdown mode    | -1.8                   |       | +1.8                   |        |
|                                    |                     | MAX1188,<br>-10V ≤ V <sub>AIN</sub> ≤ +10V                                                 | Normal operation | -1.8                   |       | +1.2                   |        |
|                                    |                     |                                                                                            | Shutdown mode    | -1.8                   |       | +1.8                   |        |
| Input Current Step at Power-Up     | I <sub>PU</sub>     | MAX1178, V <sub>AIN</sub> = +5V, shutdown mode to operating mode                           |                  | 1                      |       | 1.4                    | mA     |
|                                    |                     | MAX1188, V <sub>AIN</sub> = +10V, shutdown mode to operating mode                          |                  | 0.5                    |       | 0.7                    |        |
| Input Capacitance                  | C <sub>IN</sub>     |                                                                                            |                  | 10                     |       |                        | pF     |
| INTERNAL REFERENCE                 |                     |                                                                                            |                  |                        |       |                        |        |
| REF Output Voltage                 | V <sub>REF</sub>    |                                                                                            |                  | 4.056                  | 4.096 | 4.136                  | V      |
| REF Output Tempco                  |                     |                                                                                            |                  | ±35                    |       |                        | ppm/°C |
| REF Short-Circuit Current          | I <sub>REF-SC</sub> |                                                                                            |                  | ±10                    |       |                        | mA     |
| EXTERNAL REFERENCE                 |                     |                                                                                            |                  |                        |       |                        |        |
| REF and REFADJ Input-Voltage Range |                     |                                                                                            |                  | 3.8                    |       | 4.2                    | V      |
| REFADJ Buffer-Disable Threshold    |                     |                                                                                            |                  | AV <sub>DD</sub> - 0.4 |       | AV <sub>DD</sub> - 0.1 | V      |
| REF Input Current                  | I <sub>REF</sub>    | Normal mode, f <sub>SAMPLE</sub> = 135ksps                                                 |                  | 60                     |       | 100                    | μA     |
|                                    |                     | Shutdown mode (Note 1)                                                                     |                  | ±0.1                   |       | ±10                    |        |
| REFADJ Input Current               | I <sub>REFADJ</sub> | REFADJ = AV <sub>DD</sub>                                                                  |                  | 16                     |       |                        | μA     |
| DIGITAL INPUTS/OUTPUTS             |                     |                                                                                            |                  |                        |       |                        |        |
| Output High Voltage                | V <sub>OH</sub>     | I <sub>SOURCE</sub> = 0.5mA, DV <sub>DD</sub> = +2.7V to +5.25V, AV <sub>DD</sub> = +5.25V |                  | DV <sub>DD</sub> - 0.4 |       |                        | V      |
| Output Low Voltage                 | V <sub>OL</sub>     | I <sub>SINK</sub> = 1.6mA, DV <sub>DD</sub> = +2.7V to +5.25V, AV <sub>DD</sub> = +5.25V   |                  |                        |       | 0.4                    | V      |
| Input High Voltage                 | V <sub>IH</sub>     |                                                                                            |                  | 0.7 × DV <sub>DD</sub> |       |                        | V      |
| Input Low Voltage                  | V <sub>IL</sub>     |                                                                                            |                  |                        |       | 0.3 × DV <sub>DD</sub> | V      |
| Input Leakage Current              |                     | Digital input = DV <sub>DD</sub> or 0V                                                     |                  | -1                     |       | +1                     | μA     |
| Input Hysteresis                   | V <sub>HYST</sub>   |                                                                                            |                  | 0.2                    |       |                        | V      |
| Input Capacitance                  | C <sub>IN</sub>     |                                                                                            |                  | 15                     |       |                        | pF     |
| Tri-State Output Leakage           | I <sub>OZ</sub>     |                                                                                            |                  | ±10                    |       |                        | μA     |
| Tri-State Output Capacitance       | C <sub>OZ</sub>     |                                                                                            |                  | 15                     |       |                        | pF     |

# 16-Bit, 135ksps, Single-Supply ADCs with Bipolar Analog Input Range

## ELECTRICAL CHARACTERISTICS (continued)

(AVDD = DVDD = +5V  $\pm$ 5%, external reference = +4.096V, CREF = 10 $\mu$ F, CREFADJ = 0.1 $\mu$ F, VREFADJ = AVDD, TA = TMIN to TMAX, unless otherwise noted. Typical values are at TA = +25°C.)

| PARAMETER               | SYMBOL | CONDITIONS                                         | MIN  | TYP | MAX  | UNITS   |
|-------------------------|--------|----------------------------------------------------|------|-----|------|---------|
| <b>POWER SUPPLIES</b>   |        |                                                    |      |     |      |         |
| Analog Supply Voltage   | AVDD   |                                                    | 4.75 |     | 5.25 | V       |
| Digital Supply Voltage  | DVDD   |                                                    | 2.70 |     | 5.25 | V       |
| Analog Supply Current   | IAVDD  | External reference, 135ksps                        |      | 4   | 5.3  | mA      |
|                         |        | Internal reference, 135ksps                        |      | 5.2 | 6.2  |         |
| Shutdown Supply Current | ISHDN  | Shutdown mode (Note 1), digital input = DVDD or 0V |      | 0.5 | 5    | $\mu$ A |
|                         |        | Standby mode                                       |      | 3.7 |      | mA      |
| Digital Supply Current  | IDVDD  |                                                    |      |     | 0.75 | mA      |
| Power-Supply Rejection  |        | AVDD = DVDD = 4.75V to 5.25V                       |      | 3.5 |      | LSB     |

## TIMING CHARACTERISTICS (Figures 1 and 2)

(AVDD = +4.75V to +5.25V, DVDD = +2.7V to AVDD, external reference = +4.096V, CREF = 10 $\mu$ F, CREFADJ = 0.1 $\mu$ F, VREFADJ = AVDD, CLOAD = 20pF, TA = TMIN to TMAX.)

| PARAMETER                                            | SYMBOL      | CONDITIONS            | MIN | TYP | MAX | UNITS   |
|------------------------------------------------------|-------------|-----------------------|-----|-----|-----|---------|
| Maximum Sampling Rate                                | fSAMPLE-MAX |                       |     |     | 135 | ksps    |
| Acquisition Time                                     | tACQ        |                       | 2   |     |     | $\mu$ s |
| Conversion Time                                      | tCONV       |                       |     |     | 4.7 | $\mu$ s |
| $\overline{CS}$ Pulse-Width High                     | tCSH        | (Note 2)              | 40  |     |     | ns      |
| $\overline{CS}$ Pulse-Width Low (Note 2)             | tCSL        | DVDD = 4.75V to 5.25V | 40  |     |     | ns      |
|                                                      |             | DVDD = 2.7V to 5.25V  | 60  |     |     |         |
| R/ $\overline{C}$ to $\overline{CS}$ Fall Setup Time | tDS         |                       | 0   |     |     | ns      |
| R/ $\overline{C}$ to $\overline{CS}$ Fall Hold Time  | tDH         | DVDD = 4.75V to 5.25V | 40  |     |     | ns      |
|                                                      |             | DVDD = 2.7V to 5.25V  | 60  |     |     |         |
| $\overline{CS}$ to Output Data Valid                 | tDO         | DVDD = 4.75V to 5.25V |     |     | 40  | ns      |
|                                                      |             | DVDD = 2.7V to 5.25V  |     |     | 80  |         |
| $\overline{EOC}$ Fall to $\overline{CS}$ Fall        | tDV         |                       | 0   |     |     | ns      |
| $\overline{CS}$ Rise to $\overline{EOC}$ Rise        | tEOC        | DVDD = 4.75V to 5.25V |     |     | 40  | ns      |
|                                                      |             | DVDD = 2.7V to 5.25V  |     |     | 80  |         |
| Bus Relinquish Time                                  | tBR         | DVDD = 4.75V to 5.25V |     |     | 40  | ns      |
|                                                      |             | DVDD = 2.7V to 5.25V  |     |     | 80  |         |
| HBEN Transition to Output Data Valid                 | tDO1        | DVDD = 4.75V to 5.25V |     |     | 40  | ns      |
|                                                      |             | DVDD = 2.7V to 5.25V  |     |     | 80  |         |

**Note 1:** Maximum specification is limited by automated test equipment.

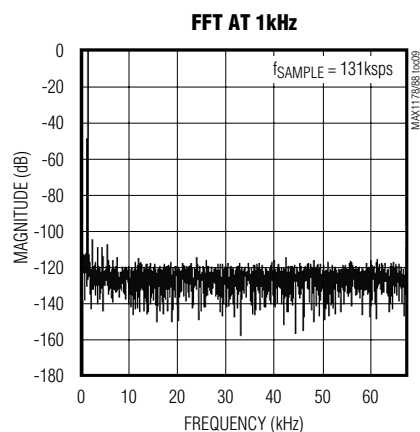
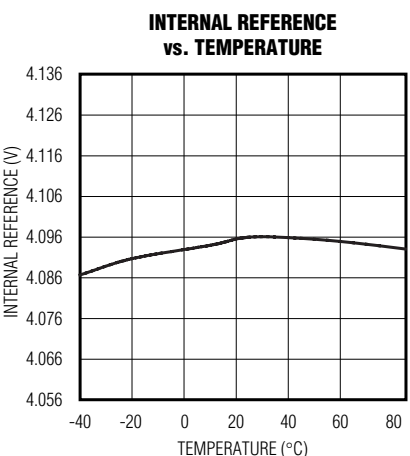
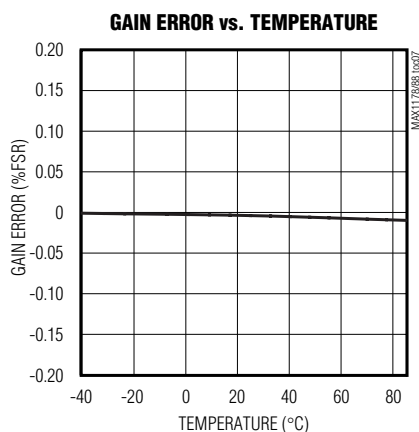
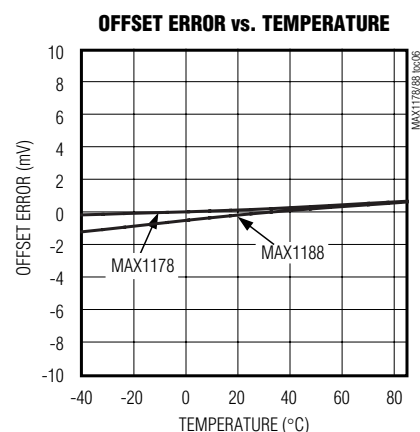
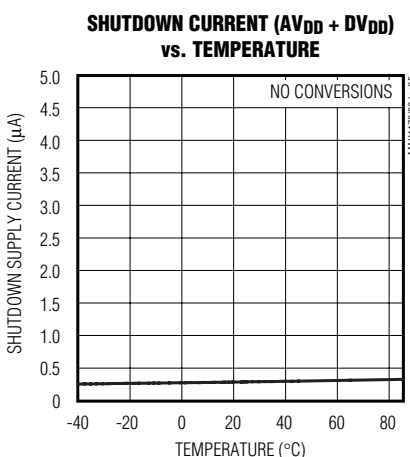
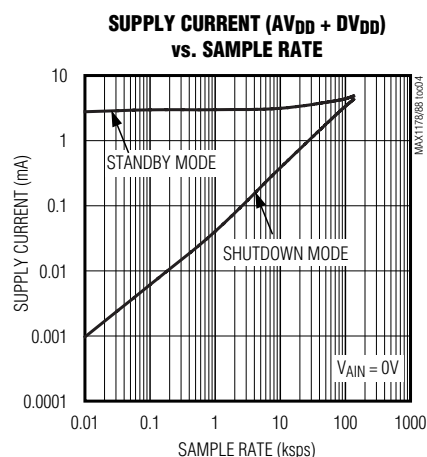
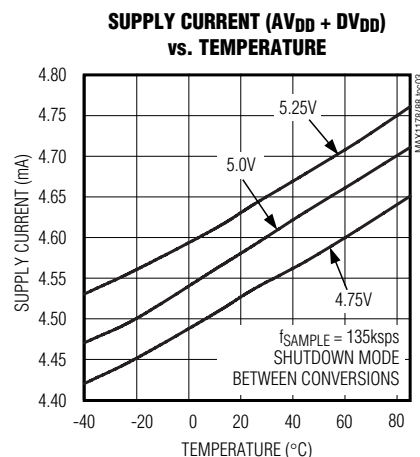
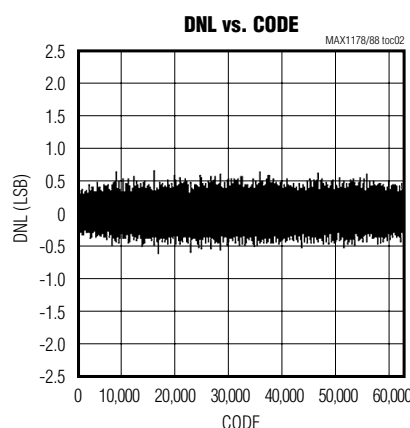
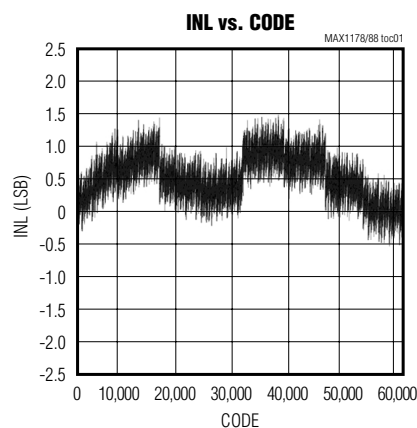
**Note 2:** To ensure best performance, finish reading the data and wait tBR before starting a new acquisition.

# 16-Bit, 135ksps, Single-Supply ADCs with Bipolar Analog Input Range

## Typical Operating Characteristics

(Typical Operating Circuit,  $AV_{DD} = DV_{DD} = +5V$ , external reference = +4.096V,  $C_{REF} = 10\mu F$ ,  $C_{REFADJ} = 0.1\mu F$ ,  $V_{REFADJ} = AV_{DD}$ ,  $C_{LOAD} = 20pF$ . Typical values are at  $T_A = +25^\circ C$ , unless otherwise noted.)

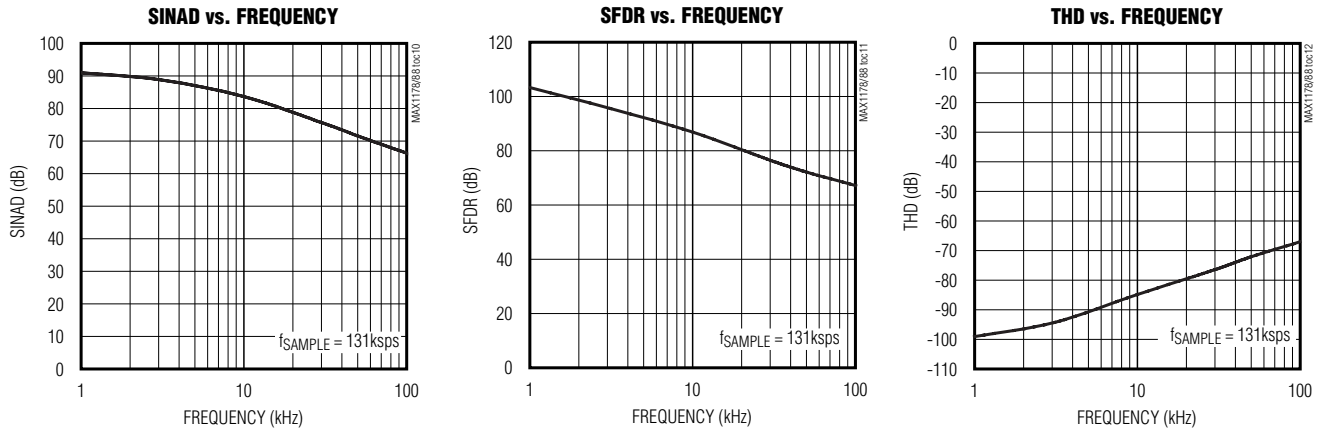
MAX1178/MAX1188



# 16-Bit, 135ksps, Single-Supply ADCs with Bipolar Analog Input Range

## Typical Operating Characteristics (continued)

(Typical Operating Circuit,  $AV_{DD} = DV_{DD} = +5V$ , external reference = +4.096V,  $C_{REF} = 10\mu F$ ,  $C_{REFADJ} = 0.1\mu F$ ,  $V_{REFADJ} = AV_{DD}$ ,  $C_{LOAD} = 20pF$ . Typical values are at  $T_A = +25^\circ C$ , unless otherwise noted.)



## Pin Description

| PIN | NAME             | FUNCTION                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
|-----|------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1   | D4/D12           | Tri-State Digital-Data Output                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
| 2   | D5/D13           | Tri-State Digital-Data Output                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
| 3   | D6/D14           | Tri-State Digital-Data Output                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
| 4   | D7/D15           | Tri-State Digital-Data Output. D15 is the MSB.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| 5   | $R/\overline{C}$ | Read/Convert Input. Power up and put the MAX1178/MAX1188 in acquisition mode by holding $R/\overline{C}$ low during the first falling edge of $\overline{CS}$ . During the second falling edge of $\overline{CS}$ , the level on $R/\overline{C}$ determines whether the reference and reference buffer power down or remain on after conversion. Set $R/\overline{C}$ high during the second falling edge of $\overline{CS}$ to power down the reference and buffer, or set $R/\overline{C}$ low to leave the reference and buffer powered up. Set $R/\overline{C}$ high during the third falling edge of $\overline{CS}$ to put valid data on the bus. |
| 6   | $\overline{EOC}$ | End of Conversion. $\overline{EOC}$ drives low when conversion is complete.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
| 7   | $AV_{DD}$        | Analog Supply Input. Bypass with a $0.1\mu F$ capacitor to AGND.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
| 8   | AGND             | Analog Ground. Primary analog ground (star ground).                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| 9   | AIN              | Analog Input                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
| 10  | AGND             | Analog Ground. Connect pin 10 to pin 8.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| 11  | REFADJ           | Reference Buffer Output. Bypass REFADJ with a $0.1\mu F$ capacitor to AGND for internal reference mode. Connect REFADJ to $AV_{DD}$ to select external reference mode.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| 12  | REF              | Reference Input/Output. Bypass REF with a $10\mu F$ capacitor to AGND for internal reference mode. External reference input when in external reference mode.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |

# 16-Bit, 135ksps, Single-Supply ADCs with Bipolar Analog Input Range

## Pin Description (continued)

| PIN | NAME            | FUNCTION                                                                                                                                                                                                                                                                                                  |
|-----|-----------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 13  | HBEN            | High-Byte Enable Input. Used to multiplex the 16-bit conversion result.<br>1: MSB available on the data bus.<br>0: LSB available on the data bus.                                                                                                                                                         |
| 14  | $\overline{CS}$ | Convert Start. The first falling edge of $\overline{CS}$ powers up the device and enables acquire mode when $R/\overline{C}$ is low. The second falling edge of $\overline{CS}$ starts conversion. The third falling edge of $\overline{CS}$ loads the result onto the bus when $R/\overline{C}$ is high. |
| 15  | DGND            | Digital Ground                                                                                                                                                                                                                                                                                            |
| 16  | DVDD            | Digital Supply Voltage. Bypass with a 0.1 $\mu$ F capacitor to DGND.                                                                                                                                                                                                                                      |
| 17  | D0/D8           | Tri-State Digital-Data Output. D0 is the LSB.                                                                                                                                                                                                                                                             |
| 18  | D1/D9           | Tri-State Digital-Data Output                                                                                                                                                                                                                                                                             |
| 19  | D2/D10          | Tri-State Digital-Data Output                                                                                                                                                                                                                                                                             |
| 20  | D3/D11          | Tri-State Digital-Data Output                                                                                                                                                                                                                                                                             |

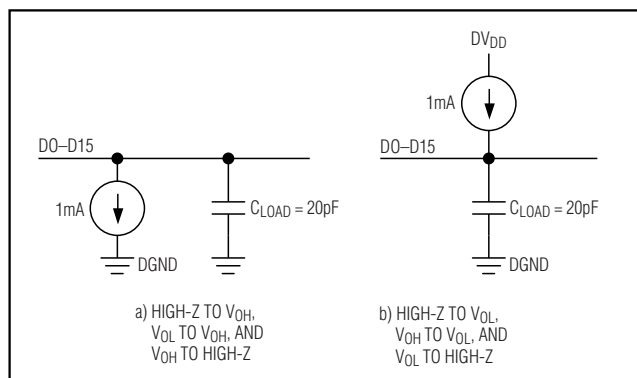


Figure 1. Load Circuits

## Detailed Description

### Converter Operation

The MAX1178/MAX1188 use a successive-approximation (SAR) conversion technique with an inherent track-and-hold (T/H) stage to convert an analog input into a 16-bit digital output. Parallel outputs provide a high-speed interface to microprocessors ( $\mu$ Ps). The *Functional Diagram* shows a simplified internal architecture of the MAX1178/MAX1188. Figure 3 shows a typical operating circuit for the MAX1178/MAX1188.

### Analog Input

#### Input Scaler

The MAX1178/MAX1188 have an input scaler, which allows conversion of true bipolar input voltages and input voltages greater than the power supply, while operating from a single +5V analog supply. The input scaler attenuates and shifts the analog input to match the input range of the internal digital-to-analog converter (DAC). The MAX1178 input voltage range is  $\pm 5V$ , while the MAX1188 input voltage range is  $\pm 10V$ . Figure 4 shows the equivalent input circuit of the MAX1178/MAX1188. This circuit limits the current going into or out of AIN to less than 1.8mA.

#### Track and Hold (T/H)

In track mode, the internal hold capacitor acquires the analog signal (Figure 4). In hold mode, the T/H switches open and the capacitive DAC samples the analog input. During the acquisition, the analog input (AIN) charges capacitor  $C_{HOLD}$ . The acquisition ends on the second falling edge of  $\overline{CS}$ . At this instant, the T/H switches open. The retained charge on  $C_{HOLD}$  represents a sample of the input. In hold mode, the capacitive DAC adjusts during the remainder of the conversion time to restore node T/H OUT to zero within the limits of 16-bit resolution. Force  $\overline{CS}$  low to put valid data on the bus after conversion is complete.

# 16-Bit, 135ksps, Single-Supply ADCs with Bipolar Analog Input Range

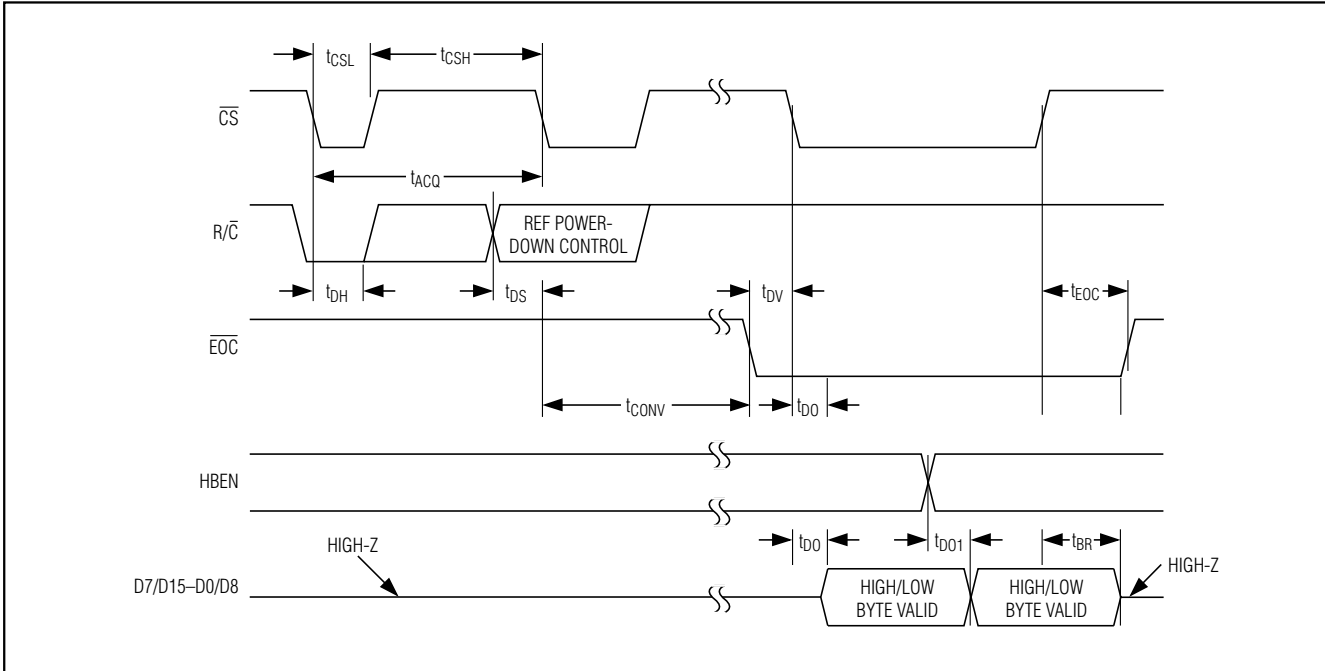


Figure 2. MAX1178/MAX1188 Timing Diagram

## Power-Down Modes

Select standby mode or shutdown mode with the  $\overline{R/\overline{C}}$  bit during the second falling edge of  $\overline{CS}$  (see the *Selecting Standby or Shutdown Mode* section). The MAX1178/MAX1188 automatically enter either standby mode (reference and buffer on) or shutdown mode (reference and buffer off) after each conversion, depending on the status of  $\overline{R/\overline{C}}$  during the second falling edge of  $\overline{CS}$ .

## Internal Clock

The MAX1178/MAX1188 generate an internal conversion clock to free the  $\mu P$  from the burden of running the SAR conversion clock. Total conversion time ( $t_{CONV}$ ) after entering hold mode (second falling edge of  $\overline{CS}$ ) to end-of-conversion ( $\overline{EOC}$ ) falling is 4.7 $\mu s$  (max).

## Applications Information

### Starting a Conversion

$\overline{CS}$  and  $\overline{R/\overline{C}}$  control acquisition and conversion in the MAX1178/MAX1188 (Figure 2). The first falling edge of  $\overline{CS}$  powers up the device and puts it in acquire mode if  $\overline{R/\overline{C}}$  is low. The convert start is ignored if  $\overline{R/\overline{C}}$  is high. The MAX1178/MAX1188 need at least 12ms for the internal reference to wake up and settle before starting the conversion ( $C_{REFADJ} = 0.1\mu F$ ,  $C_{REF} = 10\mu F$ ), if powering up from shutdown.

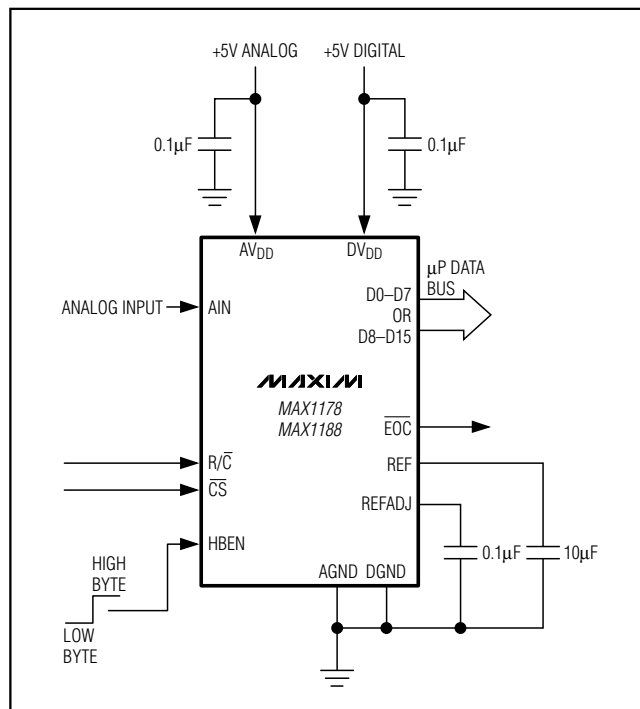


Figure 3. Typical Operating Circuit for the MAX1178/MAX1188



# 16-Bit, 135ksps, Single-Supply ADCs with Bipolar Analog Input Range

## Selecting Standby or Shutdown Mode

The MAX1178/MAX1188 have a selectable standby or low-power shutdown mode. In standby mode, the ADC's internal reference and reference buffer do not power down between conversions, eliminating the need to wait for the reference to power up before performing the next conversion. Shutdown mode powers down the reference and reference buffer after completing a conversion. The reference and reference buffer require a minimum of 12ms to power up and settle from shutdown ( $C_{REFADJ} = 0.1\mu\text{F}$ ,  $C_{REF} = 10\mu\text{F}$ ).

The state of  $R/\overline{C}$  at the second falling edge of  $\overline{CS}$  selects which power-down mode the MAX1178/MAX1188 enter upon conversion completion. Holding  $R/\overline{C}$  low causes the MAX1178/MAX1188 to enter standby mode. The reference and buffer are left on after the conversion completes.  $R/\overline{C}$  high causes the MAX1178/MAX1188 to enter shutdown mode and power-down the reference and buffer after conversion (Figures 5 and 6). Set the voltage at  $R/\overline{C}$  high during the second falling edge of  $\overline{CS}$  to realize the lowest current operation.

### Standby Mode

While in standby mode, the supply current is less than 3.7mA (typ). The next falling edge of  $\overline{CS}$  with  $R/\overline{C}$  low causes the MAX1178/MAX1188 to exit standby mode and begin acquisition. The reference and reference buffer remain active to allow quick turn-on time.

### Shutdown Mode

In shutdown mode, the reference and reference buffer are shut down between conversions. Shutdown mode reduces supply current to 0.5 $\mu\text{A}$  (typ) immediately after the conversion. The next falling edge of  $\overline{CS}$  with  $R/\overline{C}$  low causes the reference and buffer to wake up and enter acquisition mode. To achieve 16-bit accuracy, allow 12ms for the internal reference to wake up ( $C_{REFADJ} = 0.1\mu\text{F}$ ,  $C_{REF} = 10\mu\text{F}$ ).

## Internal and External Reference

### Internal Reference

The internal reference of the MAX1178/MAX1188 is internally buffered to provide +4.096V output at REF. Bypass REF to AGND and REFADJ to AGND with 10 $\mu\text{F}$  and 0.1 $\mu\text{F}$ , respectively. Sink or source current at REFADJ to make fine adjustments to the internal reference. The input impedance of REFADJ is nominally 5k $\Omega$ . Use the circuit in Figure 7 to adjust the internal reference to  $\pm 1.5\%$ .

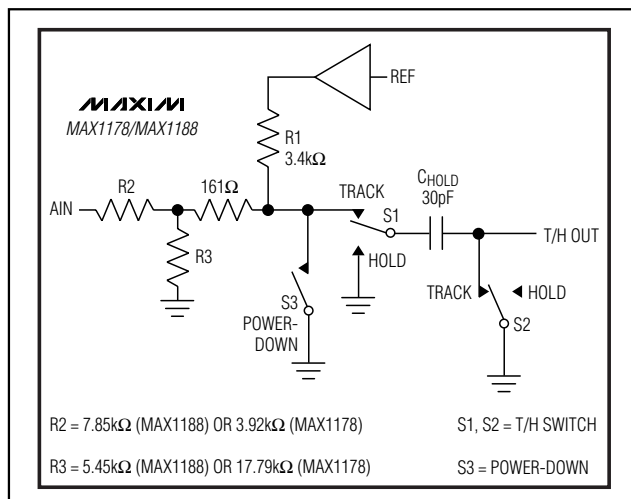


Figure 4. Equivalent Input Circuit

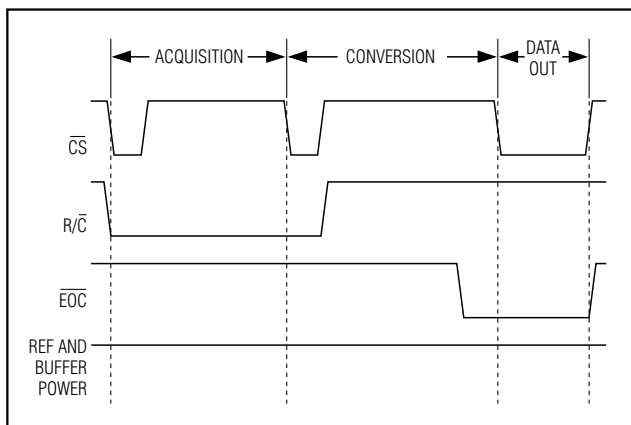


Figure 5. Selecting Standby Mode

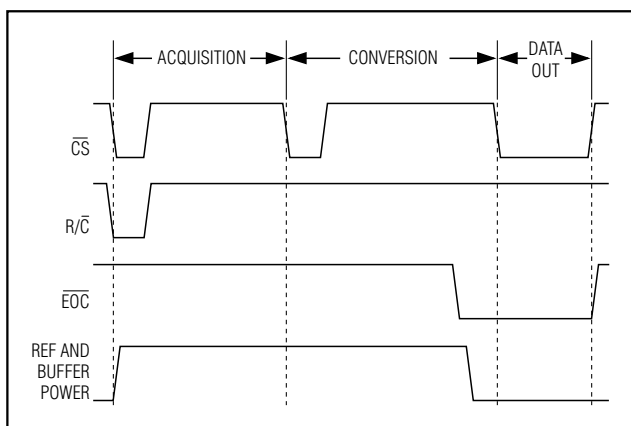


Figure 6. Selecting Shutdown Mode

# 16-Bit, 135ksps, Single-Supply ADCs with Bipolar Analog Input Range

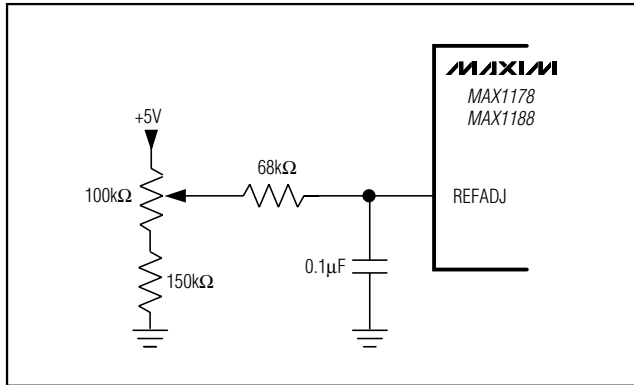


Figure 7. MAX1178/MAX1188 Reference-Adjust Circuit

## External Reference

An external reference can be placed at either the input (REFADJ) or the output (REF) of the MAX1178/MAX1188s' internal buffer amplifier. Using the buffered REFADJ input makes buffering the external reference unnecessary. The input impedance of REFADJ is typically 5kΩ. The internal buffer output must be bypassed at REF with a 10μF capacitor.

Connect REFADJ to AVDD to disable the internal buffer. Directly drive REF using an external 3.8V to 4.2V reference. During conversion, the external reference must be able to drive 100μA of DC load current and have an output impedance of 10Ω or less.

For optimal performance, buffer the reference through an op amp and bypass REF with a 10μF capacitor. Consider the MAX1178/MAX1188s' equivalent input noise (0.6 LSB) when choosing a reference.

## Reading the Conversion Result

$\overline{EOC}$  is provided to flag the μP when a conversion is complete. The falling edge of  $\overline{EOC}$  signals that the data is valid and ready to be output to the bus. D0–D15 are the parallel outputs of the MAX1178/MAX1188. These tri-state outputs allow for direct connection to a microcontroller I/O bus. The outputs remain high impedance during acquisition and conversion. Data is loaded onto the output bus with the third falling edge of  $\overline{CS}$  with  $\overline{R/C}$  high (after  $t_{DO}$ ). Bringing  $\overline{CS}$  high forces the output bus back to high impedance. The MAX1178/MAX1188 then wait for the next falling edge of  $\overline{CS}$  to start the next conversion cycle (Figure 2).

HBEN toggles the output between the high/low byte. The low byte is loaded onto the output bus when HBEN is low, and the high byte is on the bus when HBEN is high.

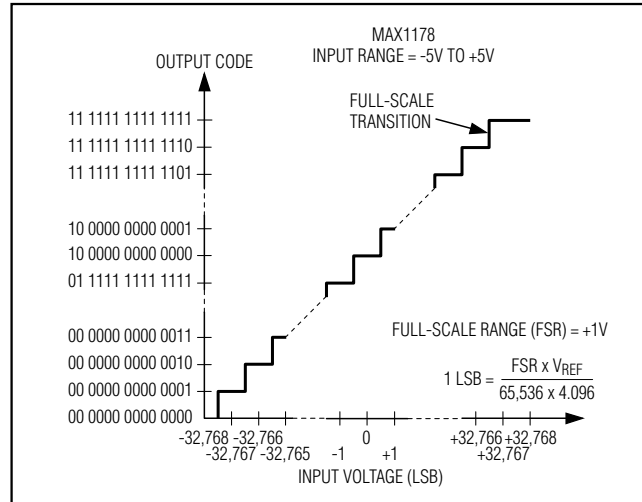


Figure 8. MAX1178 Transfer Function

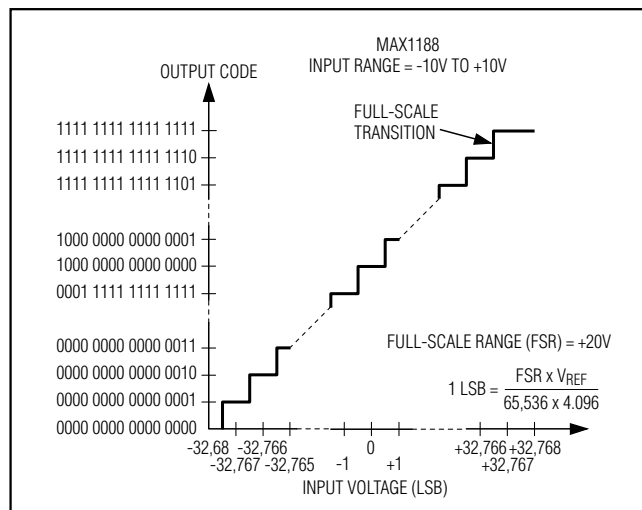


Figure 9. MAX1188 Transfer Function

## Transfer Function

Figures 8 and 9 show the MAX1178/MAX1188 output transfer functions. The MAX1178 and MAX1188 outputs are coded in offset binary.

## Input Buffer

Most applications require an input buffer amplifier to achieve 16-bit accuracy and prevent loading the source. When the input signal is multiplexed, switch the channels immediately after acquisition, rather than near the end of, or after, a conversion. This allows more time for the input buffer amplifier to respond to a large step

# 16-Bit, 135ksps, Single-Supply ADCs with Bipolar Analog Input Range

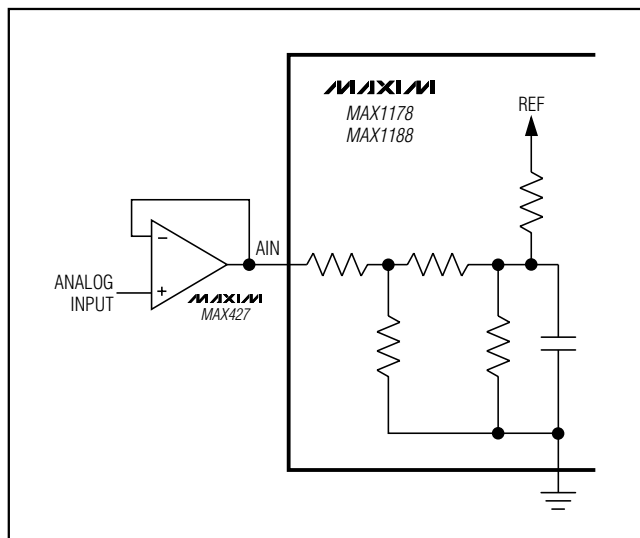


Figure 10. MAX1178/MAX1188 Fast-Settling Input Buffer

change in input signal. The input amplifier must have a high enough slew rate to complete the required output voltage change before the beginning of the acquisition time. Figure 10 shows an example of this circuit using the MAX427.

Figures 11 and 12 show how the MAX1178/MAX1188 analog input current varies depending on whether the chip is operating or powered down. The part is fully powered down between conversions if the voltage at R/C is set high during the second falling edge of CS. The input current abruptly steps to the powered-up value at the start of acquisition. This step in the input current can disrupt the ADC input, depending on the driving circuit's output impedance at high frequencies. If the driving circuit cannot fully settle by the end of acquisition, the accuracy of the system can be compromised. To avoid this situation, increase the acquisition time, use a driving circuit that can settle within  $t_{ACQ}$ , or leave the MAX1178/MAX1188 powered up by setting the voltage at R/C low during the second falling edge of CS.

## Layout, Grounding, and Bypassing

For best performance, use printed circuit boards. Do not run analog and digital lines parallel to each other, and do not lay out digital signal paths underneath the ADC package. Use separate analog and digital ground planes with only one point connecting the two ground systems (analog and digital) as close to the device as possible.

Route digital signals far away from sensitive analog and reference inputs. If digital lines must cross analog lines,

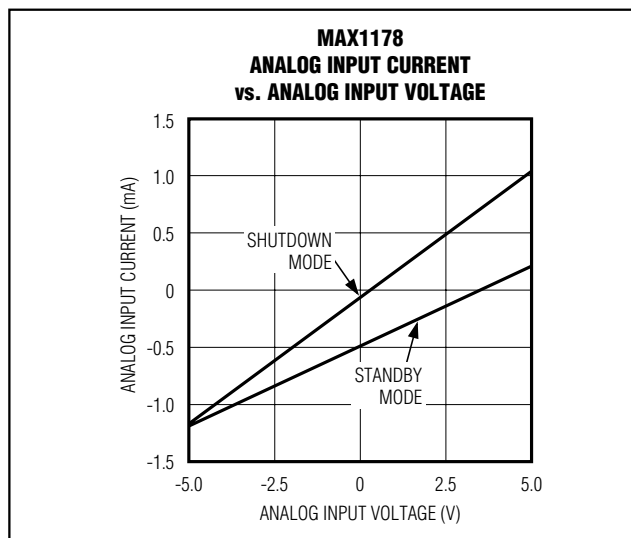


Figure 11. MAX1178 Analog Input Current

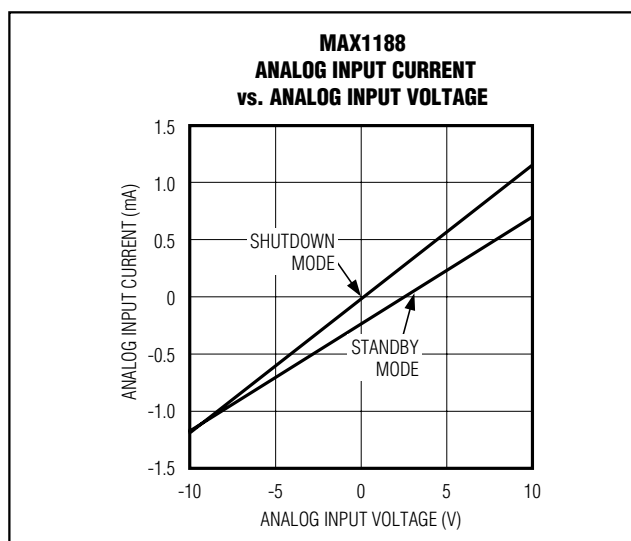


Figure 12. MAX1188 Analog Input Current

do so at right angles to minimize coupling digital noise onto the analog lines. If the analog and digital sections share the same supply, isolate the digital and analog supply by connecting them with a low-value ( $10\Omega$ ) resistor or ferrite bead.

The ADC is sensitive to high-frequency noise on the  $AV_{DD}$  supply. Bypass  $AV_{DD}$  to AGND with a  $0.1\mu F$  capacitor in parallel with a  $1\mu F$  to  $10\mu F$  low-ESR capacitor with the smallest capacitor closest to the device. Keep capacitor leads short to minimize stray inductance.

# 16-Bit, 135ksps, Single-Supply ADCs with Bipolar Analog Input Range

## Definitions

### Integral Nonlinearity

Integral nonlinearity (INL) is the deviation of the values on an actual transfer function from a straight line. This straight line can be either a best-straight-line fit or a line drawn between the end points of the transfer function, once offset and gain errors have been nullified. The static linearity parameters for the MAX1178/MAX1188 are measured using the end-point method.

### Differential Nonlinearity

Differential nonlinearity (DNL) is the difference between an actual step width and the ideal value of 1 LSB. A DNL error specification of 1 LSB guarantees no missing codes and a monotonic transfer function.

### Signal-to-Noise Ratio

For a waveform perfectly reconstructed from digital samples, signal-to-noise ratio (SNR) is the ratio of the full-scale analog input (RMS value) to the RMS quantization error (residual error). The ideal, theoretical minimum analog-to-digital noise is caused by quantization noise error only and results directly from the ADC's resolution (N bits):

$$\text{SNR} = (6.02 \times N + 1.76)\text{dB}$$

where N = 16 bits.

In reality, there are other noise sources besides quantization noise: thermal noise, reference noise, clock jitter, etc. The SNR is computed by taking the ratio of the RMS signal to the RMS noise, which includes all spectral components minus the fundamental, the first five harmonics, and the DC offset.

### Signal-to-Noise Plus Distortion

Signal-to-noise plus distortion (SINAD) is the ratio of the fundamental input frequency's RMS amplitude to the RMS equivalent of all the other ADC output signals:

$$\text{SINAD(dB)} = 20 \times \log \left[ \frac{\text{Signal}_{\text{RMS}}}{(\text{Noise} + \text{Distortion})_{\text{RMS}}} \right]$$

### Effective Number of Bits

Effective number of bits (ENOB) indicates the global accuracy of an ADC at a specific input frequency and sampling rate. An ideal ADC error consists of quantization noise only. With an input range equal to the full-scale range of the ADC, calculate the ENOB as follows:

$$\text{ENOB} = \frac{\text{SINAD} - 1.76}{6.02}$$

### Total Harmonic Distortion

Total harmonic distortion (THD) is the ratio of the RMS sum of the first five harmonics of the input signal to the fundamental itself. This is expressed as:

$$\text{THD} = 20 \times \log \left[ \frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + V_5^2}}{V_1} \right]$$

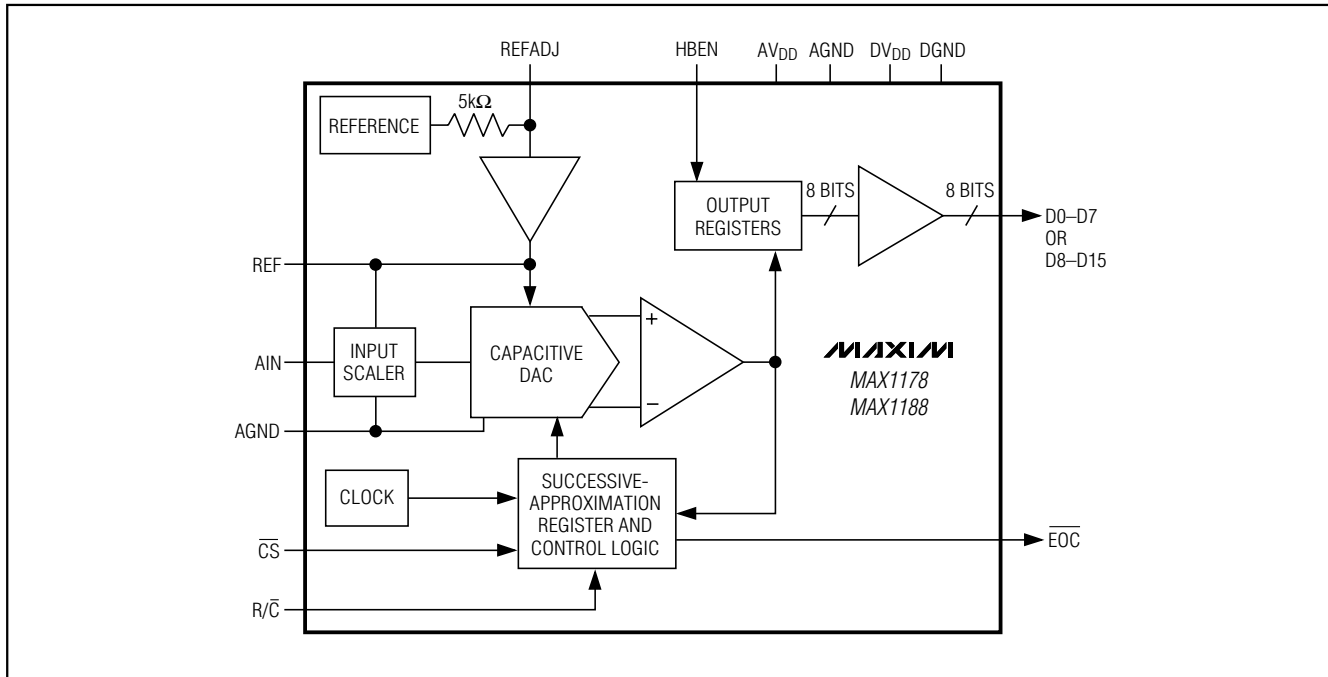
where  $V_1$  is the fundamental amplitude and  $V_2$  through  $V_5$  are the 2nd- through 5th-order harmonics.

### Spurious-Free Dynamic Range

Spurious-free dynamic range (SFDR) is the ratio of the RMS amplitude of the fundamental (maximum signal component) to the RMS value of the next-largest frequency component.

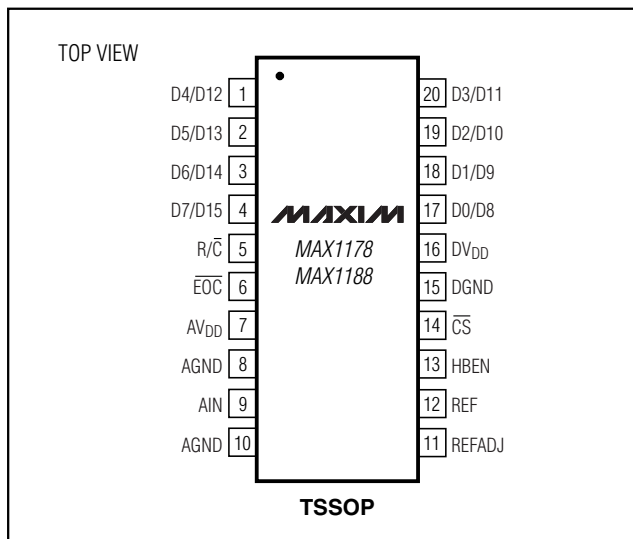
# 16-Bit, 135ksps, Single-Supply ADCs with Bipolar Analog Input Range

## Functional Diagram



**MAX1178/MAX1188**

## Pin Configuration



## Ordering Information (continued)

| PART                | TEMP RANGE     | PIN-PACKAGE | INPUT VOLTAGE RANGE (V) |
|---------------------|----------------|-------------|-------------------------|
| <b>MAX1188</b> ACUP | 0°C to +70°C   | 20 TSSOP    | ±10                     |
| MAX1188BCUP         | 0°C to +70°C   | 20 TSSOP    | ±10                     |
| MAX1188CCUP         | 0°C to +70°C   | 20 TSSOP    | ±10                     |
| MAX1188AEUP         | -40°C to +85°C | 20 TSSOP    | ±10                     |
| MAX1188BEUP         | -40°C to +85°C | 20 TSSOP    | ±10                     |
| MAX1188CEUP         | -40°C to +85°C | 20 TSSOP    | ±10                     |

## Chip Information

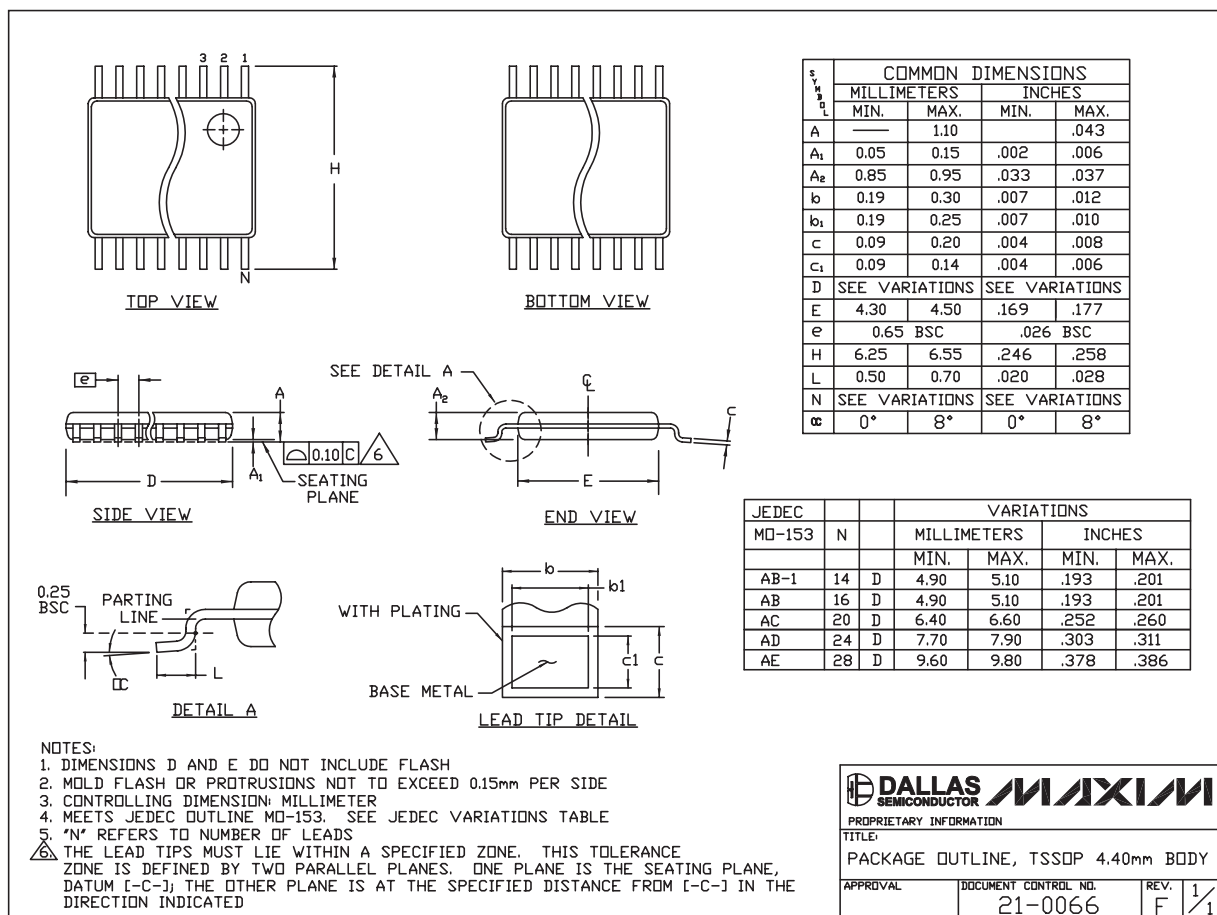
TRANSISTOR COUNT: 15,383

PROCESS: BiCMOS

# 16-Bit, 135ksp/s, Single-Supply ADCs with Bipolar Analog Input Range

## Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to [www.maxim-ic.com/packages](http://www.maxim-ic.com/packages).)



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