19-1425; Rev 0; 1/99

MAXIM

Low-Voltage, High-Isolation, Dual 4-Channel RF/Video Multiplexer

General Description

The MAX4588 low-voltage, dual 4-channel multiplexer is designed for RF and video signal processing at frequencies up to 180MHz in 50Ω and 75Ω systems. A flexible digital interface allows control of on-chip functions through either a parallel interface or an SPI™/MICROWIRE™ serial port.

Each channel of the MAX4588 is designed using a "T" switch configuration, ensuring excellent high-frequency off-isolation. The MAX4588 has low on-resistance of 60Ω max, with an on-resistance match across all channels of 4Ω max. Additionally, on-resistance is flat across the specified signal range (2Ω max). The off-leakage current is under 1nA at T_A = +25°C, and less than 10nA at T_A = +85°C.

The MAX4588 operates from single +2.7V to +12V or dual ±2.7V to ±6V supplies. When operating with a +5V supply, the inputs maintain TTL- and CMOS-level compatibility. The MAX4588 is available in 28-pin narrow DIP, wide SO, and space-saving SSOP packages.

Applications

RF Switching

Video Signal Routing

High-Speed Data Acquisition

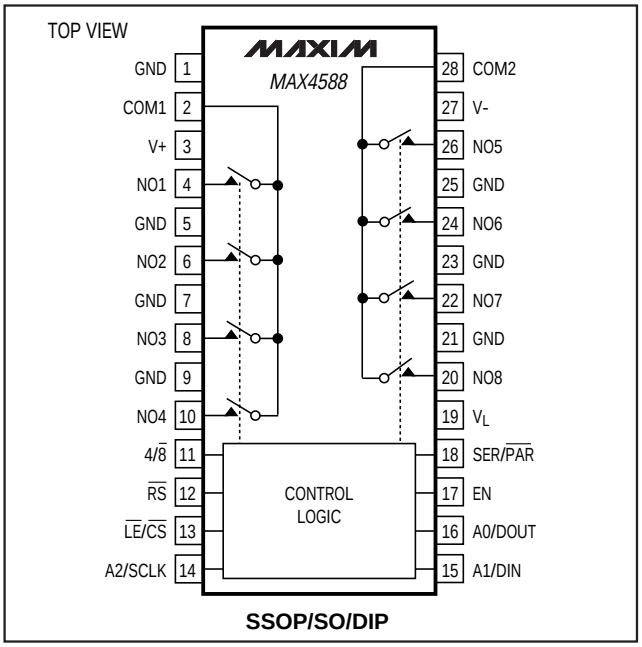
Automatic Test Equipment

Networking

Features

- **Low Insertion Loss: -2.5dB up to 100MHz**
- **High Off-Isolation: -74dB at 10MHz**
- **Low Crosstalk: -70dB up to 10MHz**
- **16MHz -0.1dB Signal Bandwidth**
- **180MHz -3dB Signal Bandwidth**
- **60Ω (max) On-Resistance with ±5V Supplies**
- **4Ω (max) On-Resistance Matching with ±5V Supplies**
- **2Ω (max) On-Resistance Flatness with ±5V Supplies**
- **+2.7V to +12V Single Supply ±2.7V to ±6V Dual Supplies**
- **Low Power Consumption: <20µW**
- **Rail-to-Rail®, Bidirectional Signal Handling**
- **Parallel or SPI/MICROWIRE-Compatible Serial Interface**
- **>±2kV ESD Protection per Method 3015.7**
- **TTL/CMOS-Compatible Inputs with V_L = +5V**

Pin Configuration



SSOP/SO/DIP

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX4588CAI	0°C to +70°C	28 SSOP
MAX4588CWI	0°C to +70°C	28 Wide SO
MAX4588CPI	0°C to +70°C	28 Narrow Plastic DIP
MAX4588EAI	-40°C to +85°C	28 SSOP
MAX4588EWI	-40°C to +85°C	28 Wide SO
MAX4588EPI	-40°C to +85°C	28 Narrow Plastic DIP

SPI is a trademark of Motorola, Inc.
MICROWIRE is a trademark of National Semiconductor Corp.
Rail-to-Rail is a registered trademark of Nippon Motorola, Ltd.

Low-Voltage, High-Isolation, Dual 4-Channel RF/Video Multiplexer

ABSOLUTE MAXIMUM RATINGS

(Voltages referenced to GND)
V+ .....-0.3V to +13.0V
V_L .....-0.3V to (V+ + 0.3V) or 7V (whichever is lower)
V- .....-13.0V to +0.3V
V+ to V-.....-0.3V to +13.0V
$V_{NO\_}$, $V_{COM\_}$ (Note 1) .....(V- - 0.3V) to (V+ + 0.3V)
4/$\overline{8}$, $\overline{RS}$, $\overline{LE}$/$\overline{CS}$, A2/SCLK, A1/DIN,
A0/DOUT, EN, SER/$\overline{PAR}$ to GND .....-0.3V to (V+ + 0.3V)
Continuous Current into Any Terminal.....±20mA
Peak Current into Any Terminal
(pulsed at 1ms, 10% duty cycle).....±40mA
ESD per Method 3015.7.....±2kV
Continuous Power Dissipation (T_A = +70°C)
SSOP (derate 9.52mW/°C above +70°C) 762mW
Wide SO (derate 12.50mW/°C above +70°C).....1.00W
Plastic DIP (derate 14.29mW/°C above +70°C) 1.14W
Operating Temperature Ranges
MAX4588C_ I .....0°C to +70°C
MAX4588E_ I .....-40°C to +85°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10sec) .....+300°C

Note 1: Voltages on these pins exceeding V+ or V- are clamped by internal diodes. Limit forward diode current to maximum current rating.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS—Dual Supplies

(V+ = V_L = +4.5V to +5.5V, V- = -4.5V to -5.5V, V_{INH} = +2.4V, V_{INL} = +0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C, V+ = V_L = +5V, V- = -5V.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	T_A	MIN	TYP	MAX	UNITS
ANALOG SWITCH							
Analog Signal Range (Note 3)	$V_{COM\_}$, V_{NO}			V-		V+	V
On-Resistance	R_{ON}	V+ = 5V, V- = -5V, $V_{NO\_}$ = ±2V, $I_{COM\_}$ = 4mA	+25°C		40	60	Ω
			C, E			75	
On-Resistance Match Between Channels (Note 4)	ΔR_{ON}	V+ = 5V, V- = 5V, $V_{NO\_}$ = ±2V, $I_{COM\_}$ = 4mA	+25°C		1	4	Ω
			C, E			5	
On-Resistance Flatness (Note 5)	$R_{FLAT(ON)}$	V+ = 5V; V- = -5V; $V_{NO\_}$ = 1V, 0, -1V; $I_{COM\_}$ = 1mA	+25°C		0.5	2.5	Ω
			C, E			3	
NO_ Off-Leakage Current (Note 6)	$I_{NO\_(OFF)}$	V+ = 5.5V, V- = -5.5V, $V_{COM\_}$ = ±4.5V, $V_{NO\_}$ = ∓ 4.5V	+25°C	-1	0.01	1	nA
			C, E	-10		10	
COM_ Off-Leakage Current (Note 6)	$I_{COM\_(OFF)}$	V+ = 5.5V, V- = -5.5V, $V_{COM\_}$ = ±4.5V, $V_{NO\_}$ = ∓ 4.5V	+25°C	-2	0.01	2	nA
			C, E	-20		20	
COM_ On-Leakage Current (Note 6)	$I_{COM\_(ON)}$	V+ = 5.5V, V- = -5.5V, $V_{COM\_}$ = ±4.5V, $V_{NO\_}$ = ±4.5V or floating	+25°C	-2	0.01	2	nA
			C, E	-20		20	
LOGIC INPUTS (4/$\overline{8}$, $\overline{RS}$, $\overline{LE}$/$\overline{CS}$, A2/SCLK, A1/DIN, A0/DOUT, EN, SER/$\overline{PAR}$)							
Input Logic Threshold High	V_{INH}		C, E	2.4	1.7		V
Input Logic Threshold Low	V_{INL}		C, E		1.5	0.8	V
Input Threshold Hysteresis					0.2		V
Input Current	I_{IN}	$V_{IN\_}$ = 0 or V_L	C, E	-1	0.03	1	µA
LOGIC OUTPUT (SERIAL INTERFACE)							
DOUT Logic Low Output	V_{OL}	I_{SINK} = 3.2mA	C, E			0.4	V
DOUT Logic High Output	V_{OH}	I_{SOURCE} = -1mA	C, E	V_L - 1			V

ELECTRICAL CHARACTERISTICS—Dual Supplies (continued)

(V+ = V_L = +4.5V to +5.5V, V- = -4.5V to -5.5V, V_{INH} = +2.4V, V_{INL} = +0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C, V+ = V_L = +5V, V- = -5V.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		T_A	MIN	TYP	MAX	UNITS
SWITCH DYNAMIC CHARACTERISTICS								
Turn-On Time	t_{ON}	$V_{NO\_}$ = 3V, V+ = 4.5V, V- = -4.5V, Figure 1		+25°C		380	550	ns
				C, E			600	
Turn-Off Time	t_{OFF}	$V_{NO\_}$ = 3V, V+ = 4.5V, V- = -4.5V, Figure 1		+25°C		150	300	ns
				C, E			350	
Break-Before-Make Time Delay (Note 3)	t_{BBM}	$V_{NO\_}$ = ±3V, V+ = 5.5V, V- = -5.5V, Figure 2		C, E	10	180		ns
Charge Injection	Q	C_L = 1.0nF, $V_{NO\_}$ = 0, R_S = 0, Figure 3		+25°C		15		pC
NO_ Off-Capacitance	$C_{NO\_(OFF)}$	$V_{NO\_}$ = 0, f_{IN} = 1MHz, Figure 4		+25°C		2		pF
COM_ Off-Capacitance	$C_{COM\_(OFF)}$	$V_{COM\_}$ = 0, f_{IN} = 1MHz, Figure 4		+25°C		4		pF
COM_ On-Capacitance	$C_{COM\_(ON)}$	$V_{COM\_}$ = 0, f_{IN} = 1MHz, Figure 4		+25°C		7		pF
Off-Isolation (Note 7)	V_{ISO}	$V_{NO\_}$ = $1V_{RMS}$, f = 10MHz, all channels off, Figure 5		+25°C		-74		dB
Channel-to-Channel Crosstalk	V_{CT}	$V_{NO\_}$ = $1V_{RMS}$, f = 10MHz, Figure 5		+25°C		-70		dB
-3dB Bandwidth	BW	Figure 5	4-channel mode	+25°C		180		MHz
			8-channel mode			140		
-0.1dB Bandwidth	BW	Figure 5	4-channel mode	+25°C		16		MHz
			8-channel mode			11		
PARALLEL-INTERFACE TIMING								
A_, EN to $\overline{LE}$ Rise Setup Time	t_{DS}	Figure 6		C, E	80			ns
A_, EN to $\overline{LE}$ Rise Hold Time	t_{DH}	Figure 6		C, E	0			ns
$\overline{LE}$ Low Pulse Width	t_L	Figure 6		C, E	80			ns
$\overline{RS}$ Low Pulse Width	t_{RS}	Figure 6		C, E	80			ns
SERIAL-INTERFACE TIMING								
Operating Frequency	f_{CLK}	Figure 7		C, E			6.25	MHz
SCLK Pulse Width High	t_{CH}	Figure 7		C, E	80			ns
SCLK Pulse Width Low	t_{CL}	Figure 7		C, E	80			ns
DIN to SCLK Rise Setup Time	t_{DS}	Figure 7		C, E	60			ns
DIN to SCLK Rise Hold Time	t_{DH}	Figure 7		C, E	0			ns
$\overline{CS}$ Fall to SCLK Rise Setup Time	t_{CSS0}	Figure 7		C, E	50			ns
SCLK Rise to DOUT Valid	t_{DO}	C_L = 50pF, Figure 7		C, E			150	ns
$\overline{CS}$ Rise to SCLK Rise Hold Time	t_{CSH1}	Figure 7		C, E	0			ns
$\overline{CS}$ Rise to SCLK Rise Setup Time	t_{CSS1}	Figure 7		C, E	80			ns
$\overline{CS}$ Fall to SCLK Rise Hold Time	t_{CSS1}	Figure 7		C, E	80			ns
$\overline{RS}$ Low Pulse Width	t_{RS}	Figure 6		C, E	80			ns

Low-Voltage, High-Isolation, Dual 4-Channel RF/Video Multiplexer

ELECTRICAL CHARACTERISTICS—Dual Supplies (continued)

(V+ = V_L = +4.5V to +5.5V, V- = -4.5V to -5.5V, V_{INH} = +2.4V, V_{INL} = +0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C, V+ = V_L = +5V, V- = -5V.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	T_A	MIN	TYP	MAX	UNITS
POWER SUPPLY							
Power-Supply Range	V+, V-			±2.7		±6	V
	V_L			2.7		V+	
V+ Supply Current	I+	V+ = 5.5V, V- = -5.5V	+25°C	-1	0.0001	1	µA
			C, E	-10		10	
V - Supply Current	I-	V+ = 5.5V, V- = -5.5V	+25°C	-1	0.0001	1	µA
			C, E	-10		10	
V_L Supply Current	I_L	V_L = 5.5V, all $V_{IN\_}$ = 0 or V_L	C, E	-10	2	10	µA

ELECTRICAL CHARACTERISTICS—Single +5V Supply

(V+ = V_L = +4.5V to +5.5V, V- = 0, V_{INH} = +2.4V, V_{INL} = +0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C, V+ = V_L = +5V.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	T_A	MIN	TYP	MAX	UNITS
ANALOG SWITCH							
Analog Signal Range (Note 3)	$V_{COM\_}$, $V_{NO\_}$			0		V+	V
On-Resistance	R_{ON}	V+ = 5V, $V_{NO\_}$ = 3V, $I_{COM\_}$ = 4mA	+25°C		80	120	Ω
			C, E			150	
On-Resistance Match Between Channels (Note 4)	ΔR_{ON}	V+ = 5V, $V_{NO\_}$ = 3V, $I_{COM\_}$ = 4mA	+25°C		1	8	Ω
			C, E			10	
On-Resistance Flatness (Note 5)	$R_{FLAT(ON)}$	V+ = 5V, $I_{COM\_}$ = 4mA, $V_{NO\_}$ = 2V, 3V, 4V	+25°C		4	10	Ω
			C, E			12	
NO_ Off Leakage Current (Notes 6, 9)	$I_{NO\_(OFF)}$	V+ = 5.5V; $V_{COM\_}$ = 4.5V, 1V; $V_{NO\_}$ = 1V, 4.5V	+25°C	-1	0.005	1	nA
			C, E	-10		10	
COM_ Off Leakage Current (Notes 6, 9)	$I_{COM(OFF)}$	V+ = 5.5V; $V_{COM\_}$ = 4.5V, 1V; $V_{NO\_}$ = 1V, 4.5V	+25°C	-2	0.005	2	nA
			C, E	-20		20	
COM_ On Leakage Current (Notes 6, 9)	$I_{COM\_(ON)}$	V+ = 5.5V; $V_{COM\_}$ = 4.5V, 1V; $V_{NO\_}$ = 4.5V, 1V, or floating	+25°C	-2	0.005	2	nA
			C, E	-20		20	
LOGIC INPUTS (4/$\overline{8}$, $\overline{RS}$, $\overline{LE}$/$\overline{CS}$, A2/SCLK, A1/DIN, A0/DOUT, EN, SER/$\overline{PAR}$)							
Input Logic Threshold High	V_{INH}		C, E	2.4	1.7		V
Input Logic Threshold Low	V_{INL}		C, E		1.5	0.8	V
Input Threshold Hysteresis					0.2		V
Input Current	I_{IN}	V_{IN} = 0 or V_L	C, E	-1		1	µA
LOGIC OUTPUT (SERIAL INTERFACE)							
DOUT Logic Low Output	V_{OL}	I_{SINK} = 3.2mA	C, E			0.4	V
DOUT Logic High Output	V_{OH}	I_{SOURCE} = -1mA	C, E	V_L - 1			V

ELECTRICAL CHARACTERISTICS—Single +5V Supply (continued)

(V+ = V_L = +4.5V to +5.5V, V- = 0, V_{INH} = +2.4V, V_{INL} = +0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C, V+ = V_L = +5V.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		T_A	MIN	TYP	MAX	UNITS
SWITCH DYNAMIC CHARACTERISTICS								
Turn-On Time	t_{ON}	$V_{NO\_}$ = 3V, V+ = 4.5V, Figure 1		+25°C		550	800	ns
				C, E			900	
Turn-Off Time	t_{OFF}	$V_{NO\_}$ = 3V, V+ = 4.5V, Figure 1		+25°C		150	300	ns
				C, E			350	
Break-Before-Make Time Delay (Note 3)	t_{BBM}	$V_{NO\_}$ = 3V, V+ = 5.5V, Figure 2		C, E	10	200		ns
Charge Injection	Q	C_L = 1.0nF, $V_{NO\_}$ = 2.5V, R_S = 0, Figure 3		+25°C		5		pC
Off-Isolation	V_{ISO}	$V_{NO\_}$ = $1V_{RMS}$, f = 10MHz, all channels off, Figure 5		+25°C		-65		dB
Channel-to-Channel Crosstalk	V_{CT}	$V_{NO\_}$ = $1V_{RMS}$, f = 10MHz, Figure 5		+25°C		-70		dB
-3dB Bandwidth	BW	Figure 5	4-channel mode	+25°C		100		MHz
			8-channel mode			75		
-0.1dB Bandwidth	BW	Figure 5	4-channel mode	+25°C		10		MHz
			8-channel mode			7		
PARALLEL-INTERFACE TIMING								
A_, EN to $\overline{LE}$ Rise Setup Time	t_{DS}	Figure 6		C, E	80			ns
A_, EN to $\overline{LE}$ Rise Hold Time	t_{DH}	Figure 6		C, E	0			ns
$\overline{LE}$ Low Pulse Width	t_L	Figure 6		C, E	80			ns
$\overline{RS}$ Low Pulse Width	t_{RS}	Figure 6		C, E	80			ns
SERIAL-INTERFACE TIMING								
Operating Frequency	f_{CLK}	Figure 7		C, E			6.25	MHz
SCLK Pulse Width High	t_{CH}	Figure 7		C, E	80			ns
SCLK Pulse Width Low	t_{CL}	Figure 7		C, E	80			ns
DIN to SCLK Rise Setup Time	t_{DS}	Figure 7		C, E	60			ns
DIN to SCLK Rise Hold Time	t_{DH}	Figure 7		C, E	0			ns
$\overline{CS}$ Fall to SCLK Rise Setup Time	t_{CSS0}	Figure 7		C, E	50			ns
$\overline{CS}$ Fall to SCLK Rise Hold Time	t_{CSS1}	Figure 7		C, E	80			ns
$\overline{CS}$ Rise to SCLK Rise Hold Time	t_{CSH1}	Figure 7		C, E	0			ns
$\overline{CS}$ Rise to SCLK Rise Setup Time	t_{CSS1}	Figure 7		C, E	80			ns
SCLK Rise to DOUT Valid	t_{DO}	C_L = 50pF, Figure 7		C, E			150	ns
$\overline{RS}$ Low Pulse Width	t_{RS}	Figure 6		C, E	80			ns

Low-Voltage, High-Isolation, Dual 4-Channel RF/Video Multiplexer

ELECTRICAL CHARACTERISTICS—Single +5V Supply (continued)

(V+ = V_L = +4.5V to +5.5V, V- = 0, V_{INH} = +2.4V, V_{INL} = +0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C, V+ = V_L = +5V.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	T_A	MIN	TYP	MAX	UNITS
POWER SUPPLY							
Power-Supply Range	V+			2.7		12	V
	V_L	V+ ≤ 6.5V		2.7		V+	
		V+ > 6.5V		2.7		6.5	
V+ Supply Current	I+	V+ = 5.5V, V_{IN} = 0 or V_L	+25°C	-1		1	µA
			C, E	-10		10	
V_L Supply Current	I_L	V_L = 5.5V, all $V_{IN\_}$ = 0 or V_L	C, E	-10	2	10	µA

ELECTRICAL CHARACTERISTICS—Single +3V Supply

(V+ = V_L = +2.7V to +3.6V, V- = 0, V_{INH} = +2V, V_{INL} = +0.5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C, V+ = V_L = +3.0V.)

PARAMETER	SYMBOL	CONDITIONS	T_A	MIN	TYP	MAX	UNITS
ANALOG SWITCH							
Analog Signal Range	$V_{COM\_}$, $V_{NO\_}$			0		V+	V
On-Resistance	R_{ON}	V+ = 2.7V, $V_{NO\_}$ = 1V, $I_{COM\_}$ = 1mA	+25°C		240	350	Ω
			C, E			450	
LOGIC INPUTS (4/$\overline{8}$, $\overline{RS}$, $\overline{LE}$/$\overline{CS}$, A2/SCLK, A1/DIN, A0/DOUT, EN, SER/$\overline{PAR}$)							
Input Logic Threshold High	V_{INH}		C, E	2.0			V
Input Logic Threshold Low	V_{INL}		C, E			0.5	V
Input Current	I_{IN}	$V_{IN\_}$ = 0 or V_L	C, E	-1		1	µA
SWITCH DYNAMIC CHARACTERISTICS							
Turn-On Time	t_{ON}	$V_{NO\_}$ = 1.5V, V+ = 2.7V, Figure 1	+25°C		700	1000	ns
			C, E			200	
Turn-Off Time	t_{OFF}	$V_{NO\_}$ = 1.5V, V+ = 2.7V, Figure 1	+25°C		250	400	ns
			C, E			500	
Break-Before-Make Time Delay (Note 3)	t_{BBM}	$V_{NO\_}$ = 1.5V, V+ = 3.6V, Figure 2	+25°C	10	350		ns
PARALLEL-INTERFACE TIMING							
A_, EN to $\overline{LE}$ Rise Setup Time	t_{DS}	Figure 6	C, E	200			ns
A_, EN to $\overline{LE}$ Rise Hold Time	t_{DH}	Figure 6	C, E	0			ns
$\overline{LE}$ Low Pulse Width	t_L	Figure 6	C, E	200			ns
$\overline{RS}$ Low Pulse Width	t_{RS}	Figure 6	C, E	200			ns
SERIAL-INTERFACE TIMING							
Operating Frequency	f_{CLK}	Figure 7	C, E			2.1	MHz
SCLK Pulse Width High	t_{CH}	Figure 7	C, E	200			ns
SCLK Pulse Width Low	t_{CL}	Figure 7	C, E	200			ns
DIN to SCLK Rise Setup Time	t_{DS}	Figure 7	C, E	100			ns
DIN to SCLK Rise Hold Time	t_{DH}	Figure 7	C, E	0			ns
$\overline{RS}$ Low Pulse Width	t_{RS}	Figure 6	C, E	200			ns

ELECTRICAL CHARACTERISTICS—Single +3V Supply (continued)

(V+ = V_L = +2.7V to +3.6V, V- = 0, V_{INH} = +2V, V_{INL} = +0.5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C, V+ = V_L = +3.0V.)

PARAMETER	SYMBOL	CONDITIONS	T_A	MIN	TYP	MAX	UNITS
$\overline{CS}$ Fall to SCLK Rise Setup Time	t_{CSS0}	Figure 7	C, E	100			ns
$\overline{CS}$ Rise to SCLK Rise Hold Time	t_{CSH1}	Figure 7	C, E	0			ns
$\overline{CS}$ Rise to SCLK Rise Setup Time	t_{CSS1}	Figure 7	C, E	200			ns
$\overline{CS}$ Fall to SCLK Rise Hold Time	t_{CSS1}	Figure 7	C, E	200			ns
SCLK Rise to DOUT Valid	t_{DO}	C_L = 50pF, Figure 7	C, E			250	ns
POWER SUPPLY							
V+ Supply Current	I+	V+ = 3.6V, V_{IN} = 0 or V_L	+25°C	-1		1	µA
			C, E	-10		10	
V_L Supply Current	I_L	V_L = 3.6V, all V_{IN} = 0 or V_L	C, E	-10	1	10	µA

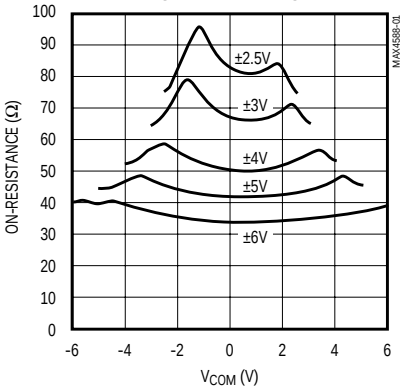
Note 2: The algebraic convention is used in this data sheet; the most negative value is shown in the minimum column.
Note 3: Guaranteed by design.
Note 4: $\Delta R_{ON} = \Delta R_{ON(MAX)} - \Delta R_{ON(MIN)}$.
Note 5: Resistance flatness is defined as the difference between the maximum and the minimum value of on-resistance as measured over the specified analog-signal range.
Note 6: Leakage parameters are 100% tested at maximum rated hot temperature and guaranteed by correlation at T_A = +25°C.
Note 7: Off isolation = $20\log_{10}$ [$V_{COM\_}$ / ($V_{NC\_}$ or $V_{NO\_}$)], $V_{COM\_}$ = output, $V_{NC\_}$ or $V_{NO\_}$ = input to off switch.
Note 8: Between any two switches.
Note 9: Leakage testing for single-supply operation is guaranteed by testing with dual supplies.

Low-Voltage, High-Isolation, Dual 4-Channel RF/Video Multiplexer

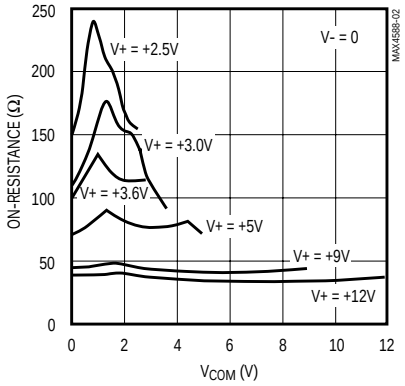
Typical Operating Characteristics

(V+ = V_L = +5V, V- = -5V, T_A = +25°C, unless otherwise noted.)

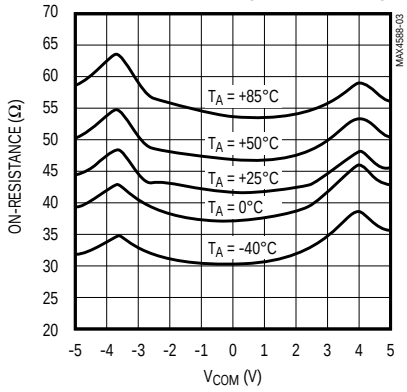
ON-RESISTANCE vs. V_{COM} (DUAL SUPPLIES)



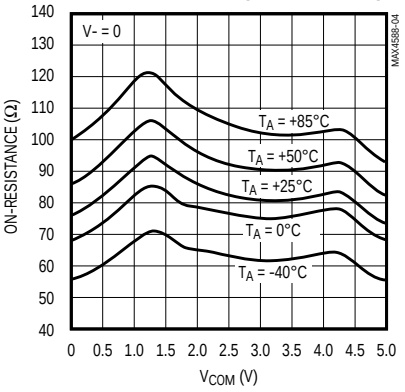
ON-RESISTANCE vs. V_{COM} (SINGLE SUPPLY)



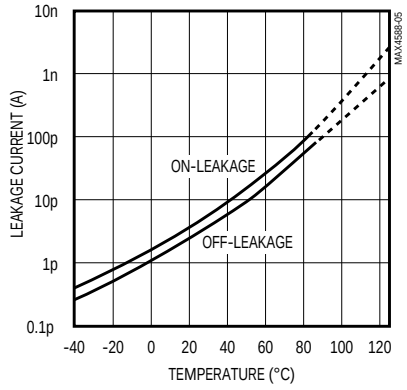
ON-RESISTANCE vs. V_{COM} AND TEMPERATURE (DUAL SUPPLIES)



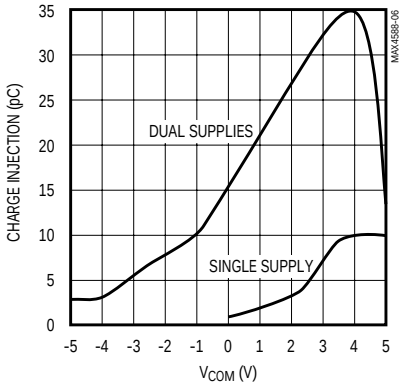
ON-RESISTANCE vs. V_{COM} AND TEMPERATURE (SINGLE SUPPLY)



ON/OFF-LEAKAGE CURRENT vs. TEMPERATURE



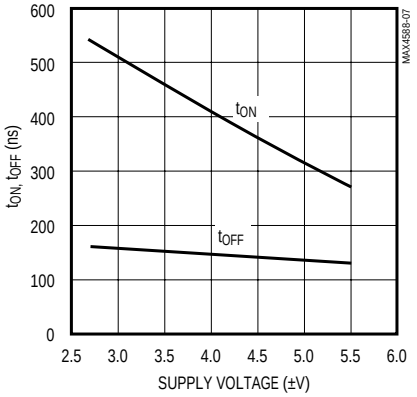
CHARGE INJECTION vs. V_{COM}



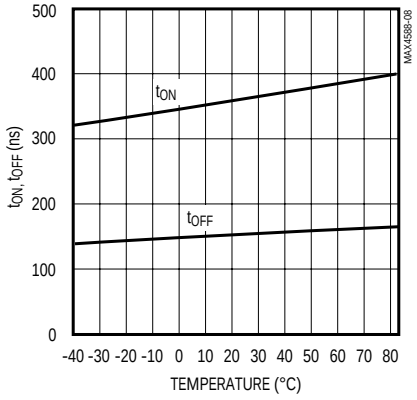
Typical Operating Characteristics (continued)

(V+ = V_L = +5V, V- = -5V, T_A = +25°C, unless otherwise noted.)

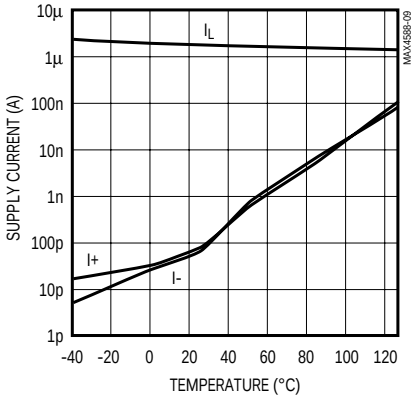
ON/OFF TIME vs. SUPPLY VOLTAGE



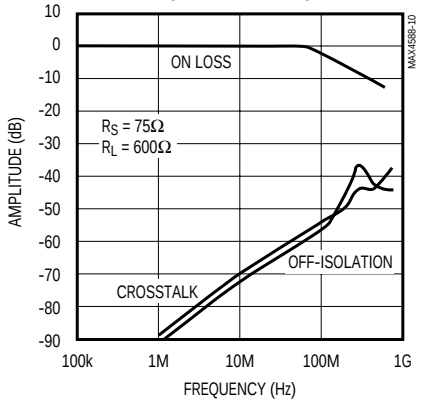
ON/OFF TIME vs. TEMPERATURE



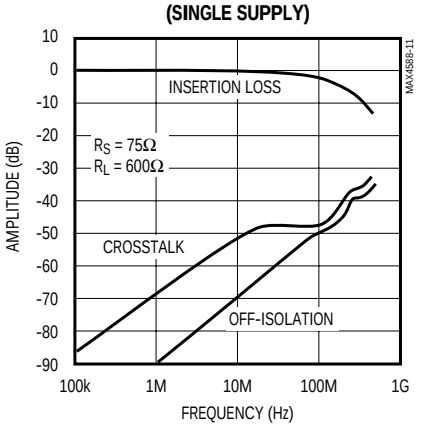
SUPPLY CURRENT vs. TEMPERATURE



INSERTION LOSS, OFF-ISOLATION, AND CROSSTALK vs. FREQUENCY (DUAL SUPPLIES)



INSERTION LOSS, OFF-ISOLATION, AND CROSSTALK vs. FREQUENCY (SINGLE SUPPLY)



Low-Voltage, High-Isolation, Dual 4-Channel RF/Video Multiplexer

Pin Description

PIN	NAME	FUNCTION
1, 5, 7, 9, 21, 23, 25	GND	Ground. Connect all ground pins to a ground plane. See *Grounding* section.
2	COM1	Analog Switch Common Terminal. See *Truth Table.*
3	V+	Analog Positive Supply Voltage Input
4	NO1	Normally Open Analog Input Terminal. See *Truth Tables.*
6	NO2	Normally Open Analog Input Terminal. See *Truth Tables.*
8	NO3	Normally Open Analog Input Terminal. See *Truth Tables.*
10	NO4	Normally Open Analog Input Terminal. See *Truth Tables.*
11	4/$\overline{8}$	Multiplexer Configuration Control. Connect to V_L to select dual 2-channel mode. Connect to GND for single 4-channel multiplexer operation. See *Truth Tables*.
12	$\overline{RS}$	Active-Low Reset Input. In serial mode, drive $\overline{RS}$ low to force the latches and shift registers to the power-on reset state and force all switches open. In parallel mode, drive RS low to force the latches to the power-on reset state and force all switches open. See *Truth Tables*.
13	$\overline{LE}$/$\overline{CS}$	In parallel mode, this pin is the transparent Latch Enable. In the serial mode, this pin is the Chip-Select Input. See *Truth Tables.*
14	A2/SCLK	Most Significant Address Bit in parallel mode with 4/$\overline{8}$ low. If 4/$\overline{8}$ pin is high, this pin is ignored. In the serial mode, this is the Serial Shift Clock Input. Data is loaded on the rising edge of SCLK. See *Truth Tables*.
15	A1/DIN	Address Input in the parallel mode. Serial Data Input in serial mode. In serial mode, data is loaded on SCLK's rising edge.
16	A0/DOUT	Least Significant Address Input in the parallel mode. In the serial mode this is an output from the internal 4-bit shift register. DOUT is intended for daisy-chain cascading. DOUT is not three-stated by $\overline{CS}$. See *Serial Operation*.
17	EN	Switch Enable. Drive EN low to force all channels off. Drive high to allow normal multiplexer operation. Operates asynchronously in serial mode. In parallel mode, EN is latched when $\overline{LE}$ signal is high.
18	SER/$\overline{PAR}$	Interface Select Input. Drive low for parallel data interface operation. Drive high for serial data interface operation and to enable the DOUT driver.
19	V_L	Logic Supply Input. Powers the DOUT driver and other digital circuitry. V_L sets both the digital input and output logic levels.
20	NO8	Normally Open Analog Input Terminal. See *Truth Tables*.
22	NO7	Normally Open Analog Input Terminal. See *Truth Tables*.
24	NO6	Normally Open Analog Input Terminal. See *Truth Tables*.
26	NO5	Normally Open Analog Input Terminal. See *Truth Tables*.
27	V-	Analog Negative Supply Voltage Input. Connect to ground plane for single-supply operation.
28	COM2	Analog Switch Common Terminal. See *Truth Tables*.

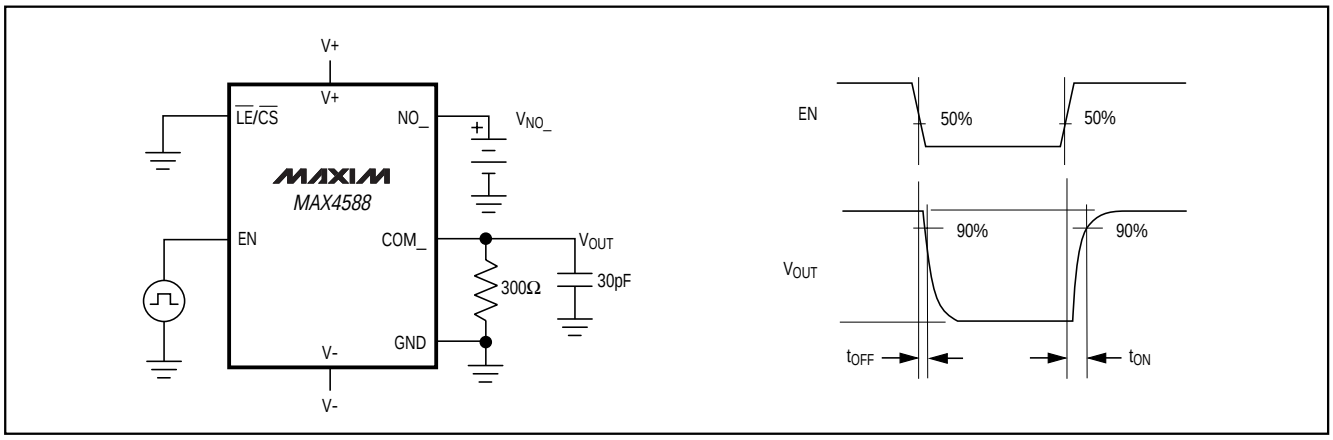


Figure 1. Turn-On/Turn-Off Time

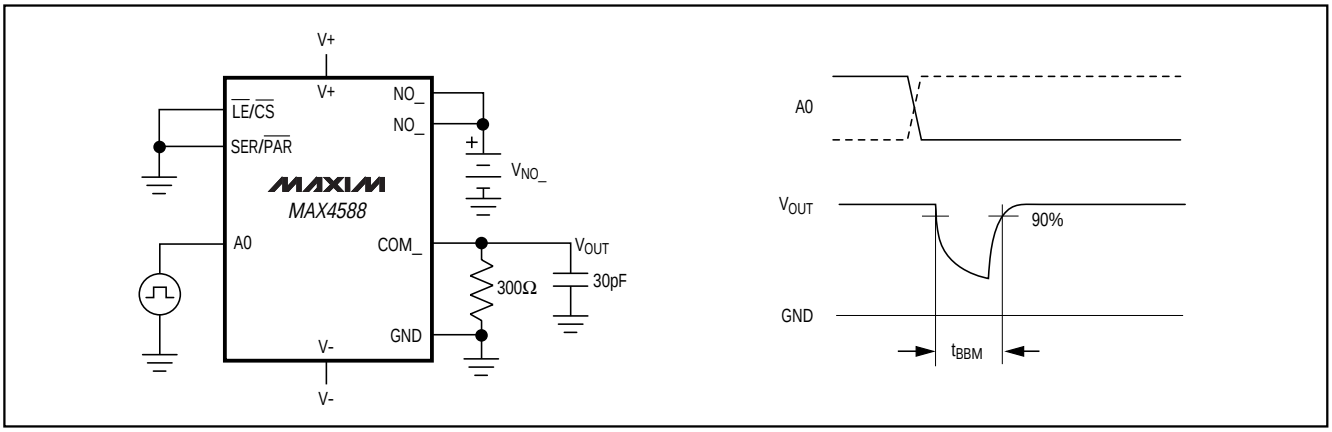


Figure 2. Break-Before-Make Time Delay

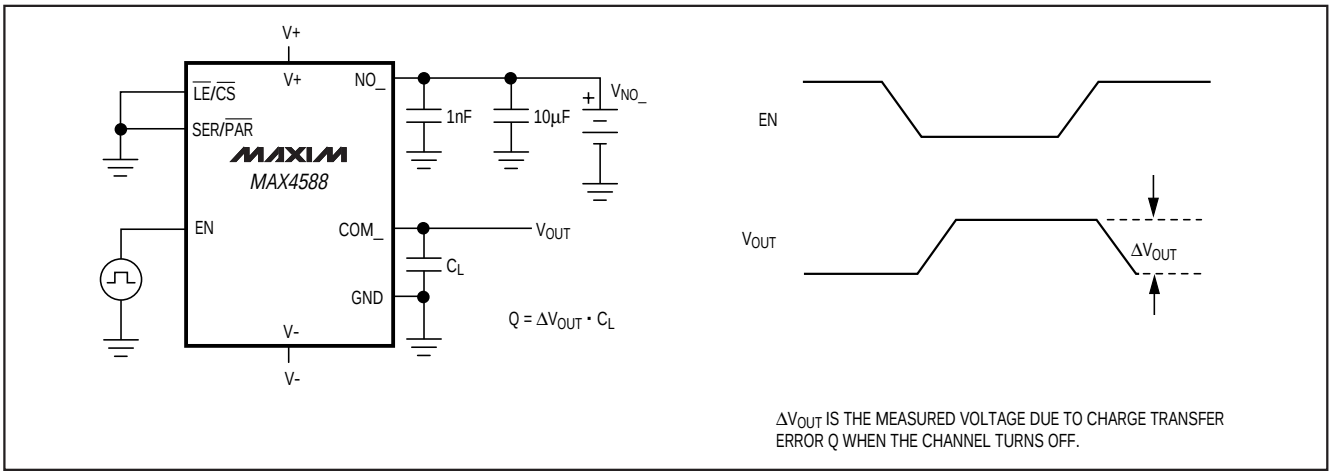


Figure 3. Charge Injection

Low-Voltage, High-Isolation, Dual 4-Channel RF/Video Multiplexer

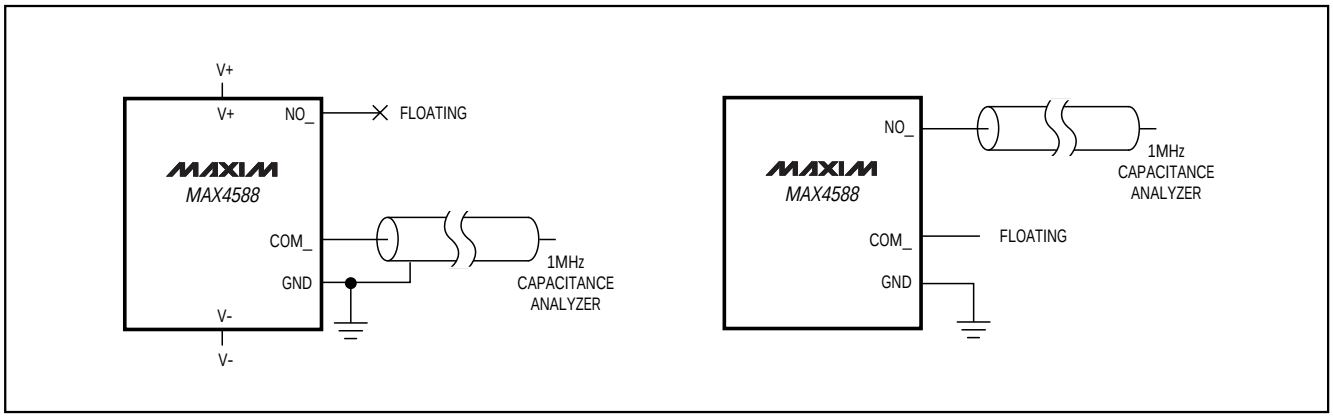


Figure 4. NO_, COM_ Capacitance

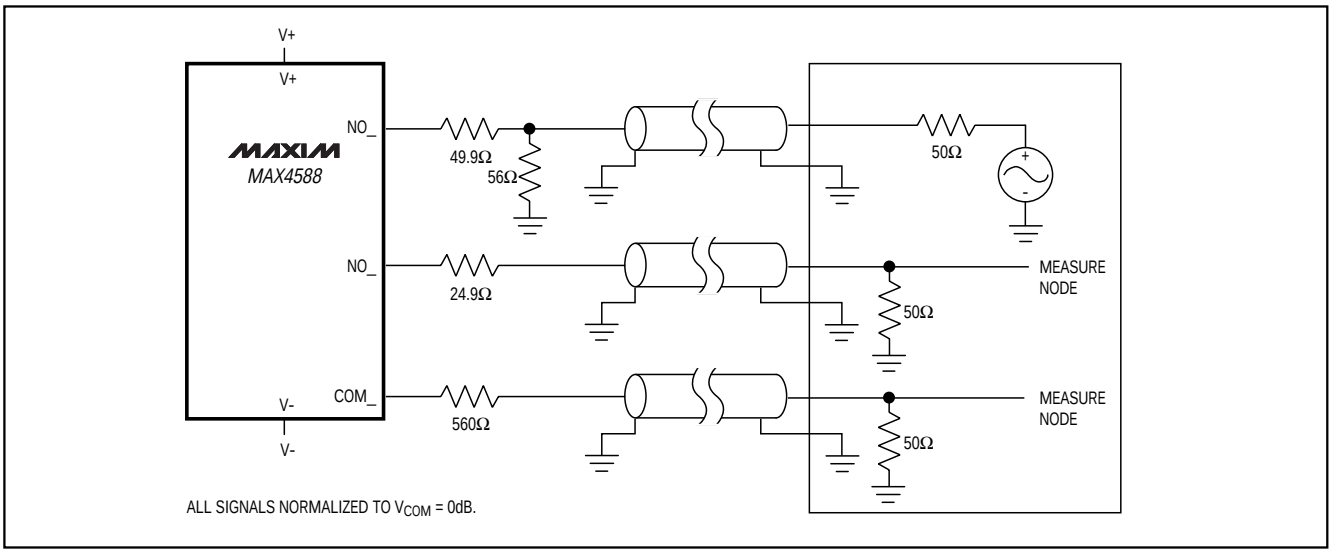


Figure 5. Off-Isolation, Crosstalk, and Bandwidth

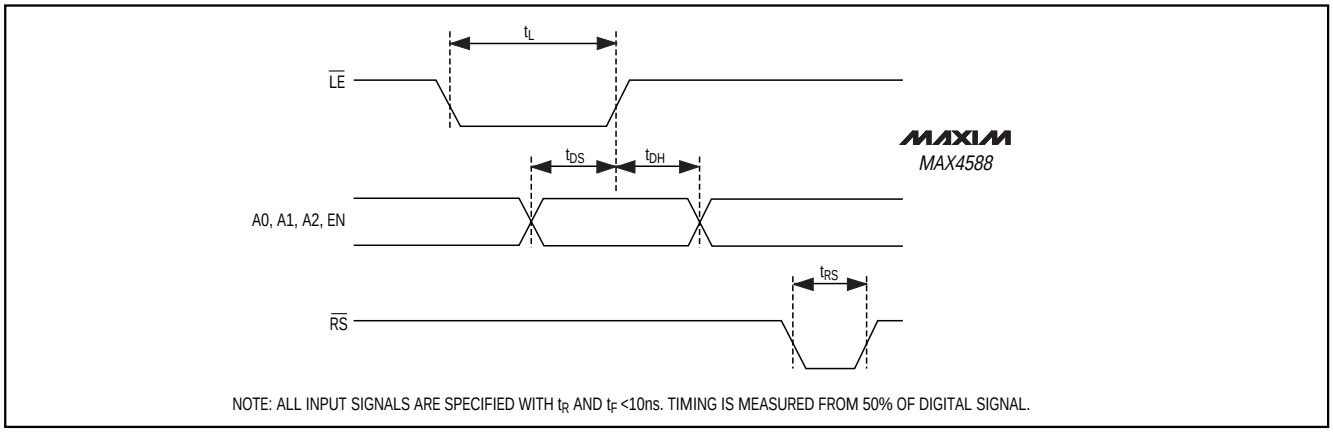


Figure 6. Parallel Timing Diagram

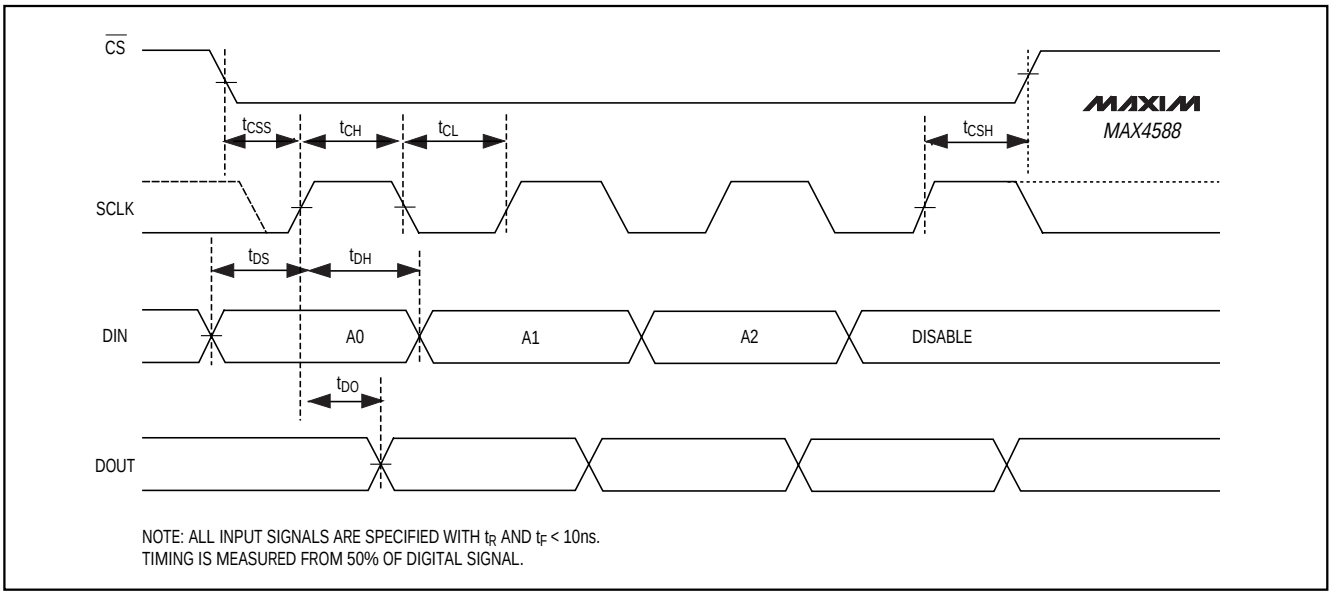


Figure 7. Serial Timing Diagram

Detailed Description

Logic-Level Translators

The MAX4588 is constructed of high-frequency "T" switches, as shown in Figure 8. The logic-level inputs are translated by amplifier A1 into a V+ to V- logic signal that drives amplifier A2. Amplifier A2 drives the gates of N-channel MOSFETs N1 and N2 from V+ to V-, turning them fully on or off. The same signal drives inverter A3 (which drives the P-channel MOSFETs P1 and P2, turning them fully on or off) from V+ to V-, and turns the N-channel MOSFET N3 on and off. The logic-level threshold is determined by V_L and GND.

Switch On Condition

When the switch is on, MOSFETs N1, N2, P1, and P2 are on and MOSFET N3 is off (Figure 8). The signal path is COM_ to NO_, and because both N-channel and P-channel MOSFETs act as pure resistances, it is symmetrical (i.e., signals may pass in either direction). The off MOSFET, N3, has no DC conduction, but has a small amount of capacitance to GND. The four on MOSFETs also have capacitance to ground that, together with the series resistance, forms a lowpass filter. All of these capacitances are distributed evenly along the series resistance, so they act as a transmission line rather than a simple R-C filter. The MAX4588's construction allows an exceptional 180MHz bandwidth when the switches are on.

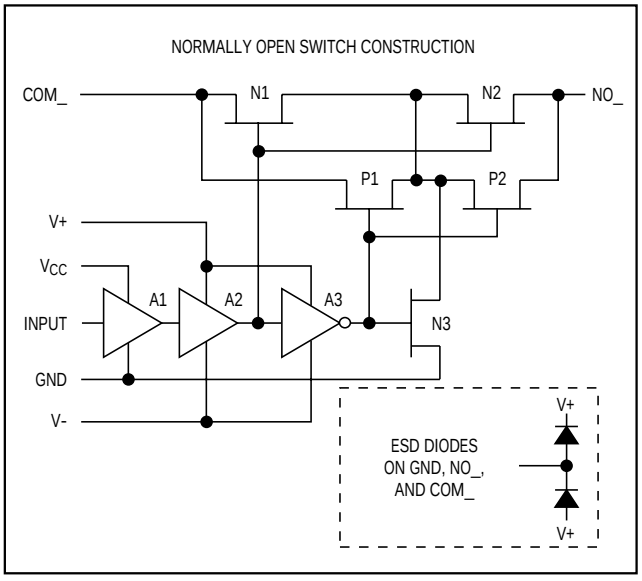


Figure 8. T-Switch Construction

Typical attenuation in 75Ω systems is 2.5dB and is reasonably flat up to 50MHz. Higher-impedance circuits show even lower attenuation (and vice versa), but slightly lower bandwidth due to the increased effect of the internal and external capacitance and the switch's internal resistance.

Low-Voltage, High-Isolation, Dual 4-Channel RF/Video Multiplexer

The MAX4588 is optimized for ±5V operation. Using lower supply voltages or a single supply increases switching time, on-resistance (and therefore on-state attenuation), and nonlinearity.

Switch Off Condition

When the switch is off, MOSFETs N1, N2, P1, and P2 are off and MOSFET N3 is on (Figure 8). The signal path is through the parasitic off-capacitances of the series MOSFETs, but it is shunted to ground by N3. This forms a highpass filter whose exact characteristics are dependent on the source and load impedances. In 75Ω systems, and below 10MHz, the attenuation can exceed 80dB. This value decreases with increasing frequency and increasing circuit impedances. External capacitance and board layout have a major role in determining overall performance.

Applications Information

Power-Supply Considerations

Overview

The MAX4588 construction is typical of many CMOS analog switches. It has four supply pins: V+, V-, V_L, and GND. V+ and V- are used to drive the internal CMOS switches and set the limits of the analog voltage on any switch. Reverse ESD-protection diodes are internally connected between each analog signal pin and both V+ and V-. If the voltage on any pin exceeds V+ or V-, one of these diodes will conduct. During normal operation these reverse-biased ESD diodes leak, forming the only current drawn from V- and V+.

Virtually all the analog leakage current is through the ESD diodes. Although the ESD diodes on a given signal pin are identical, and therefore fairly well balanced, they are reverse-biased differently. Each is biased by either V+ or V- and the analog signal. This means their leakages vary as the signal varies. The difference in the two diode leakages from the signal path to the V+ and V- pins constitutes the analog signal-path leakage current. All analog leakage current flows to the supply terminals, not to the other switch terminal. This explains how both sides of a given switch can show leakage currents of either the same or opposite polarity.

There is no connection between the analog signal paths and GND. The analog signal paths consist of an N-channel and P-channel MOSFET with their sources and drains paralleled and their gates driven out of phase with V+ and V- by the logic-level translators.

V_L and GND power the internal logic and logic-level translators, and set the input logic thresholds. The logic-level translators convert the logic levels to switched V+ and V- signals to drive the gates of the analog switches. This drive signal is the only connection between the logic supplies and the analog supplies.

Bipolar-Supply Operation

The MAX4588 operates with bipolar supplies between ±2.7V and ±6V. The V+ and V- supplies are not required to be symmetrical, but their sum cannot exceed the absolute maximum rating of 13.0V. **Do not connect the MAX4588 V+ pin to +3V and connect the logic-level input pins to +5V logic-level signals. This level exceeds the absolute maximum ratings, and may cause damage to the part and/or external circuits.**

CAUTION: The absolute maximum V+ to V- differential voltage is 13.0V. Typical "±6-Volt" or "12-Volt" supplies with ±10% tolerances can be as high as 13.2V. This voltage can damage the MAX4588. Even ±5% tolerance supplies may have overshoot or noise spikes that exceed 13.0V.

Single-Supply Operation

The MAX4588 operates from a single supply between +2.7V and +12V when V- is connected to GND. Observe all of the precautions listed in the *Bipolar-Supply Operation* section. Note, however, that these parts are optimized for ±5V operation, and AC and DC characteristics are degraded significantly when operating at less than ±5V. As the overall supply voltage (V+ to V-) is reduced, switching speed, on-resistance, off-isolation, and distortion are degraded (see *Typical Operating Characteristics*).

Single-supply operation also limits signal levels and interferes with grounded signals. When V- = 0, AC signals are limited to -0.3V. Voltages below -0.3V can be clipped by the internal ESD-protection diodes, and the parts can be damaged if excessive current flows.

Power Off

When power to the MAX4588 is off (i.e., V+ = 0 and V- = 0), the *Absolute Maximum Ratings* still apply. This means that none of the MAX4588 pins can exceed ±0.3V. Voltages beyond ±0.3V cause the internal ESD-protection diodes to conduct, with potentially catastrophic consequences.

Power-Supply Sequencing

When applying power to the MAX4588, follow this sequence: V+, V- (if biased to potential other than ground), V_L, then logic inputs. Apply signals on the analog NO_ and COM_ pins any time after V+, V-, and GND voltages are set. Turning on all pins simultaneously is acceptable only if the circuit design guarantees concurrent power-up.

The power-down sequence is the opposite of the power-up sequence. That is, the V_L and logic inputs must go to zero potential before (or simultaneously with) the V- then V+ supplies. The *Absolute Maximum Ratings* must always be observed in order to ensure proper operation.

Grounding

DC Ground Considerations

Satisfactory high-frequency operation requires that careful consideration be given to grounding. **For most applications, a ground plane is strongly recommended, and all GND pins must connect to it with solid copper.** While the V+ and V- power-supply pins are common to all switches in a given package, each input is separated with ground pins that are not internally connected to each other. This contributes to the overall high-frequency performance by reducing channel-to-channel crosstalk. All the GND pins have ESD diodes to V+ and V-.

In systems that have separate digital and analog (signal) grounds, connect all GND pins to analog signal ground. Preserving a good signal ground is much more important than preserving a digital ground. Ground current is only a few nanoamperes.

The digital inputs have voltage thresholds determined by V_L and GND (V- does not influence the logic-level threshold). With +5V applied to V_L, the threshold is about 1.6V, ensuring compatibility with TTL- and CMOS-logic drivers.

AC Ground and Bypassing

A ground plane is mandatory for satisfactory high-frequency operation. Prototyping using hand wiring or wire-wrap boards is not recommended. Connect all GND pins to the ground plane with solid copper. (The GND pins extend the high-frequency ground through the package wire-frame, into the silicon itself, thus improving isolation.) Make the ground plane solid metal underneath the device, without interruptions. There should be no traces under the device itself. For DIP packages, this applies to both sides of a two-sided board. Failure to observe this has a minimal effect on the “on” characteristics of the switch at high frequencies, but will degrade the off-isolation and crosstalk.

When using the MAX4588’s SO package on PC boards with a buried ground plane, connect each GND pin to the ground plane with a separate via. Do not share this via with any other ground path. Providing a ground via on both sides of the SMT land further enhances the off-isolation by lowering the parasitic inductance. The DIP package can have the through-holes directly tied to the buried plane, or thermally relieved as required to meet manufacturability requirements. Again, do not use the through-hole pads as the current path for any other components.

Bypass all V+ and V- pins to the ground plane with surface-mount 0.01µF capacitors. Locate these capacitors as close as possible to the pins on the same side of the board as the device. Do not use feedthroughs or vias for bypass capacitors. If board layout dictates that the bypass capacitors are mounted on the opposite side of the PC board, use short feedthroughs or vias, directly under the V+ and V- pins. Use multiple vias if possible. If V- is 0, connect it directly to the ground plane with solid copper. Keep all traces short.

Signal Routing

Keep all signal leads as short as possible. Separate all signal leads from each other, and keep them away from any other traces that could induce interference. Separating the signal traces with generously sized ground wires also helps minimize interference. Routing signals via coaxial cable, terminated as close to the MAX4588 as possible, provides the highest isolation.

Board Layout

IC sockets degrade high-frequency performance and should not be used if signal bandwidth exceeds 5MHz. Surface-mount parts, having shorter internal lead frames, provide the best high-frequency performance. Keep all bypass capacitors close to the device, and separate all signal leads with ground planes. Such grounds tend to be wedge-shaped as they get closer to the device. Use vias to connect the ground planes on each side of the board, and place the vias in the apex of the wedge-shaped grounds that separate signal leads. Logic-level signal lead placement is not critical.

Impedance Matching

The MAX4588 is intended for use in 75Ω systems, where the inputs are terminated external to the IC and the COM terminals see an impedance of 600Ω or higher. The MAX4588 can operate in 50Ω and 75Ω systems with terminations through the IC. However, variations in R_{ON} and R_{ON} flatness cause nonlinearities.

Crosstalk and Off-Isolation

The graphs shown in *Typical Operating Characteristics* for crosstalk and off-isolation are taken on adjacent channels. The adjacent channel is the worst-case condition. For example, NO1 has the worst off-isolation to COM1 due to their proximity. Furthermore, NO1 has the most crosstalk to NO2, and the least crosstalk to NO4. Choosing channels wisely necessitates separating the most sensitive channels from the most offensive. Conversely, the above information also applies to the NO5–NO8 inputs to the COM2 pin.

Low-Voltage, High-Isolation, Dual 4-Channel RF/Video Multiplexer

Power-On Reset (POR)

The MAX4588 has internal circuitry to guarantee a known state on power-up. In the default state, A0 = A1 = A2 = 0, disable = 1, and all switches are off. This state is equivalent to asserting $\overline{RS}$ during normal operation.

Serial Operation

The serial mode is activated by driving the SER/$\overline{PAR}$ input pin to a logic high. The data is then entered using a normal SPI/MICROWIRE write operation. Refer to Figure 7 for a detailed diagram of the serial-interface logic. There are four flip-flops in the shift register, with the output of the fourth shift register being output on the DOUT pin. **Note: DOUT changes on the rising edge of SCLK.** This allows cascading of multiple MAX4588s using only one chip-select line. For example, one 16-bit write could load the shift registers of four cascaded MAX4588s. The data from the shift register is moved to the internal control latches only upon the rising edge of $\overline{CS}$, so all four MAX4588s change state simultaneously.

Parallel Operation

The parallel mode is activated by driving SER/$\overline{PAR}$ to a logic low. The MAX4588 is programmed by a latched parallel bus scheme. Refer to Figure 6 for a detailed diagram of the parallel-interface logic. Note that 4/$\overline{8}$ is not latched. It is best to hard-wire 4/$\overline{8}$ to a known state for the desired mode of operation, or to use a dedicated microcontroller port pin.

Truth Tables

Parallel Operation

SER/$\overline{PAR}$	A2	A1	A0	EN	$\overline{LE}$	$\overline{RS}$	4/$\overline{8}$	SWITCH STATES
0	x	x	x	x	1	1	x	Maintain previous state.
x	x	x	x	x	x	0	x	All switches off, latches are cleared.
1	x	x	x	x	x	1	x	Serial Mode. Refer to *Serial Operation Truth Table*.
0	x	x	x	0	0	1	x	All switches off.
0	0	0	0	1	0	1	0	Connects NO1 to COM1
0	0	0	1	1	0	1	0	Connects NO2 to COM1
0	0	1	0	1	0	1	0	Connects NO3 to COM1
0	0	1	1	1	0	1	0	Connects NO4 to COM1
0	1	0	0	1	0	1	0	Connects NO5 to COM2
0	1	0	1	1	0	1	0	Connects NO6 to COM2
0	1	1	0	1	0	1	0	Connects NO7 to COM2
0	1	1	1	1	0	1	0	Connects NO8 to COM2
0	x	0	0	1	0	1	1	Connect NO1 to COM1 and NO5 to COM2
0	x	0	1	1	0	1	1	Connect NO2 to COM1 and NO6 to COM2
0	x	1	0	1	0	1	1	Connect NO3 to COM1 and NO7 to COM2
0	x	1	1	1	0	1	1	Connect NO4 to COM1 and NO8 to COM2

x = Don't Care

Note: *4/8 is not latched when LE is high. When LE is low, all latches are transparent. A2, A1, A0, and EN are latched. Connect COM1 to COM2 externally for 1-of-8 single-ended operation.*

Truth Tables (continued)

Serial Operation

SER/$\overline{PAR}$	$\overline{CS}$	SCLK	DIN	EN	$\overline{RS}$	DOUT	ON SWITCHES/STATES
1	x	x	x	x	0	0	All switches off. Latches and shift register are cleared. This is the power-on reset (POR) state.
0	x	x	x	x	x	High-Z	Parallel Mode. Refer to *Parallel Operation Truth Table.*
1	x	x	x	0	1	*	All switches off.
1	1	x	x	1	1	*	Chip unselected.
1	0	⎍	0	1	1	*	Input shift register loads one bit from DIN. DOUT updates on SCLK's rising edge.
1	0	⎍	1	1	1	*	Input shift register loads one bit from DIN. DOUT updates on SCLK's rising edge.
1	⎍	x	x	1	1	*	Contents of shift register transferred to control latches.

x = Don't Care
**DOUT is delayed by 4 clock cycles from DIN.*

Control Bit and 4/$\overline{8}$ Logic

DISABLE BIT	A2 BIT	A1 BIT	A0 BIT	4/$\overline{8}$ PIN	ON SWITCHES/STATES
1	x	x	x	x	All switches off.
0	0	0	0	0	Connect NO1 to COM1
0	0	0	1	0	Connect NO2 to COM1
0	0	1	0	0	Connect NO3 to COM1
0	0	1	1	0	Connect NO4 to COM1
0	1	0	0	0	Connect NO5 to COM2
0	1	0	1	0	Connect NO6 to COM2
0	1	1	0	0	Connect NO7 to COM2
0	1	1	1	0	Connect NO8 to COM2
0	x	0	0	1	Connect NO1 to COM1 and NO5 to COM2
0	x	0	1	1	Connect NO2 to COM1 and NO6 to COM2
0	x	1	0	1	Connect NO3 to COM2 and NO7 to COM2
0	x	1	1	1	Connect NO4 to COM2 and NO8 to COM2

x = Don't Care
Note: *DISABLE, A2, A1, and A0 are the 4 bits latched into the MAX4588 with a MICROWIRE/SPI write. A0 is the LSB (first bit in time). DISABLE is the MSB (last bit in time).*

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Chip Information

TRANSISTOR COUNT: 1033

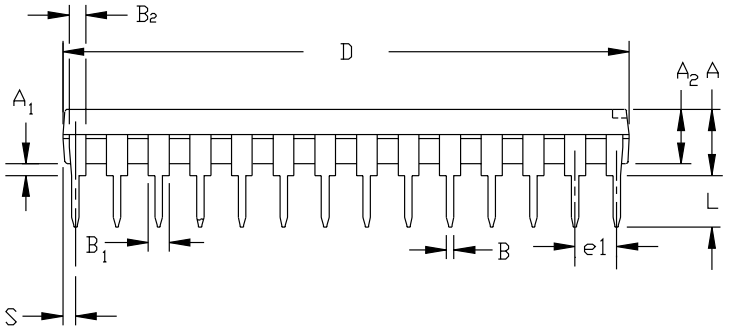
Package Information

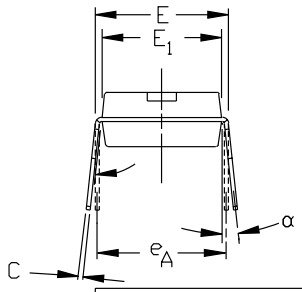
28LNPDIP.EPS

NOTES:

1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .254mm(.010").
3. CONTROLLING DIMENSION: MILLIMETER.
4. MEETS JEDEC MO-095-AH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	---	0.180	---	4.572
A1	0.020	---	0.508	---
A2	0.125	0.150	3.175	3.810
B	0.015	0.022	0.381	0.559
B1	0.045	0.060	1.143	1.524
B2	0.035	0.045	0.889	1.143
C	0.008	0.012	0.203	0.305
D	1.350	1.380	34.290	35.052
E	0.300	0.325	7.620	8.255
E1	0.275	0.295	6.985	7.493
e1	.100 BSC		2.540 BSC	
eA	.300 BSC		7.62 BSC	
L	0.115	0.150	2.921	3.810
α	0°	15°	0°	15°





MAXIM

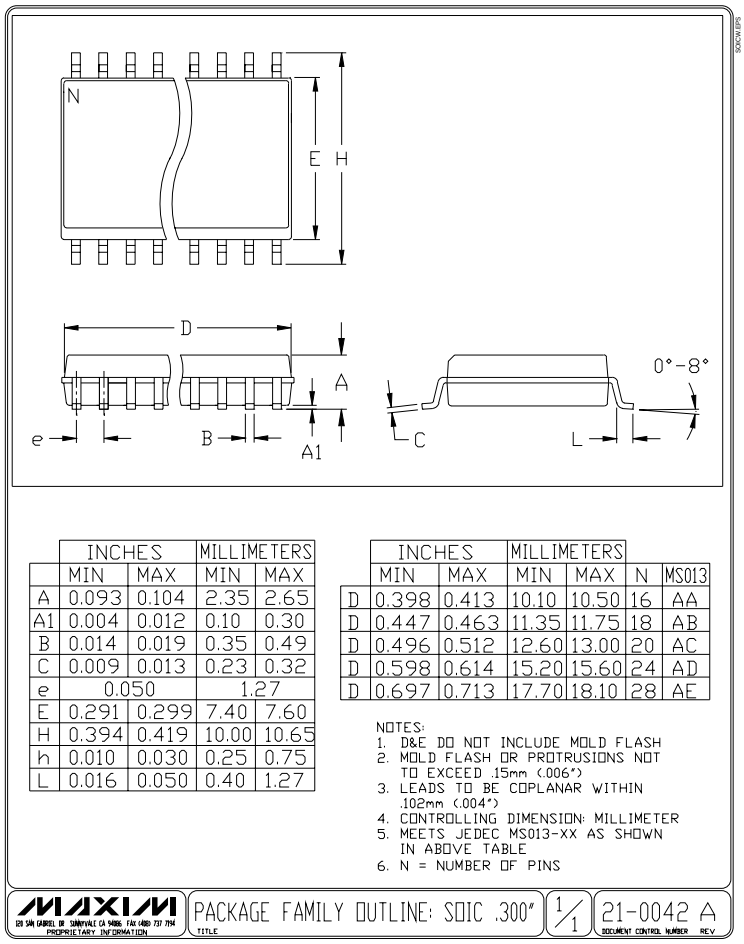
PROPRIETARY INFORMATION

TITLE:

28L(NAR) PDIP OUTLINE

APPROVAL	DOCUMENT CONTROL NO.	REV	
	21-0400	A	1/1

Package Information (continued)



	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.093	0.104	2.35	2.65
A1	0.004	0.012	0.10	0.30
B	0.014	0.019	0.35	0.49
C	0.009	0.013	0.23	0.32
e	0.050		1.27	
E	0.291	0.299	7.40	7.60
H	0.394	0.419	10.00	10.65
h	0.010	0.030	0.25	0.75
L	0.016	0.050	0.40	1.27

	INCHES		MILLIMETERS			
	MIN	MAX	MIN	MAX	N	MS013
D	0.398	0.413	10.10	10.50	16	AA
D	0.447	0.463	11.35	11.75	18	AB
D	0.496	0.512	12.60	13.00	20	AC
D	0.598	0.614	15.20	15.60	24	AD
D	0.697	0.713	17.70	18.10	28	AE

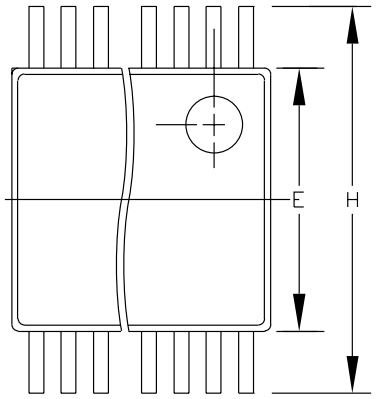
NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15mm (.006")
3. LEADS TO BE COPLANAR WITHIN .102mm (.004")
4. CONTROLLING DIMENSION: MILLIMETER
5. MEETS JEDEC MS013-XX AS SHOWN IN ABOVE TABLE
6. N = NUMBER OF PINS

MAXIM | 120 SAN GABRIEL DR SUNNYVALE CA 94086 FAX (408) 737 7194 PROPRIETARY INFORMATION | PACKAGE FAMILY OUTLINE: SOIC .300" TITLE | 1/1 | 21-0042 A DOCUMENT CONTROL NUMBER REV

Low-Voltage, High-Isolation, Dual 4-Channel RF/Video Multiplexer

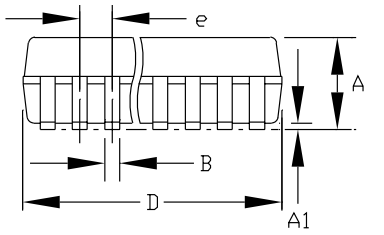
Package Information (continued)

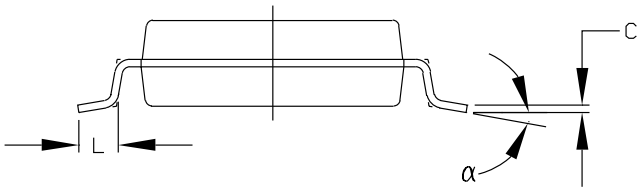
SSOP.EPS



	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.068	0.078	1.73	1.99
A1	0.002	0.008	0.05	0.21
B	0.010	0.015	0.25	0.38
C	0.004	0.008	0.09	0.20
D	SEE VARIATIONS			
E	0.205	0.209	5.20	5.38
e	0.0256 BSC		0.65 BSC	
H	0.301	0.311	7.65	7.90
L	0.025	0.037	0.63	0.95
α	0°	8°	0°	8°

	INCHES		MILLIMETERS		
	MIN	MAX	MIN	MAX	
D	0.239	0.249	6.07	6.33	14L
D	0.239	0.249	6.07	6.33	16L
D	0.278	0.289	7.07	7.33	20L
D	0.317	0.328	8.07	8.33	24L
D	0.397	0.407	10.07	10.33	28L





NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15mm (.006")
3. CONTROLLING DIMENSION: MILLIMETER

MAXIM
PROPRIETARY INFORMATION

TITLE:
PACKAGE OUTLINE, SSOP, 5.3X.65mm

APPROVAL	DOCUMENT CONTROL NO.	REV	
	21-0056	A	1/1

Общество с ограниченной ответственностью «МосЧип» ИНН 7719860671 / КПП 771901001
Адрес: 105318, г.Москва, ул.Щербаковская д.3, офис 1107

Данный компонент на территории Российской Федерации

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Для оперативного оформления запроса Вам необходимо перейти по данной ссылке:

http://moschip.ru/get-element

Вы можете разместить у нас заказ для любого Вашего проекта, будь то серийное производство или разработка единичного прибора.

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Нашей специализацией является поставка электронной компонентной базы двойного назначения, продукции таких производителей как XILINX, Intel (ex.ALTERA), Vicor, Microchip, Texas Instruments, Analog Devices, Mini-Circuits, Amphenol, Glenair.

Сотрудничество с глобальными дистрибьюторами электронных компонентов, предоставляет возможность заказывать и получать с международных складов практически любой перечень компонентов в оптимальные для Вас сроки.

На всех этапах разработки и производства наши партнеры могут получить квалифицированную поддержку опытных инженеров.

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Офис по работе с юридическими лицами:

105318, г.Москва, ул.Щербаковская д.3, офис 1107, 1118, ДЦ «Щербаковский»

Телефон: +7 495 668-12-70 (многоканальный)

Факс: +7 495 668-12-70 (доб.304)

E-mail: info@moschip.ru

Skype отдела продаж:
moschip.ru
moschip.ru_4
moschip.ru_6
moschip.ru_9