

# PFE1500-12-054 Series

## AC-DC Power Supply

The PFE1500-12-054 is a series of 1500 Watt AC to DC power-factor-corrected (PFC) power supplies that convert standard AC or HVDC power into a main output of 12 VDC for powering intermediate bus architectures (IBA) in high performance and reliability servers, routers, and network switches.

The PFE1500-12-054series meet international safety standards and displays the CE-Mark for the European Low Voltage Directive (LVD).



### Key Features & Benefits

- High Efficiency, typ. 94% efficiency at half load
- Universal input voltage range: 90-264 VAC
- High voltage DC input: 180-350 VDC (Option for 400 VDC)
- AC input with power factor correction
- Always-On 16.5 W programmable standby output (3.3/5 V)
- Hot-plug capable
- Parallel operation with active digital current sharing
- Digital controls for improved performance
- High density design: 35 W/in<sup>3</sup>
- Small form factor: 54.5(W) x 40.0(H) x 321.5(L) in mm
- I2C communication interface for control, programming and monitoring with PMBus™ protocol and PSMI Protocol
- Over temperature, output over voltage and overcurrent protection
- 256 Bytes of EEPROM for user information
- 2 Status LEDs: OK and FAIL with fault signaling

### Applications

- High Performance Servers
- Routers
- Switches



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## 1. ORDERING INFORMATION

PFE	1500	-	12	-	054	X	X
Product Family	Power Level	Dash	V1 Output	Dash	Width	Airflow	Input <sup>3</sup>
PFE Front-Ends	1500 W		12 V		54 mm	N: Normal <sup>1</sup> R: Reverse <sup>2</sup>	A: C14 Socket AC: C16 Socket AH: HVDC Socket

- <sup>1</sup> "N" Normal Airflow from Output connector to Input AC socket  
 Ordering PN: PFE1500-12-054NA for C14 AC input connector, input range is 180 VDC ~ 350 VDC and 90 VAC ~ 264 VAC  
 Ordering PN: PFE1500-12-054NAC for C16 AC input connector, input range is 180 VDC ~ 350 VDC and 90 VAC ~ 264 VAC  
 Ordering PN: PFE1500-12-054NAH for both AC and HVDC (RF-203-D-1.0) input connector, input range is 180 VDC ~ 400 VDC and 90 VAC ~ 264 VAC
- <sup>2</sup> "R" Reverse Airflow from Input AC socket to Output connector  
 Ordering PN: PFE1500-12-054RA for C14 AC input connector, input range is 180 VDC ~ 350 VDC and 90 VAC ~ 264 VAC  
 Ordering PN: PFE1500-12-054RAC for C16 AC input connector, input range is 180 VDC ~ 350 VDC and 90 VAC ~ 264 VAC  
 Ordering PN: PFE1500-12-054RAH for both AC and HVDC (RF-203-D-1.0) input connector, input range is 180 VDC ~ 400 VDC and 90 VAC ~ 264 VAC
- <sup>3</sup> For difference of the AC socket and mechanical outline refer to section 13.

## 2. OVERVIEW

The PFE1500-12-054 Series AC/DC power supply is combination of analog and DSP control, highly efficient front-end power supply. It incorporates resonance-soft-switching technology and interleaved power trains to reduce component stresses, providing increased system reliability and very high efficiency. With a wide input operational voltage range and minimal derating of output power with input voltage and temperature, the PFE1500-12-054 maximizes power availability in demanding server, network, and other high availability applications. The supply is fan cooled and ideally suited for integration with a matching airflow paths. The PFC stage is an analogue solution; MCU is used to communicate with DSP chip on secondary side. The DC/DC stage uses soft switching resonant techniques in conjunction with synchronous rectification. An active OR-ing device on the output ensures no reverse load current and renders the supply ideally suited for operation in redundant power systems. The always-on standby output, with selectable voltage level (3.3/5 V), provides power to external power distribution and management controllers. It is protected with an active OR-ing device for maximum reliability. Status information is provided with front-panel LEDs. In addition, the power supply can be controlled and the fan speed set via the I2C bus. The I2C bus allows full monitoring of the supply, including input and output voltage, current, power, and inside temperatures. The fan speed is adjusted automatically depending on the actual power demand and supply temperature and can be overridden through the I2C bus.

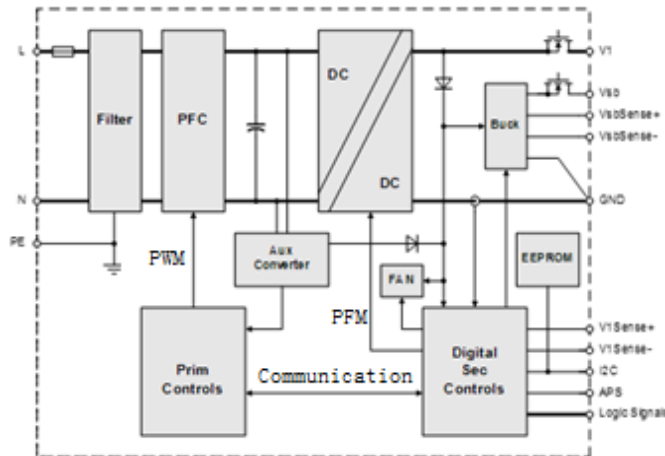


Figure 1. PFE1500-12-054 Block Diagram

## 3. ABSOLUTE MAXIMUM RATINGS

Stresses in excess of the absolute maximum ratings may cause performance degradation, adversely affect long-term reliability, and cause permanent damage to the supply.

PARAMETER	DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
$V_{i\ maxc}$	Maximum Input			264	VAC

## 4. INPUT SPECIFICATIONS

General Condition:  $T_A = 0 \dots 45^\circ\text{C}$  unless otherwise specified.

PARAMETER	DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
$V_{i\ nom}$	Nominal Input Voltage	100		240	VAC
		200		350 <sup>1</sup>	VDC
$V_i$	Input Voltage Ranges	Normal operating ( $V_{i\ min}$ to $V_{i\ max}$ )		264	VAC
		90		350	VDC
$V_{i\ red}$	Derating Input Voltage Range	90		180	VAC
$I_{i\ max}$	Max Input Current			15	A <sub>rms</sub>
$I_{i\ p}$	Inrush Current Limitation	$V_{i\ min}$ to $V_{i\ max}$ , $T_{NTC} = 25^\circ\text{C}$ (Figure 5)		40	A <sub>p</sub>
$F_i$	Input Frequency	47	50/60	64	Hz
$PF$	Power Factor	$V_{i\ nom}$ , 50Hz, $> 0.3 I_{i\ nom}$		0.96	W/VA
$V_{i\ on}$	Turn-on Input Voltage <sup>2</sup>	Ramping up		89	VAC
		80	84	180	VDC
$V_{i\ off}$	Turn-off Input Voltage	Ramping down		85	VAC
		75	80	176	VDC
$\eta$	Efficiency without Fan at AC input	$V_{i\ nom}$ , $0.1 \cdot k_{nom}$ , $V_{x\ nom}$ , $T_A = 25^\circ\text{C}$		90	
		$V_{i\ nom}$ , $0.2 \cdot k_{nom}$ , $V_{x\ nom}$ , $T_A = 25^\circ\text{C}$		92	
		$V_{i\ nom}$ , $0.5 \cdot k_{nom}$ , $V_{x\ nom}$ , $T_A = 25^\circ\text{C}$		94	
	Efficiency without Fan at DC input	$V_{i\ nom}$ , $k_{nom}$ , $V_{x\ nom}$ , $T_A = 25^\circ\text{C}$		92	%
		$V_{i\ nom}=336\text{VDC}$ , $0.1 \cdot k_{nom}$ , $V_{x\ nom}$ , $T_A = 25^\circ\text{C}$		89	
		$V_{i\ nom}=336\text{VDC}$ , $0.2 \cdot k_{nom}$ , $V_{x\ nom}$ , $T_A = 25^\circ\text{C}$		92	
$T_{hold}$	Hold-up Time	$V_{i\ nom}=336\text{VDC}$ , $0.5 \cdot k_{nom}$ , $V_{x\ nom}$ , $T_A = 25^\circ\text{C}$		93.5	
		$V_{i\ nom}=336\text{VDC}$ , $k_{nom}$ , $V_{x\ nom}$ , $T_A = 25^\circ\text{C}$		92	
		After last AC zero point to $V_i \geq 10.8\text{V}$ , $V_{SB}$ within regulation, $V_i = 230\text{VAC}$ , $P_{x\ nom}$		10	ms

<sup>1</sup> For PFE1500-12-054NAH and PFE1500-12-054RAH, Normal DC operation input range is 200 VDC to 380 VDC and Input range is 180 VDC to 400 VDC; input AC range is 90 VAC ~ 264 VAC.

<sup>2</sup> The Front-End is provided with a minimum hysteresis of 3 V during turn-on and turn-off within the ranges.



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## 4.1 INPUT FUSE

Quick-acting 16 A input fuse (5 x 20 mm) in series the L line inside the power supply protect against severe defects. The fuses are not accessible from the outside and are therefore not serviceable parts.

## 4.2 INRUSH CURRENT

The AC-DC power supply exhibits an X-capacitance of only 3.2  $\mu\text{F}$ , resulting in a low and short peak current, when the supply is connected to the mains. The internal bulk capacitor will be charged through an NTC which will limit the inrush current.

**NOTE:** Do not repeat plug-in / out operations within a short time, or else the internal in-rush current limiting device (NTC) may not sufficiently cool down and excessive inrush current or component failure(s) may result.

## 4.3 INPUT UNDER-VOLTAGE

If the sinusoidal input voltage stays below the input under voltage lockout threshold  $V_{i\text{on}}$ , the supply will be inhibited. Once the input voltage returns within the normal operating range, the supply will return to normal operation again.

## 4.4 POWER FACTOR CORRECTION

Power factor correction (PFC) is achieved by controlling the input current waveform synchronously with the input voltage. An analog controller is implemented giving outstanding PFC results over a wide input voltage and load ranges. The input current will follow the shape of the input voltage.

## 4.5 EFFICIENCY

High efficiency (see Figure 2) is achieved by using state-of-the-art silicon power devices in conjunction with soft-transition topologies minimizing switching losses and a full digital control scheme. Synchronous rectifiers on the output reduce the losses in the high current output path. The speed of the fan is digitally controlled to keep all components at an optimal operating temperature regardless of the ambient temperature and load conditions.

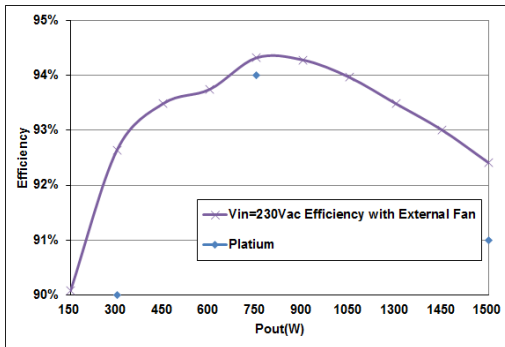


Figure 2. Efficiency vs. Load current (ratio metric loading)

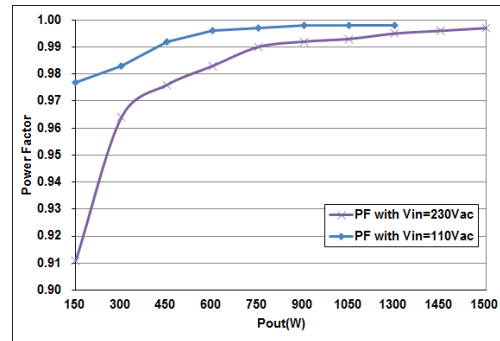


Figure 3. Power factor vs. Load current

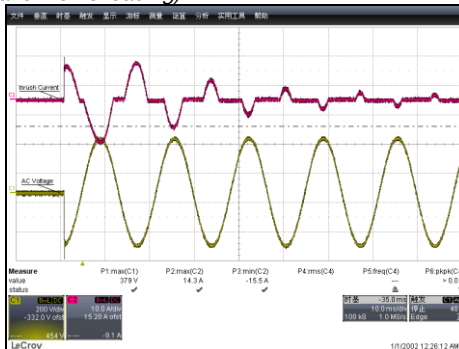


Figure 4. Inrush current,  $V_m = 264 \text{ VAC}$ ,  $90^\circ$ , CH1:  $V_m$  (200V/div), CH2:  $I_m$  (10A/div)

## 5. OUTPUT SPECIFICATIONS

General Condition:  $T_a = 0 \dots 45^\circ\text{C}$  unless otherwise specified.

PARAMETER	DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
<b>Main Output <math>V_1</math></b>					
$V_{1\text{ nom}}$	Nominal Output Voltage		12.0		VDC
$V_{1\text{ set}}$	Output Setpoint Accuracy	$0.5 \cdot I_{1\text{ nom}}, T_{\text{amb}} = 25^\circ\text{C}$	-0.5	+0.5	% $V_{1\text{ nom}}$
$dV_{1\text{ tot}}$	Total Regulation	$V_{1\text{ min}}$ to $V_{1\text{ max}}, 0$ to 100% $I_{1\text{ nom}}, T_{\text{a min}}$ to $T_{\text{a max}}$	-2	+2	% $V_{1\text{ nom}}$
$P_{1\text{ nom}}$	Nominal Output Power	$264\text{ VAC} > V_{1\text{ in}} \geq 180\text{ VAC}, V_1 = 12\text{ VDC}$ $400\text{ VDC} > V_{1\text{ in}} \geq 180\text{ VDC}, V_1 = 12\text{ VDC}$	1500		W
	Refer to Figure 7 for derating curve	$180\text{ VAC} > V_{1\text{ in}} \geq 90\text{ VAC}, V_1 = 12\text{ VDC}$	1000		W
$I_{1\text{ nom}}$	Nominal Output Current	$264\text{ VAC} > V_{1\text{ in}} \geq 180\text{ VAC}, V_1 = 12\text{ VDC}$ $400\text{ VDC} > V_{1\text{ in}} \geq 180\text{ VDC}, V_1 = 12\text{ VDC}$	125		ADC
	Refer to Figure 7 for derating curve	$180\text{ VAC} > V_{1\text{ in}} \geq 90\text{ VAC}, V_1 = 12\text{ VDC}$	83.4		ADC
$V_{1\text{ pp}}$	Output Ripple Voltage	$V_{1\text{ nom}}, I_{1\text{ nom}}, 20\text{ MHz BW}$ (See Section 5.1)		150	mVpp
$dV_{1\text{ Load}}$	Load Regulation	$V_1 = V_{1\text{ nom}}, 0 - 100\% I_{1\text{ nom}}$	80		mV
$dV_{1\text{ Line}}$	Line Regulation	$V_1 = V_{1\text{ min}} \dots V_{1\text{ max}}$	40		mV
$dI_{\text{share}}$	Current Sharing	Deviation from $I_{1\text{ tot}} / N, I_1 > 10\%$	-3	+3	A
$dV_{1\text{ dyn}}$	Dynamic Load Regulation	$\Delta I_1 = 50\% I_{1\text{ nom}}, I_1 = 5 \dots 100\% I_{1\text{ nom}}, dI_1/dt = 1\text{ A}/\mu\text{s}$	-0.6	0.6	V
$T_{\text{rec}}$	Recovery Time	$\Delta I_1 = 50\% I_{1\text{ nom}}, I_1 = 5 \dots 100\% I_{1\text{ nom}}, dI_1/dt = 1\text{ A}/\mu\text{s},$ recovery within 1% of $V_{1\text{ nom}}$		1	ms
$t_{\text{AC } V_1}$	Start-up Time from AC			2	sec
$t_{V_1\text{ rise}}$	Rise Time	$V_1 = 10 \dots 90\% V_{1\text{ nom}}$	0.5	10	ms
$C_{\text{Load}}$	Capacitive Loading	$T_a = 25^\circ\text{C}$		30000	$\mu\text{F}$
<b>Standby Output <math>V_{\text{SB}}</math></b>					
$V_{\text{SB nom}}$	Nominal Output Voltage	VSB_SEL = 1	3.3		VDC
$V_{\text{SB set}}$	Output Setpoint Accuracy	VSB_SEL = 0	5.0		VDC
		VSB_SEL = 0 / 1	-0.5	+0.5	% $V_{1\text{ nom}}$
$dV_{\text{SB tot}}$	Total Regulation	$V_{1\text{ min}}$ to $V_{1\text{ max}}, 0$ to 100% $I_{\text{SB nom}}, T_{\text{a min}}$ to $T_{\text{a max}}$	-1	+1	% $V_{\text{SB nom}}$
$P_{\text{SB nom}}$	Nominal Output Power	$V_{\text{SB}} = 3.3\text{ VDC},$	16.5		W
		$V_{\text{SB}} = 5.0\text{ VDC},$	16.5		
$I_{\text{SB nom}}$	Nominal Output Current	$V_{\text{SB}} = 3.3\text{ VDC},$	5		ADC
		$V_{\text{SB}} = 5.0\text{ VDC},$	3.3		
$V_{\text{SB pp}}$	Output Ripple Voltage	$V_{\text{SB nom}}, I_{\text{SB nom}}, 20\text{ MHz BW}$ (See Section 5.1)		100	mVpp
$dV_{\text{SB}}$	Droop	VSB_SEL = 1	67		mV
		VSB_SEL = 0	44		
$I_{\text{SB max}}$	Current Limitation	VSB_SEL = 1,	5.25	6	ADC
		VSB_SEL = 0,	3.45	4.3	
$dV_{\text{SB dyn}}$	Dynamic Load Regulation	$\Delta I_{\text{SB}} = 50\% I_{\text{SB nom}}, I_{\text{SB}} = 5 \dots 100\% I_{\text{SB nom}}, dI_{\text{SB}}/dt = 0.5\text{ A}/\mu\text{s},$ recovery within 1% of $V_{1\text{ nom}}$	-3	3	% $V_{\text{SB nom}}$
$T_{\text{rec}}$	Recovery Time			250	$\mu\text{s}$
$t_{\text{AC } V_{\text{SB}}}$	Start-up Time from AC	$V_{\text{SB}} = 90\% V_{\text{SB nom}}$		2	sec
$t_{V_{\text{SB}}\text{ rise}}$	Rise Time	$V_{\text{SB}} = 10 \dots 90\% V_{\text{SB nom}}$	0.5	30	ms
$C_{\text{Load}}$	Capacitive Loading	$T_{\text{amb}} = 25^\circ\text{C}$		10000	$\mu\text{F}$



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## 5.1 OUTPUT VOLTAGE RIPPLE

Internal capacitance at the 12 V output (behind the OR-ing circuitry) is minimized to prevent disturbances during hot plug. In order to provide low output ripple voltage in the application, external capacitors should be added close to the power supply output.

The setup of Figure 6 has been used to evaluate suitable capacitor types. The capacitor combinations of Table 1 and Table 2 should be used to reduce the output ripple voltage. The ripple voltage is measured with 20 MHz BWL, close to the external capacitors.

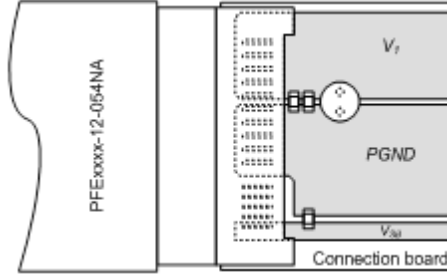


Figure 5. Output ripple test setup

**NOTE:** Care must be taken when using ceramic capacitors with a total capacitance of 1  $\mu\text{F}$  to 50  $\mu\text{F}$  on output V1, due to their high quality factor the output ripple voltage may be increased in certain frequency ranges due to resonance effects.

EXTERNAL CAPACITOR V1	DV1MAX	UNIT
Standard test condition: 1 Pc 10 $\mu\text{F}$ / 63 V Electrolytic Capacitor 1 pc 0.1 $\mu\text{F}$ / 100 V ceramic capacitor		
1Pcs 1000 $\mu\text{F}$ /16V/Low ESR Aluminum/ $\phi$ 10x20	120	mVpp
2Pcs 47 $\mu\text{F}$ /16V/X5R/1210	100	mVpp
2Pcs 47 $\mu\text{F}$ /16V/X5R/1210 plus 1Pcs 1000 $\mu\text{F}$ Low ESR AlCap	90	mVpp

Table 1. Suitable capacitors for V1

EXTERNAL CAPACITOR VSB	DV1MAX	UNIT
Standard test condition: 1 Pc 10 $\mu\text{F}$ / 63 V Electrolytic Capacitor 1 pc 0.1 $\mu\text{F}$ / 100 V ceramic capacitor		
Add 1Pcs 10 $\mu\text{F}$ /16 V/X5R/1206	50	mVpp
Add 2Pcs 10 $\mu\text{F}$ /1V/X5R/1206	40	mVpp

Table 2. Suitable capacitors for VSB

The output ripple voltage on VSB is influenced by the main output V1. Evaluating VSB output ripple must be done when maximum load is applied to V1.

## 6. PROTECTION SPECIFICATIONS

PARAMETER	DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
F	Input Fuse (L)	Not user accessible, quick-acting (F)		16	A
V1 <sub>OV</sub>	OV Threshold V1	13.3		14.5	VDC
t <sub>OV V1</sub>	OV Latch Off Time V1			1	ms
VSB <sub>OV</sub>	OV Threshold VSB	110		120	% VSB
t <sub>OV VSB</sub>	OV Latch Off Time VSB			1	ms
I <sub>V1 lim</sub>	Over Current Limitation V1	V1 > 180 VAC, Ta < 45°C V1 > 90 VAC, Ta < 45°C		128 93	A
I <sub>V1 SC</sub>	Max Short Circuit Current V1	V1 < 3V		200	A
t <sub>V1 SC</sub>	Short Circuit Regulation Time	V1 < 3 V, time until I <sub>V1</sub> is limited to < I <sub>V1 SC</sub>		2	ms
TSD	Over Temperature On Heat Sinks	Automatic shut-down		115 120	°C

**6.1 OVERVOLTAGE PROTECTION**

The PFE front-ends provide a fixed threshold overvoltage (OV) protection implemented with a HW comparator. Once an OV condition has been triggered, the supply will shut down and latch the fault condition. The latch can be unlocked by disconnecting the supply from the AC mains or by toggling the PSON\_L input.

**6.2 VSB UNDERVOLTAGE DETECTION**

Both main and standby outputs are monitored. LED and PWOK\_H pin signal if the output voltage exceeds  $\pm 5\%$  of its nominal voltage. Output undervoltage protection is provided on the standby output only. When  $V_{SB}$  falls below 75% of its nominal voltage, the main output  $V_1$  is inhibited.

**6.3 CURRENT LIMITATION**

**6.3.1 MAIN OUTPUT**

When main output runs in current limitation mode its output will turn OFF below 2V but will retry to recover every 1s interval. If current limitation mode is still present after the unit retry, output will continuously perform this routine until current is below the current limitation point. The supply will go through soft start every time it retry from current limitation mode.

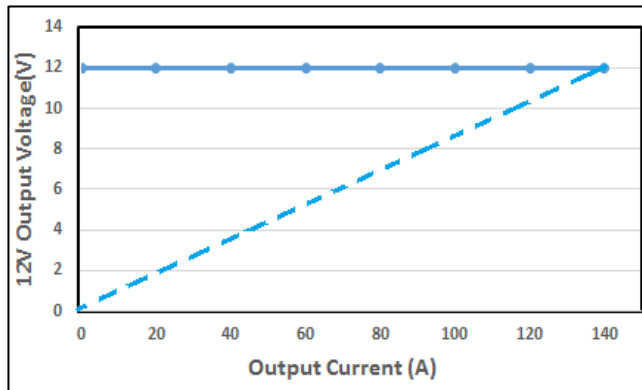


Figure 6. Current Limitation on V<sub>1</sub> (V<sub>i</sub> = 230VAC)

The main output current limitation will decrease if the ambient (inlet) temperature increases beyond 45°C or if the AC input voltage below 180VAC (see Figure 7A and Figure 7B for power supply applied in Canada and United States of American and other district respectively). Note that the actual over current protection on V<sub>1</sub> will begin at a current level approximately 5 A higher, see Figure 8. (See also Chapter 9 Temperature and Fan Control for additional information.)

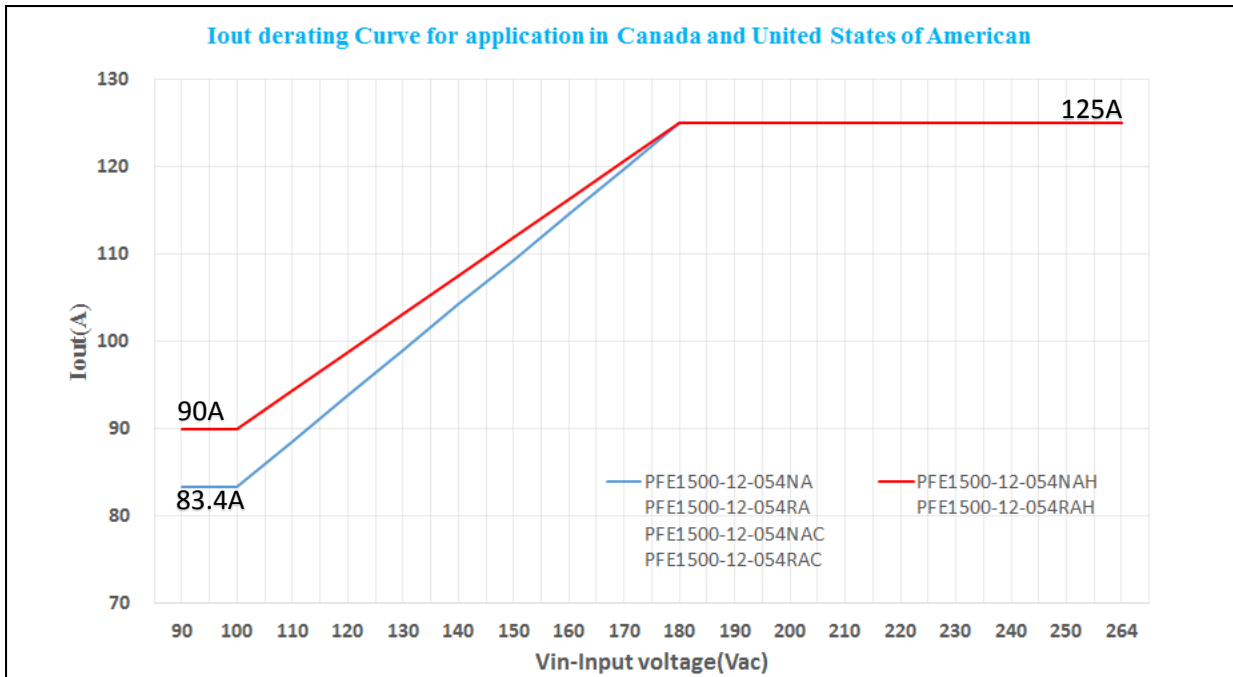


Figure 7A. Iout Derating Curve for application in Canada and United States of America at 45C ambient

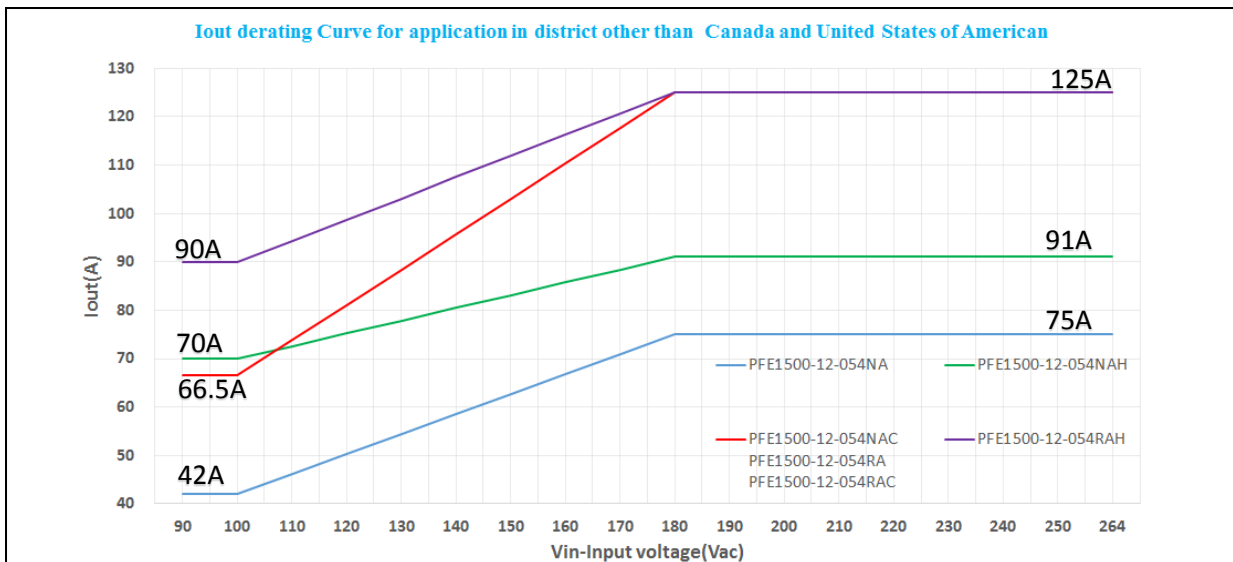


Figure 7B. Iout Derating Curve for application in district other than Canada and United States of America at 45C ambient



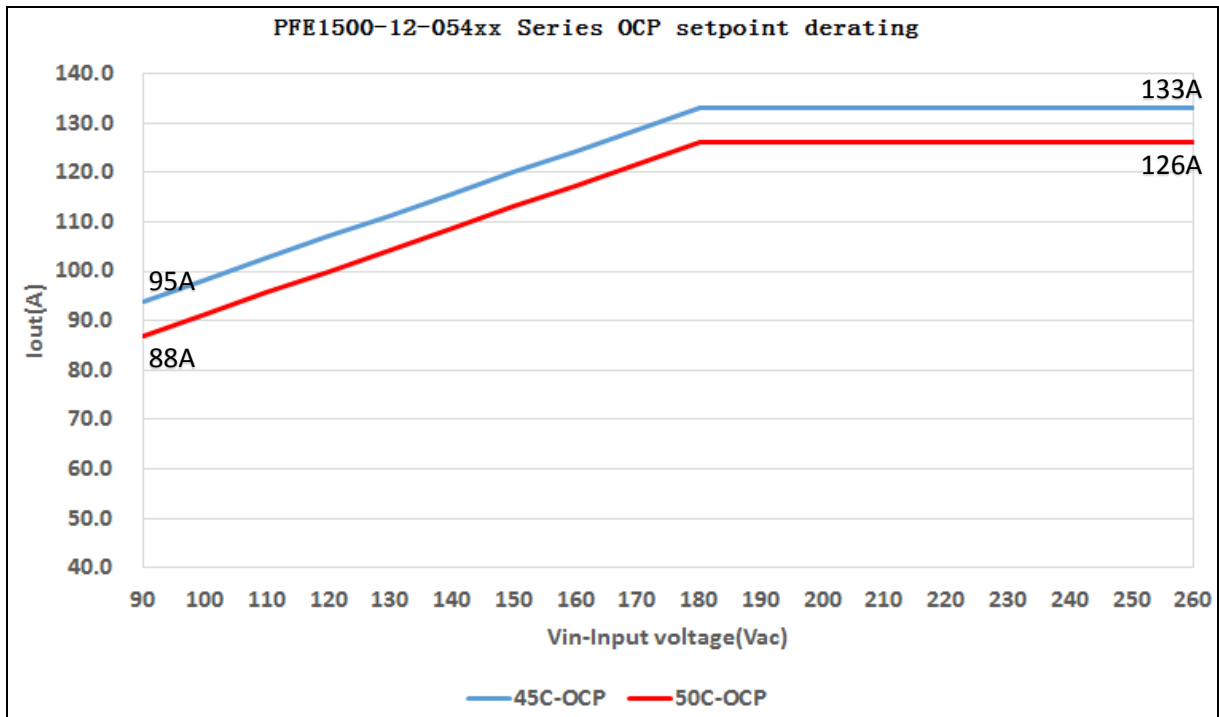


Figure 8. OCP Derating Curve with Vinac and Ambient Temperature for both PFE1500-12-054Series

6.3.2 STANDBY OUTPUT

The standby output exhibits a substantially rectangular output characteristic down to 0V (no hiccup mode / latch off). If it runs in current limitation and its output voltage drops below the UV threshold, then the main output will be inhibited (standby remains on). The current limitation of the standby output is independent of the AC input voltage.

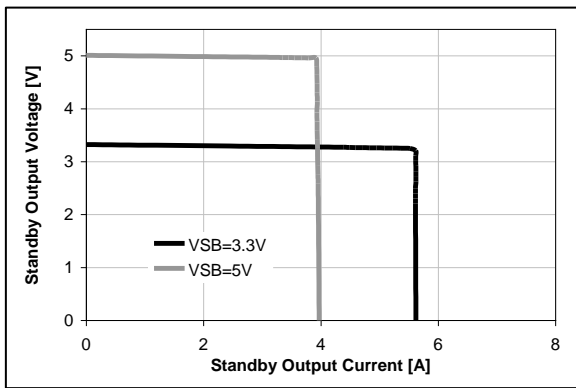


Figure 9. Current Limitation on Vsb

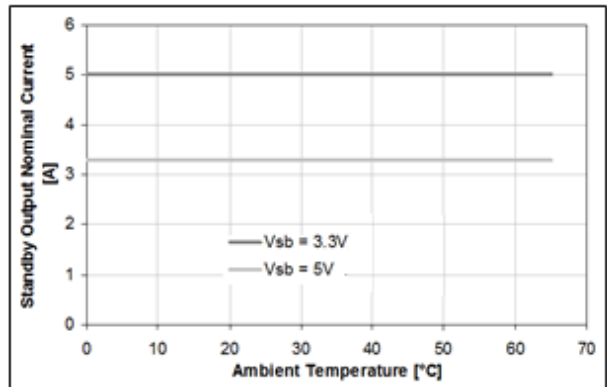


Figure 10. Temperature Derating on Vsb



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## 7. MONITORING

PARAMETER	DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
$V_{mon}$	Input RMS Voltage $V_{min} \leq V \leq V_{max}$	-2.5		+2.5	%
$I_{mon}$	Input RMS Current $I > 2 A_{rms}$	-5		+5	%
$P_{mon}$	True Input Power $I > 2 A_{rms}$	-5		+5	%
$V_{1\ mon}$	$V_1$ Voltage	-2		+2	%
$I_{1\ mon}$	$V_1$ Current	$I_1 > 25 A$		+2	%
		$I_1 \leq 25 A$	-0.5	+0.5	A
$P_{o\ nom}$	Total Output Power	$P_o > 120 W$		+5	%
		$P_o \leq 120 W$	-6	+6	W
$V_{SB\ mon}$	Standby Voltage	-0.1		+0.1	V
$I_{SB\ mon}$	Standby Current $I_{SB} \leq I_{SB\ nom}$	-0.5		+0.5	A

## 8. SIGNAL & CONTROL SPECIFICATIONS

### 8.1 ELECTRICAL CHARACTERISTICS

PARAMETER	DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
<b><i>PSKILL_H / PSON_L / VSB_SEL / HOTSTANDBYEN_H Inputs</i></b>					
$V_L$	Input Low Level Voltage	-0.2		0.8	V
$V_H$	Input High Level Voltage	2.4		3.5	V
$I_{L, H}$	Maximum Input Sink or Source Current	0		1	mA
$R_{puPSKILL\_H}$	Internal Pull Up Resistor on PSKILL_H		100		k $\Omega$
$R_{puPSON\_L}$	Internal Pull Up Resistor on PSON_L		10		k $\Omega$
$R_{puVSB\_SEL}$	Internal Pull Up Resistor on VSB_SEL		10		k $\Omega$
$R_{puHOTSTANDBYEN\_H}$	Internal Pull Up Resistor on HOTSTANDBYEN_H		10		k $\Omega$
$R_{LOW}$	Resistance Pin to SGND for Low Level	0		1	k $\Omega$
$R_{HIGH}$	Resistance Pin to SGND for High Level	50			k $\Omega$
<b><i>PWOK_H Output</i></b>					
$V_{OL}$	Output Low Level Voltage $I_{sink} < 4\ mA$	0		0.4	V
$V_{OH}$	Output High Level Voltage $I_{source} < 0.5\ mA$	2.6		3.5	V
$R_{puPWOK\_H}$	Internal Pull Up Resistor on PWOK_H		1		k $\Omega$
<b><i>ACOK_H Output</i></b>					
$V_{OL}$	Output Low Level Voltage $I_{sink} < 2\ mA$	0		0.4	V
$V_{OH}$	Output High Level Voltage $I_{source} < 50\ \mu A$	2.6		3.5	V
$R_{puACOK\_H}$	Internal Pull Up Resistor on ACOK_H		10		k $\Omega$
<b><i>SMB_ALERT_L Output</i></b>					
$V_{ext}$	Maximum External Pull Up Voltage			12	V
$V_{OL}$	Output Low Level Voltage $I_{source} < 4\ mA$	0		0.4	V
$I_{OH}$	Maximum High Level Leakage Current			10	$\mu A$
$R_{puSMB\_ALERT\_L}$	Internal Pull Up Resistor on SMB_ALERT_L		None		k $\Omega$

### 8.2 INTERFACING WITH SIGNALS

All signal pins have protection diodes implemented to protect internal circuits. When the power supply is not powered, the protection devices start clamping at signal pin voltages exceeding  $\pm 0.5$  V. Therefore all input signals should be driven only by an open collector/drain to prevent back feeding inputs when the power supply is switched off. If interconnecting of signal pins of several power supplies is required, then this should be done by decoupling with small signal schottky diodes as shown in examples in (Figure 11) except for SMB\_ALERT\_L, ISHARE and I<sup>2</sup>C pins. SMB\_ALERT\_L pins can be interconnected without decoupling diodes, since these pins have no internal pull up resistor and use a 15 V zener diode as protection device against positive voltage on pins. ISHARE pins must be interconnected without any additional components. This in-/output is disconnected from internal circuits when the power supply is switched off.

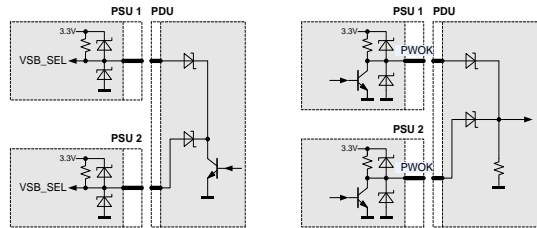


Figure 11. Interconnection of Signal Pins

### 8.3 FRONT LEDS

There will be 2 separate LED indicators, one green and one amber to indicate the power supply status. There will be a (slow) blinking green POWER LED (OK) to indicate that AC is applied to the PSU and the Standby Voltage is available. This same LED shall go steady to indicate that all the Power Outputs are available. This same LED or separate one will blink (slow) or be solid ON amber to indicate that the power supply has failed or reached a warning status and therefore a replacement of the unit is/maybe necessary. The LED are visible on the power supply's exterior face. The LED location meets ESD Requirements.

POWER SUPPLY CONDITION	GREEN (OK) LED STATUS	AMBER (FAIL) LED STATUS
No AC power to all power supplies	OFF	OFF
Power Supply Failure (includes over voltage, over current, over temperature and fan failure)	OFF	ON
Power Supply Warning events where the power supply continues to operate (high temperature, high power and slow fan)	OFF	Blinking
AC Present/ 12VSB on (PSU OFF)	Blinking	OFF
Power Supply ON and OK	ON	OFF

Table 3. LED Status

### 8.4 PRESENT\_L

This signaling pin is recessed within the connector and will contact only once all other connector contacts are closed. This active-low pin is used to indicate to a power distribution unit controller that a supply is plugged in. The maximum current on PRESENT\_L pin should not exceed 10 mA.

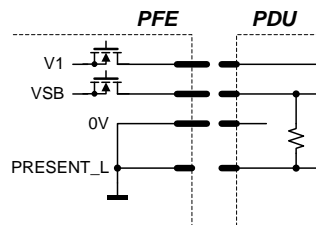


Figure 12. PRESENT\_L signal pin

### 8.5 PSKILL\_H INPUT

The PSKILL\_H input is active-high and is located on a recessed pin on the connector and is used to disconnect the main output as soon as the power supply is being plugged out. This pin should be connected to SGND in the power distribution unit. The standby output will remain on regardless of the PSKILL\_H input state.

### 8.6 AC TURN-ON / DROP-OUTS / ACOK\_H

The power supply will automatically turn-on when connected to the AC line under the condition that the PSON\_L signal is pulled low and the AC line is within range. The ACOK\_H signal is active-high. The timing diagram is shown in Figure 13 and referenced in Table 4.

OPERATING CONDITION		MIN	MAX	UNIT
$t_{AC\ VSB}$	AC Line to 90% $V_{SB}$		2	sec
$t_{AC\ V1}$	AC Line to 90% $V_1$		2	sec
$t_{ACOK\_H\ on1}$	ACOK_H signal on delay (start-up)		2000	ms
$t_{ACOK\_H\ on2}$	ACOK_H signal on delay (dips)		100	ms
$t_{ACOK\_H\ off}$	ACOK_H signal off delay		5	ms
$t_{VSB\ V1\ del}$	$V_{SB}$ to $V_1$ delay	10	500	ms
$t_{V1\ holdup}$	Effective $V_1$ holdup time	10		ms
$t_{VSB\ holdup}$	Effective $V_{SB}$ holdup time	20		ms
$t_{ACOK\_H\ V1}$	ACOK_H to $V_1$ holdup	7		ms
$t_{ACOK\_H\ VSB}$	ACOK_H to $V_{SB}$ holdup	15		ms
$t_{V1\ off}$	Minimum $V_1$ off time	1	2	sec
$t_{VSB\ off}$	Minimum $V_{SB}$ off time	1	2	sec

Remark<sup>3</sup>: AC short dips means below 10ms; AC long dips means 10 ms to 100 ms

Table 4. AC Turn-on / Dip Timing

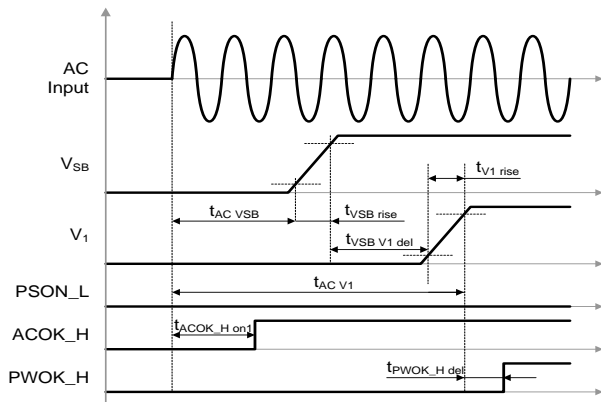


Figure 13. AC turn-on timing

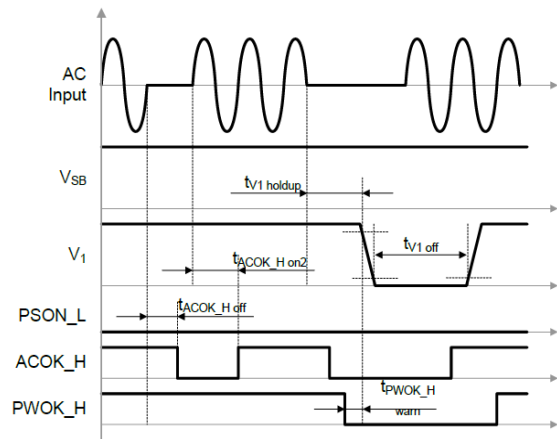


Figure 14. AC short dips

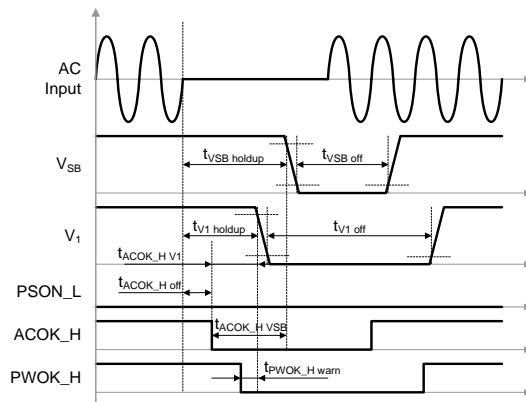


Figure 15. AC long dips

### 8.7 PSON\_L INPUT

The PSON\_L is an internally pulled-up (3.3 V) input signal to enable/disable the main output V1 of the front-end. This active-low pin is also used to clear any latched fault condition. The timing diagram is given in Figure 27 and the parameters in Table 5.

OPERATING CONDITION		MIN	MAX	UNIT
$t_{PSON\_L\ V1on}$	PSON_L to $V_1$ delay (on)	2	20	ms
$t_{PSON\_L\ V1off}$	PSON_L to $V_1$ delay (off)	2	20	ms
$t_{PSON\_L\ H\ min}$	PSON_L minimum High time	10		ms

Table 5. PSON\_L timing

### 8.8 PWOK\_H SIGNAL

The PWOK\_H is an open drain output with an internal pull-up to 3.3 V indicating whether both  $V_{SB}$  and  $V_1$  outputs are within regulation. This pin is active-low. The timing diagram is shown in Figure 16 and referenced in the Table 6.

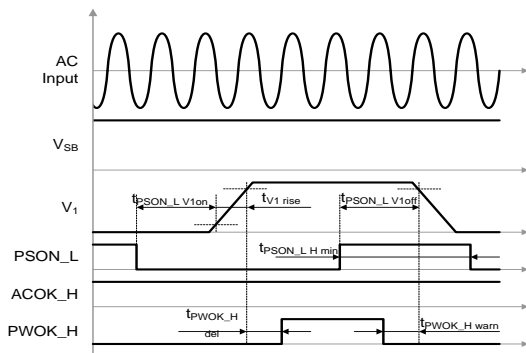


Figure 16. PSON\_L and PWOK\_H turn-on/off timing

OPERATING CONDITION		MIN	MAX	UNIT
$t_{PWOK\_H\ del}$	PWOK_H to $V_1$ delay (on)	100	500	ms
$t_{PWOK\_H\ warn}$	PWOK_H to $V_1$ delay (off) caused by:			
	PSKILL_H	0	1	ms
	PSON_L, OT, Fan Failure	0.5	2.5	ms
	ACOK_H (time change with loading condition)	0.5	100	ms
	UV and OV on VSB	1	30	ms
	OC on V1 (Software trigger)	-11	0	ms
	OC on V1 (Hardware trigger)	-1	0	ms
	OV on V1	-3	0	ms

\* A positive value means a warning time, a negative value a delay (after fact).

Table 6. PWOK\_H timing

### 8.9 CURRENT SHARE

The PFE front-ends have an active current share scheme implemented for  $V_1$ . All the ISHARE current share pins need to be interconnected in order to activate the sharing function. If a supply has an internal fault or is not turned on, it will disconnect its ISHARE pin from the share bus. This will prevent dragging the output down (or up) in such cases.

The current share function uses a digital bi-directional data exchange on a recessive bus configuration to transmit and receive current share information. The controller implements a Master/Slave current share function. The power supply providing the largest current among the group is automatically the Master. The other supplies will operate as Slaves and increase their output current to a value close to the Master by slightly increasing their output voltage. The voltage increase is limited to +250 mV.

The standby output uses a passive current share method (droop output voltage characteristic).

### 8.10 SENSE INPUTS

Both main and standby outputs have sense lines implemented to compensate for voltage drop on load wires. The maximum allowed voltage drop is 200 mV on the positive rail and 100 mV on the PGND rail.



Asia-Pacific +86 755 298 85888 Europe, Middle East +353 61 225 977 North America +1 408 785 5200

With open sense inputs the main output voltage will rise by 270 mV and the standby output by 50 mV. Therefore if not used, these inputs should be connected to the power output and PGND close to the power supply connector. The sense inputs are protected against short circuit. In this case the power supply will shut down.

## 8.11 HOT-STANDBY OPERATION

The hot-standby operation is an operating mode allowing to further increase efficiency at light load conditions in a redundant power supply system. Under specific conditions one of the power supplies is allowed to disable its DC/DC stage. This will save the power losses associated with this power supply and at the same time the other power supply will operate in a load range having a better efficiency. In order to enable the hot standby operation, the HOTSTANDBYEN\_H and the ISHARE pins need to be interconnected. A power supply will only be allowed to enter the hot-standby mode, when the HOTSTANDBYEN\_H pin is high, the load current is low (see *Figure 17*) and the supply was allowed to enter the hot-standby mode by the system controller via the appropriate I<sup>2</sup>C command (by default disabled). The system controller needs to ensure that only one of the power supplies is allowed to enter the hot-standby mode.

If a power supply is in a fault condition, it will pull low its active-high HOTSTANDBYEN\_H pin which indicates to the other power supply that it is not allowed to enter the hot-standby mode or that it needs to return to normal operation should it already have been in the hot-standby mode.

NOTE: The system controller needs to ensure that only one of the power supplies is allowed to enter the hot-standby model.

*Figure 18* shows the achievable power loss savings when using the hot-standby mode operation. A total power loss reduction of 5W is achievable.

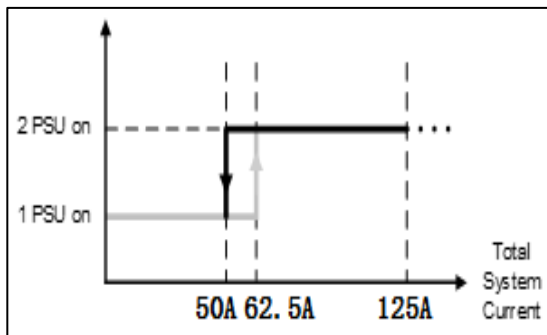


Figure 17. Hot-standby enable/disable current thresholds

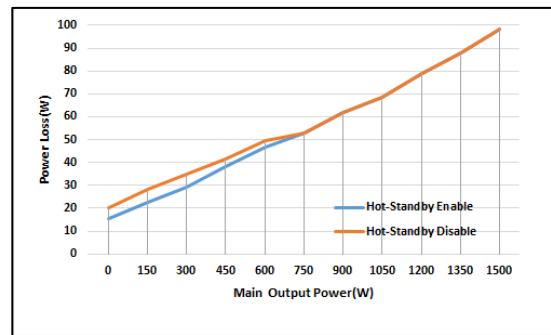


Figure 18. PSU power losses with/without hot-standby mode

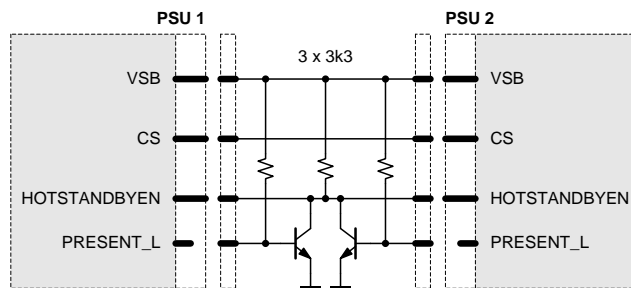


Figure 19. Recommended hot-standby configuration

In order to prevent voltage dips when the active power supply is unplugged while the other is in hot-standby mode, it is strongly recommended to add the external circuit as shown in *Figure 19*. If the PRESENT\_L pin status needs also to be read by the system controller, it is recommended to exchange the bipolar transistors with small signal MOS transistors or with digital transistors.

## 8.12 I<sup>2</sup>C / SMBUS COMMUNICATION

The interface driver in the PFE supply is referenced to the V1 Return. The PFE supply is a communication Slave device only; it never initiates messages on the I2C/SMBus by itself. The communication bus voltage and timing is defined in Table 7 further characterized through:

- There are no internal pull-up resistors
- The SDA/SCL IOs are 3.3/5 V tolerant
- Full SMBus clock speed of 100 kbps
- Clock stretching limited to 1 ms
- SCL low time-out of >25 ms with recovery within 10 ms
- Recognizes any time Start/Stop bus conditions

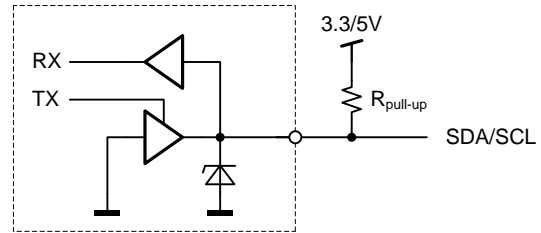


Figure 20. Physical layer of communication interface

The SMB\_ALERT\_L signal indicates that the power supply is experiencing a problem that the system agent should investigate. This is a logical OR of the Shutdown and Warning events. The power supply responds to a read command on the general SMB\_ALERT\_L call address 25(0x19) by sending its status register.

Communication to the DSP or the EEPROM will be possible as long as the input AC voltage is provided. If no AC is present, communication to the unit is possible as long as it is connected to a life V1 output (provided e.g. by the redundant unit). If only VSB is provided, communication is not possible.

PARAMETER	DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
$V_{IL}$	Input low voltage	-0.5		1.0	V
$V_{IH}$	Input high voltage	2.3		5.5	V
$V_{hys}$	Input hysteresis	0.15			V
$V_{oL}$	Output low voltage		3 mA sink current	0.4	V
$t_r$	Rise time for SDA and SCL	20+0.1Cb <sup>3</sup>		300	Ns
$t_{of}$	Output fall time $V_{IHmin} \rightarrow V_{ILmax}$	10 pF < Cb <sup>4</sup> < 400 pF	20+0.1Cb	250	Ns
$I_i$	Input current SCL/SDA	0.1 VDD < $V_i$ < 0.9 VDD	-10	10	μA
$C_i$	Internal Capacitance for each SCL/SDA			50	pF
$f_{SCL}$	SCL clock frequency	0		100	kHz
$R_{pu}$	External pull-up resistor	$f_{SCL} \leq 100$ kHz		1000 ns / Cb	Ω
$t_{HDSTA}$	Hold time (repeated) START	$f_{SCL} \leq 100$ kHz	4.0		μs
$t_{LOW}$	Low period of the SCL clock	$f_{SCL} \leq 100$ kHz	4.7		μs
$t_{HIGH}$	High period of the SCL clock	$f_{SCL} \leq 100$ kHz	4.0		μs
$t_{SUSTA}$	Setup time for a repeated START	$f_{SCL} \leq 100$ kHz	4.7		μs
$t_{HDDAT}$	Data hold time	$f_{SCL} \leq 100$ kHz	0	3.45	μs
$t_{SUDAT}$	Data setup time	$f_{SCL} \leq 100$ kHz	250		ns
$t_{SUSTO}$	Setup time for STOP condition	$f_{SCL} \leq 100$ kHz	4.0		μs
$t_{BUF}$	Bus free time between STOP and START	$f_{SCL} \leq 100$ kHz	5		ms

Table 7. I<sup>2</sup>C / SMBus Specification

<sup>3</sup> Cb = Capacitance of bus line in pF, typically in the range of 10...400 pF

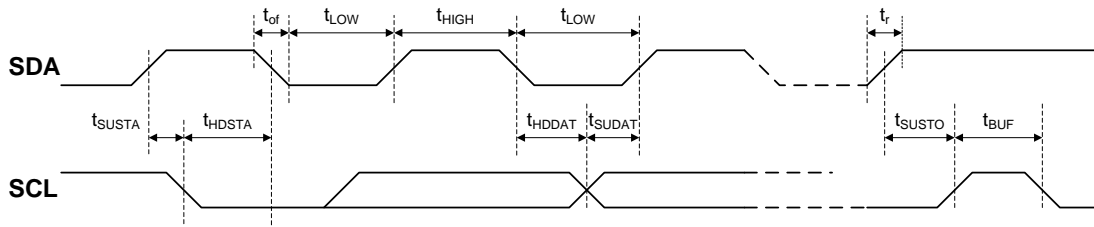


Figure 21. I<sup>2</sup>C / SMBus Timing

### 8.13 ADDRESS / PROTOCOL SELECTION (APS)

The APS pin provides the possibility to select the address by connecting a resistor to V1 return (0 V). A fixed addressing offset exists between the Controller and the EEPROM.

**NOTE:**

- If the APS pin is left open, the supply will operate with the PMBUS protocol at controller / EEPROM addresses 0xB6 / 0xA6.
- The APS pin is only read at start-up of the power supply. Therefore it is not possible to change address dynamically.

R <sub>APS</sub> (Ω) <sup>4</sup>	Protocol	I <sup>2</sup> C Address <sup>5</sup>	
		Controller	EEPROM
820	PMBus™	0xB0	0xA0
2700		0xB2	0xA2
5600		0xB4	0xA4
8200		0xB6	0xA6
15000	PSMI	0xB0	0xA0
27000		0xB2	0xA2
56000		0xB4	0xA4
180000		0xB6	0xA6

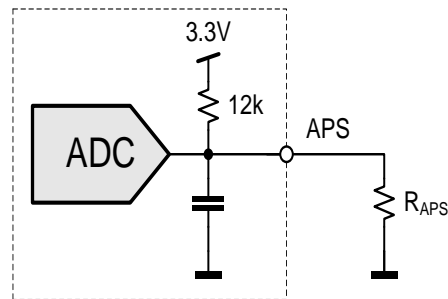


Figure 22. I<sup>2</sup>C address and protocol setting

### 8.14 CONTROLLER AND EEPROM ACCESS

The controller and the EEPROM in the power supply share the same I<sup>2</sup>C bus physical layer (see Figure 23). An I<sup>2</sup>C driver device assures logic level shifting (3.3/5 V) and a glitch-free clock stretching. The driver also pulls the SDA/SCL line to nearly 0 V when driven low by the DSP or the EEPROM providing maximum flexibility when additional external bus repeaters are needed. Such repeaters usually encode the low state with different voltage levels depending on the transmission direction.

The DSP will automatically set the I<sup>2</sup>C address of the EEPROM with the necessary offset when its own address is changed / set. In order to write to the EEPROM, first the write protection needs to be disabled by sending the appropriate command to the DSP. By default the write protection is on.

The EEPROM provides 256 bytes of user memory. None of the bytes are used for the operation of the power supply.

<sup>4</sup> E12 resistor values, use max 5% resistors, see also Figure 22

<sup>5</sup> The LSB of the address byte is the R/W bit



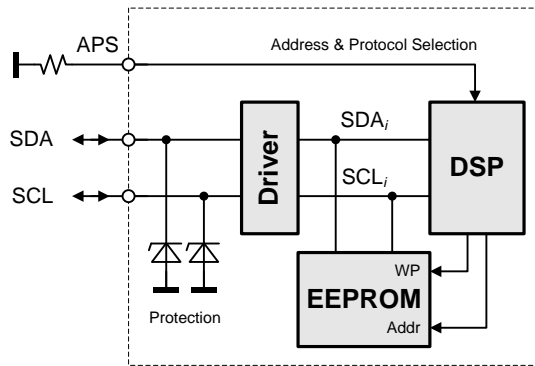


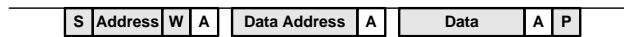
Figure 23. I<sup>2</sup>C Bus to DPS and EEPROM

### 8.15 EEPROM PROTOCOL

The EEPROM follows the industry communication protocols used for this type of device. Even though page write / read commands are defined, it is recommended to use the single byte write / read commands.

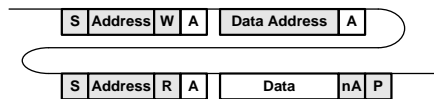
#### WRITE

The write command follows the SMBus 1.1 Write Byte protocol. After the device address with the write bit cleared a first byte with the data address to write to is sent followed by the data byte and the STOP condition. A new START condition on the bus should only occur after 5ms of the last STOP condition to allow the EEPROM to write the data into its memory.



#### READ

The read command follows the SMBus 1.1 Read Byte protocol. After the device address with the write bit cleared the data address byte is sent followed by a repeated start, the device address and the read bit set. The EEPROM will respond with the data byte at the specified location.



### 8.16 PMBUS™ PROTOCOL and PSMI PROTOCOL

#### PMBUS™ PROTOCOL

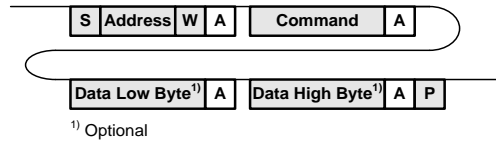
The Power Management Bus (PMBus™) is an open standard protocol that defines means of communicating with power conversion and other devices. For more information, please see the System Management Interface Forum web site at [www.powerSIG.org](http://www.powerSIG.org).

PMBus™ command codes are not register addresses. They describe a specific command to be executed. The PFE1500-12-054 supply supports the following basic command structures:

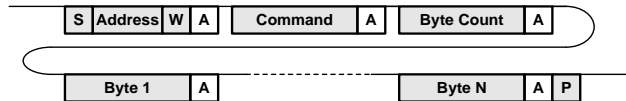
- Clock stretching limited to 1 ms
- SCL low time-out of >25 ms with recovery within 10 ms
- Recognized any time Start/Stop bus conditions

## WRITE

The write protocol is the SMBus 1.1 Write Byte/Word protocol. Note that the write protocol may end after the command byte or after the first data byte (Byte command) or then after sending 2 data bytes (Word command).

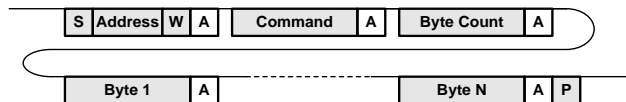


In addition, Block write commands are supported with a total maximum length of 255 bytes. See PFE Programming Manual for further information.

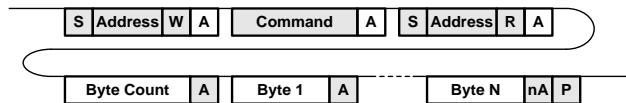


## READ

The read protocol is the SMBus 1.1 Read Byte/Word protocol. Note that the read protocol may request a single byte or word.



In addition, Block read commands are supported with a total maximum length of 255 bytes. See PFE Programming Manual BCA.00006 for further information.



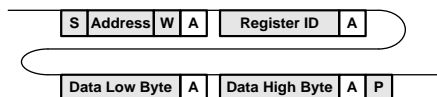
## PSMI PROTOCOL

New power management features in computer systems require the system to communicate with the power supply to access current, voltage, fan speed, and temperature information. Current measurements provide data to the system for determining potential system configuration limitations and provide actual system power consumption for facility planning. Temperature and fan monitoring allow the system to better manage fan speeds and temperatures for optimizing system acoustics. Voltage monitoring allows the system to calculate input wattage and warning of system voltage regulation problems. The Power Supply Management Interface (PSMI) supports diagnostic capabilities and allows managing of redundant power supplies. The communication method is SMBus. The current design guideline is version 2.12.

The communication protocol is register based and defines a read and write communication protocol to read / write to a single register address. All registers are accessed via the same basic command given below. No PEC (Packet Error Code) is used.

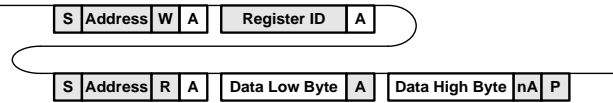
## WRITE

The write protocol used is the SMBus 2.0 Write Word protocol. All writes are 16-bit words; byte reads are not supported nor allowed. The shaded areas in the figure indicate bits and bytes written by the PSMI master device. See PFE Programming Manual for further information.



**READ**

The read protocol used is the SMBus 2.0 Read Word protocol. All reads are 16-bit words; byte reads are not supported nor allowed. The shaded areas in the figure indicate bits and bytes written by the PSMI master device. See PFE Programming Manual for further information.



**8.17 GRAPHICAL USER INTERFACE**

Bel Power Solutions provides with its “Bel Power Solutions I2C Utility” a Windows® XP/Vista/Win7 compatible graphical user interface allowing the programming and monitoring of the PFE1500-12-054 Front-End. The utility can be downloaded on: [www.belpowersolutions.com](http://www.belpowersolutions.com) and supports PMBus™ protocols.

The GUI allows automatic discovery of the units connected to the communication bus and will show them in the navigation tree. In the monitoring view the power supply can be controlled and monitored.

If the GUI is used in conjunction with the SNP-OP-BOARD-01 or YTM.G1Q01.0 Evaluation Kit it is also possible to control the PSON\_L pin(s) of the power supply.

Further there is a button to disable the internal fan for approximately 10 seconds. This allows the user to take input power measurements without fan consumptions to check efficiency compliance to the Climate Saver Computing Platinum specification.

The monitoring screen also allows to enable the hot-standby mode on the power supply. The mode status is monitored and by changing the load current it can be monitored when the power supply is being disabled for further energy savings. This obviously requires 2 power supplies being operated as a redundant system (as in the evaluation kit).

**NOTE:** The user of the GUI needs to ensure that only one of the power supplies have the hot-standby mode enabled.

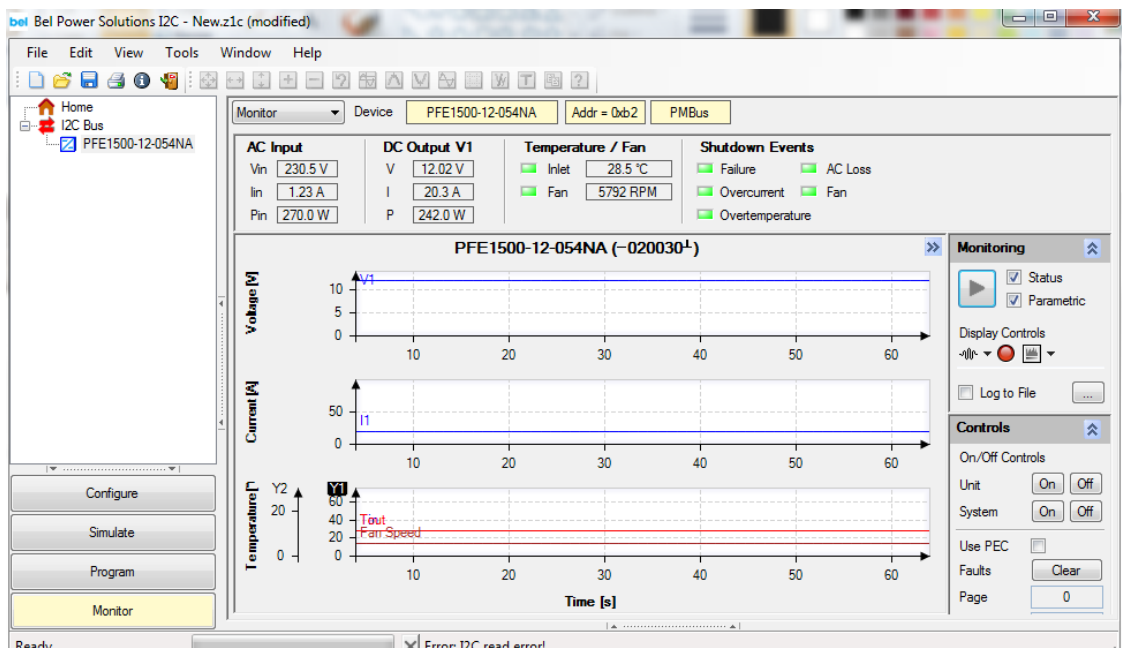


Figure 24. Monitoring dialog of the I2C Utility

## 9. TEMPERATURE AND FAN CONTROL

To achieve best cooling results sufficient airflow through the supply must be ensured. Do not block or obstruct the airflow at the rear of the supply by placing large objects directly at the output connector. The PFE1500-12-054NA, PFE1500-12-054NAC and PFE1500-12-054NAH are provided with normal airflow, which means the air enters through the DC-output of the supply and leaves at the AC-inlet. PFE supplies have been designed for horizontal operation.

The fan inside of the supply is controlled by a microprocessor. The RPM of the fan is adjusted to ensure optimal supply cooling and is a function of output power and the inlet temperature.

For the normal airflow version additional constraints apply because of the AC-connector. In a normal airflow unit, the hot air is exiting the power supply unit at the AC-inlet.

The IEC connector on the unit is rated 105°C. If 70°C mating connector is used then end user must derated the input power to meet a maximum 70°C temperature at the front, see Figure 7 in above section.

**NOTE:** It is the responsibility of the user to check the front temperature in such cases. The unit is not limiting its power automatically to meet such a temperature limitation.

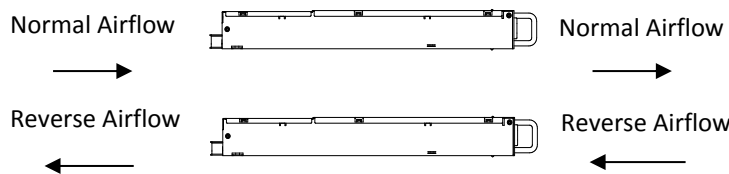


Figure 25. Airflow direction

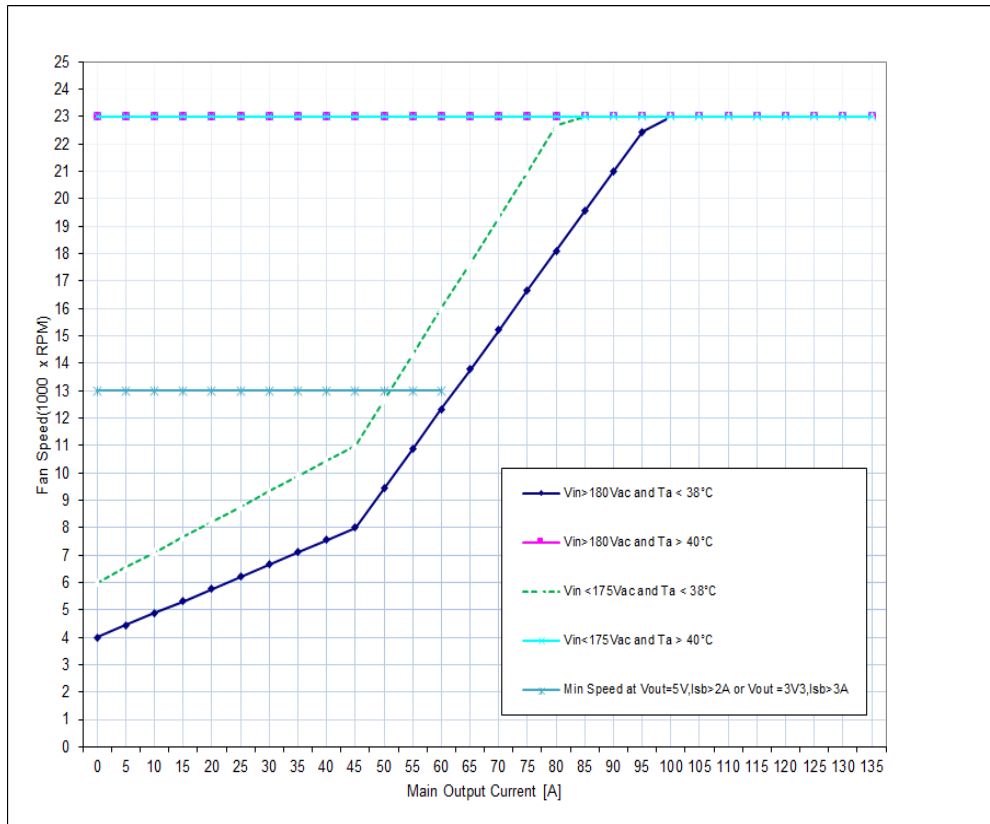


Figure 26. Fan speed vs. main output load

## 10. ELECTROMAGNETIC COMPATIBILITY

### 10.1 IMMUNITY

**NOTE:** Most of the immunity requirements are derived from EN 55024:1998/A2:2003.

PARAMETER	DESCRIPTION / CONDITION	CRITERION
ESD Contact Discharge	IEC / EN 61000-4-2, ±8 kV, 25+25 discharges per test point (metallic case, LEDs, connector body)	A
ESD Air Discharge	IEC / EN 61000-4-2, ±15 kV, 25+25 discharges per test point (non-metallic user accessible surfaces)	A
Radiated Electromagnetic Field	IEC / EN 61000-4-3, 10 V/m, 1 kHz/80% Amplitude Modulation, 1 µs Pulse Modulation, 10 kHz...2 GHz	A
Burst	IEC / EN 61000-4-4, level 3 AC port ±2 kV, 1 minute DC port ±1 kV, 1 minute	A
Surge	IEC / EN 61000-4-5 Line to earth: level 3, ±2 kV Line to line: level 2, ±1 kV	A
RF Conducted Immunity	IEC/EN 61000-4-6, Level 3, 10 Vrms, CW, 0.1 ... 80 MHz	A
Voltage Dips and Interruptions	IEC/EN 61000-4-11 1: Vi 230 V, 100% Load, Phase 0°, Dip 100%, Duration 10 ms 2: Vi 230 V, 100% Load, Phase 0°, Dip 100%, Duration 20 ms 3: Vi 230 V, 100% Load, Phase 0°, Dip 100%, Duration >20 ms	A V <sub>SB</sub> : A, V <sub>I</sub> : B B

### 10.2 EMISSION

PARAMETER	DESCRIPTION / CONDITION	CRITERION
Conducted Emission	EN55022 / CISPR 22: 0.15 ... 30 MHz, QP and AVG, single unit	Class A
	EN55022 / CISPR 22: 0.15 ... 30 MHz, QP and AVG, 2 units in rack system	Class A
Radiated Emission	EN55022 / CISPR 22: 30 MHz ... 1 GHz, QP, single unit	Class A
	EN55022 / CISPR 22: 30 MHz ... 1 GHz, QP, 2 units in rack system	Class A
Harmonic Emissions	IEC61000-3-2, Vin = 115 VAC / 60 Hz, & Vin = 230VAC/ 50 Hz, 100% Load	Class A
AC Flicker	IEC61000-3-3, Vin = 230 VAC / 60 Hz, 100% Load	Pass

## 11. SAFETY APPROVALS

Maximum electric strength testing is performed in the factory according to IEC/EN 60950, and UL 60950. Input-to-output electric strength tests should not be repeated in the field. Bel Power Solutions will not honor any warranty claims resulting from electric strength field tests.

PARAMETER	DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
Agency Approvals	UL 60950-1 Second Edition CAN/CSA-C22.2 No. 60950-1-07 Second Edition IEC 60950-1:2005 EN 60950-1:2006			Approved by independent body (see CE Declaration)	
Isolation Strength	Input (L/N) to case (PE)		Basic		
	Input (L/N) to output		Reinforced		
	Output to case (PE)		Functional		
$\delta c$ Creepage / Clearance	Primary (L/N) to protective earth (PE) Primary to secondary		According to safety standard		mm
Electrical Strength Test	Input to case		According to safety standard		kVAC
	Input to output				
	Output and Signals to case				

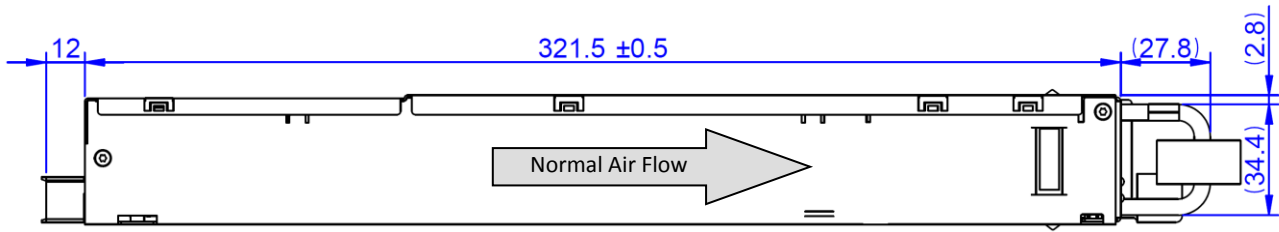
## 12. ENVIRONMENTAL SPECIFICATIONS

PARAMETER	DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT	
$T_A$	Ambient Temperature	$V_{I \min}$ to $V_{I \max}$ , $I_{N \text{ nom}}$ , $I_{SB \text{ nom}}$ below 5000 feet Altitude	0		+45	°C
		$V_{I \min}$ to $V_{I \max}$ , $I_{N \text{ nom}}$ , $I_{SB \text{ nom}}$ below 10,000 feet Altitude	0		+40	°C
$T_{\text{Aext}}$	Extended Temp. Range	Derating output	+46	+60	°C	
$T_S$	Storage Temperature	Non-operational	-20	+70	°C	
	Altitude	Operational, above Sea Level, refer derating to $T_A$	-	10,000	Feet	
$N_a$	Audible Noise	$V_{I \text{ nom}}$ , 50% $I_{O \text{ nom}}$ , $T_A = 25^\circ\text{C}$	60		dBA	

## 13. MECHANICAL SPECIFICATIONS

PARAMETER	DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
Dimensions	Width		54.5		mm
	Height		40.0		
	Depth		321.5		
$M$	Weight		1.13		kg

## PFE1500-12-054NAH and PFE1500-12-054RAH: Input AC connector RongFeng RF-203-D-1.0



**NOTE:** A 3D step file of the power supply casing is available on request.

Figure 27. Side View 1

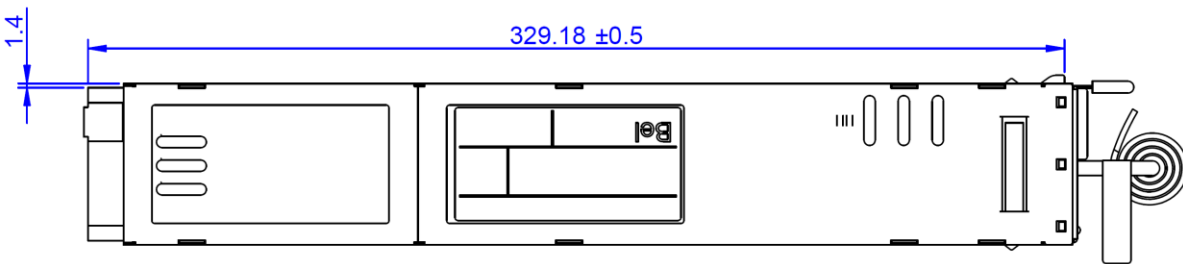


Figure 28. Top View

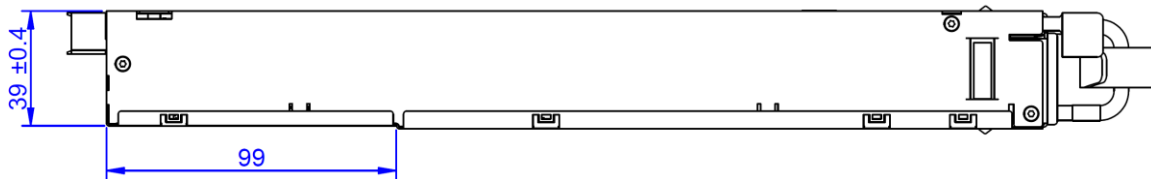


Figure 29. Side View 2

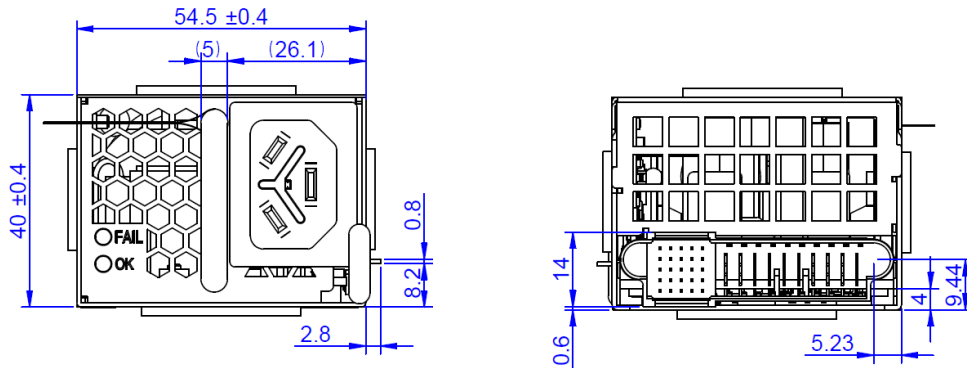
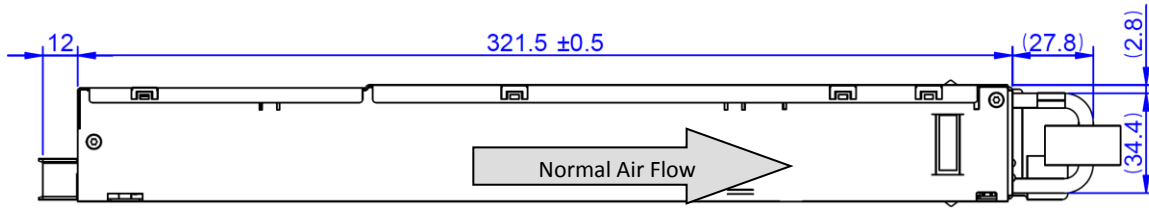


Figure 30. Front and Rear View

**PFE1500-12-054NA and PFE1500-12-054RA:**  
**C14 type Input AC connector RongFeng SS-120-1.0B-2.8BV or equivalent**



**NOTE:** A 3D step file of the power supply casing is available on request.  
 Figure 31. Side View 1

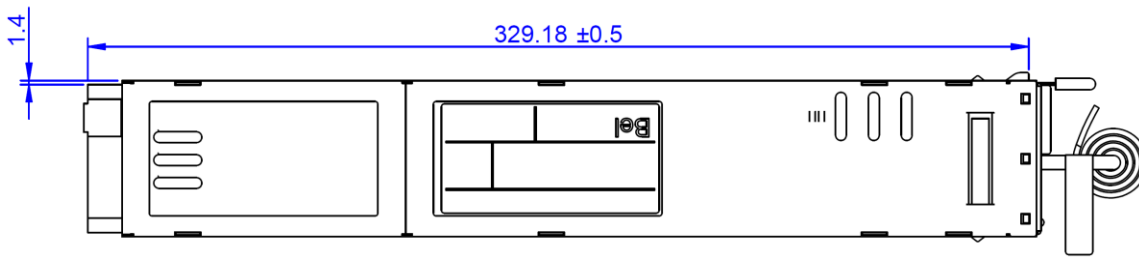


Figure 32. Top View

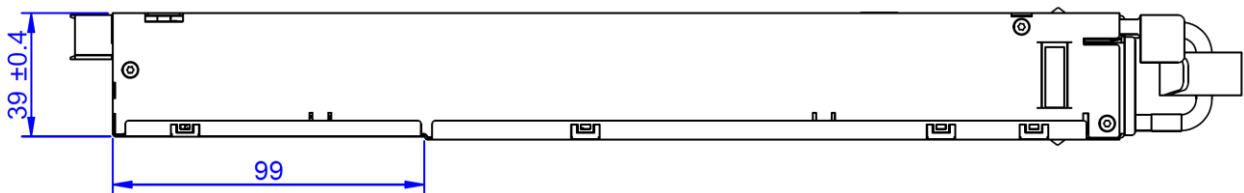


Figure 33. Side View 2

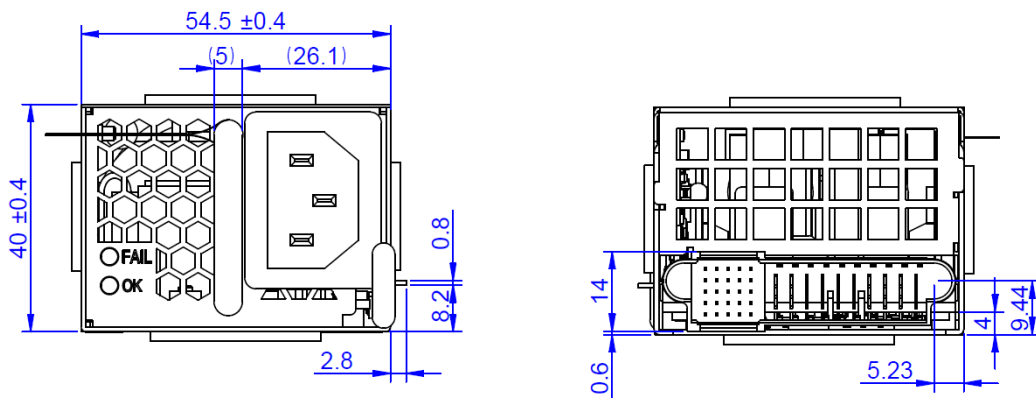
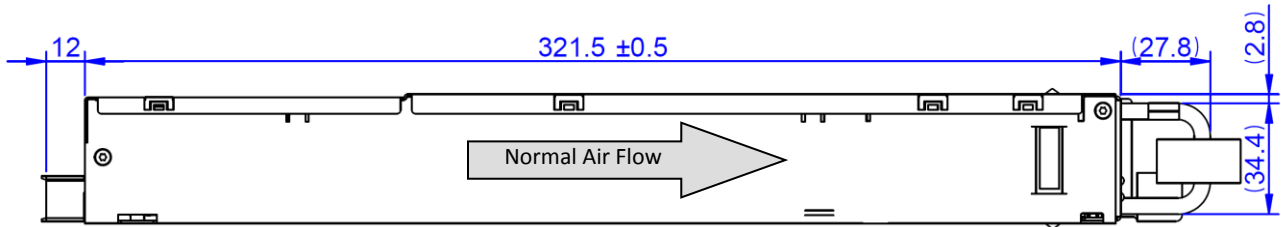


Figure 34. Front and Rear View



**PFE1500-12-054NAC and PFE1500-12-054RAC:**  
**C16 Type Input AC connector, RongFeng SS-120B-1.0-4.0Ad or equivalent**



**NOTE:** A 3D step file of the power supply casing is available on request.  
 Figure 35. Side View 1

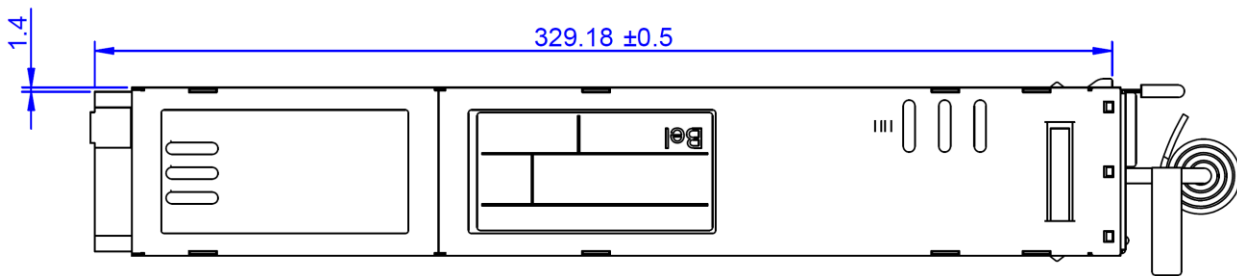


Figure 36. Top View

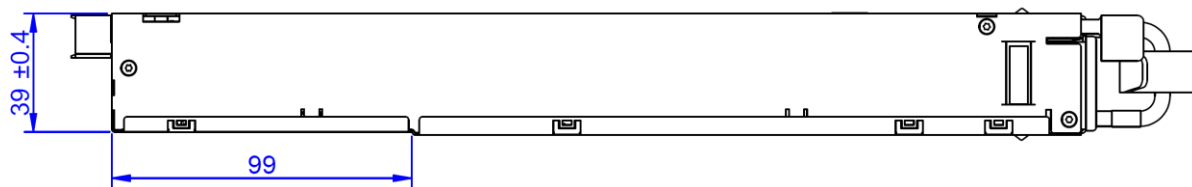


Figure 37. Side View 2

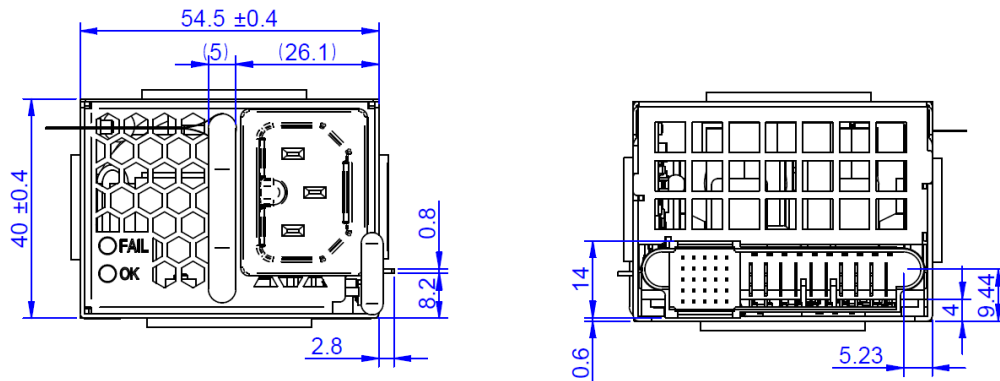


Figure 38. Front and Rear View

## 14. CONNECTIONS

AC input connector:

PFE1500-12-054NA/RA: Power supplier connector: IEC320 C14 type

PFE1500-12-054NAC/RAC: Power supplier connector: IEC320 C16 type

PFE1500-12-054NAH/RAH:

Power supplier connector: RongFeng P/N RF-203-D-1.0

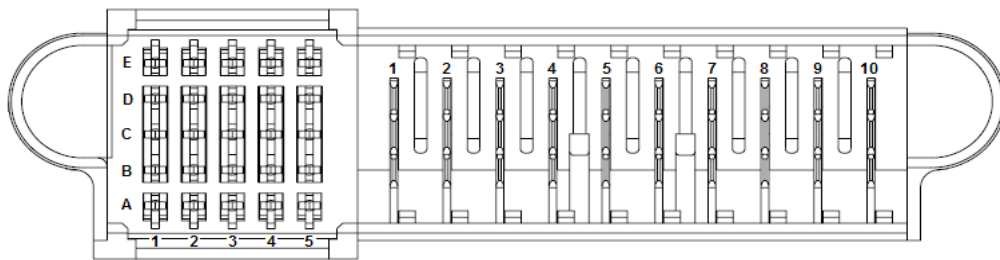
Mating connector:

BizLink, type: BC-326, <http://www.bizlinktech.com/>

LongWell, type: LS-26, <http://www.longwell.com/cn/>

LINETEK, type: LS-24, [http://w3.linetek.com.tw/html/F2\\_E.htm](http://w3.linetek.com.tw/html/F2_E.htm)

DC output connector:





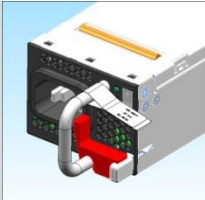
Power Supply Connector: Tyco Electronics P/N 2-1926736-3 (NOTE: Column 5 is recessed (short pins))

Mating Connector: Tyco Electronics P/N 2-1926739-5 or FCI 10108888-R10253SLF

PIN	NAME	DESCRIPTION
<b>Output</b>		
6, 7, 8, 9, 10	V1	+12 VDC main output
1, 2, 3, 4, 5	PGND	Power ground (return)
<b>Control Pins</b>		
A1	VSB	Standby positive output (+3.3/5 V)
B1	VSB	Standby positive output (+3.3/5 V)
C1	VSB	Standby positive output (+3.3/5 V)
D1	VSB	Standby positive output (+3.3/5 V)
E1	VSB	Standby positive output (+3.3/5 V)
A2	SGND	Signal ground (return)
B2	SGND	Signal ground (return)
C2	HOTSTANDBYEN_H	Hot standby enable signal: active-high
D2	VSB_SENSE_R	Standby output negative sense
E2	VSB_SENSE	Standby output positive sense
A3	APS	I <sup>2</sup> C address and protocol selection (select by a pull down resistor)
B3	N/C	Reserved
C3	SDA	I <sup>2</sup> C data signal line
D3	V1_SENSE_R	Main output negative sense
E3	V1_SENSE	Main output positive sense

A4	SCL	I <sup>2</sup> C clock signal line
B4	PSON_L	Power supply on input (connect to A2/B2 to turn unit on): active-low
C4	SMB_ALERT_L	SMB Alert signal output: active-low
D4	N/C	Reserved
E4	ACOK_H	AC input OK signal: active-high
A5	PSKILL_H	Power supply kill (lagging pin): active-high
B5	ISHARE	Current share bus (lagging pin)
C5	PWOK_H	Power OK signal output (lagging pin): active-high
D5	VSB_SEL	Standby voltage selection (lagging pin)
E5	PRESENT_L	Power supply present (lagging pin): active-low

## 15. ACCESSORIES

ITEM	DESCRIPTION	ORDERING PART NUMBER	SOURCE
	<b>Bel Power Solutions I<sup>2</sup>C Utility</b> Windows XP/Vista/7 compatible GUI to program, control and monitor PFE Front-Ends (and other I <sup>2</sup> C units)	N/A	<a href="http://belpowersolutions.com">belpowersolutions.com</a>
	<b>Dual Connector Board</b> Connector board to operate 2 PFE units in parallel. Includes an on-board USB to I <sup>2</sup> C converter (use <i>Bel Power Solutions PC Utility</i> as desktop software).	SNP-OP-BOARD-01 or YTM.G1Q01.0	<a href="http://belpowersolutions.com">belpowersolutions.com</a>
	<b>Latch Lock</b> Optional latch lock to prevent accidental removal of the power supply from the system while the AC plug is engaged.	XSL.00019.0	Bel Power Solutions

**For more information on these products consult: [tech.support@psbel.com](mailto:tech.support@psbel.com)**

**NUCLEAR AND MEDICAL APPLICATIONS** - Products are not designed or intended for use as critical components in life support systems, equipment used in hazardous environments, or nuclear control systems.

**TECHNICAL REVISIONS** - The appearance of products, including safety agency certifications pictured on labels, may change depending on the date manufactured. Specifications are subject to change without notice.



Asia-Pacific  
+86 755 298 85888

Europe, Middle East  
+353 61 225 977

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### Офис по работе с юридическими лицами:

105318, г.Москва, ул.Щербаковская д.3, офис 1107, 1118, ДЦ «Щербаковский»

Телефон: +7 495 668-12-70 (многоканальный)

Факс: +7 495 668-12-70 (доб.304)

E-mail: [info@moschip.ru](mailto:info@moschip.ru)

Skype отдела продаж:

moschip.ru

moschip.ru\_4

moschip.ru\_6

moschip.ru\_9