



N-Channel 100-V (D-S) MOSFET

CHARACTERISTICS

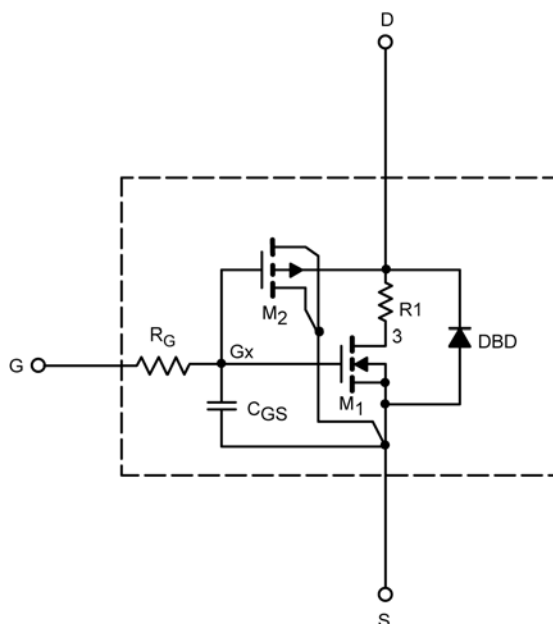
- N-Channel Vertical DMOS
- Macro Model (Subcircuit Model)
- Level 3 MOS
- Apply for both Linear and Switching Application
- Accurate over the -55 to 125°C Temperature Range
- Model the Gate Charge, Transient, and Diode Reverse Recovery Characteristics

DESCRIPTION

The attached spice model describes the typical electrical characteristics of the n-channel vertical DMOS. The subcircuit model is extracted and optimized over the -55 to 125°C temperature ranges under the pulsed 0-V to 10-V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched C_{gd} model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

SUBCIRCUIT MODEL SCHEMATIC



SPICE Device Model Si4100DY

Vishay Siliconix



SPECIFICATIONS ($T_J = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)					
Parameter	Symbol	Test Condition	Simulated Data	Measured Data	Unit
Static					
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 250\ \mu\text{A}$	3		V
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} \geq 5\ \text{V}$, $V_{GS} = 10\ \text{V}$	88		A
Drain-Source On-State Resistance ^a	$r_{DS(on)}$	$V_{GS} = 10\ \text{V}$, $I_D = 4.4\ \text{A}$	0.051	0.051	Ω
		$V_{GS} = 6\ \text{V}$, $I_D = 3.8\ \text{A}$	0.069	0.069	
Forward Transconductance ^a	g_{fs}	$V_{DS} = 15\ \text{V}$, $I_D = 4.4\ \text{A}$	12	10	S
Diode Forward Voltage ^a	V_{SD}	$I_S = 3.5\ \text{A}$, $V_{GS} = 0\ \text{V}$	0.70	0.80	V
Dynamic^b					
Input Capacitance	C_{iss}	$V_{DS} = 50\ \text{V}$, $V_{GS} = 0\ \text{V}$, $f = 1\ \text{MHz}$	608	600	pF
Output Capacitance	C_{oss}		90	90	
Reverse Transfer Capacitance	C_{rss}		43	50	
Total Gate Charge	Q_g	$V_{DS} = 50\ \text{V}$, $V_{GS} = 10\ \text{V}$, $I_D = 4.4\ \text{A}$	12.5	13.5	nC
			9	9	
Gate-Source Charge	Q_{gs}	$V_{DS} = 50\ \text{V}$, $V_{GS} = 6\ \text{V}$, $I_D = 4.4\ \text{A}$	3	3	
Gate-Drain Charge	Q_{gd}		4.6	4.6	

Notes

a. Pulse test; pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$.

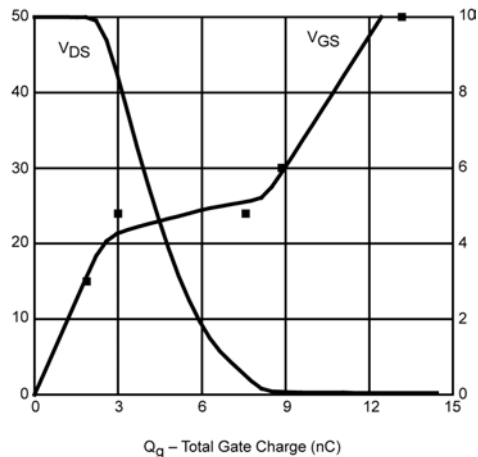
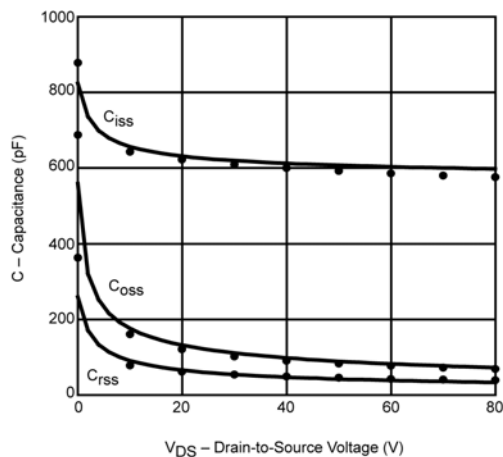
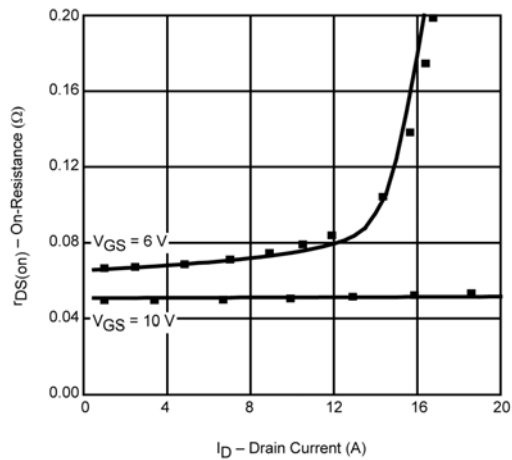
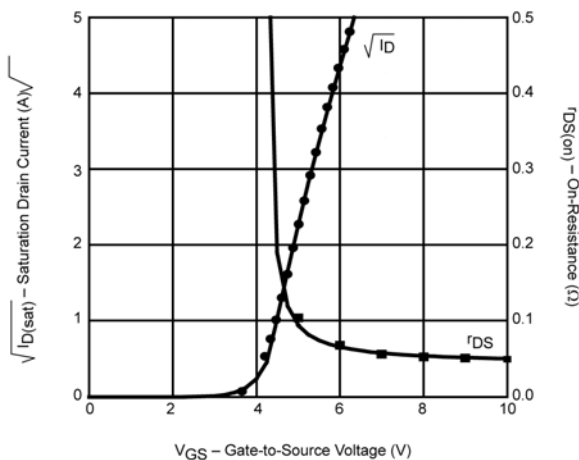
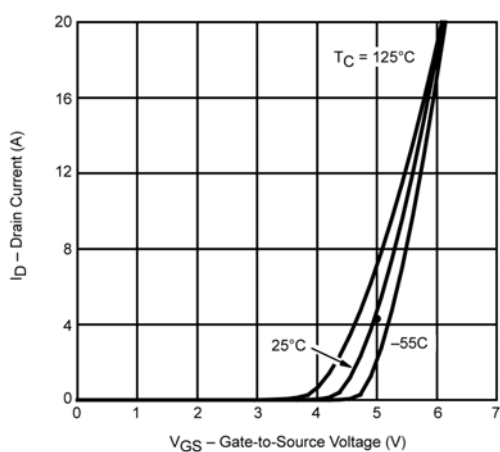
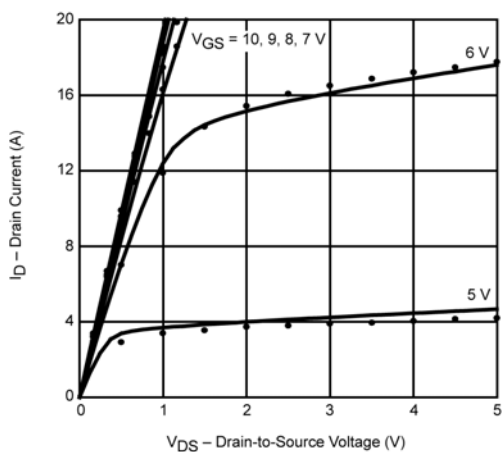
b. Guaranteed by design, not subject to production testing.



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COMPARISON OF MODEL WITH MEASURED DATA ($T_J=25^\circ\text{C}$ UNLESS OTHERWISE NOTED)



Note: Dots and squares represent measured data.



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Офис по работе с юридическими лицами:

105318, г.Москва, ул.Щербаковская д.3, офис 1107, 1118, ДЦ «Щербаковский»

Телефон: +7 495 668-12-70 (многоканальный)

Факс: +7 495 668-12-70 (доб.304)

E-mail: info@moschip.ru

Skype отдела продаж:

moschip.ru

moschip.ru_4

moschip.ru_6

moschip.ru_9