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S98GL064NB0-007 MCP
S98GL064NB0-008 MCP

**64 Mbit (4M x 16-bit), 3 V, Flash and
32 Mbit (2M x 16-bit) Async Pseudo Static RAM**

Distinctive Characteristics

MCP Features

- Power supply voltage of 2.7 to 3.6 volt
- High performance
 - 90 ns access time (90 ns Flash, 70 ns pSRAM/SRAM)
 - 25 ns page read times
- Packages
 - 7 x 9 x 1.2 mm 56-ball FBGA
- Operating temperature
 - -40°C to +85°C

General Description

The S98GL064NB0-007, -008 product series consists of:

- One S29GL064N flash memory device
- Top Boot (-007)
- Bottom Boot (-008)
- One 32 Mb asynchronous pSRAM (SPG032D970R3R)

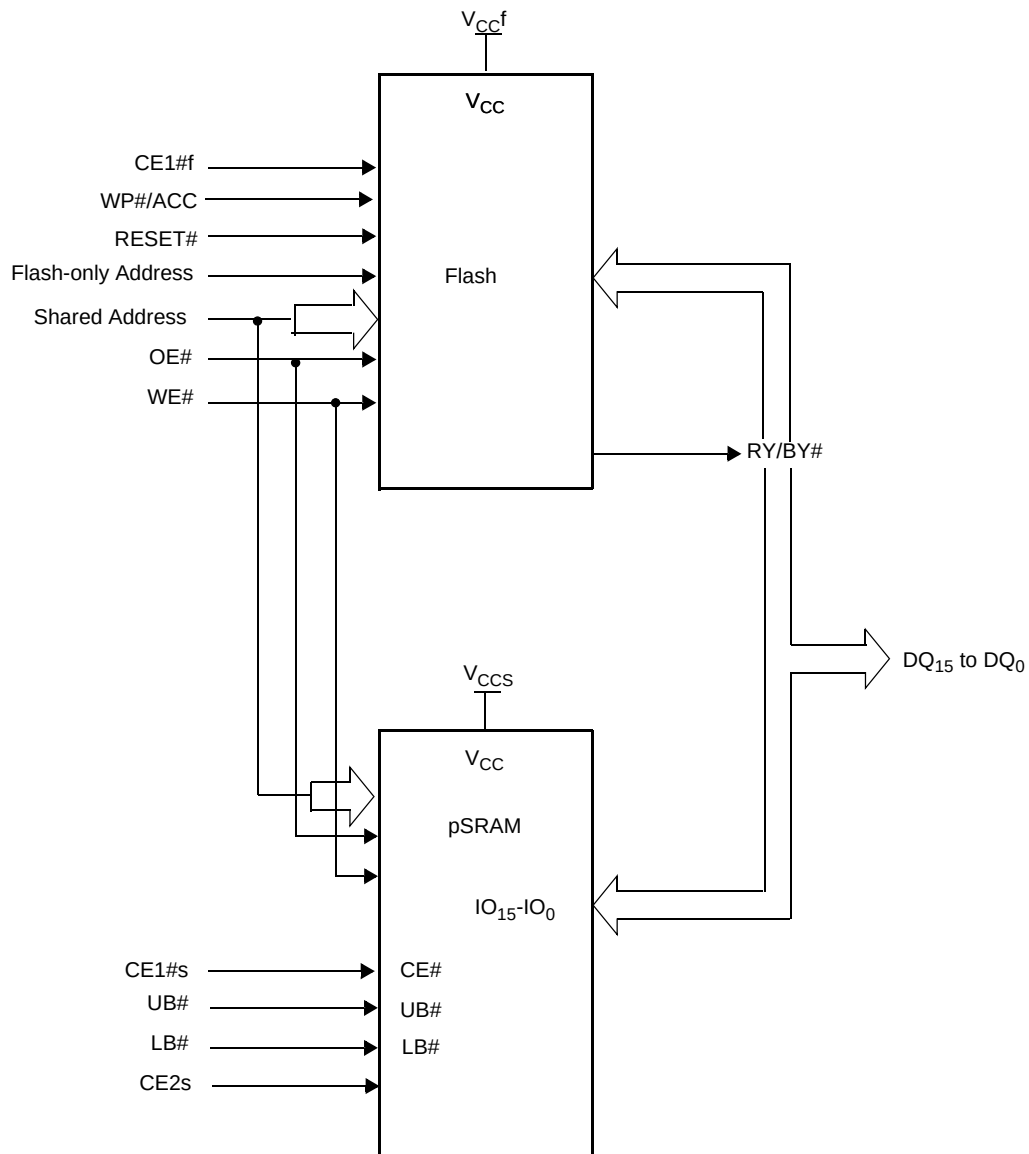
For detailed specifications, please refer to the individual data sheets.

Document	Publication Identification Number (PID)
S29GL-N	S29GL-N_00
SPG032D970R3R	SPG032D970R3R

1. Product Selector Guide

Device-Model#	Flash Access time (ns)	(p)SRAM density	(p)SRAM Access time (ns)	(p)SRAM type	Package
S98GL064NB0-007, -008	90	32 Mb	70	SPG032D970R3R	TLC056

2. MCP Block Diagram



Legend

- Shared (Black circle)
- Flash only (Light Gray circle)
- RAM only (Medium Gray circle)
- Reserved for Future Use (Dashed circle)

Pin	Function	Category
A2		Flash only
A3		Flash only
A4		Flash only
A5		Flash only
A6		Flash only
A7		Flash only
A8		Flash only
A9		Flash only
A10		Flash only
A11		Flash only
A12		Flash only
A13		Flash only
A14		Flash only
A15		Flash only
A16		Flash only
A17		Flash only
A18		Flash only
A19		Flash only
A20		Flash only
A21		Flash only
B1		Flash only
B2		Flash only
B3		Flash only
B4		Flash only
B5		Flash only
B6		Flash only
B7		Flash only
B8		Flash only
C1		Flash only
C2		Flash only
C3		Shared
C4		Flash only
C5		Shared
C6		Flash only
C7		Flash only
C8		Flash only
D1		Flash only
D2		Flash only
D3		Flash only
D4		Flash only
D5		Flash only
D6		Flash only
D7		Flash only
D8		Reserved for Future Use
D9		Flash only
D10		Flash only
D11		Flash only
D12		Flash only
D13		Flash only
D14		Flash only
D15		Flash only
D16		Flash only
D17		Flash only
D18		Flash only
D19		Flash only
D20		Flash only
D21		Flash only
E1		Flash only
E2		Flash only
E3		Flash only
E4		Flash only
E5		Flash only
E6		Flash only
E7		Reserved for Future Use
E8		Flash only
F1		Flash only
F2		Flash only
F3		Flash only
F4		Flash only
F5		Flash only
F6		Flash only
F7		Flash only
F8		Reserved for Future Use
G1		Shared
G2		Flash only
G3		Flash only
G4		Flash only
G5		RAM only
G6		Flash only
G7		Flash only
G8		Flash only
H1		Flash only
H2		Flash only
H3		Flash only
H4		Flash only
H5		Reserved for Future Use
H6		Flash only
H7		Flash only

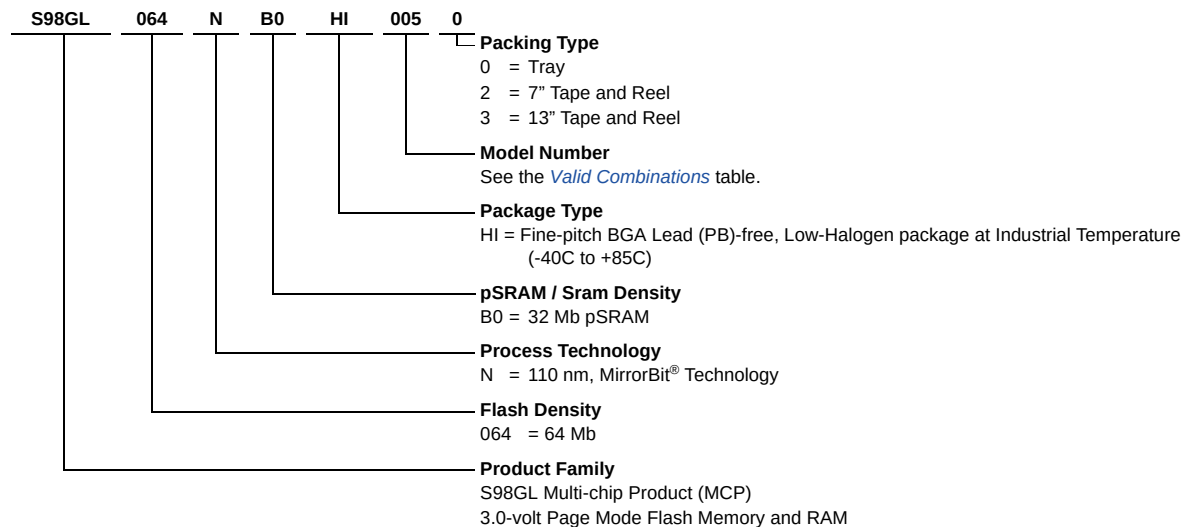
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4. Pin Description

Pin	Description
A21–A0	22 Address Inputs (Common and Flash only) (A20–A0 for the S71GL032N)
DQ15–DQ0	16 Data Inputs/Outputs (Common)
CE1#f	Chip Enable (Flash)
CE1#s	Chip Enable 1 (pSRAM/SRAM)
CE2s	Chip Enable 2 (pSRAM/SRAM)
OE#	Output Enable (Common)
WE#	Write Enable (Common)
RY/BY#	Ready/Busy Output (Flash 1)
UB#	Upper Byte Control (pSRAM/SRAM)
LB#	Lower Byte Control (pSRAM/SRAM)
RESET#	Hardware Reset Pin, Active Low (Flash)
WP#/ACC	Hardware Write Protect/Acceleration Pin (Flash)
V _{CCf}	Flash 3.0 volt-only single power supply (see Product Selector Guide for speed options and voltage supply tolerances)
V _{CCS}	pSRAM/SRAM Power Supply
V _{SS}	Device Ground (Common)
NC	Not Connected. No device internal signal is connected to the package connector nor is there any future plan to use the connector for a signal. The connection may safely be used for routing space for a signal on a Printed Circuit Board (PCB).
RFU	Reserved for Future Use. No device internal signal is currently connected to the package connector but there is potential future use for the connector for a signal. It is recommended to not use RFU connectors for PCB routing channels so that the PCB may take advantage of future enhanced features in compatible footprint devices.

5. Ordering Information

The order number is formed by a valid combinations of the following:



Valid Combinations

S98GL064NB0 Valid Combinations				Speed Options (ns) / Boot Sector Option	(p)SRAM Type / Access Time (ns)	Package
Base Ordering Part Number	Package & Temperature	Package Modifier / Model Number	Packing Type			
S98GL064NB0	HI	007	0, 2, 3 (1)	90 / Top Boot Sector	SPG032D970R3R	TLC056
		008		90 / Bottom Boot Sector		

Note

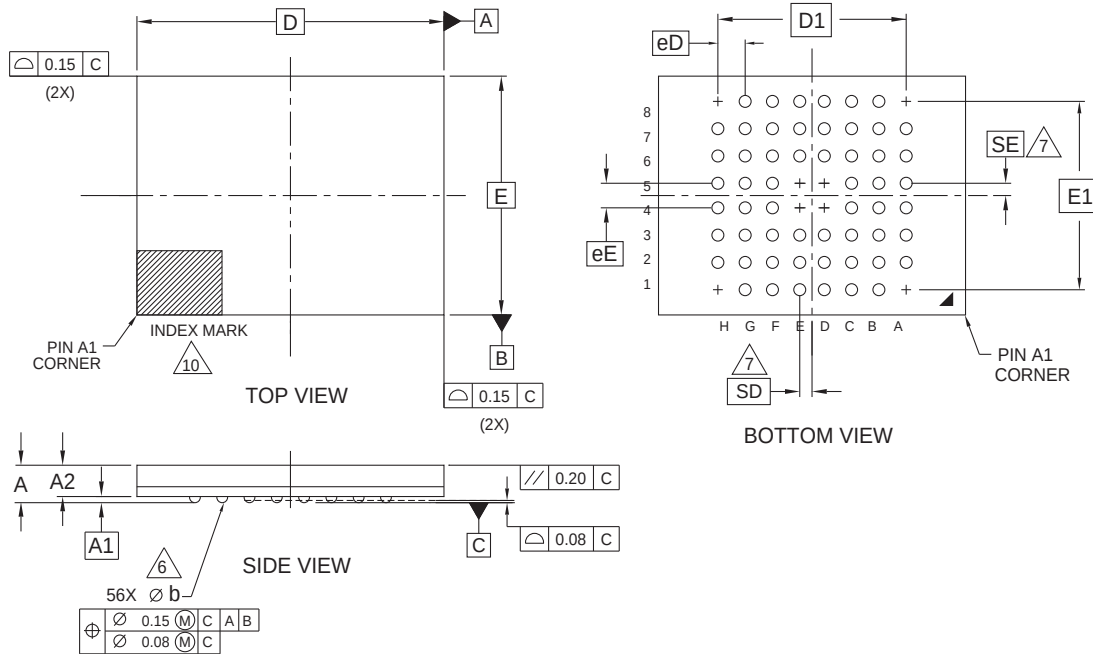
1. Type 0 is standard. Specify other options as required.

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult your local sales office to confirm availability of specific valid combinations and to check on newly released combinations.

6. Physical Dimensions

6.1 TLC056—56-ball Fine-Pitch Ball Grid Array (FBGA) 9 x 7 mm Package



PACKAGE	TLC 056			
JEDEC	N/A			
D x E	9.00 mm x 7.00 mm PACKAGE			
SYMBOL	MIN	NOM	MAX	NOTE
A	---	---	1.20	PROFILE
A1	0.20	---	---	BALL HEIGHT
A2	0.81	---	0.97	BODY THICKNESS
D	9.00 BSC.			BODY SIZE
E	7.00 BSC.			BODY SIZE
D1	5.60 BSC.			MATRIX FOOTPRINT
E1	5.60 BSC.			MATRIX FOOTPRINT
MD	8			MATRIX SIZE D DIRECTION
ME	8			MATRIX SIZE E DIRECTION
n	56			BALL COUNT
φb	0.35	0.40	0.45	BALL DIAMETER
eE	0.80 BSC.			BALL PITCH
eD	0.80 BSC.			BALL PITCH
SD / SE	0.40 BSC.			SOLDER BALL PLACEMENT
	A1,A8,D4,D5,E4,E5,H1,H8			DEPOPULATED SOLDER BALLS

NOTES:

- DIMENSIONING AND TOLERANCING METHODS PER ASME Y14.5M-1994.
- ALL DIMENSIONS ARE IN MILLIMETERS.
- BALL POSITION DESIGNATION PER JESD 95-1, SPP-010.
- [e] REPRESENTS THE SOLDER BALL GRID PITCH.
- SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.
SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.
n IS THE NUMBER OF POPULATED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
- DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
- SD AND SE ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.
WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW SD OR SE = 0.000.
WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, SD OR SE = [e/2]
- "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.
- N/A
- A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK, METALLIZED MARK INDENTATION OR OTHER MEANS.

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7. Revision History

Spanion Publication Number: S98GL064NB0-007_008

Section	Description
Revision 01 (October 21, 2014)	
	Initial release

Document History Page

Document Title: S98GL064NB0-007 MCP, S98GL064NB0-008 MCP 64 Mbit (4M x 16 bit), 3 V, Flash and 32 Mbit (2M x 16 bit) Async Pseudo Static RAM Document Number: 002-00509				
Rev.	ECN No.	Orig. of Change	Submission Date	Description of Change
**	—	RYSU	10/21/2014	Initial release
*A	4996550	RYSU	10/30/2015	Updated to Cypress template

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