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DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

74HC/HCT390
Dual decade ripple counter

Product specification
File under Integrated Circuits, IC06

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Philips Semiconductors

PHILIPS

Dual decade ripple counter — 74HC/HCT390

FEATURES

- Two BCD decade or bi-quinary counters
- One package can be configured to divide-by-2, 4, 5, 10, 20, 25, 50 or 100
- Two master reset inputs to clear each decade counter individually
- Output capability: standard
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT390 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT390 are dual 4-bit decade ripple counters divided into four separately clocked sections. The counters have two divide-by-2 sections and two divide-by-5 sections. These sections are normally used in a BCD decade or bi-quinary configuration, since they share a common master reset input (nMR). If the two master reset inputs (1MR and 2MR) are used to simultaneously clear all 8 bits of the counter, a number of counting configurations are possible within one package. The separate clocks ($n\overline{CP}_0$ and $n\overline{CP}_1$) of each section allow ripple counter or frequency division applications of divide-by-2, 4, 5, 10, 20, 25, 50 or 100.

Each section is triggered by the HIGH-to-LOW transition of the clock inputs ($n\overline{CP}_0$ and $n\overline{CP}_1$). For BCD decade operation, the nQ_0 output is connected to the $n\overline{CP}_1$ input of, the divide-by-5 section. For bi-quinary decade operation, the nQ_3 output is connected to the $n\overline{CP}_0$ input and nQ_0 becomes the decade output.

The master reset inputs (1MR and 2MR) are active HIGH asynchronous inputs to each decade counter which operates on the portion of the counter identified by the “1” and “2” prefixes in the pin configuration. A HIGH level on the nMR input overrides the clocks and sets the four outputs LOW.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/ t_{PLH}	propagation delay	C_L = 15 pF; V_{CC} = 5 V			
	$n\overline{CP}_0$ to nQ_0		14	18	ns
	$n\overline{CP}_1$ to nQ_1		15	19	ns
	$n\overline{CP}_1$ to nQ_2		23	26	ns
	$n\overline{CP}_1$ to nQ_3		15	19	ns
	nMR to Q_n		16	18	ns
f_{max}	maximum clock frequency $n\overline{CP}_0$, $n\overline{CP}_1$		66	61	MHz
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per counter	notes 1 and 2	20	21	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} –1.5 V

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ORDERING INFORMATION

See *"74HC/HCT/HCU/HCMOS Logic Package Information"*.

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 15	$1\overline{CP}_0$, $2\overline{CP}_0$	clock input divide-by-2 section (HIGH-to-LOW, edge-triggered)
2, 14	1MR, 2MR	asynchronous master reset inputs (active HIGH)
3, 5, 6, 7	$1Q_0$ to $1Q_3$	flip-flop outputs
4, 12	$1\overline{CP}_1$, $2\overline{CP}_1$	clock input divide-by-5 section (HIGH-to-LOW, edge triggered)
8	GND	ground (0 V)
13, 11, 10, 9	$2Q_0$ to $2Q_3$	flip-flop outputs
16	V_{CC}	positive supply voltage

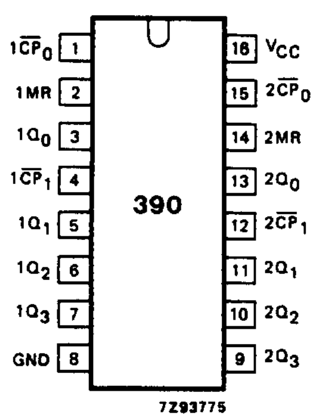

Fig.1 Pin configuration.

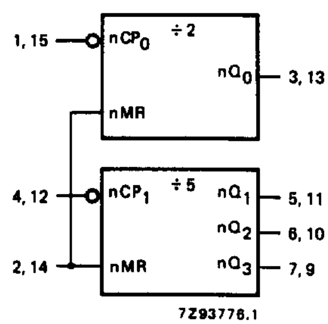

Fig.2 Logic symbol.

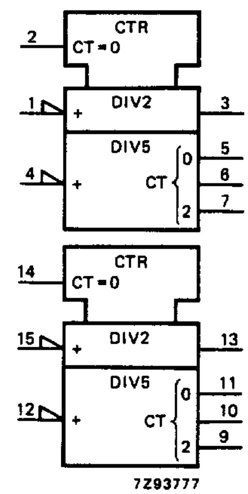

Fig.3 IEC logic symbol.

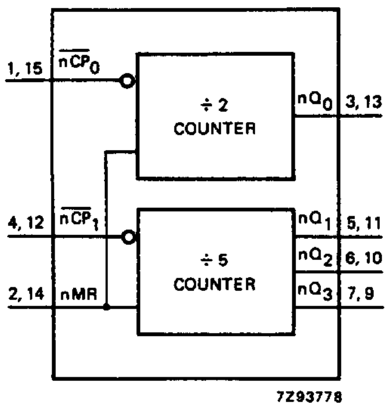

Fig.4 Functional diagram.

BCD COUNT SEQUENCE FOR 1/2 THE "390"

COUNT	OUTPUTS			
	Q_0	Q_1	Q_2	Q_3
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H

Notes

1. Output Q_0 connected to $n\overline{CP}_1$ with counter input on $n\overline{CP}_0$.
   H = HIGH voltage level
   L = LOW voltage level

BI-QUINARY COUNT SEQUENCE FOR 1/2 THE "390"

COUNT	OUTPUTS			
	Q_0	Q_1	Q_2	Q_3
0	L	L	L	L
1	L	H	L	L
2	L	L	H	L
3	L	H	H	L
4	L	L	L	H
5	H	L	L	L
6	H	H	L	L
7	H	L	H	L
8	H	H	H	L
9	H	L	L	H

Note

1. Output Q_3 connected to $n\overline{CP}_0$ with counter input on $n\overline{CP}_1$.

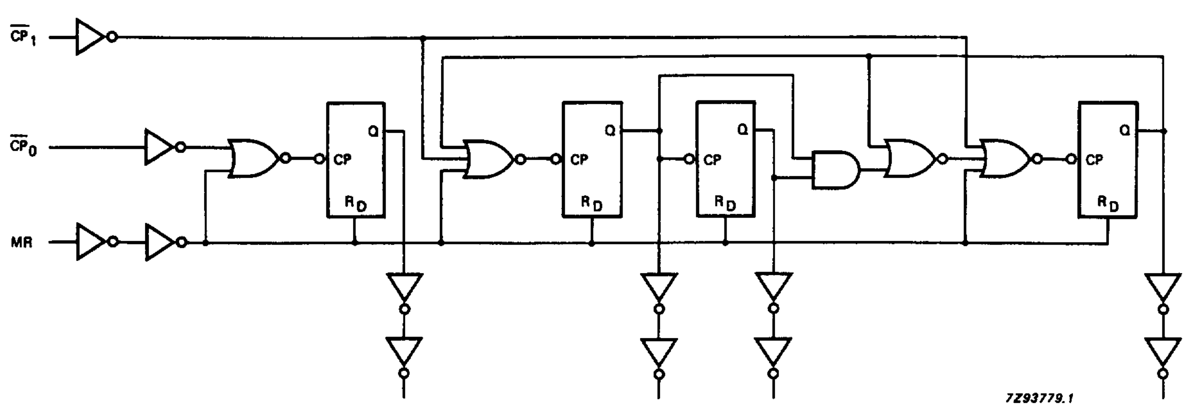

Fig.5 Logic diagram (one counter).

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f = 6$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} (V)	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay $n\overline{CP}_0$ to nQ_0		47 17 14	145 29 25		180 36 31		220 44 38	ns	2.0 4.5 6.0	Fig.6
t_{PHL}/ t_{PLH}	propagation delay $n\overline{CP}_1$ to nQ_1		50 18 14	155 31 26		195 39 33		235 47 40	ns	2.0 4.5 6.0	Fig.6
t_{PHL}/ t_{PLH}	propagation delay $n\overline{CP}_1$ to nQ_2		74 27 22	210 42 36		265 53 45		315 63 54	ns	2.0 4.5 6.0	Fig.6
t_{PHL}/ t_{PLH}	propagation delay $n\overline{CP}_1$ to nQ_3		50 18 14	155 31 26		195 39 33		235 47 40	ns	2.0 4.5 6.0	Fig.6
t_{PHL}	propagation delay nMR to nQ_n		52 19 15	165 33 28		205 41 35		250 50 43	ns	2.0 4.5 6.0	Fig.7
t_{THL}/ t_{TLH}	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig.6
t_W	clock pulse width $n\overline{CP}_0$, $n\overline{CP}_1$	80 16 14	19 7 6		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig.6
t_W	master reset pulse width HIGH	80 17 14	28 10 8		105 21 18		130 26 22		ns	2.0 4.5 6.0	Fig.7
t_{rem}	removal time nMR to $n\overline{CP}_n$	75 15 13	22 8 6		95 19 16		110 22 19		ns	2.0 4.5 6.0	Fig.7
f_{max}	maximum clock pulse frequency $n\overline{CP}_0$, $n\overline{CP}_1$	6.0 30 35	20 60 71		4.8 24 28		4.0 20 24		MHz	2.0 4.5 6.0	Fig.6

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DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard
I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

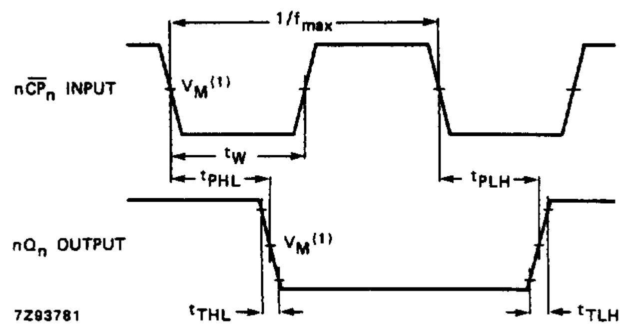
INPUT	UNIT LOAD COEFFICIENT
$n\overline{CP}_0$	0.45
$n\overline{CP}_1$, nMR	0.60

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f = 6$ ns; $C_L = 50$ pF

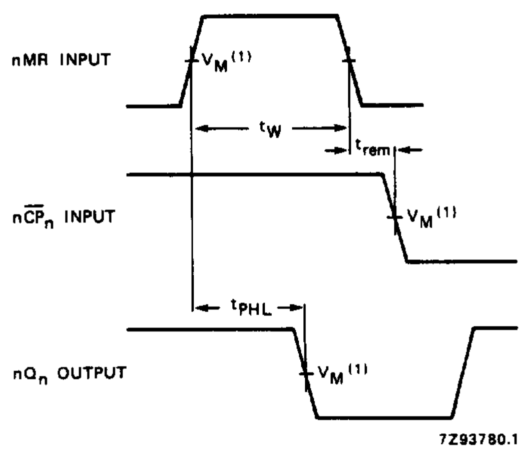
SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT									
		+25			−40 to +85		−40 to +125			V_{CC} (V)	WAVEFORMS
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay $n\overline{CP}_0$ to nQ_0		21	34		43		51	ns	4.5	Fig.6
t_{PHL}/ t_{PLH}	propagation delay $n\overline{CP}_1$ to nQ_1		22	38		48		57	ns	4.5	Fig.6
t_{PHL}/ t_{PLH}	propagation delay $n\overline{CP}_1$ to nQ_2		30	51		64		77	ns	4.5	Fig.6
t_{PHL}/ t_{PLH}	propagation delay $n\overline{CP}_1$ to nQ_3		22	38		48		57	ns	4.5	Fig.6
t_{PHL}	propagation delay nMR to nQ_n		21	36		45		54	ns	4.5	Fig.7
t_{THL}/ t_{TLH}	output transition time		7	15		19		22	ns	4.5	Fig.6
t_W	clock pulse width $n\overline{CP}_0$, $n\overline{CP}_1$	18	8		23		27		ns	4.5	Fig.6
t_W	master reset pulse width HIGH	17	10		21		26		ns	4.5	Fig.7
t_{rem}	removal time nMR to $n\overline{CP}_n$	15	8		19		22		ns	4.5	Fig.7
f_{max}	maximum clock pulse frequency $n\overline{CP}_0$, $n\overline{CP}_1$	27	55		22		18		MHz	4.5	Fig.6

AC WAVEFORMS



(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT : V_M = 1.3 V; V_I = GND to 3 V.

Fig.6 Waveforms showing the clock ($n\overline{CP}_n$) to output (nQ_n) propagation delays, the clock pulse width, the output transition times and the maximum clock frequency.



(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT : V_M = 1.3 V; V_I = GND to 3 V.

Fig.7 Waveforms showing the master reset (nMR) pulse width, the master reset to output (nQ_n) propagation delays and the master reset to clock ($n\overline{CP}_n$) removal time.

PACKAGE OUTLINES

See *"74HC/HCT/HCU/HCMOS Logic Package Outlines"*.

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