ISL78010

Automotive Grade TFT-LCD Power Supply

FN6501
Rev 2.00
December 4, 2013

The ISL78010 is a multiple output regulator for use in all TFT-LCD automotive applications. It features a single boost converter with an integrated 2A FET, two positive LDOs for V_{ON} and V_{LOGIC} generation, and a single negative LDO for V_{OFF} generation. The boost converter can be programmed to operate in either P-mode for optimal transient response or PI-mode for improved load regulation.

The ISL78010 includes fault protection for all four channels. Once a fault is detected on either the V_{BOOST}, V_{ON} or V_{OFF} channels, the device is latched off until the input supply or EN is cycled. If a fault is detected on the V_{LOGIC} channel, the device is latched off until the input supply is cycled. The V_{LOGIC} channel is not affected by the EN function.

The ISL78010 also includes an integrated start-up sequence for V_{LOGIC}, V_{BOOST}, V_{OFF}, then V_{ON} or for V_{LOGIC}, V_{OFF}, V_{BOOST}, and V_{ON}. The latter sequence requires a single external transistor. The timing of the start-up sequence is set using an external capacitor.

The ISL78010 comes in a 32 Ld 5x5 TQFP package and is specified for operation over a -40°C to +105°C temperature range. It is AEC-Q100 rated.

Ordering Information

PART NUMBER (Notes 1, 2, 3)	PART MARKING	PACKAGE (Pb-free)	PKG. DWG. #
ISL78010ANZ	78010 ANZ	32 Ld 5x5 TQFP	Q32.5x5
ISL78010EVAL1Z	Evaluation Board		

1. Add “-T*” suffix for tape and reel. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see product information page for ISL78010. For more information on MSL please see techbrief TB363.

Features

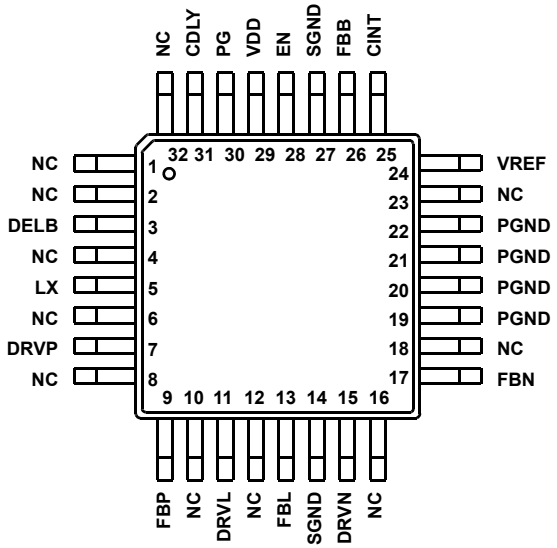
- 2A current FET
- 3V to 5V input
- Up to 20V boost output
- 1% regulation on boost output
- V_{LOGIC}-V_{BOOST}-V_{OFF}-V_{ON} or V_{LOGIC}-V_{OFF}-V_{BOOST}-V_{ON} sequence control
- Programmable sequence delay
- Fully fault protected
- Thermal shutdown
- Internal soft-start
- 32 Ld 5x5 TQFP packages
- AEC-Q100 Tested
- Pb-free (RoHS compliant)

Applications

- All Automotive LCD Displays

Pinout

ISL78010
(32 LD 5x5 TQFP)
TOP VIEW



Absolute Maximum Ratings (T_A = +25°C)

V_{DELB} 24V
V_{DRVP} 36V
V_{DRVN} . . . . . -20V
V_{DD} 6.5V
V_{LX} 24V
V_{DRVL} 6.5V

Thermal Information

Thermal Resistance (Typical) (Notes 4, 5)	Θ_{JA} (°C/W)	Θ_{JC} (°C/W)
32 Ld 5x5 TQFP	71	25

Storage Temperature . . . . . -65°C to +150°C
Power Dissipation . . . . .see “Typical Performance Curves” (page 5)
Maximum Continuous Junction Temperature . . . . . +125°C
Pb-free reflow profile . . . . . .see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

Recommended Operating Conditions

Ambient Operating Temperature . . . . . -40°C to +105°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

4. Θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
5. For Θ_{JC}, the “case temp” location is taken at the package top center.

IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typical values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$.

Electrical Specifications

V_{DD} = 5V, V_{BOOST} = 11V, I_{LOAD} = 200mA, V_{ON} = 15V, V_{OFF} = -5V, V_{LOGIC} = 2.5V, limits over -40°C to +105°C temperature range, unless otherwise specified. **Boldface limits apply over the operating temperature range, -40°C to +105°C.**

PARAMETER	DESCRIPTION	CONDITION	MIN (Note 6)	TYP	MAX (Note 6)	UNIT
SUPPLY						
V_S	Supply Voltage		**3**		**5.5**	V
I_S	Quiescent Current	Enabled, LX not switching		1.7	**2.5**	mA
		Disabled		750	**900**	µA
CLOCK						
f_{OSC}	Oscillator Frequency		**900**	1000	**1100**	kHz
BOOST						
V_{BOOST}	Boost Output Range		**5.5**		**20**	V
V_{FBB}	Boost Feedback Voltage	T_A = +25°C	1.192	1.205	1.218	V
			1.188	1.205	**1.222**	V
V_{F_FBB}	FBB Fault Trip Point			0.9		V
V_{REF}	Reference Voltage	T_A = +25°C	1.19	1.215	1.235	V
			1.187	1.215	**1.238**	V
D_{MAX}	Maximum Duty Cycle		**85**			%
I_{LXMAX}	Current Switch			2.0		A
I_{LEAK}	Switch Leakage Current	V_{LX} = 16V			**10**	µA
$r_{DS(ON)}$	Switch ON-Resistance			320		mΩ
Eff	Boost Efficiency	See “Typical Performance Curves” (page 5)	**85**	92		%
$I(V_{FBB})$	Feedback Input Bias Current	PI mode, V_{FBB} = 1.35V		50	**500**	nA
$\Delta V_{BOOST}/\Delta V_{IN}$	Line Regulation	C_{INT} = 4.7nF, I_{OUT} = 100mA, V_{IN} = 3V to 5.5V		0.05		%/V
$\Delta V_{BOOST}/\Delta I_{BOOST}$	Load Regulation - “P” Mode	C_{INT} pin strapped to V_{DD}, 50mA < I_{LOAD} < 250mA		3		%
$\Delta V_{BOOST}/\Delta I_{BOOST}$	Load Regulation - “PI” Mode	C_{INT} = 4.7nF, 50mA < I_O < 250mA		0.1		%

Electrical Specifications V_{DD} = 5V, V_{BOOST} = 11V, I_{LOAD} = 200mA, V_{ON} = 15V, V_{OFF} = -5V, V_{LOGIC} = 2.5V, limits over -40°C to +105°C temperature range, unless otherwise specified. **Boldface limits apply over the operating temperature range, -40°C to +105°C. (Continued)**

PARAMETER	DESCRIPTION	CONDITION	MIN (Note 6)	TYP	MAX (Note 6)	UNIT
V_{CINT_T}	CINT PI Mode Select Threshold			4.7	**4.8**	V
V_{ON} LDO						
V_{FBP}	FBP Regulation Voltage	I_{DRVP} = 0.2mA, T_A = +25°C	1.176	1.2	1.224	V
		I_{DRVP} = 0.2mA	**1.172**	1.2	**1.228**	V
V_{F_FBP}	FBP Fault Trip Point	V_{FBP} falling	**0.82**	0.87	**0.92**	V
I_{FBP}	FBP Input Bias Current	V_{FBP} = 1.35V	**-250**		**250**	nA
GMP	FBP Effective Transconductance	V_{DRVP} = 25V, I_{DRVP} = 0.2mA to 2mA		50		ms
$\Delta V_{ON}/\Delta I(V_{ON})$	V_{ON} Load Regulation	$I(V_{ON})$ = 0mA to 20mA		-0.5		%
I_{DRVP}	DRVP Sink Current Max	V_{FBP} = 1.1V, V_{DRVP} = 25V	**2**	4		mA
I_{L_DRVP}	DRVP Leakage Current	V_{FBP} = 1.5V, V_{DRVP} = 35V		0.1	**5**	µA
V_{OFF} LDO						
V_{FBN}	FBN Regulation Voltage	I_{DRVN} = 0.2mA, T_A = +25°C	0.173	0.203	0.233	V
		I_{DRVN} = 0.2mA	**0.171**	0.203	**0.235**	V
V_{F_FBN}	FNN Fault Trip Point	V_{FBN} falling	**0.38**	0.43	**0.48**	V
I_{FBN}	FBN Input Bias Current	V_{FBN} = 0.2V	**-250**		**250**	nA
GMN	FBN Effective Transconductance	V_{DRVN} = -6V, I_{DRVN} = 0.2mA to 2mA		50		mS
$\Delta V_{OFF}/\Delta I(V_{OFF})$	V_{OFF} Load Regulation	$I(V_{OFF})$ = 0mA to 20mA		-0.5		%
I_{DRVN}	DRVN Source Current Max	V_{FBN} = 0.3V, V_{DRVN} = -6V	**2**	4		mA
I_{L_DRVN}	DRVN Leakage Current	V_{FBN} = 0V, V_{DRVN} = -20V		0.1	**5**	µA
V_{LOGIC} LDO						
V_{FBL}	FBL Regulation Voltage	I_{DRVL} = 1mA, T_A = +25°C	1.176	1.2	1.224	V
		I_{DRVL} = 1mA	**1.174**	1.2	**1.226**	V
V_{F_FBL}	FBL Fault Trip Point	V_{FBL} falling	**0.82**	0.87	**0.92**	V
I_{FBL}	FBL Input Bias Current	V_{FBL} = 1.35V	**-500**		**500**	nA
G_{ML}	FBL Effective Transconductance	V_{DRVL} = 2.5V, I_{DRVL} = 1mA to 8mA		200		mS
$\Delta V_{LOGIC}/\Delta I(V_{LOGIC})$	V_{LOGIC} Load Regulation	$I(V_{LOGIC})$ = 100mA to 500mA		0.5		%
I_{DRVL}	DRVL Sink Current Max	V_{FBL} = 1.1V, V_{DRVL} = 2.5V	**8**	16		mA
I_{L_DRL}	I_{L_DRVL}	V_{FBL} = 1.5V, V_{DRVL} = 5.5V		0.1	**5**	µA
SEQUENCING						
t_{ON}	Turn On Delay	C_{DLY} = 0.22µF		30		ms
t_{SS}	Soft-start Time	C_{DLY} = 0.22µF		2		ms
t_{DEL1}	Delay Between A_{VDD} and V_{OFF}	C_{DLY} = 0.22µF		10		ms
t_{DEL2}	Delay Between V_{ON} and V_{OFF}	C_{DLY} = 0.22µF		17		ms
I_{DELB}	DELB Pull-down Current	V_{DELB} > 0.6V		50		µA
		V_{DELB} < 0.6V		1.4		mA

Electrical Specifications V_{DD} = 5V, V_{BOOST} = 11V, I_{LOAD} = 200mA, V_{ON} = 15V, V_{OFF} = -5V, V_{LOGIC} = 2.5V, limits over -40°C to +105°C temperature range, unless otherwise specified. **Boldface limits apply over the operating temperature range, -40°C to +105°C. (Continued)**

PARAMETER	DESCRIPTION	CONDITION	MIN (Note 6)	TYP	MAX (Note 6)	UNIT
FAULT DETECTION						
t_{FAULT}	Fault Time Out	C_{DLY} = 0.22µF		50		ms
OT	Over-temperature Threshold			140		°C
I_{PG}	PG Pull-down Current	VPG > 0.6V		15		µA
		VPG < 0.6V		1.7		mA
LOGIC ENABLE						
V_{HI}	Logic High Threshold		**2.3**			V
V_{LO}	Logic Low Threshold				**0.8**	V
I_{LOW}	Logic Low Bias Current			0.2	**2**	µA
I_{HIGH}	Logic High Bias Current	at V_{EN} = 5V	**12**	18	**24**	µA

NOTE:

6. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

Pin Descriptions

PIN NAME	PIN NUMBER	DESCRIPTION
1, 2, 4, 6, 8, 10, 12, 16, 18, 23, 32	NC	Not connected
3	DELB	Open drain output for gate drive of optional V_{BOOST} delay FET
5	LX	Drain of the internal N-Channel boost FET
7	DRVP	Positive LDO base drive; open drain of an internal N-Channel FET
9	FBP	Positive LDO voltage feedback input pin; regulates to 1.2V nominal
11	DRVL	Logic LDO base drive; open drain of an internal N-Channel FET
13	FBL	Logic LDO voltage feedback input pin; regulates to 1.2V nominal
14, 27	SGND	Low noise signal ground
15	DRVN	Negative LDO base drive; open drain of an internal P-Channel FET
17	FBN	Negative LDO voltage feedback input pin; regulates to 0.2V nominal
19, 20, 21, 22	PGND	Power ground, connected to source of internal N-Channel boost FET
24	VREF	Bandgap reference output voltage; bypass with a 0.1µF to SGND
25	CINT	V_{BOOST} integrator output; connect capacitor to SGND for PI-mode or connect to V_{DD} for P-mode operation
26	FBB	Boost regulator voltage feedback input pin; regulates to 1.2V nominal
28	EN	Enable pin; High = Enable; Low or floating = Disable
29	VDD	Positive supply
30	PG	Push-pull gate drive of optional fault protection FET; when chip is disabled or when a fault has been detected, this is high
31	CDLY	A capacitor connected from this pin to SGND sets the delay time for start-up sequence and sets the fault timeout time

Typical Performance Curves T_A = +25°C, unless otherwise specified.

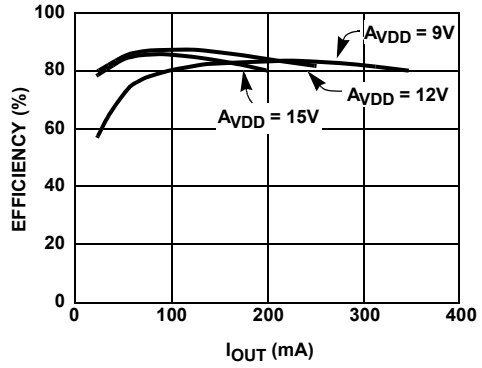


FIGURE 1. V_{BOOST} EFFICIENCY AT V_{IN} = 3V (PI-MODE)

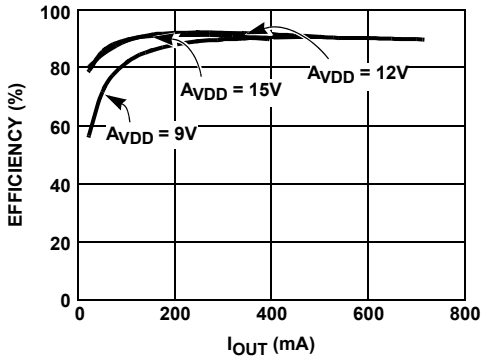


FIGURE 2. V_{BOOST} EFFICIENCY AT V_{IN} = 5V (PI-MODE)

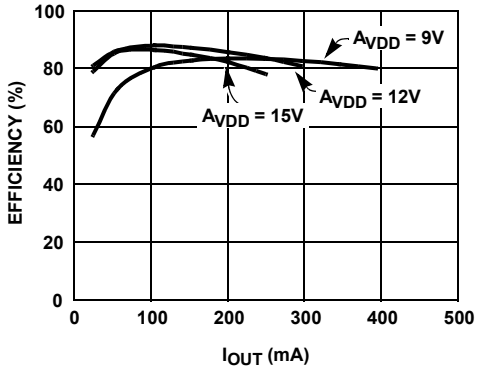


FIGURE 3. V_{BOOST} EFFICIENCY AT V_{IN} = 3V (P-MODE)

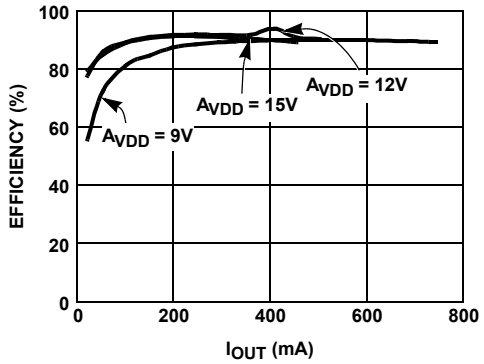


FIGURE 4. V_{BOOST} EFFICIENCY AT V_{IN} = 5V (P-MODE)

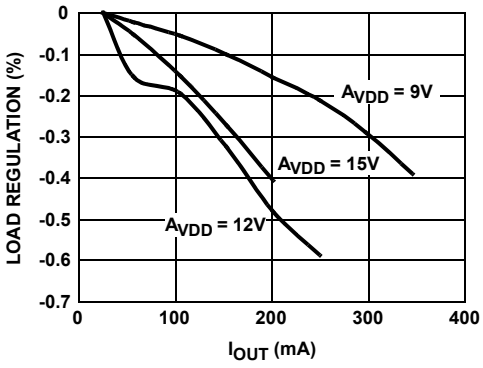


FIGURE 5. V_{BOOST} LOAD REGULATION AT V_{IN} = 3V (PI-MODE)

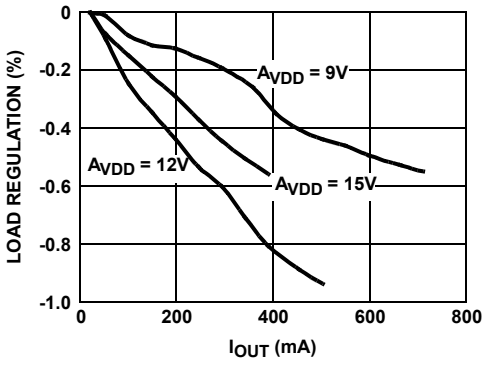


FIGURE 6. V_{BOOST} LOAD REGULATION AT V_{IN} = 5V (PI-MODE)

Typical Performance Curves T_A = +25°C, unless otherwise specified. **(Continued)**

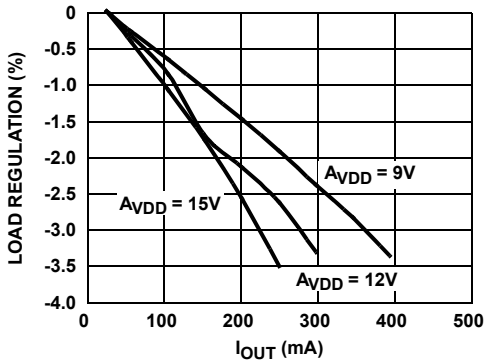


FIGURE 7. V_{BOOST} LOAD REGULATION AT V_{IN} = 3V (P-MODE)

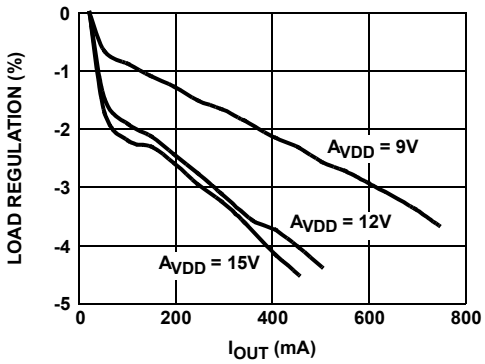


FIGURE 8. V_{BOOST} LOAD REGULATION AT V_{IN} = 5V (P-MODE)

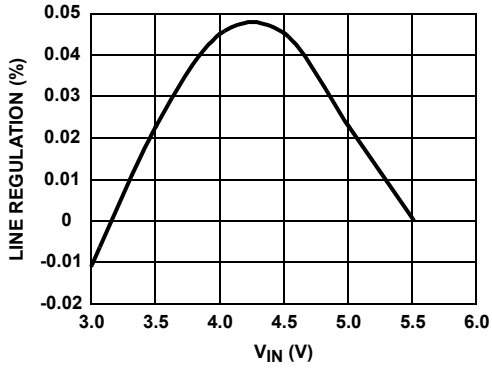


FIGURE 9. V_{BOOST} LINE REGULATION (PI-MODE)

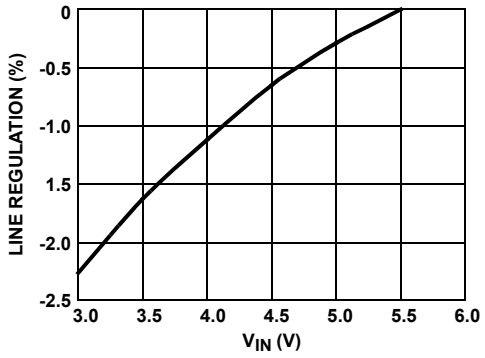


FIGURE 10. V_{BOOST} LINE REGULATION (P-MODE)

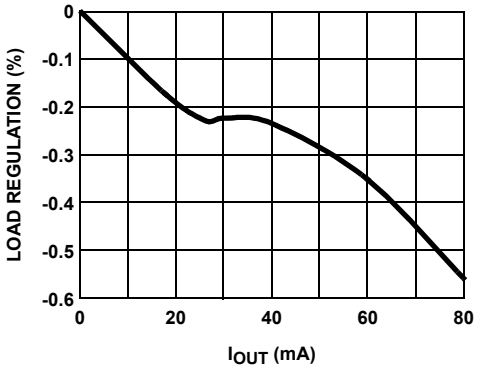


FIGURE 11. V_{ON} LOAD REGULATION

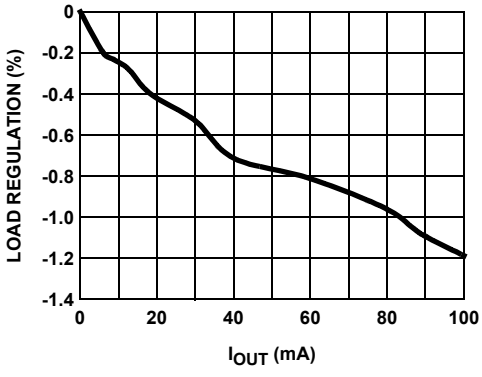


FIGURE 12. V_{OFF} LOAD REGULATION

Typical Performance Curves T_A = +25°C, unless otherwise specified. **(Continued)**

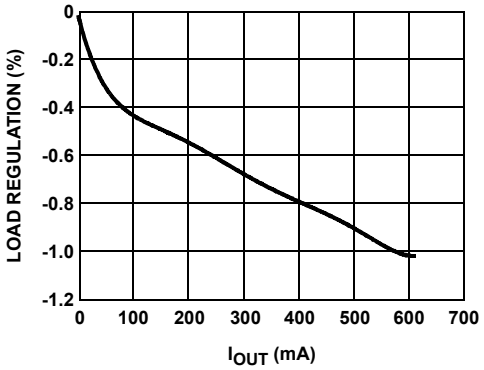


FIGURE 13. V_{LOGIC} LOAD REGULATION

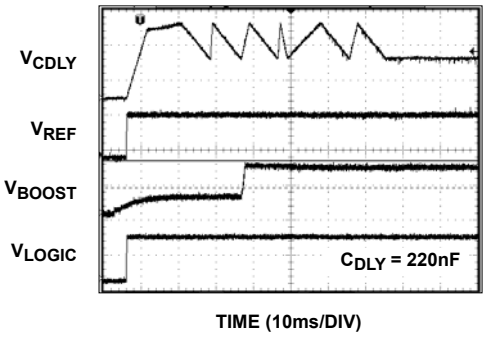


FIGURE 14. START-UP SEQUENCE

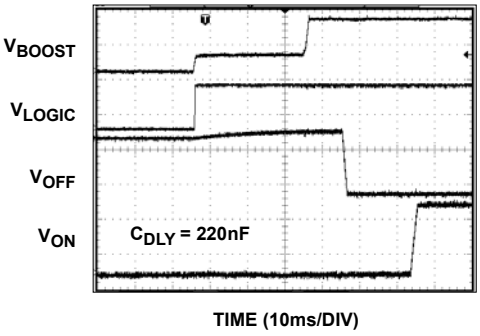


FIGURE 15. START-UP SEQUENCE

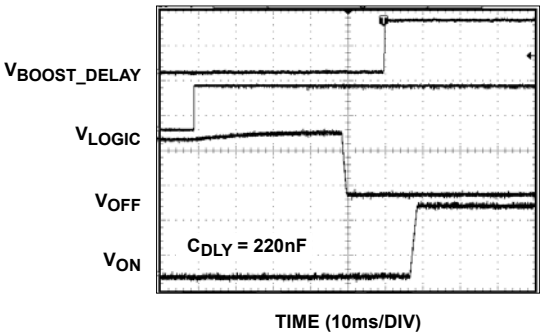


FIGURE 16. START-UP SEQUENCE

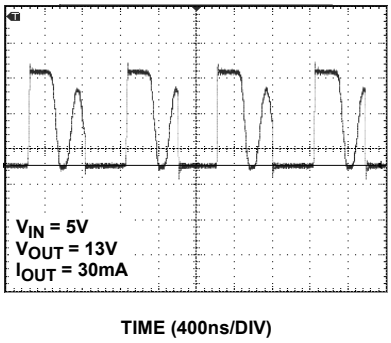


FIGURE 17. LX WAVEFORM - DISCONTINUOUS MODE

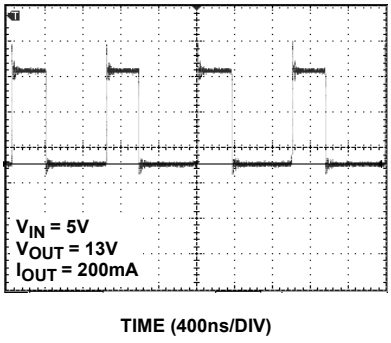


FIGURE 18. LX WAVEFORM - CONTINUOUS MODE

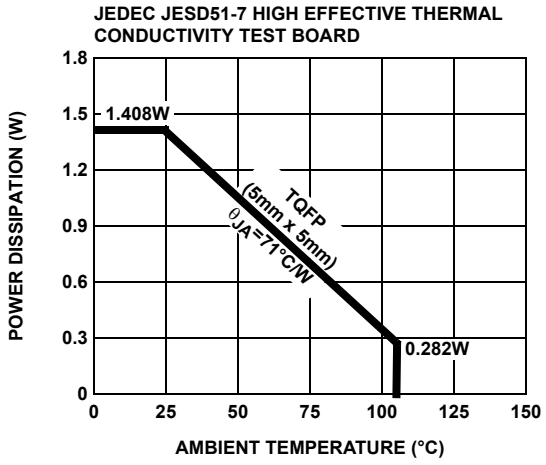


FIGURE 19. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

Applications Information

The ISL78010 provides a highly integrated multiple output power solution for TFT-LCD automotive applications. The system consists of one high efficiency boost converter and three linear-regulator controllers (V_{ON}, V_{OFF}, and V_{LOGIC}) with multiple protection functions. A block diagram is shown in Figure 20. Table 1 lists the recommended components.

The ISL78010 integrates an N-Channel MOSFET boost converter to minimize external component count and cost. The A_{VDD}, V_{ON}, V_{OFF}, and V_{LOGIC} output voltages are independently set using external resistors. V_{ON}, V_{OFF} voltages require external charge pumps which are post regulated using the integrated LDO controllers.

TABLE 1. RECOMMENDED TYPICAL APPLICATION DIAGRAM COMPONENTS

DESIGNATION	DESCRIPTION
C_1, C_2, C_3	10µF, 16V X7R ceramic capacitor (1206) TDK C3216X7RIC106M
C_{20}, C_{31}	4.7µF, 25V X5R ceramic capacitor (1206) TDK C3216X5R1A475K
D_1	1A, 20V low leakage Schottky rectifier (CASE 457-04) ON SEMI MBRM120ET3
D_{11}, D_{12}, D_{21}	200mA, 30V Schottky barrier diode (SOT-23) Fairchild BAT54S
L_1	6.8µH, 1.3A Inductor TDK SLF6025T-6R8M1R3-PF
Q_1	-2.4, -20V P-Channel 1.8V specified PowerTrench MOSFET (SuperSOT-3) Fairchild FDN304P
Q_2	200mA, 40V NPN amplifier (SOT-23) Fairchild MMBT3904
Q_3	200mA, 40V PNP amplifier (SOT-23) Fairchild MMBT3906
Q_4	-2A, -30V single P-Channel logic level PowerTrench MOSFET (SuperSOT-3) Fairchild FDN360P
Q_5	1A, 30V PNP low saturation amplifier (SOT-23) Fairchild FMMT549

Boost Converter

The main boost converter is a current mode PWM converter at a fixed frequency of 1MHz, which enables the use of low profile inductors and multi-layer ceramic capacitors. This results in a compact, low cost power system for LCD panel design.

The ISL78010 is designed for continuous current mode, but it can also operate in discontinuous current mode at light load. In continuous current mode, current flows continuously in the inductor during the entire switching cycle in steady state operation. The voltage conversion ratio in continuous current mode is given by Equation 1:

$$\frac{A_{VDD}}{V_{IN}} = \frac{1}{1-D} \quad \text{(EQ. 1)}$$

where D is the duty cycle of the switching MOSFET.

Figure 21 shows the block diagram of the boost regulator. It uses a summing amplifier architecture consisting of GM stages for voltage feedback, current feedback and slope compensation. A comparator looks at the peak inductor current cycle by cycle and terminates the PWM cycle if the current limit is reached.

An external resistor divider is required to divide the output voltage down to the nominal reference voltage. Current drawn by the resistor network should be limited to maintain the overall converter efficiency. The maximum value of the resistor network is limited by the feedback input bias current and the potential for noise being coupled into the feedback pin. A resistor network in the order of 60kΩ is recommended. The boost converter output voltage is determined by Equation 2:

$$A_{VDD} = \frac{R_1 + R_2}{R_1} \times V_{REF} \quad \text{(EQ. 2)}$$

The current through the MOSFET is limited to 2A peak. This restricts the maximum output current based on Equation 3:

$$I_{OMAX} = \left(I_{LMT} - \frac{\Delta I_L}{2}\right) \times \frac{V_{IN}}{V_O} \quad \text{(EQ. 3)}$$

Where ΔI_L is peak to peak inductor ripple current, and is set by Equation 4:

$$\Delta I_L = \frac{V_{IN}}{L} \times \frac{D}{f_S} \quad \text{(EQ. 4)}$$

where f_S is the switching frequency.

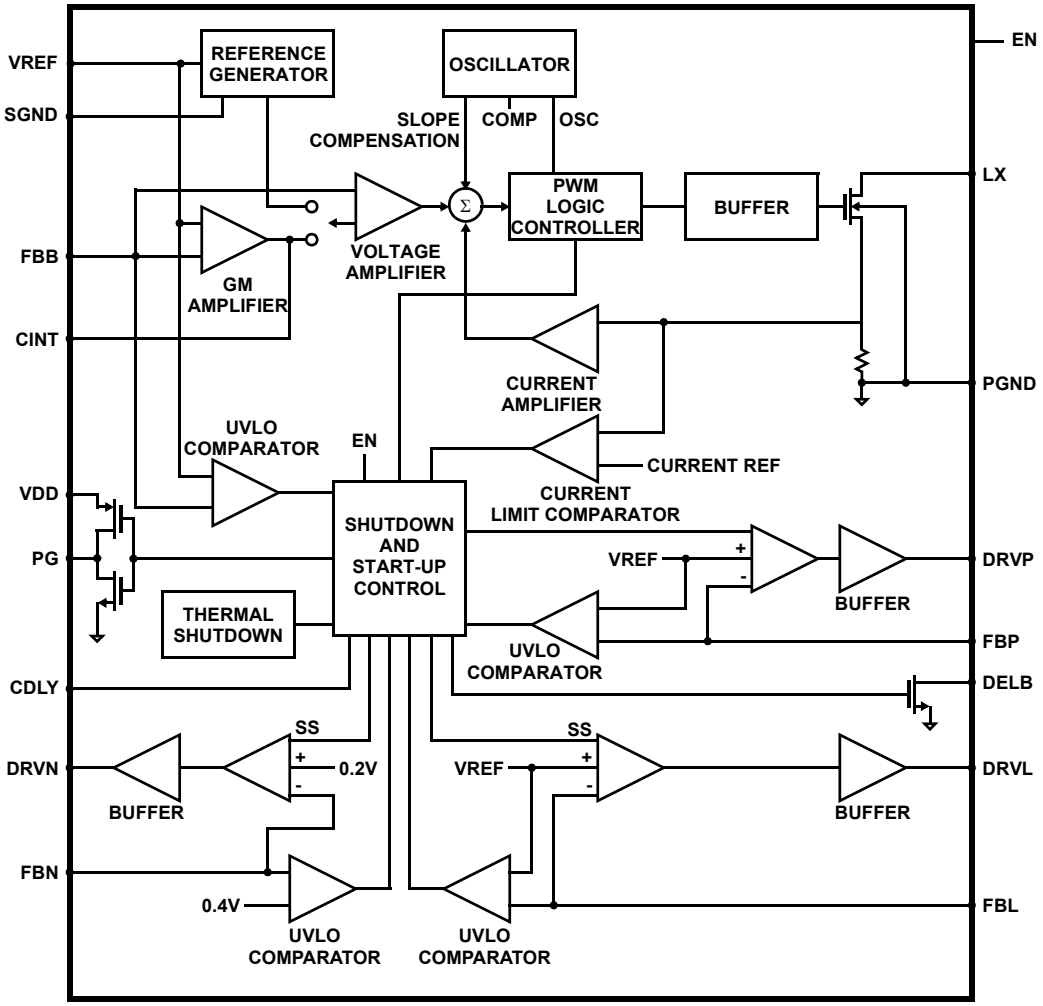


FIGURE 20. BLOCK DIAGRAM

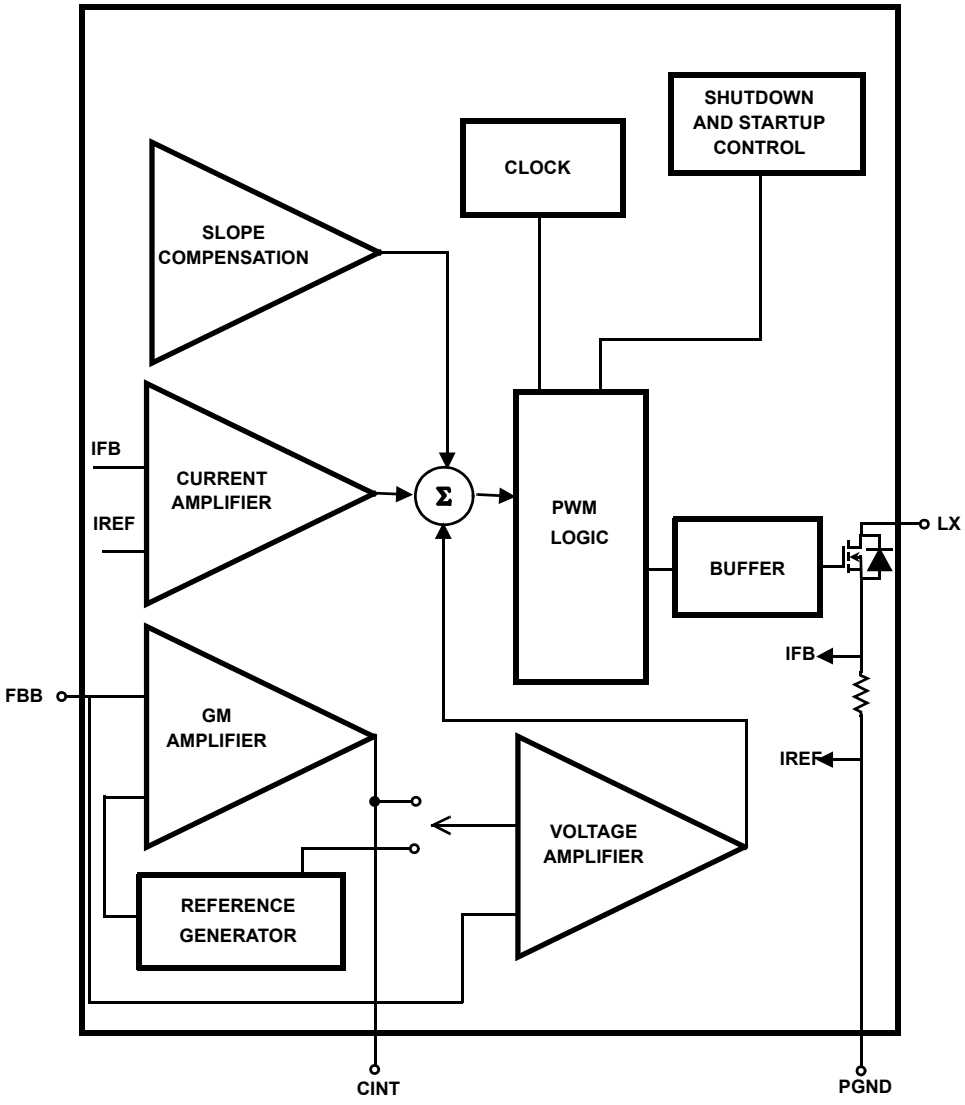


FIGURE 21. BLOCK DIAGRAM OF THE BOOST REGULATOR

Table 2 gives typical values (margins are considered 10%, 3%, 20%, 10%, and 15%) on V_{IN}, V_O, L, f_S, and I_{OMAX}.

TABLE 2. TYPICAL V_{IN}, V_O, L, f_S, AND I_{OMAX} VALUES

V_{IN} (V)	V_O (V)	L (µH)	f_S (MHz)	I_{OMAX} (A)
3.3	9	6.8	1	0.490686
3.3	12	6.8	1	0.307353
3.3	15	6.8	1	0.197353
5	9	6.8	1	0.743464
5	12	6.8	1	0.465686
5	15	6.8	1	0.29902

Input Capacitor

An input capacitor is used to supply the peak charging current to the converter. It is recommended that C_{IN} be larger than 10µF. The reflected ripple voltage will be smaller with larger C_{IN}. The voltage rating of the input capacitor should be larger than the maximum input voltage.

Boost Inductor

The boost inductor is a critical part which influences the output voltage ripple, transient response, and efficiency. Values of 3.3µH to 10µH are to match the internal slope compensation. The inductor must be able to handle the following average (Equation 5) and peak (Equation 6) current:

$$I_{LAVG} = \frac{I_O}{1-D} \quad \text{(EQ. 5)}$$

$$I_{LPK} = I_{LAVG} + \frac{\Delta I_L}{2} \quad \text{(EQ. 6)}$$

Rectifier Diode

A high-speed diode is necessary due to the high switching frequency. Schottky diodes are recommended because of their fast recovery time and low forward voltage. The rectifier diode must meet the output current and peak inductor current requirements.

Output Capacitor

The output capacitor supplies the load directly and reduces the ripple voltage at the output. Output ripple voltage consists of two components: the voltage drop due to the inductor ripple current flowing through the ESR of output capacitor, and the charging and discharging of the output capacitor (Equation 7).

$$V_{RIPPLE} = I_{LPK} \times ESR + \frac{V_O - V_{IN}}{V_O} \times \frac{I_O}{C_{OUT}} \times \frac{1}{f_S} \quad \text{(EQ. 7)}$$

For low ESR ceramic capacitors, the output ripple is dominated by the charging and discharging of the output capacitor. The voltage rating of the output capacitor should be greater than the maximum output voltage.

NOTE: Capacitors have a voltage coefficient that makes their effective capacitance drop as the voltage across them increases. C_{OUT} in Equation 7 assumes the effective value of the capacitor at a particular voltage and not the manufacturer's stated value, measured at zero volts.

Compensation

The ISL78010 can operate in either P-mode or PI-mode. P-mode may be preferred in applications where excellent transient load performance is required but regulation is not critical. Connecting the CINT pin directly to V_{IN} will enable P-mode; for better load regulation, use PI-mode with a 4.7nF capacitor in series with a 10k resistor between CINT and ground. This value may be reduced to improve transient performance; however, very low values will reduce loop stability. Figures 5 through 10 show a comparison of P-mode vs PI-mode performance.

Boost Feedback Resistors

As the boost output voltage, A_{VDD}, is reduced below 12V, the effective voltage feedback in the IC increases the ratio of voltage to current feedback at the summing comparator because R_2 decreases relative to R_1. To maintain stable operation over the complete current range of the IC, the voltage feedback to the FBB pin should be reduced proportionally, as A_{VDD} is reduced. This can be accomplished by means of a series resistor-capacitor network (R_7 and C_7; Equations 8 and 9) in parallel with R_1, with a pole frequency (f_p) set to approximately 10kHz for C_2 (effective) = 10µF and 4kHz for C_2 (effective) = 30µF.

$$R_7 = \left(\left(\frac{1}{0.1 \times R_2}\right) - \frac{1}{R_1}\right)^{-1} \quad \text{(EQ. 8)}$$

$$C_7 = \frac{1}{2 \times 3.142 \times f_p \times R_7} \quad \text{(EQ. 9)}$$

PI-Mode C_{INT} (C_{23}) and R_{INT} (R_{10})

The IC is designed to operate with a minimum C_{23} capacitor of 4.7nF and a minimum C_2 (effective) = 10µF.

Note that, for high voltage A_{VDD}, the voltage coefficient of ceramic capacitors (C_2) reduces their effective capacitance greatly; a 16V, 10µF ceramic can drop to around 3µF at 15V.

To improve the transient load response of A_{VDD} in PI-mode, a resistor may be added in series with the C_{23} capacitor. The larger the resistor, the lower the overshoot, but at the expense of stability of the converter loop, especially at high currents.

With L = 10µH, A_{VDD} = 15V, and C_{23} = 4.7nF, C_2 (effective) should have a capacitance of greater than 10µF. R_{INT} (R_7) can have values up to 5kΩ for C_2 (effective) up to 20µF and up to 10k for C_2 (effective) up to 30µF.

Larger values of R_{INT} (R_7) may be possible if maximum A_{VDD} load currents less than the current limit are used. To ensure A_{VDD} stability, the IC should be operated at the maximum desired current and then the transient load response of A_{VDD} should be used to determine the maximum value of R_{INT}.

Operation of the DELB Output Function

An open drain DELB output is provided to allow the boost output voltage, developed at C_2 (see "Typical Application Diagram" on page 18), to be delayed via an external switch (Q_4) to a time after the V_{BOOST} supply and negative V_{OFF} charge pump supply have achieved regulation during the start-up sequence shown in Figures 14 and 16. This then allows the A_{VDD} and V_{ON} supplies to start-up from 0V instead of the normal offset voltage of V_{IN}-V_{DIODE} (D_1) if Q_4 were not present.

When DELB is activated by the start-up sequencer, it sinks 50µA, allowing a controlled turn-on of Q_4 and charge-up of C_9. C_{16} can be used to control the turn-on time of Q_4 to reduce in-rush current into C_9. The potential divider formed by R_9 and R_8 can be used to limit the V_{GS} voltage of Q_4 if required by the voltage rating of this device. When the voltage at DELB falls to less than 0.6V, the sink current is increased to ~1.2mA to firmly pull DELB to 0V.

The voltage at DELB is monitored by the fault protection circuit so that if the initial 50µA sink current fails to pull DELB below ~0.6V after the start-up sequencing has completed, then a fault condition will be detected and a fault time-out ramp will be initiated on the C_{DEL} capacitor (C_7).

Operation of the PG Output Function

The PG output consists of an internal pull-up PMOS device to V_{IN}, to turn off the external Q_1 protection switch, and a current-limited pull-down NMOS device which sinks ~15µA, allowing a controlled turn-on of Q_1 gate capacitance. C_O is used to control how fast Q_1 turns on and limiting inrush current into C_1. When the voltage at the PG pin falls to less than 0.6V, the PG sink current is increased to ~1.2mA to firmly pull the pin to 0V.

The voltage at PG is monitored by the fault protection circuit so that if the initial 15µA sink current fails to pull PG below ~0.6V after the start-up sequencing has completed, then a fault condition will be detected, and a fault time-out ramp will be initiated on the C_{DEL} capacitor (C_7).

Cascaded MOSFET Application

A 20V N-Channel MOSFET is integrated in the boost regulator. For applications where the output voltage is greater than 20V, an external cascaded MOSFET is needed as shown in Figure 22. The voltage rating of the external MOSFET should be greater than V_{BOOST}.

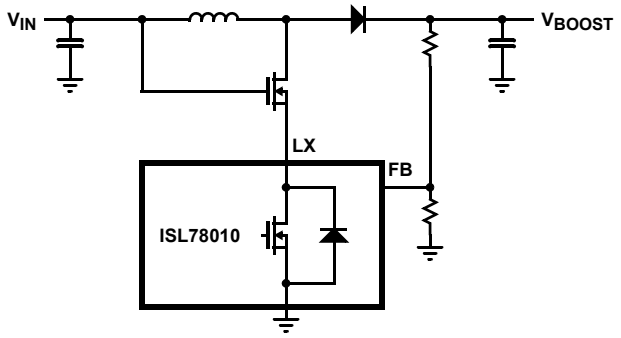


FIGURE 22. CASCADED MOSFET TOPOLOGY FOR HIGH OUTPUT VOLTAGE APPLICATIONS

Linear-Regulator Controllers (V_{ON}, V_{LOGIC}, and V_{OFF})

The ISL78010 includes three independent linear-regulator controllers, in which two are positive output voltage (V_{ON} and V_{LOGIC}) and one is negative. The V_{ON}, V_{OFF}, and V_{LOGIC} linear-regulator controller functional diagrams are shown in Figures 23, 24, and 25, respectively.

Calculation of the Linear Regulator Base-Emitter Resistors (R_{BL}, R_{BP} and R_{BN})

For the pass transistor of the linear regulator, low frequency gain (h_{FE}) and unity gain frequency (f_T) are usually specified in the datasheet. The pass transistor adds a pole to the loop transfer function at $f_p = f_T/h_{FE}$. Therefore, in order to maintain phase margin at low frequency, the best choice for a pass device is often a high-frequency, low-gain switching transistor. Further improvement can be obtained by adding a base-emitter resistor R_{BE} (R_{BP}, R_{BL}, R_{BN} in the Functional Block Diagrams on page 13), which increase the pole frequency to $f_p = f_T*(1+ h_{FE} *re/R_{BE})/h_{FE}$, where re = KT/qIc. Choose the lowest value R_{BE} in the design as long as there is still enough base current (I_B) to support the maximum output current (I_C).

For example, if in the V_{LOGIC} linear regulator, a Fairchild FMMT549 PNP transistor is used as the external pass transistor (Q_5 in the application diagram), then for a maximum V_{LOGIC} operating requirement of 500mA, the data sheet indicates h_{FE}(min) = 100.

The base-emitter saturation voltage is Vbe_max = 1.25V. Note that this is normally Vbe ~ 0.7V; however, for the Q_5 transistor, an internal Darlington arrangement is used to increase its current gain, giving a "base-emitter" voltage of 2 x V_{BE}.

Note also that using a high current Darlington PNP transistor for Q_5 requires that $V_{IN} > V_{LOGIC} + 2V$. Should a lower input voltage be required, then an ordinary high-gain PNP transistor should be selected for Q_5 to allow a lower collector-emitter saturation voltage.

For the ISL78010, the minimum drive current is as shown in Equation 10:

$$I_{DRVL}(min) = 8mA \quad \text{(EQ. 10)}$$

The minimum base-emitter resistor, R_{BL}, can now be calculated as shown in Equation 11:

$$R_{BL}(min) = V_{BE}(max)/(I_{DRVL}(min) - I_C/h_{FE}(min)) = 1.25V/(8mA - 500mA/100) = 417\Omega \quad \text{(EQ. 11)}$$

This is the minimum value that can be used. Choose a convenient value greater than this minimum value; for example, 500Ω. Larger values may be used to reduce quiescent current; however, regulation may be adversely affected by supply noise if the value of R_{BL} is too high.

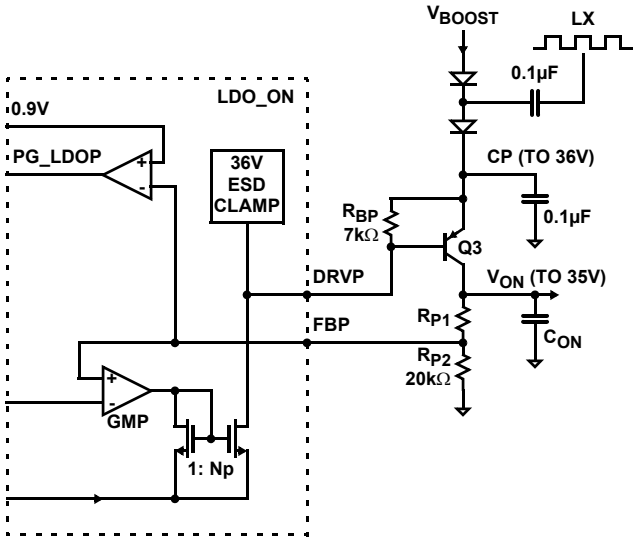


FIGURE 23. V_{ON} FUNCTIONAL BLOCK DIAGRAM

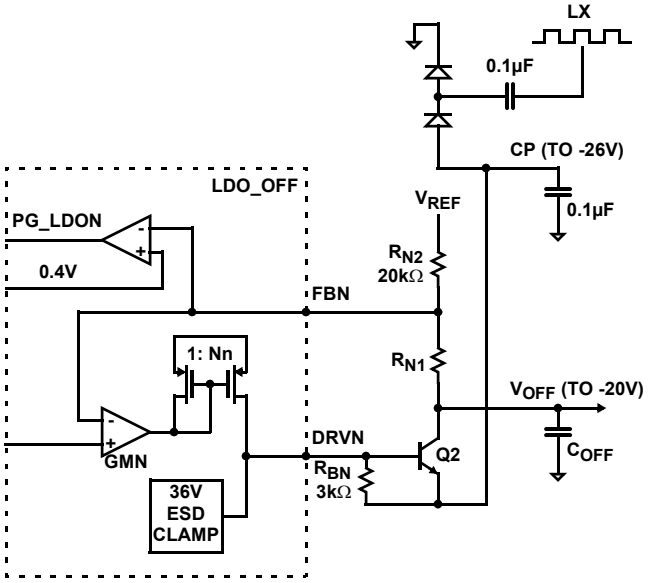


FIGURE 24. V_{OFF} FUNCTIONAL BLOCK DIAGRAM

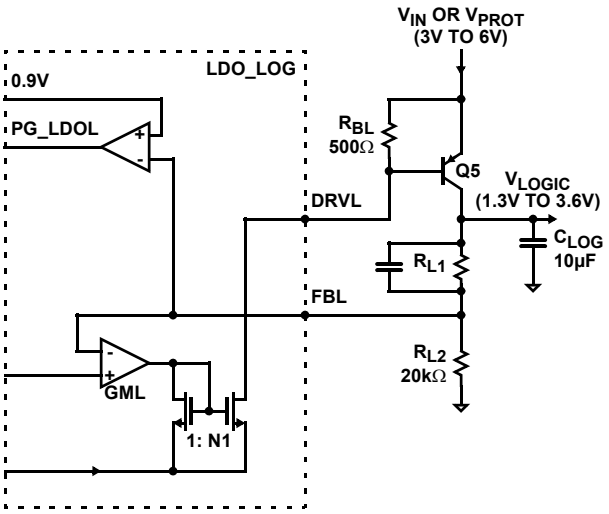


FIGURE 25. V_{LOGIC} FUNCTIONAL BLOCK DIAGRAM

The V_{ON} power supply is used to power the positive supply of the row driver in the LCD panel. The DC/DC consists of an external diode-capacitor charge pump powered from the inductor (LX) of the boost converter, followed by a low dropout linear regulator (LDO_ON). The LDO_ON regulator uses an external PNP transistor as the pass element. The on-board LDO controller is a wide band (>10MHz) transconductance amplifier capable of 4mA drive current, which is sufficient for up to 40mA or more output current under the low dropout condition (forced beta of 10). Typical V_{ON} voltage supported by the ISL78010 ranges from +15V to +36V. A fault comparator is also included for monitoring the output voltage. The undervoltage threshold is set at 25% below the 1.2V reference.

The V_{OFF} power supply is used to power the negative supply of the row driver in the LCD panel. The DC/DC consists of an external diode-capacitor charge pump powered from the inductor (LX) of the boost converter, followed by a low dropout linear regulator (LDO_OFF). The LDO_OFF regulator uses an external NPN transistor as the pass element. The on-board LDO controller is a wide band (>10MHz) transconductance amplifier capable of 4mA drive current, which is sufficient for up to 40mA or more output current under the low dropout condition (forced beta of 10). Typical V_{OFF} voltage supported by the ISL78010 ranges from -5V to -20V. A fault comparator is also included for monitoring the output voltage. The undervoltage threshold is set at 200mV above the 0.2V reference level.

The V_{LOGIC} power supply is used to power the logic circuitry within the LCD panel. The DC/DC may be powered directly from the low voltage input, 3.3V or 5.0V, or it may be powered through the fault protection switch. The LDO_LOGIC regulator uses an external PNP transistor as the pass element. The on-board LDO controller is a wide band (>10MHz) transconductance amplifier capable of 16mA drive current, which is sufficient for up to 160mA or more output current under the low dropout condition (forced beta of 10). Typical

V_{LOGIC} voltage supported by the ISL78010 ranges from +1.3V to V_{DD} - 0.2V. A fault comparator is also included for monitoring the output voltage. The undervoltage threshold is set at 25% below the 1.2V reference.

Set-Up Output Voltage

As shown in the “Typical Application Diagram” on page 18, the output voltages of V_{ON}, V_{OFF}, and V_{LOGIC} are as determined by Equations 12, 13 and 14:

$$V_{ON} = V_{REF} \times \left(1 + \frac{R_{12}}{R_{11}}\right) \quad \text{(EQ. 12)}$$

$$V_{OFF} = V_{REFN} + \frac{R_{22}}{R_{21}} \times (V_{REFN} - V_{REF}) \quad \text{(EQ. 13)}$$

$$V_{LOGIC} = V_{REF} \times \left(1 + \frac{R_{42}}{R_{41}}\right) \quad \text{(EQ. 14)}$$

where V_{REF} = 1.2V and V_{REFN} = 0.2V.

Resistor networks in the order of 250kΩ, 120kΩ and 10kΩ are recommended for V_{ON}, V_{OFF} and V_{LOGIC}, respectively.

Charge Pump

To generate an output voltage higher than V_{BOOST}, single or multiple stages of charge pumps are needed. The number of stages is determined by the input and output voltage. Use Equation 15 to calculate positive charge pump stages:

$$N_{POSITIVE} \geq \frac{V_{OUT} + V_{CE} - V_{INPUT}}{V_{INPUT} - 2 \times V_F} \quad \text{(EQ. 15)}$$

where V_{CE} is the dropout voltage of the pass component of the linear regulator. It ranges from 0.3V to 1V depending on the transistor. V_F is the forward-voltage of the charge pump rectifier diode.

The number of negative charge pump stages is given by Equation 16:

$$N_{NEGATIVE} \geq \frac{|V_{OUTPUT}| + V_{CE}}{V_{INPUT} - 2 \times V_F} \quad \text{(EQ. 16)}$$

To achieve high efficiency and low material cost, the lowest number of charge pump stages that can meet the above requirements is preferred.

High Charge Pump Output Voltage (>36V) Applications

In applications where the charge pump output voltage is over 36V, an external NPN transistor must be inserted between the DRVP pin and the base of pass transistor Q_3 as shown in Figure 26, or the linear regulator can control only one stage charge pump and regulate the final charge pump output as shown in Figure 27.

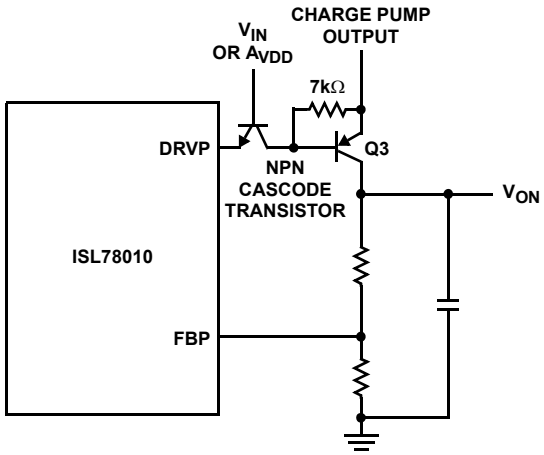


FIGURE 26. CASCODE NPN TRANSISTOR CONFIGURATION FOR HIGH CHARGE PUMP OUTPUT VOLTAGE (>36V)

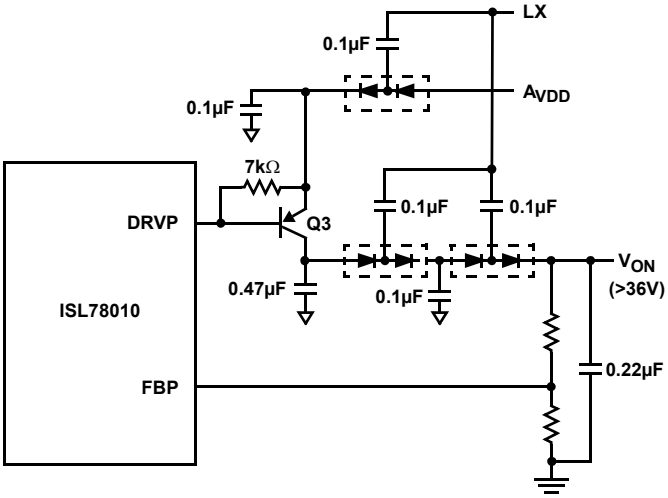


FIGURE 27. THE LINEAR REGULATOR CONTROLS ONE STAGE OF CHARGE PUMP

Discontinuous/Continuous Boost Operation and its Effect on the Charge Pumps

The ISL78010 V_{ON} and V_{OFF} architecture uses LX switching edges to drive diode charge pumps from which LDO regulators generate the V_{ON} and V_{OFF} supplies. Should a regular supply of LX switching edges be interrupted - for example, during discontinuous operation at light A_{VDD} boost load currents - it may affect the performance of V_{ON} and V_{OFF} regulation, depending on their exact loading conditions at the time.

To optimize V_{ON}/V_{OFF} regulation, the boundary of discontinuous/continuous operation of the boost converter can be adjusted, by suitable choice of inductor (given V_{IN}, V_{OUT}, switching frequency and the A_{VDD} current loading), to be in continuous operation.

Equation 17 gives the boundary between discontinuous and continuous boost operation. Continuous operation (LX switching every clock cycle) requires:

$$\frac{I_{AVDD}(load) > D \times (1 - D) \times V_{IN}}{2 \times L \times f_{OSC}} \quad \text{(EQ. 17)}$$

where the duty cycle, $D = (A_{VDD} - V_{IN})/A_{VDD}$

For example, with V_{IN} = 5V, f_{OSC} = 1.0MHz and A_{VDD} = 12V, continuous operation of the boost converter can be guaranteed as shown in Equations 18, 19, and 20:

$$L = 10\mu H \text{ and } I_{AVDD} > 61mA \quad \text{(EQ. 18)}$$

$$L = 6.8\mu H \text{ and } I_{AVDD} > 89mA \quad \text{(EQ. 19)}$$

$$L = 3.3\mu H \text{ and } I_{AVDD} > 184mA \quad \text{(EQ. 20)}$$

Charge Pump Output Capacitors

Ceramic capacitors with low ESR are recommended. With ceramic capacitors, the output ripple voltage is dominated by the capacitance value. The capacitance value can be calculated as shown in Equation 21:

$$C_{OUT} \geq \frac{I_{OUT}}{2 \times V_{RIPPLE} \times f_{OSC}} \quad \text{(EQ. 21)}$$

where f_{OSC} is the switching frequency.

Start-Up Sequence

Figure 28 shows a detailed start-up sequence waveform. For a successful power-up, there should be six peaks at V_{CDLY}. When a fault is detected, the device will latch off until either EN is toggled or the input supply is recycled.

When the input voltage is higher than 2.5V, an internal current source starts to charge C_{CDLY} to an upper threshold using a fast ramp followed by a slow ramp. During the initial slow ramp, the device checks whether there is a fault condition. If no fault is found, C_{CDLY} is discharged after the first peak, and V_{REF} turns on.

During the second ramp, the device checks the status of V_{REF} and over-temperature. At the peak of the second ramp, PG output goes low and enables the input protection PMOS Q_1. Q_1 is a controlled FET used to prevent in-rush current into V_{BOOST} before V_{BOOST} is enabled internally. Its rate of turn-on is controlled by C_o. When a fault is detected, M1 will turn off and disconnect the inductor from V_{IN}.

With the input protection FET on, NODE1 (see “Typical Application Diagram” on page 18) will rise to ~V_{IN}. Initially the boost is not enabled, so V_{BOOST} rises to V_{IN}-V_{DIODE} through the output diode. Hence, there is a step at V_{BOOST} during this part of the start-up sequence. If this step is not desirable, an external P-MOSFET can be used to delay the output until the boost is enabled internally. The delayed output appears at A_{VDD}.

V_{BOOST} soft-starts at the beginning of the third ramp. The soft-start ramp depends on the value of the C_{DLY} capacitor. For C_{DLY} of 220nF, the soft-start time is ~2ms.

V_{REF} and V_{LOGIC} turn on when input voltage (V_{DD}) exceeds 2.5V. When a fault is detected, the outputs and the input protection will turn off but V_{REF} will stay on.

V_{OFF} turns on at the start of the fourth peak. At the fifth peak, the open drain o/p DELB goes low to turn on the external PMOS Q_4 to generate a delayed V_{BOOST} output.

V_{ON} is enabled at the beginning of the sixth ramp. A_{VDD}, PG, V_{OFF}, DELB and V_{ON} are checked at end of this ramp.

Fault Protection

During the start-up sequence, prior to BOOST soft-start, V_{REF} is checked to be within ±20% of its final value, and the device temperature is checked. If either of these is not within the expected range, the part is disabled until the power is recycled or EN is toggled.

If C_{DELAY} is shorted low, then the sequence will not start, while if C_{DELAY} is shorted H, the first down ramp will not occur and the sequence will not complete.

Once the start-up sequence is completed, the chip continuously monitors C_{DLY}, DELB, FBP, FBL, FBN, V_{REF}, FBB, and PG, and checks for faults. During this time, the voltage on the C_{DLY} capacitor remains at 1.15V until either a fault is detected or the EN pin is pulled low.

A fault on C_{DELAY}, V_{REF}, or temperature will shut down the chip immediately. If a fault on any other output is detected, C_{DELAY} will ramp up linearly with a 5µA (typical) current to the upper fault threshold (typically 2.4V), at which point the chip is disabled until the power is recycled or EN is toggled. If the fault condition is removed prior to the end of the ramp, the voltage on the C_{DLY} capacitor returns to 1.15V.

Typical fault thresholds for FBP, FBL, FBN, and FBB are included in the “Electrical Specifications” table beginning on page 2. PG and DELB fault thresholds are typically 0.6V.

C_{INT} has an internal current-limited clamp to keep the voltage within its normal range. If C_{INT} is shorted low, the boost regulator will attempt to regulate to 0V. If C_{INT} is shorted H, the regulator switches to P mode.

If any of the regulated outputs (V_{BOOST}, V_{ON}, V_{OFF} or V_{LOGIC}) are driven above their target levels, the drive circuitry will switch off until the output returns to its expected value.

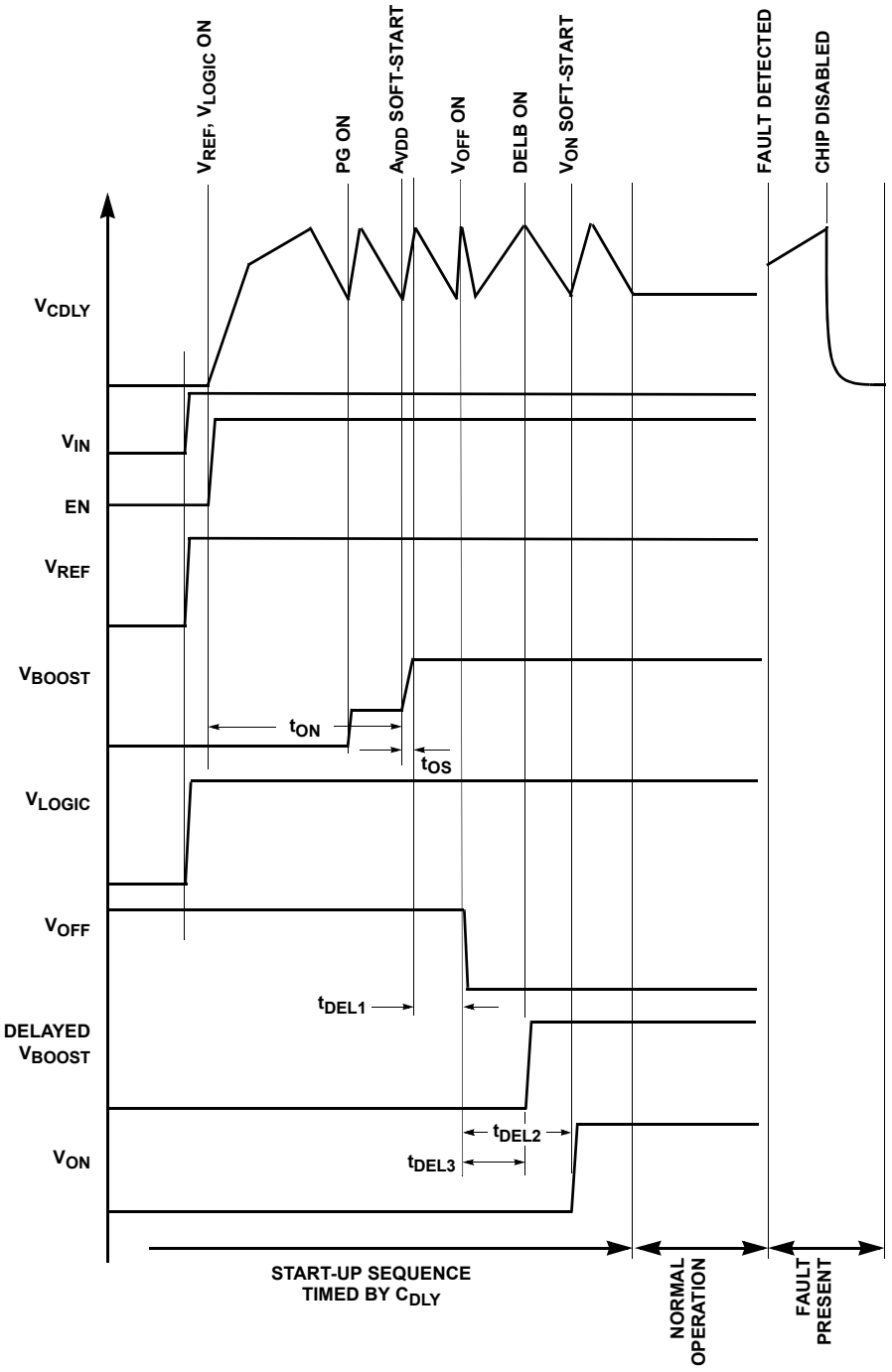


FIGURE 28. START-UP SEQUENCE

If V_{BOOST} is excessively loaded, the current limit will prevent damage to the chip. While in current limit, the part acts like a current source, and the regulated output will drop. If the output drops below the fault threshold, a ramp will be initiated on C_{DELAY} and, provided the fault is sustained, the chip will be disabled upon completion of the ramp.

In some circumstances (depending on ambient temperature and thermal design of the board), continuous operation at current limit may result in the over-temperature threshold being exceeded, which will cause the part to disable immediately.

All I/O also has ESD protection, which in many cases will also provide overvoltage protection relative to either ground or VDD. However, these will not generally operate unless absolute maximum ratings are exceeded.

Component Selection for Start-Up Sequencing and Fault Protection

The C_{REF} capacitor is typically set at 220nF and is required to stabilize the V_{REF} output. The range of C_{REF} is from 22nF to 1µF and should not be more than five times the capacitor on C_{DEL} to ensure correct start-up operation.

The C_{DEL} capacitor is typically 220nF and has a usable range from 47nF minimum to several microfarads. It is limited only by leakage in the capacitor reaching µA levels.

C_{DEL} should be at least 1/5 of the value of C_{REF}. Note that with 220nF on C_{DEL} the fault time-out will typically be 50ms, and the use of a larger or smaller value will vary this time proportionally (e.g., 1µF will give a fault time-out period of typically 230ms).

Fault Sequencing

The ISL78010 has advanced fault detection systems which protect the IC from both adjacent pin shorts during operation and shorts on the output supplies.

A high-quality layout and design of the PCB with respect to grounding and decoupling is necessary to avoid falsely triggering the fault detection scheme, especially during start-up. See “Layout Recommendation” on page 17 and “Component Selection for Start-Up Sequencing and Fault Protection” on page 17 to avoid problems during initial evaluation and prototype PCB generation.

Over-Temperature Protection

An internal temperature sensor continuously monitors the die temperature. If the die temperature exceeds the thermal trip point of +140°C, the device will shut down.

Layout Recommendation

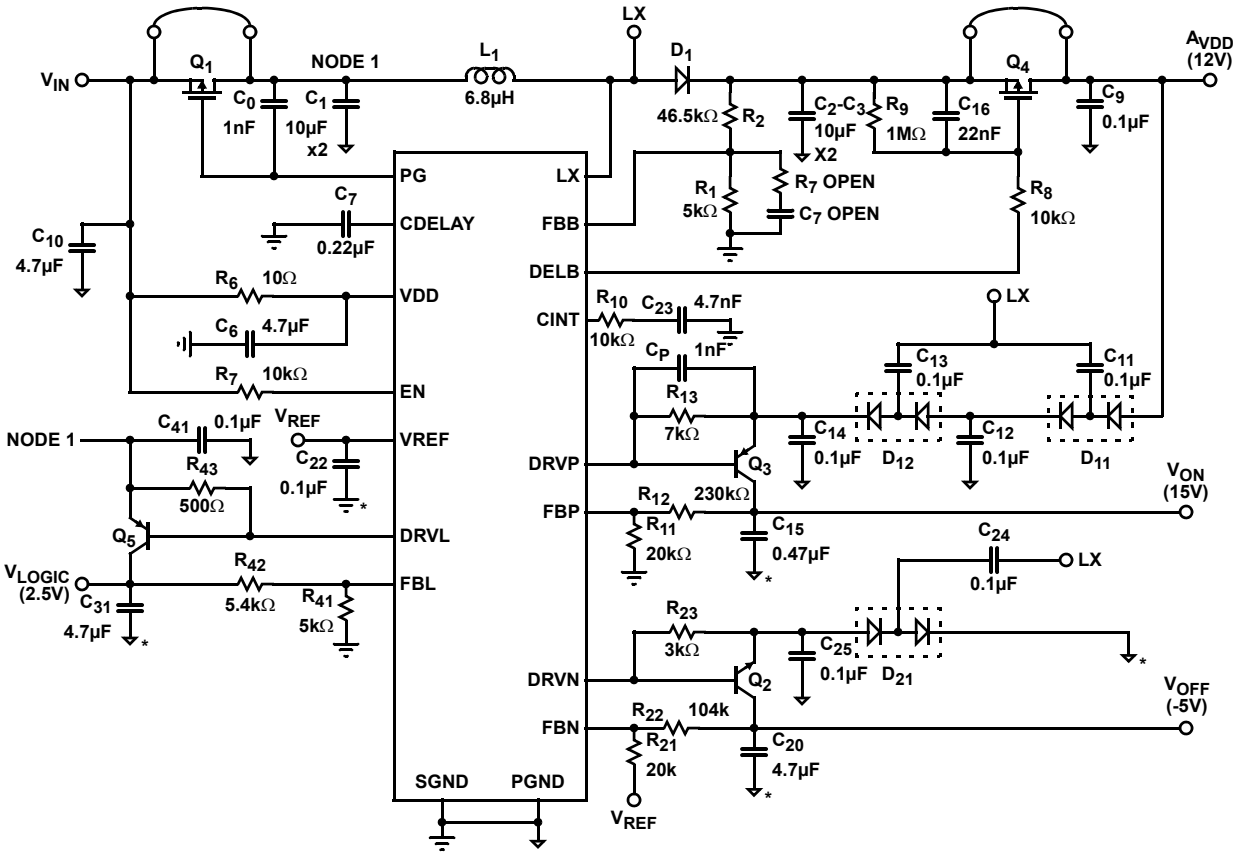
Device performance, including efficiency, output noise, transient response and control loop stability, is dramatically affected by the PCB layout. PCB layout is critical, especially at high switching frequency.

Some general guidelines for layout include:

1. Place the external power components (the input capacitors, output capacitors, boost inductor and output diodes, etc.) in close proximity to the device. Traces to these components should be kept as short and wide as possible to minimize parasitic inductance and resistance.
2. Place V_{REF} and V_{DD} bypass capacitors close to the pins.
3. Minimize the length of traces carrying fast signals and high current.
4. All feedback networks should sense the output voltage directly from the point of load, and be as far away from LX node as possible.
5. The power ground (PGND) and signal ground (SGND) pins should be connected at only one point near the main decoupling capacitors.
6. A signal ground plane, separate from the power ground plane, should be used for ground return connections for feedback resistor networks (R_1, R_{11}, R_{41}) and the V_{REF} capacitor, C_{22}; the C_{DELAY} capacitor, C_7; and the integrator capacitor, C_{23}.
7. Minimize feedback input track lengths to avoid switching noise pickup.
8. Connect all "NC" pins to the ground plane to improve thermal performance and switching noise immunity between pins.

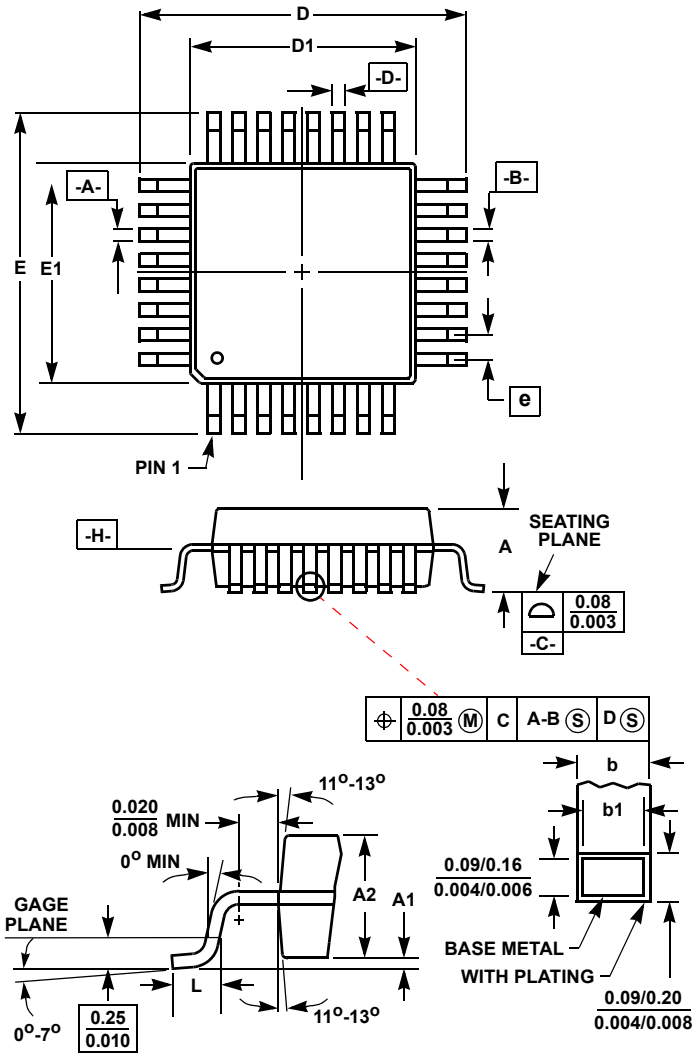
An evaluation board, ISL78010EVAL1Z, is available to illustrate the proper layout implementation. See “Ordering Information” on page 1.

Typical Application Diagram



NOTE: SGND should be connected to PGND at one point only.

Thin Plastic Quad Flatpack Packages (TQFP)



Q32.5x5 (JEDEC MS-026AAA ISSUE B)
32 LEAD THIN PLASTIC QUAD FLATPACK PACKAGE

SYMBOL	MILLIMETERS		NOTES
	MIN	MAX	
A	-	1.20	-
A1	0.05	0.15	-
A2	0.95	1.05	-
b	0.17	0.27	6
b1	0.17	0.23	-
D	6.90	7.10	3
D1	4.90	5.10	4, 5
E	6.90	7.10	3
E1	4.90	5.10	4, 5
L	0.45	0.75	-
N	32		7
e	0.50 BSC		-

Rev. 0 2/07

NOTES:

1. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.
2. All dimensions and tolerances per ANSI Y14.5M-1982.
3. Dimensions D and E to be determined at seating plane -C-.
4. Dimensions D1 and E1 to be determined at datum plane -H-.
5. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25mm (0.010 inch) per side.
6. Dimension b does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum b dimension by more than 0.08mm (0.003 inch).
7. “N” is the number of terminal positions.

Общество с ограниченной ответственностью «МосЧип» ИНН 7719860671 / КПП 771901001
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Данный компонент на территории Российской Федерации

Вы можете приобрести в компании MosChip.

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http://moschip.ru/get-element

Вы можете разместить у нас заказ для любого Вашего проекта, будь то серийное производство или разработка единичного прибора.

В нашем ассортименте представлены ведущие мировые производители активных и пассивных электронных компонентов.

Нашей специализацией является поставка электронной компонентной базы двойного назначения, продукции таких производителей как XILINX, Intel (ex.ALTERA), Vicor, Microchip, Texas Instruments, Analog Devices, Mini-Circuits, Amphenol, Glenair.

Сотрудничество с глобальными дистрибьюторами электронных компонентов, предоставляет возможность заказывать и получать с международных складов практически любой перечень компонентов в оптимальные для Вас сроки.

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