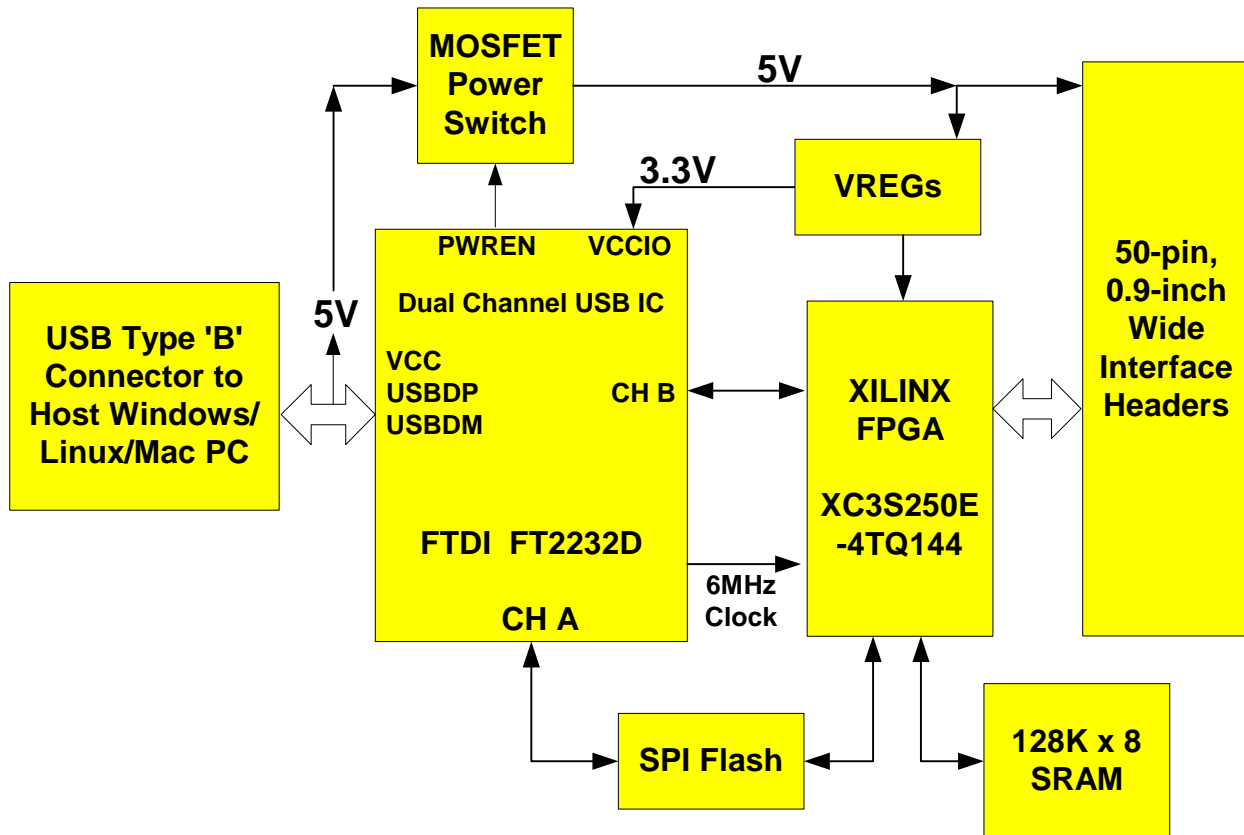




## USB - FPGA MODULE



### APPLICATIONS:

- Rapid Prototyping
- Educational Tool
- Industrial/Process Control

### FEATURES:

- Training Manual/Tutorial Available
- Built-In Configuration Loader—Writes Bit File Directly to SPI Flash via Full-Speed USB Interface
- 40 I/O Channels: 27 Input/Output; 13 Input Only
- Xilinx XC3S250E-4TQ144 FPGA
- On-Board 128K x 8, 70nS SRAM
- USB Port Powered
- USB 1.1 and 2.0 Compatible Interface
- Small Footprint: 2.8 x 1.-Inch PCB
- Standard 50-Pin, 0.9-Inch DIP Interface

## 1.0 INTRODUCTION

The DLP-FPGA Module is a low-cost, compact prototyping module that can be used for rapid proof of concept or for educational environments. The module is based on the Xilinx Spartan 3E and Future Technology Devices International's FT2232D Dual-Channel USB IC. Used by itself or with the optional 200-page training manual, the DLP-FPGA provides both the beginner as well as the experienced engineer with a rapid path to developing FPGA-based designs. When combined with the free WebPACK™ Tools from Xilinx, this module is more than sufficient for creating anything from basic logical functions to a highly complex system controller.

As a bonus feature, one channel of the dual-channel USB interface is used to load user bit files directly to the SPI Flash—no external programmer is required. This represents a savings of as much as \$200 in that no additional programming cable is required for configuring the FPGA. All that is needed to load bit files to the DLP-FPGA is a Windows software utility (free with purchase), a Windows PC and a USB cable. The module can also be programmed from within the Xilinx ISE tool environment using a Xilinx programming cable (purchased separately).

The DLP-FPGA is fully compatible with the free ISE™ WebPACK™ tools from Xilinx. ISE WebPACK offers the ideal development environment for FPGA designs with HDL synthesis and simulation, implementation, device fitting and JTAG programming.

The DLP-FPGA has on-board voltage regulators that generate all required power supply voltages from a single 5-volt source. Power for the module can be taken from either the host USB port or from a user-supplied, external 5-volt power supply.

Connection to user electronics is made via a 50-pin, 0.9-inch wide, industry-standard 0.025 square inch post DIP header. Other on-board features include a 128K x 8 static RAM IC for user projects, and both JTAG and SPI Flash interface ports for connection to Xilinx programming tools.

## 2.0 TRAINING MANUAL

A 200+ page training manual for the DLP-FPGA is also available. While this manual is designed to provide entry-level instruction for those new to designing with FPGAs, it is recommended for developers who have some experience with FPGA products and associated development tools. An ISE™ WebPACK™ Software installation DVD is included with the manual.

The manual is comprised of 5 Chapters and 4 Labs as outlined below:

**Chapter 1:** Installing the Xilinx ISE WebPACK tools and Understanding the Design Flow

**Chapter 2:** Lab 1: Implementing a Simple AND Gate: Create a New Project, Implement the Design, View the Synthesized Design, View the Placed and Routed Design

**Chapter 3:** Lab 2: Heartbeat: Understanding the Digital Clock Manager (DCM), Methods of Starting ISE Project Navigator, VHDL Module Structure, Utilizing Hierarchy, Adding the DCM Component, Adding the Heartbeat Component, Connecting the Components, Synthesizing the Design Using XST, Simulating the Design Using the ISE Simulator, Adding the User Constraint File, Implementing the Design, Download the Design to the FPGA

**Chapter 4:** Lab 3: Memory Test: Block Diagram, DCM Design, SRAM State Machine, Bi-Directional Buffers, Test Failed Indicator, User Constraint File, Synthesize the Memory Test Design, Simulate the Memory Test Design, Implementing the Design, Download the Design to the FPGA

**Chapter 5:** Lab 4: USB Loopback: Initial Design, USB State Machine Module, Language Template, Bi-Directional Buffers, Synthesize, Simulate, Pin Constraints, Implement, Download the Design to the FPGA

(The completed design files for each lab are available for download from the DLP Design website upon purchase of the DLP-FPGA and Lab Manual.)

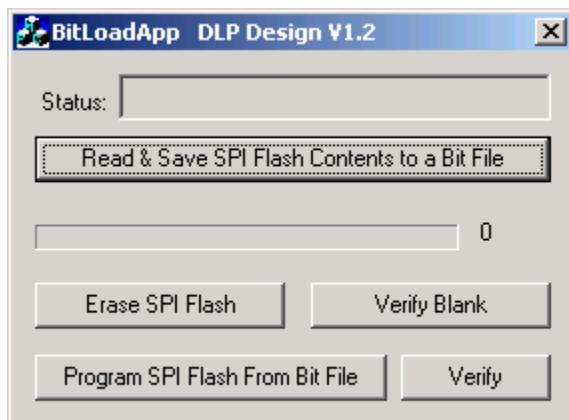
### 3.0 FPGA SPECIFICATIONS

The FPGA device used on the DLP-FPGA is the Xilinx Spartan 3E: XC3S250E-4TQ144.

- Part Number: XC3S250E
- System Gates: 250K
- Equivalent Logic Cells: 5,508
  
- CLB Array
  - Rows: 34
  - Columns: 26
  - Total CLB's: 612
  - Total Slices: 2,448
  
- Distributed RAM Bits: 38K
- Block RAM Bits: 216K
- Dedicated Multipliers: 12
- DCM's: 4

### 4.0 BITLOADAPP SOFTWARE

Windows software is provided for use with the DLP-FPGA that will load an FPGA configuration (.bit) file directly to the SPI Flash device via the USB interface. This app (shown below) will allow the user to erase the flash, verify the erasure and then program and verify the flash:



## 5.0 JTAG INTERFACE

The easiest way to load an FPGA configuration (bit file) to the FPGA is to run the BitLoadApp software, then select and program a file from the local hard drive directly to the SPI flash. Once written to the SPI flash, the configuration will load to the FPGA and execute. Alternatively, a traditional JTAG header location is provided on the DLP-FPGA giving the user access to the pins on the FPGA required by the development tools. (Refer to the schematic at the end of this datasheet for details.)

## 6.0 EEPROM SETUP / MPROG

The DLP-FPGA has a dual-channel USB interface to the host PC. Channel A is used exclusively to load an FPGA configuration (bit file) to the SPI flash. This configuration data is automatically transferred to the FPGA when power is applied to the module. Channel B is used for communication between the FPGA and host PC at run time. A 93C56B EEPROM connected to the USB interface IC is used to store the setup for the two channels. The parameters stored in the EEPROM include the Vendor ID (VID), Product ID (PID), Serial Number, Description String, driver selection (VCP or D2XX) and port type (UART serial or FIFO parallel).

As mentioned above, Channel A is used exclusively for loading the FPGA's configuration to the SPI flash, and Channel B is used for communication between the host PC and the DLP-FPGA. As such, the D2XX drivers and FIFO mode must be selected in the EEPROM for Channel A. Channel B must use the FIFO mode, but can use either the VCP or D2XX drivers. The VCP drivers make the DLP-FPGA appear as an RS232 port to the host app. The D2XX drivers provide faster throughput, but require working with a .lib or .dll library in the host app.

The operational modes and other EEPROM selections are written to the EEPROM using the MPROG utility. This utility and its manual are available for download from the bottom of the page at [www.dlpdesign.com](http://www.dlpdesign.com).

## 7.0 TEST BIT FILE

A test file is provided as a download from the DLP Design website that provides rudimentary access to the I/O features of the DLP-FPGA.

The following features are provided:

- Ping
- Read the High/Low State of the Input-Only Pins
- Drive I/O Pins High/Low or Read their High/Low State
- Simple Loopback on Channel B
- Simple Read/Write of Each Address in the SRAM

This bit file is available from the DLP-FPGA's download page.

## 8.0 USB DRIVERS

USB drivers for the following operating systems are available for download from the DLP Design website at <http://www.dlpdesign.com>:

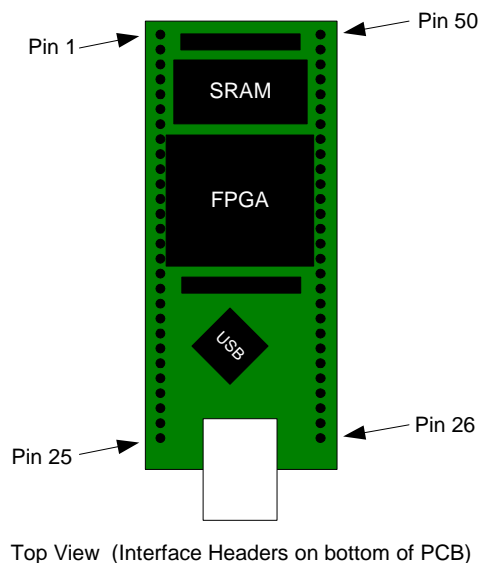
|                            |                |
|----------------------------|----------------|
| <b>Windows XP x64</b>      | <b>Mac OSX</b> |
| <b>Windows Server 2003</b> | <b>Mac OS9</b> |
| <b>Windows 2000</b>        | <b>Mac OS8</b> |
| <b>Windows 98, ME</b>      | <b>Linux</b>   |

### Notes:

1. The bit file load utility only runs on the Windows platforms.
2. The bit file load utility requires the use of USB channel A, and channel A is dedicated to this function.
3. If you are using the dual-mode drivers from FTDI (CDM2.02.04) and wish to use the Virtual COM Port (VCP) drivers for Channel B communications, then it may be necessary to disable the D2XX drivers first via Device Manager. To do so, right click on the Channel B entry under USB Controllers that appears when the DLP-FPGA is connected, select Properties, select the Advanced tab, check the option for "Load VCP" and click OK. Once you unplug and then replug the DLP-FPGA, a COM port should appear in Device Manager under Ports (COM & LPT).

## 9.0 USING THE DLP-FPGA

Select a power source via Header Pins 23 and 24, and connect the DLP-FPGA to the PC to initiate the loading of USB drivers. The easiest way to do this is to connect Pins 23 and 24 to each other. This will result in operational power being taken from the host PC. Once the drivers are loaded, the DLP-FPGA is ready for use.

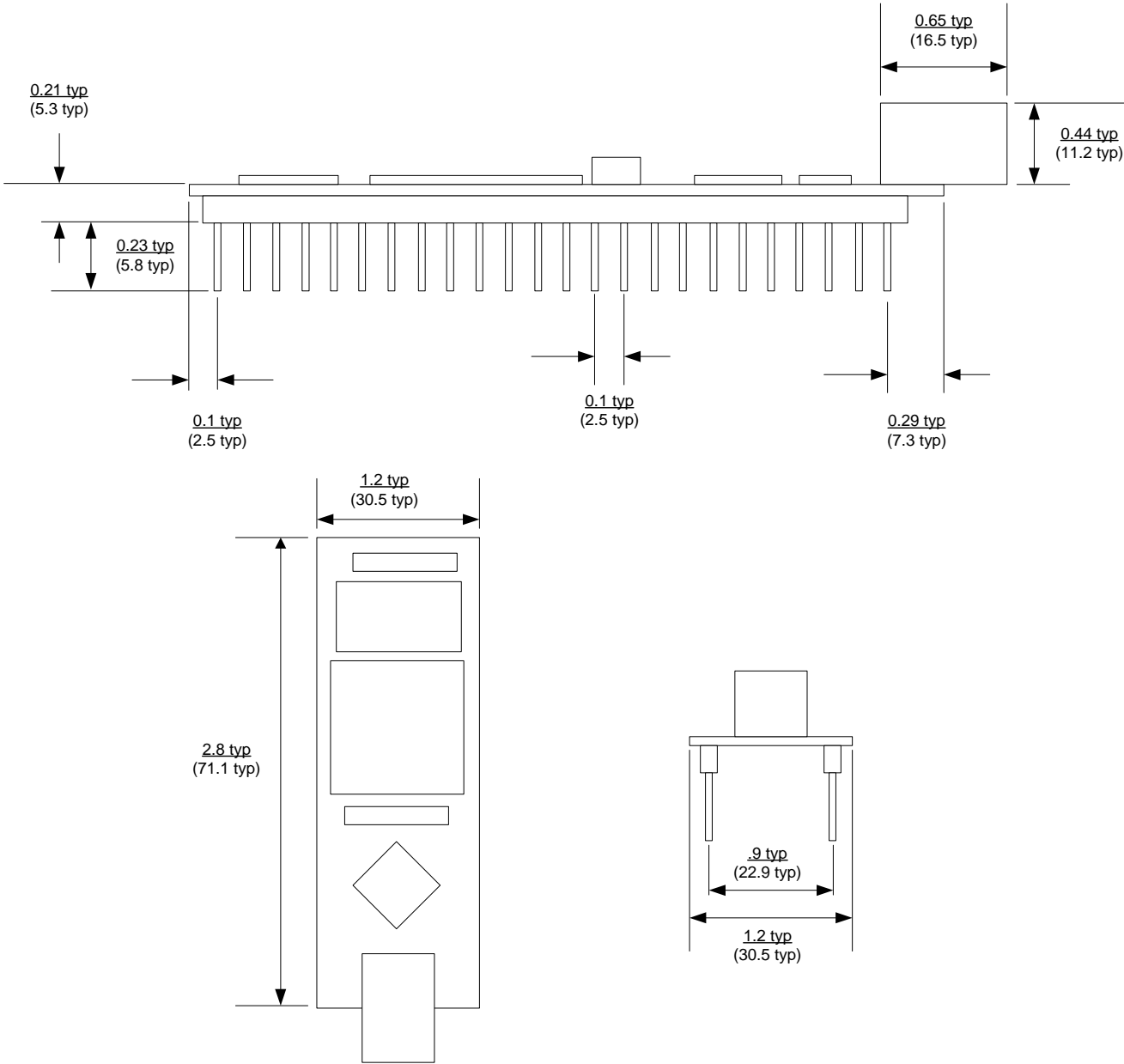


## TABLE 1

| NN (dec)*             | NN (hex)*           | Name   | FPGA Pin   | JP2 Pin          |
|-----------------------|---------------------|--|------------|------------------|
| 0                     | 0                   | user_io(0)   | U5 Pin 58  | JP2 Pin 2        |
| 1                     | 1                   | user_io(1)   | U5 Pin 59  | JP2 Pin 4        |
| 2                     | 2                   | user_io(2)   | U5 Pin 93  | JP2 Pin 5        |
| 3                     | 3                   | user_io(3)   | U5 Pin 94  | JP2 Pin 6        |
| 4                     | 4                   | user_io(4)   | U5 Pin 96  | JP2 Pin 7        |
| 5                     | 5                   | user_io(5)   | U5 Pin 97  | JP2 Pin 8        |
| 6                     | 6                   | user_io(6)   | U5 Pin 103 | JP2 Pin 9        |
| 7                     | 7                   | user_io(7)   | U5 Pin 104 | JP2 Pin 10       |
| 8                     | 8                   | user_io(8)   | U5 Pin 105 | JP2 Pin 12       |
| 9                     | 9                   | user_io(9)   | U5 Pin 106 | JP2 Pin 13       |
| 10                    | A                   | user_io(10)  | U5 Pin 112 | JP2 Pin 14       |
| 11                    | B                   | user_io(11)  | U5 Pin 113 | JP2 Pin 15       |
| 12                    | C                   | user_io(12)  | U5 Pin 116 | JP2 Pin 16       |
| 13                    | D                   | user_io(13)  | U5 Pin 117 | JP2 Pin 17       |
| 14                    | E                   | user_in(14) [INPUT ONLY!]  | U5 Pin 119 | JP2 Pin 18       |
| 15                    | F                   | user_in(15) [INPUT ONLY!]  | U5 Pin 120 | JP2 Pin 19       |
| 16                    | 10                  | user_io(16)  | U5 Pin 122 | JP2 Pin 20       |
| 17                    | 11                  | user_io(17)  | U5 Pin 123 | JP2 Pin 21       |
| 18                    | 12                  | user_io(18)  | U5 Pin 124 | JP2 Pin 22       |
| 19                    | 13                  | user_io(19)  | U5 Pin 125 | JP2 Pin 27       |
| 20                    | 14                  | user_io(20)  | U5 Pin 126 | JP2 Pin 29       |
| 21                    | 15                  | user_io(21)  | U5 Pin 130 | JP2 Pin 30       |
| 22                    | 16                  | user_io(22)  | U5 Pin 131 | JP2 Pin 31       |
| 23                    | 17                  | user_io(23)  | U5 Pin 132 | JP2 Pin 32       |
| 24                    | 18                  | user_io(24)  | U5 Pin 134 | JP2 Pin 33       |
| 25                    | 19                  | user_io(25)  | U5 Pin 135 | JP2 Pin 34       |
| 26                    | 1A                  | user_io(26)  | U5 Pin 139 | JP2 Pin 35       |
| 27                    | 1B                  | user_io(27)  | U5 Pin 140 | JP2 Pin 36       |
| 28                    | 1C                  | user_io(28)  | U5 Pin 142 | JP2 Pin 37       |
| 30                    | 1E                  | user_in(0)   | U5 Pin 10  | JP2 Pin 49       |
| 31                    | 1F                  | user_in(1)   | U5 Pin 12  | JP2 Pin 48       |
| 32                    | 20                  | user_in(2)   | U5 Pin 29  | JP2 Pin 47       |
| 33                    | 21                  | user_in(3)   | U5 Pin 31  | JP2 Pin 46       |
| 34                    | 22                  | user_in(4)   | U5 Pin 36  | JP2 Pin 45       |
| 35                    | 23                  | user_in(5)   | U5 Pin 38  | JP2 Pin 44       |
| 36                    | 24                  | user_in(6)   | U5 Pin 41  | JP2 Pin 43       |
| 37                    | 25                  | user_in(7)   | U5 Pin 47  | JP2 Pin 42       |
| 38                    | 26                  | user_in(8)   | U5 Pin 48  | JP2 Pin 41       |
| 39                    | 27                  | user_in(9)   | U5 Pin 66  | JP2 Pin 39       |
| 40                    | 28                  | user_in(10)  | U5 Pin 69  | JP2 Pin 38       |
| Read: 29,<br>>40      | Read: 1D,<br>>29    | Returns Read Pin Error E4  | n/a        | n/a              |
| Write: 14,<br>15, >30 | Write: E, F,<br>>1E | Returns Write Pin Error E2 for Pin Clear (low), or E3 for Pin Set (high) | n/a        | n/a              |
|                       |                     | Ground   |            | 1,11,25,26,40,50 |
|                       |                     | FPGA_RESET   | 128        | 3                |
|                       |                     | 5VIN – Module power source   |            | 23               |
|                       |                     | PORTVCC – Power from Host PC   |            | 24               |
|                       |                     | VCCSW – 5V power after host enumerates the USB port                      |            | 28               |

\***Note:** This is the I/O number for use with the Test Bit File described in Section 7.

# 10.0 MECHANICAL DIMENSIONS IN INCHES (MM) (PRELIMINARY)



## 11.0 DISCLAIMER

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This document provides preliminary information that may be subject to change without notice.

## 12.0 CONTACT INFORMATION

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Allen, TX 75013

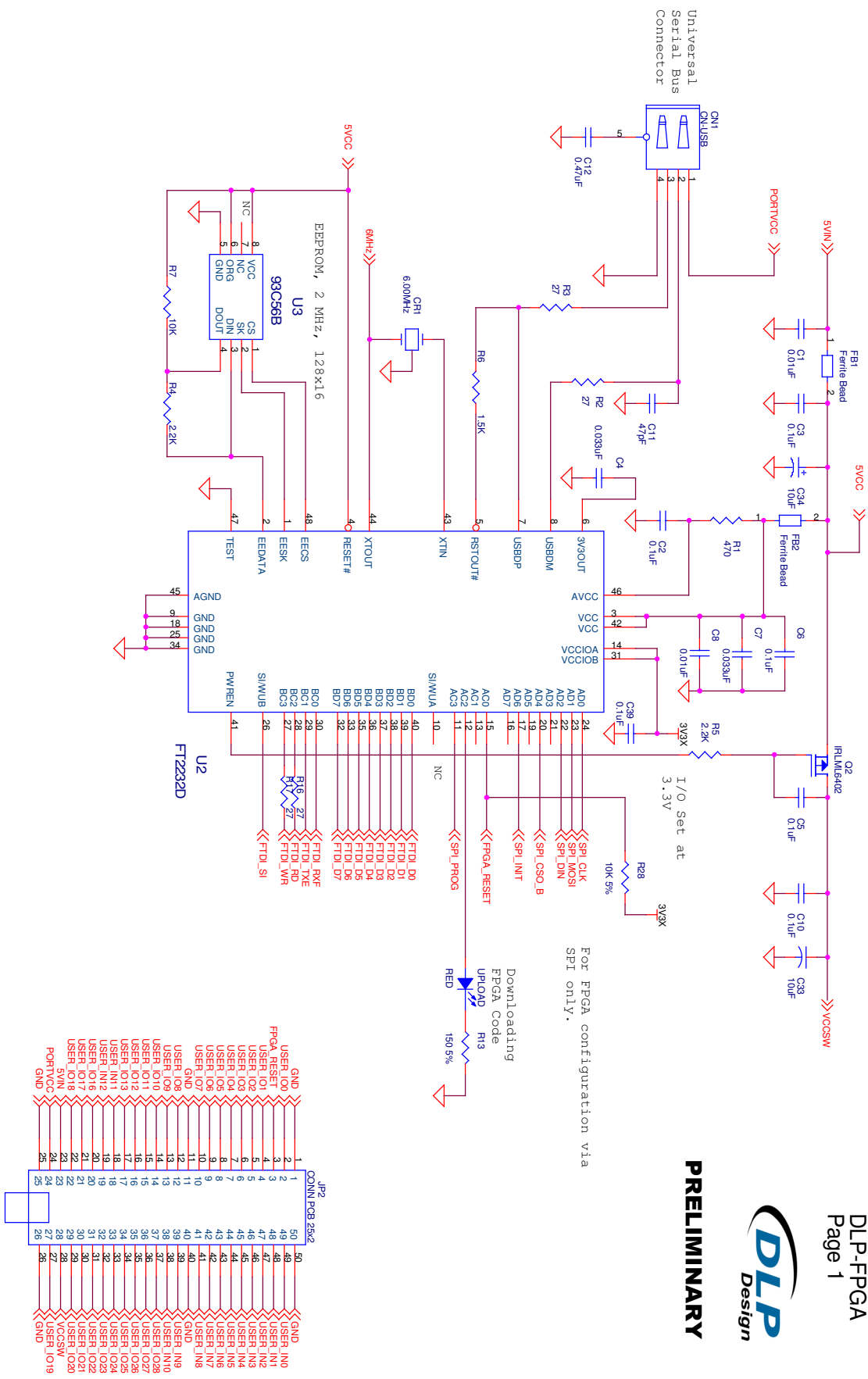
Phone: 469-964-8027  
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Email Sales: [sales@dlpdesign.com](mailto:sales@dlpdesign.com)  
Email Support: [support@dlpdesign.com](mailto:support@dlpdesign.com)  
Website URL: <http://www.dlpdesign.com>





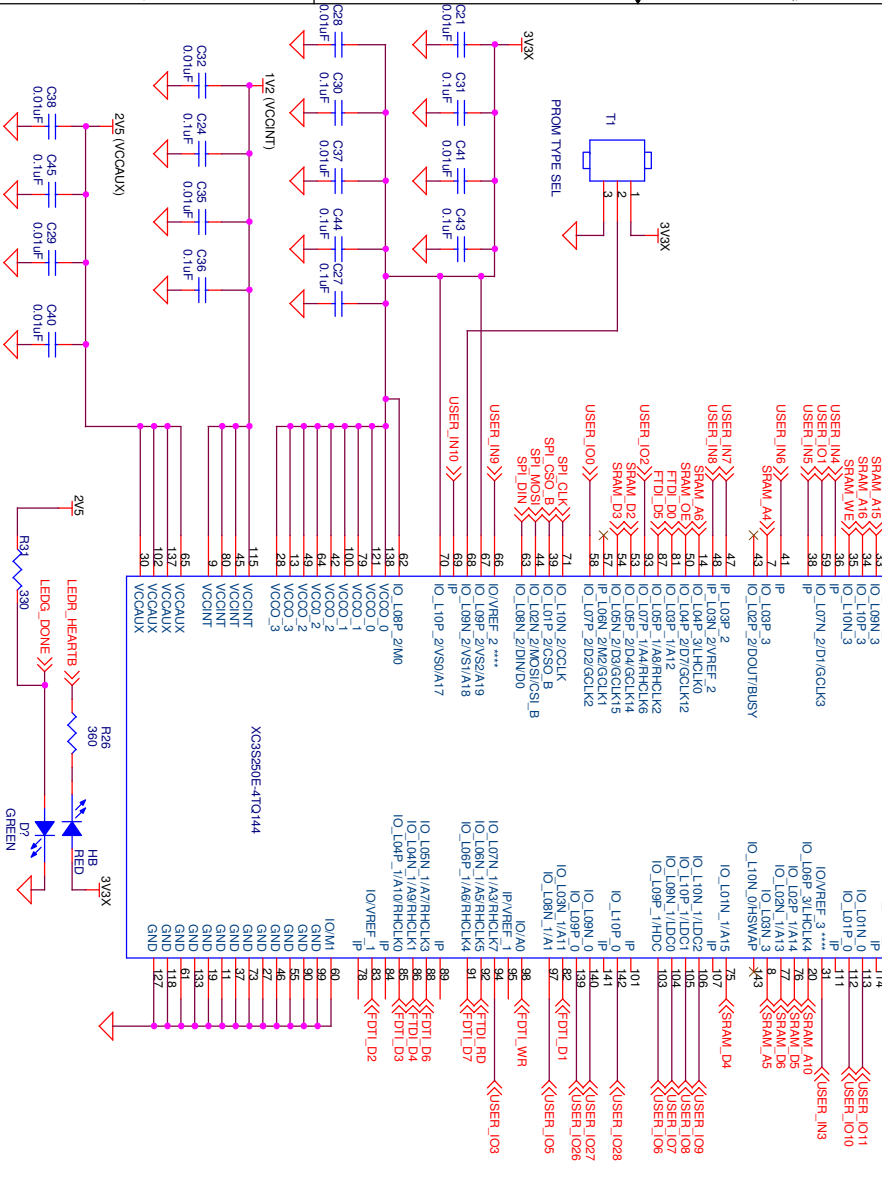
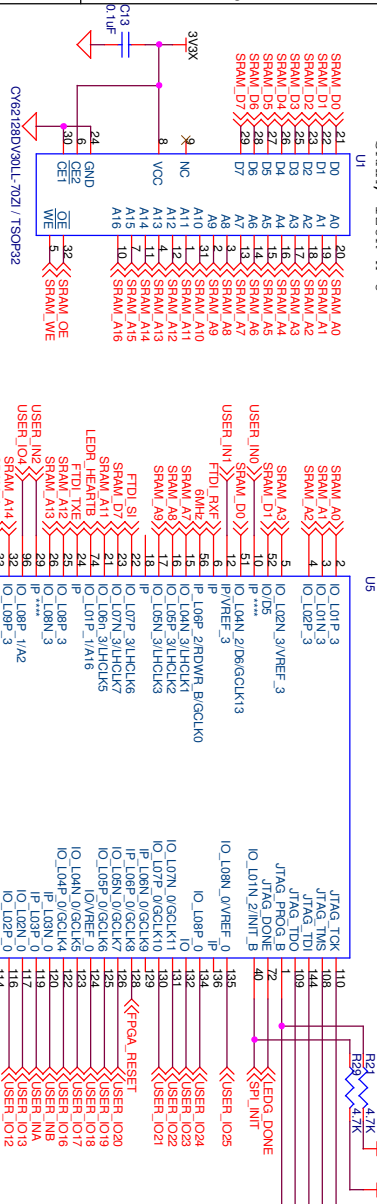
**PRELIMINARY**



For FPGA configuration via SPI only.

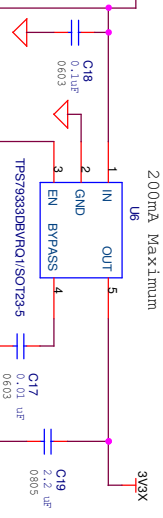
Downloading FPGA Code via UPLOAD

|    |    |          |    |    |          |
|----|----|----------|----|----|----------|
| 1  | 50 | USER_I00 | 1  | 50 | USER_I00 |
| 2  | 49 | USER_I01 | 2  | 49 | USER_I01 |
| 3  | 48 | USER_I02 | 3  | 48 | USER_I02 |
| 4  | 47 | USER_I03 | 4  | 47 | USER_I03 |
| 5  | 46 | USER_I04 | 5  | 46 | USER_I04 |
| 6  | 45 | USER_I05 | 6  | 45 | USER_I05 |
| 7  | 44 | USER_I06 | 7  | 44 | USER_I06 |
| 8  | 43 | USER_I07 | 8  | 43 | USER_I07 |
| 9  | 42 | USER_I08 | 9  | 42 | USER_I08 |
| 10 | 41 | USER_I09 | 10 | 41 | USER_I09 |
| 11 | 40 | USER_I10 | 11 | 40 | USER_I10 |
| 12 | 39 | USER_I11 | 12 | 39 | USER_I11 |
| 13 | 38 | USER_I12 | 13 | 38 | USER_I12 |
| 14 | 37 | USER_I13 | 14 | 37 | USER_I13 |
| 15 | 36 | USER_I14 | 15 | 36 | USER_I14 |
| 16 | 35 | USER_I15 | 16 | 35 | USER_I15 |
| 17 | 34 | USER_I16 | 17 | 34 | USER_I16 |
| 18 | 33 | USER_I17 | 18 | 33 | USER_I17 |
| 19 | 32 | USER_I18 | 19 | 32 | USER_I18 |
| 20 | 31 | USER_I19 | 20 | 31 | USER_I19 |
| 21 | 30 | USER_I20 | 21 | 30 | USER_I20 |
| 22 | 29 | USER_I21 | 22 | 29 | USER_I21 |
| 23 | 28 | USER_I22 | 23 | 28 | USER_I22 |
| 24 | 27 | USER_I23 | 24 | 27 | USER_I23 |
| 25 | 26 | USER_I24 | 25 | 26 | USER_I24 |
| 26 | 25 | USER_I25 | 26 | 25 | USER_I25 |
| 27 | 24 | USER_I26 | 27 | 24 | USER_I26 |
| 28 | 23 | USER_I27 | 28 | 23 | USER_I27 |
| 29 | 22 | USER_I28 | 29 | 22 | USER_I28 |
| 30 | 21 | USER_I29 | 30 | 21 | USER_I29 |
| 31 | 20 | USER_I30 | 31 | 20 | USER_I30 |
| 32 | 19 | USER_I31 | 32 | 19 | USER_I31 |
| 33 | 18 | USER_I32 | 33 | 18 | USER_I32 |
| 34 | 17 | USER_I33 | 34 | 17 | USER_I33 |
| 35 | 16 | USER_I34 | 35 | 16 | USER_I34 |
| 36 | 15 | USER_I35 | 36 | 15 | USER_I35 |
| 37 | 14 | USER_I36 | 37 | 14 | USER_I36 |
| 38 | 13 | USER_I37 | 38 | 13 | USER_I37 |
| 39 | 12 | USER_I38 | 39 | 12 | USER_I38 |
| 40 | 11 | USER_I39 | 40 | 11 | USER_I39 |
| 41 | 10 | USER_I40 | 41 | 10 | USER_I40 |
| 42 | 9  | USER_I41 | 42 | 9  | USER_I41 |
| 43 | 8  | USER_I42 | 43 | 8  | USER_I42 |
| 44 | 7  | USER_I43 | 44 | 7  | USER_I43 |
| 45 | 6  | USER_I44 | 45 | 6  | USER_I44 |
| 46 | 5  | USER_I45 | 46 | 5  | USER_I45 |
| 47 | 4  | USER_I46 | 47 | 4  | USER_I46 |
| 48 | 3  | USER_I47 | 48 | 3  | USER_I47 |
| 49 | 2  | USER_I48 | 49 | 2  | USER_I48 |
| 50 | 1  | USER_I49 | 50 | 1  | USER_I49 |
| 51 | 0  | USER_I50 | 51 | 0  | USER_I50 |



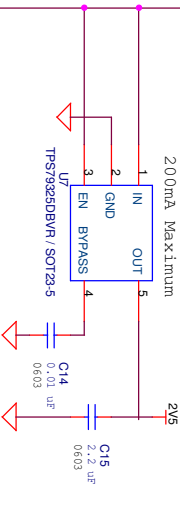
### 3.3V REGULATOR

200mA Maximum



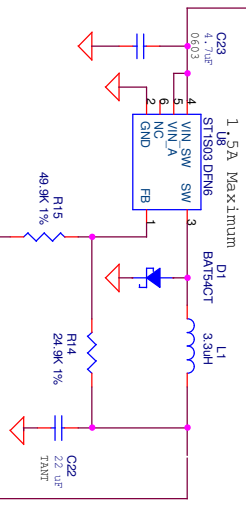
### 2.5V REGULATOR

200mA Maximum



### 1.2V REGULATOR

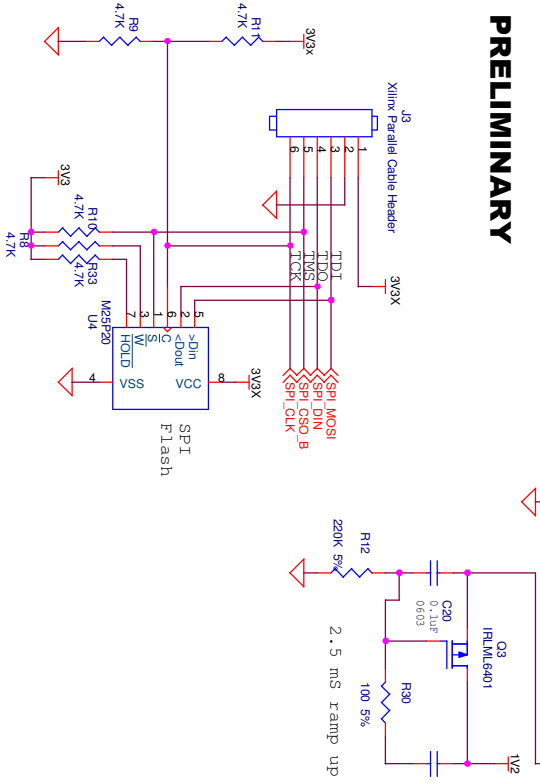
1.5A Maximum



### PRELIMINARY



DLP-FPGA  
Page 2



## Данный компонент на территории Российской Федерации

### Вы можете приобрести в компании MosChip.

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