# PCA9548A

## 8-channel I²C-bus switch with reset

Rev. 5.1 — 1 October 2015 Product data sheet

## 1. General description

The PCA9548A is an octal bidirectional translating switch controlled via the I²C-bus. The SCL/SDA upstream pair fans out to eight downstream pairs, or channels. Any individual SCx/SDx channel or combination of channels can be selected, determined by the contents of the programmable control register.

An active LOW reset input allows the PCA9548A to recover from a situation where one of the downstream I²C-buses is stuck in a LOW state. Pulling the $\overline{\text{RESET}}$ pin LOW resets the I²C-bus state machine and causes all the channels to be deselected as does the internal Power-on reset function.

The pass gates of the switches are constructed such that the $V_{DD}$ pin can be used to limit the maximum high voltage which will be passed by the PCA9548A. This allows the use of different bus voltages on each pair, so that 1.8 V or 2.5 V or 3.3 V parts can communicate with 5 V parts without any additional protection. External pull-up resistors pull the bus up to the desired voltage level for each channel. All I/O pins are 6 V tolerant.

## 2. Features and benefits

- 1-of-8 bidirectional translating switches
- I²C-bus interface logic; compatible with SMBus standards
- Active LOW reset input
- Three address pins allowing up to eight devices on the I²C-bus
- Channel selection via I²C-bus, in any combination
- Power-up with all switch channels deselected
- Low $R_{on}$ switches
- Allows voltage level translation between 1.8 V, 2.5 V, 3.3 V and 5 V buses
- No glitch on power-up
- Supports hot insertion
- Low standby current
- Operating power supply voltage range of 2.3 V to 5.5 V
- 6 V tolerant inputs
- 0 Hz to 400 kHz clock frequency
- ESD protection exceeds 2000 V HBM per JESD22-A114 and 1000 V CDM per JESD22-C101
- Latch-up testing is done to JEDEC Standard JESD78 which exceeds 100 mA
- Three packages offered: SO24, TSSOP24, and HVQFN24

# 3. Ordering information

**Table 1. Ordering information**

| Type number | Topside marking | Package | | |
|---|---|---|---|---|
| | | Name | Description | Version |
| PCA9548ABS | 548A | HVQFN24 | plastic thermal enhanced very thin quad flat package; no leads; 24 terminals; body 4 × 4 × 0.85 mm | SOT616-1 |
| PCA9548AD | PCA9548AD | SO24 | plastic small outline package; 24 leads; body width 7.5 mm | SOT137-1 |
| PCA9548APW | PCA9548A | TSSOP24 | plastic thin shrink small outline package; 24 leads; body width 4.4 mm | SOT355-1 |

## 3.1 Ordering options

**Table 2. Ordering options**

| Type number | Orderable part number | Package | Packing method | Minimum order quantity | Temperature |
|---|---|---|---|---|---|
| PCA9548ABS | PCA9548ABS,118 | HVQFN24 | Reel 13” Q1/T1 *Standard mark SMD | 6000 | $T_{amb}$ = −40 °C to +85 °C |
| | PCA9548ABSHP | HVQFN24 | Reel 13” Q2/T3 *Standard mark SMD | 6000 | $T_{amb}$ = −40 °C to +85 °C |
| PCA9548AD | PCA9548AD,112 | SO24 | Standard marking IC’s tube - DSC bulk pack | 1200 | $T_{amb}$ = −40 °C to +85 °C |
| | PCA9548AD,118 | SO24 | Reel 13” Q1/T1 *Standard mark SMD | 1000 | $T_{amb}$ = −40 °C to +85 °C |
| PCA9548APW | PCA9548APW,112 | TSSOP24 | Standard marking IC’s tube - DSC bulk pack | 1575 | $T_{amb}$ = −40 °C to +85 °C |
| | PCA9548APW,118 | TSSOP24 | Reel 13” Q1/T1 *Standard mark SMD | 2500 | $T_{amb}$ = −40 °C to +85 °C |

## 4. Block diagram

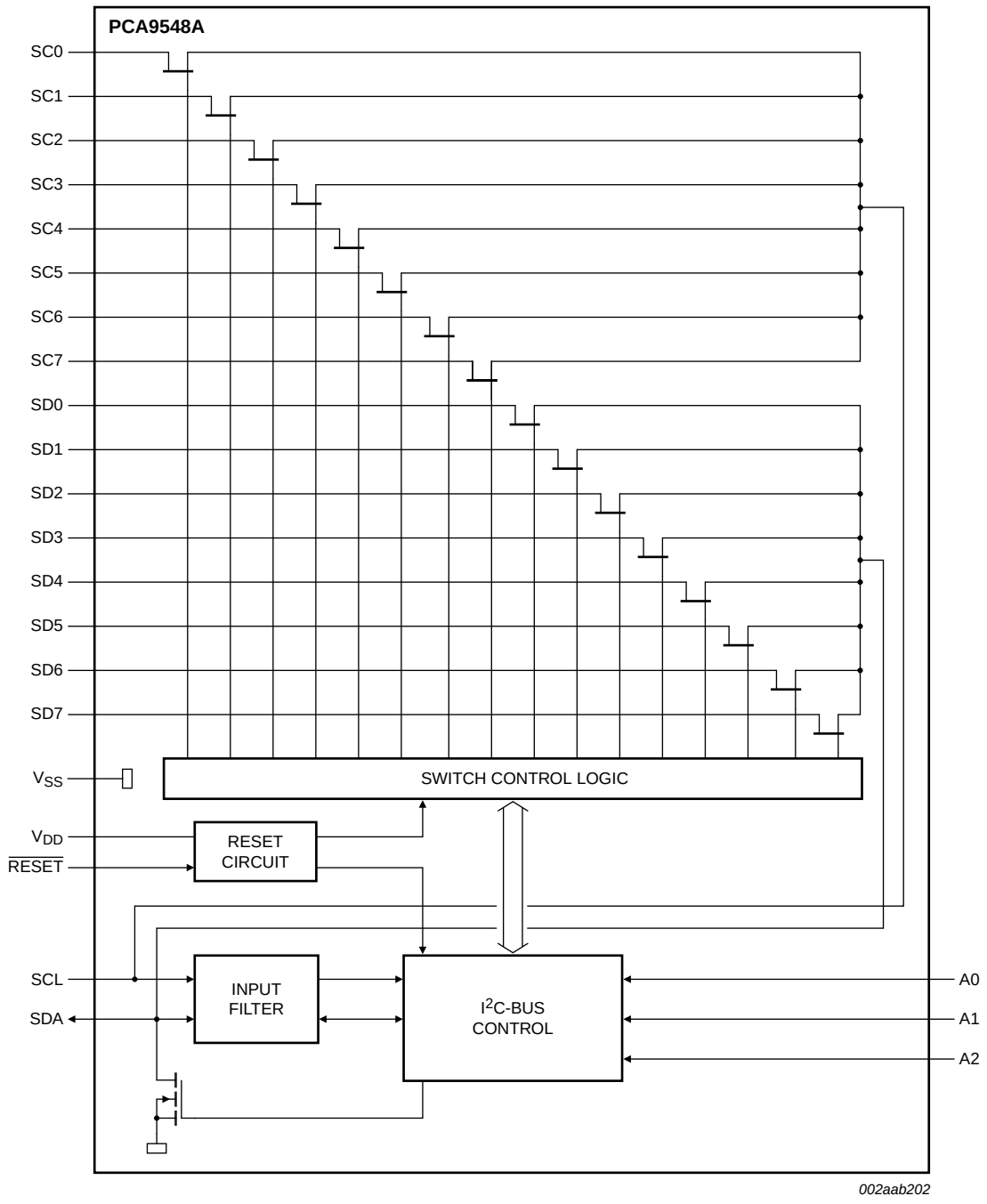



**Fig 1. Block diagram of PCA9548A**

# 5. Pinning information

## 5.1 Pinning

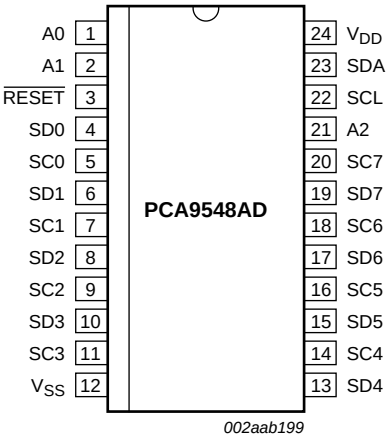



**Fig 2. Pin configuration for SO24**

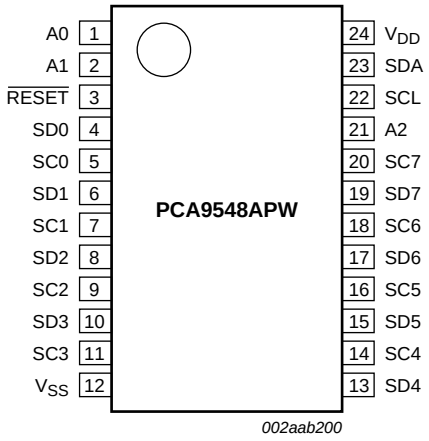
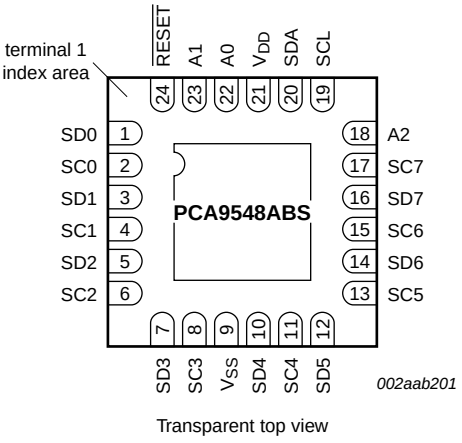



**Fig 3. Pin configuration for TSSOP24**




Transparent top view

**Fig 4. Pin configuration for HVQFN24 (transparent top view)**

## 5.2 Pin description

**Table 3. Pin description**

| Symbol | Pin | | Description |
|---|---|---|---|
| | SO24, TSSOP24 | HVQFN24 | |
| A0 | 1 | 22 | address input 0 |
| A1 | 2 | 23 | address input 1 |
| $\overline{\text{RESET}}$ | 3 | 24 | active LOW reset input |
| SD0 | 4 | 1 | serial data 0 |
| SC0 | 5 | 2 | serial clock 0 |
| SD1 | 6 | 3 | serial data 1 |
| SC1 | 7 | 4 | serial clock 1 |
| SD2 | 8 | 5 | serial data 2 |
| SC2 | 9 | 6 | serial clock 2 |
| SD3 | 10 | 7 | serial data 3 |
| SC3 | 11 | 8 | serial clock 3 |
| $V_{SS}$ | 12 | 9[1] | supply ground |
| SD4 | 13 | 10 | serial data 4 |
| SC4 | 14 | 11 | serial clock 4 |
| SD5 | 15 | 12 | serial data 5 |
| SC5 | 16 | 13 | serial clock 5 |
| SD6 | 17 | 14 | serial data 6 |
| SC6 | 18 | 15 | serial clock 6 |
| SD7 | 19 | 16 | serial data 7 |
| SC7 | 20 | 17 | serial clock 7 |
| A2 | 21 | 18 | address input 2 |
| SCL | 22 | 19 | serial clock line |
| SDA | 23 | 20 | serial data line |
| $V_{DD}$ | 24 | 21 | supply voltage |

[1] HVQFN24 package die supply ground is connected to both the $V_{SS}$ pin and the exposed center pad. The $V_{SS}$ pin must be connected to supply ground for proper device operation. For enhanced thermal, electrical, and board-level performance, the exposed pad needs to be soldered to the board using a corresponding thermal pad on the board, and for proper heat conduction through the board thermal vias need to be incorporated in the PCB in the thermal pad region.

# 6. Functional description

Refer to Figure 1 “Block diagram of PCA9548A”.

## 6.1 Device address

Following a START condition, the bus master must output the address of the slave it is accessing. The address of the PCA9548A is shown in Figure 5. To conserve power, no internal pull-up resistors are incorporated on the hardware selectable address pins and they must be pulled HIGH or LOW.

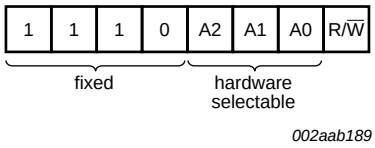



**Fig 5. Slave address**

The last bit of the slave address defines the operation to be performed. When set to logic 1 a read is selected, while a logic 0 selects a write operation.

## 6.2 Control register

Following the successful acknowledgement of the slave address, the bus master will send a byte to the PCA9548A, which will be stored in the control register. If multiple bytes are received by the PCA9548A, it will save the last byte received. This register can be written and read via the I²C-bus.

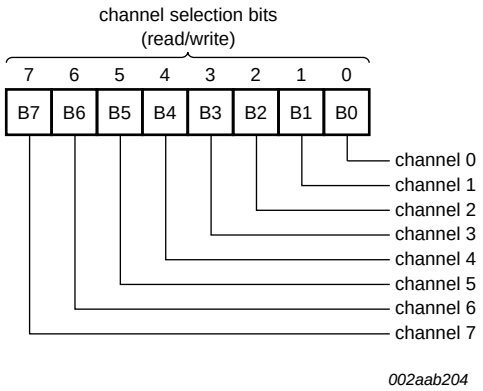



**Fig 6. Control register**

### 6.2.1 Control register definition

One or several SCx/SDx downstream pair, or channel, is selected by the contents of the control register. This register is written after the PCA9548A has been addressed. The contents of the control byte are used to determine which channel is to be selected. When a channel is selected, the channel will become active after a STOP condition has been placed on the I²C-bus. This ensures that all SCx/SDx lines will be in a HIGH state when the channel is made active, so that no false conditions are generated at the time of connection.

**Table 4. Control register: Write—channel selection; Read—channel status**

| B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 | Command |
|---|---|---|---|---|---|---|---|---|
| X | X | X | X | X | X | X | 0 | channel 0 disabled |
| | | | | | | | 1 | channel 0 enabled |
| X | X | X | X | X | X | 0 | X | channel 1 disabled |
| | | | | | | 1 | | channel 1 enabled |
| X | X | X | X | X | 0 | X | X | channel 2 disabled |
| | | | | | 1 | | | channel 2 enabled |
| X | X | X | X | 0 | X | X | X | channel 3 disabled |
| | | | | 1 | | | | channel 3 enabled |
| X | X | X | 0 | X | X | X | X | channel 4 disabled |
| | | | 1 | | | | | channel 4 enabled |
| X | X | 0 | X | X | X | X | X | channel 5 disabled |
| | | 1 | | | | | | channel 5 enabled |
| X | 0 | X | X | X | X | X | X | channel 6 disabled |
| | 1 | | | | | | | channel 6 enabled |
| 0 | X | X | X | X | X | X | X | channel 7 disabled |
| 1 | | | | | | | | channel 7 enabled |

**Remark:** Multiple channels can be enabled at the same time. Example: B7 = 0, B6 = 1, B5 = 0, B4 = 0, B3 = 1, B2 = 1, B1 = 0, B0 = 0, means that channels 7, 5, 4, 1 and 0 are disabled and channels 6, 3, and 2 are enabled. Care should be taken not to exceed the maximum bus capacitance. Default condition is all zeroes.

## 6.3 $\overline{\text{RESET}}$ input

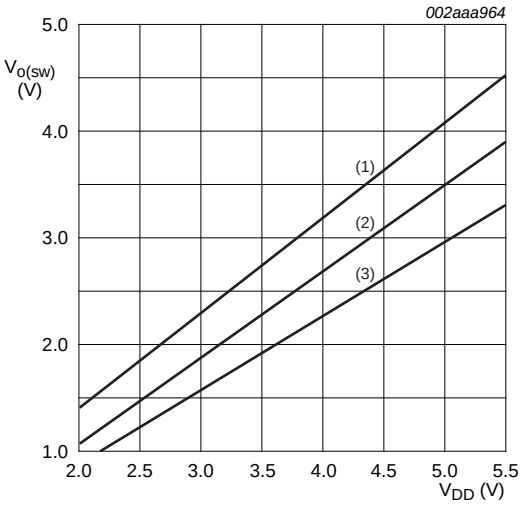
The $\overline{\text{RESET}}$ input is an active LOW signal which may be used to recover from a bus fault condition. By asserting this signal LOW for a minimum of $t_{w(rst)L}$, the PCA9548A will reset its register and I²C-bus state machine and will deselect all channels. The $\overline{\text{RESET}}$ input must be connected to $V_{DD}$ through a pull-up resistor.

## 6.4 Power-on reset

When power is applied to $V_{DD}$, an internal Power-On Reset (POR) holds the PCA9548A in a reset condition until $V_{DD}$ has reached $V_{POR}$. At this point, the reset condition is released and the PCA9548A register and I²C-bus state machine are initialized to their default states (all zeroes) causing all the channels to be deselected. Thereafter, $V_{DD}$ must be lowered below 0.2 V for at least 5 μs in order to reset the device.

## 6.5 Voltage translation

The pass gate transistors of the PCA9548A are constructed such that the $V_{DD}$ voltage can be used to limit the maximum voltage that will be passed from one I²C-bus to another.




(1) maximum
(2) typical
(3) minimum

**Fig 7. Pass gate voltage versus supply voltage**

Figure 7 shows the voltage characteristics of the pass gate transistors (note that the PCA9548A is only tested at the points specified in Section 11 “Static characteristics” of this data sheet). In order for the PCA9548A to act as a voltage translator, the $V_{O(sw)}$ voltage should be equal to, or lower than the lowest bus voltage. For example, if the main bus was running at 5 V, and the downstream buses were 3.3 V and 2.7 V, then $V_{O(sw)}$ should be equal to or below 2.7 V to effectively clamp the downstream bus voltages. Looking at Figure 7, we see that $V_{O(sw)(max)}$ will be at 2.7 V when the PCA9548A supply voltage is 3.5 V or lower, so the PCA9548A supply voltage could be set to 3.3 V. Pull-up resistors can then be used to bring the bus voltages to their appropriate levels (see Figure 14).

More Information can be found in Application Note *AN262: PCA954X family of I²C/SMBus multiplexers and switches*.

# 7. Characteristics of the I²C-bus

The I²C-bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

## 7.1 Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals (see Figure 8).

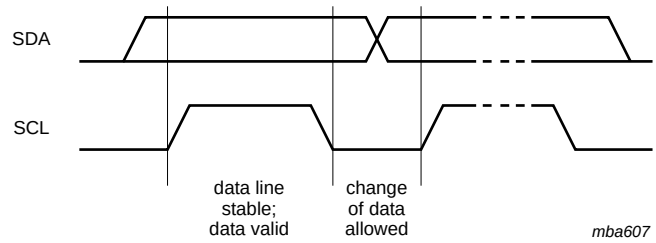



**Fig 8. Bit transfer**

## 7.2 START and STOP conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line while the clock is HIGH is defined as the START condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the STOP condition (P) (see Figure 9).

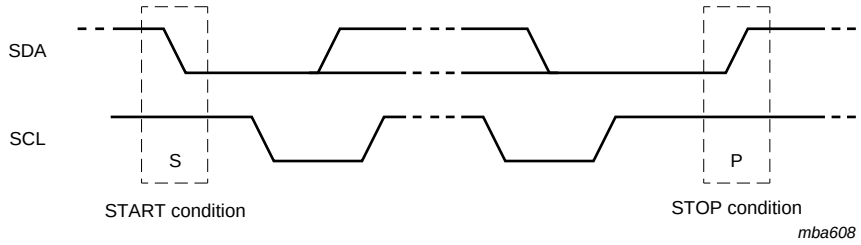



**Fig 9. Definition of START and STOP conditions**

## 7.3 System configuration

A device generating a message is a ‘transmitter’, a device receiving is the ‘receiver’. The device that controls the message is the ‘master’ and the devices which are controlled by the master are the ‘slaves’ (see Figure 10).

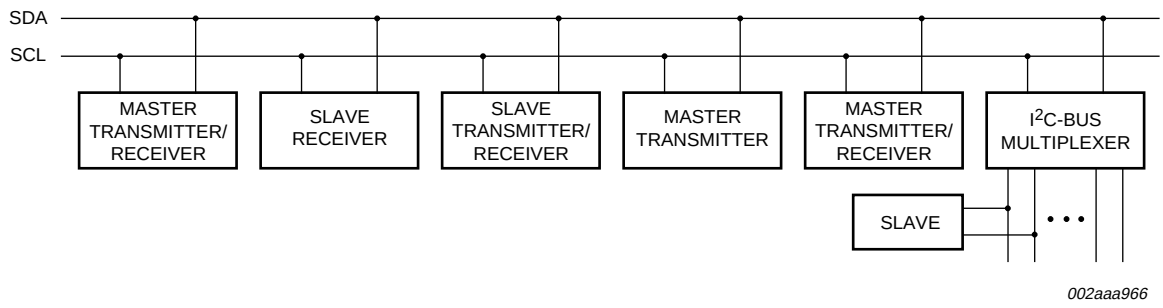



**Fig 10. System configuration**

## 7.4 Acknowledge

The number of data bytes transferred between the START and the STOP conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter, whereas the master generates an extra acknowledge related clock pulse.

A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also, a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse; set-up and hold times must be taken into account.

A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event, the transmitter must leave the data line HIGH to enable the master to generate a STOP condition.

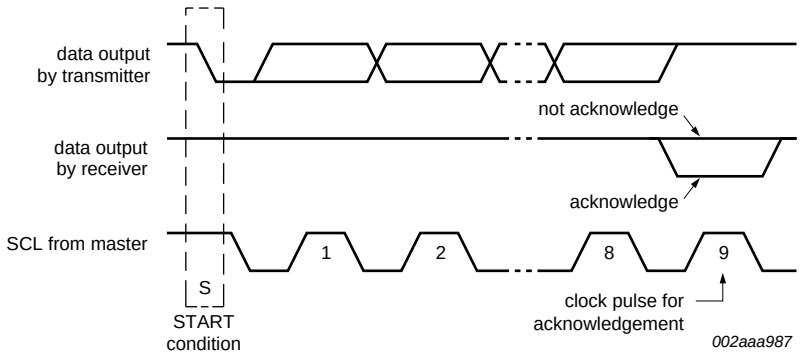



**Fig 11. Acknowledgement on the I²C-bus**

## 7.5 Bus transactions

Data is transmitted to the PCA9548A control register using the Write mode as shown in Figure 12.

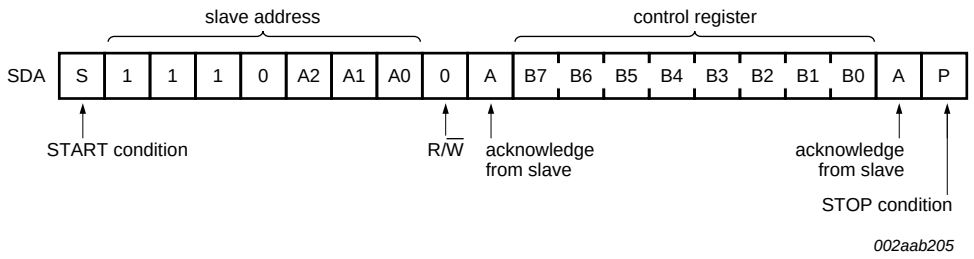



**Fig 12. Write control register**

Data is read from PCA9548A using the Read mode as shown in Figure 13.

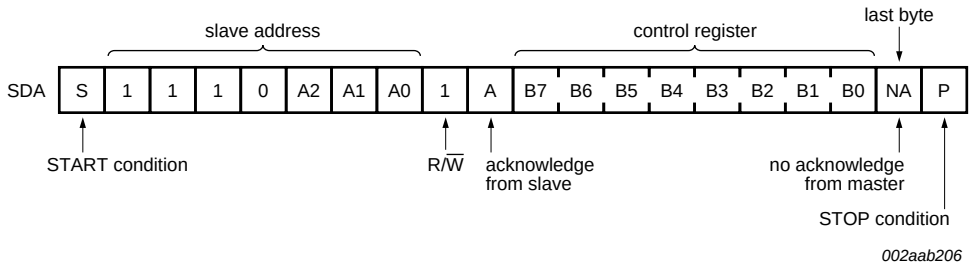



**Fig 13. Read control register**

## 8. Application design-in information

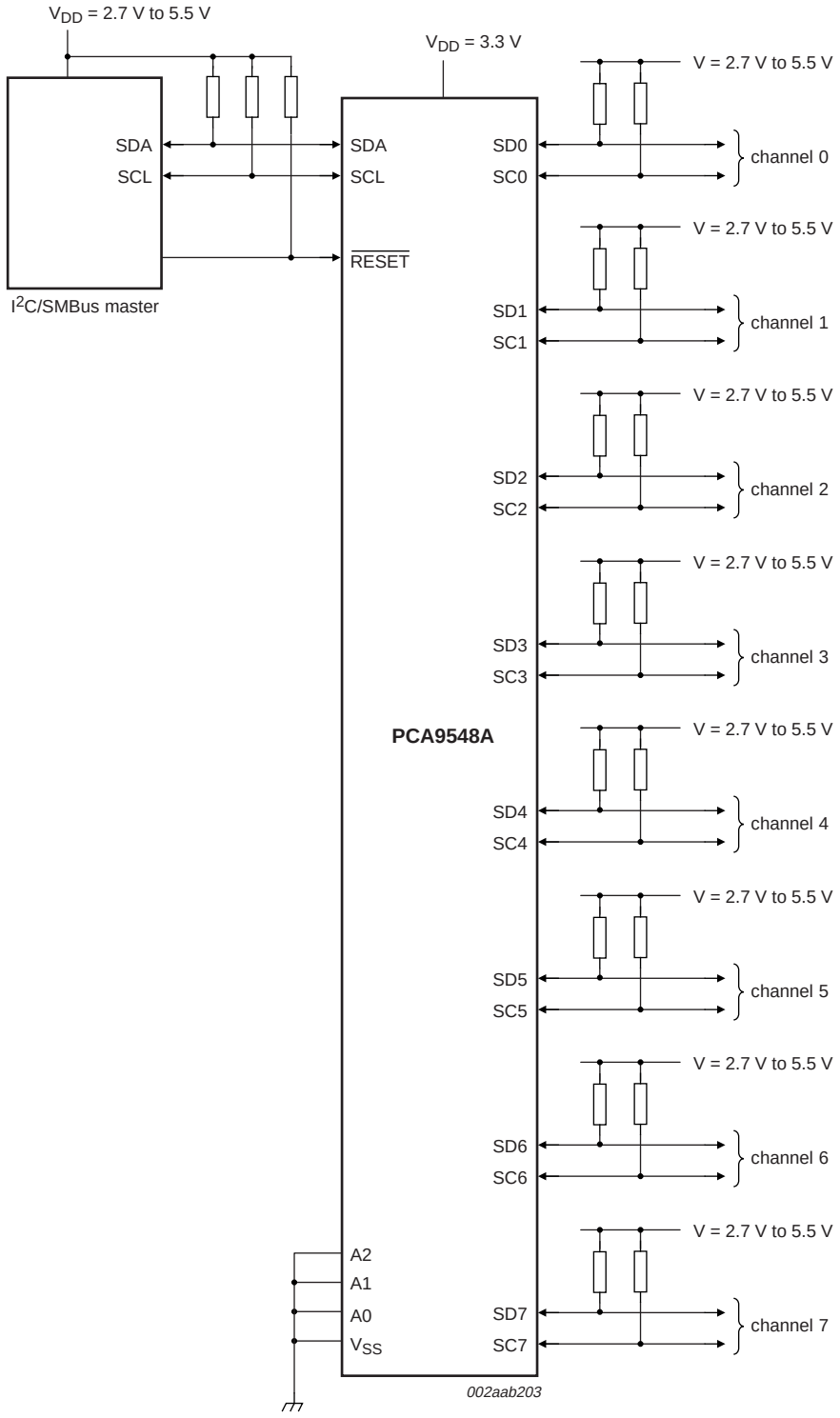



**Fig 14. Typical application**

# 9. Limiting values

**Table 5. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to $V_{SS}$ (ground = 0 V).*

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{DD}$ | supply voltage | | –0.5 | +7.0 | V |
| $V_I$ | input voltage | | –0.5 | +7.0 | V |
| $I_I$ | input current | | - | ±20 | mA |
| $I_O$ | output current | | - | ±25 | mA |
| $I_{DD}$ | supply current | | - | ±100 | mA |
| $I_{SS}$ | ground supply current | | - | ±100 | mA |
| $P_{tot}$ | total power dissipation | | - | 400 | mW |
| $T_{j(max)}$ | maximum junction temperature | [1] | - | 125 | °C |
| $T_{stg}$ | storage temperature | | –60 | +150 | °C |
| $T_{amb}$ | ambient temperature | operating | –40 | +85 | °C |

[1] The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 125 °C.

# 10. Thermal characteristics

**Table 6. Thermal characteristics**

| Symbol | Parameter | Conditions | Typ | Unit |
|---|---|---|---|---|
| $R_{th(j-a)}$ | thermal resistance from junction to ambient | HVQFN24 package | 40 | °C/W |
| | | SO24 package | 77 | °C/W |
| | | TSSOP24 package | 128 | °C/W |

## 11. Static characteristics

**Table 7. Static characteristics at $V_{DD}$ = 2.3 V to 3.6 V**

*$V_{SS}$ = 0 V; $T_{amb}$ = –40 °C to +85 °C; unless otherwise specified. See Table 8 on page 15 for $V_{DD}$ = 4.5 V to 5.5 V.*[1]

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **Supply** | | | | | | | |
| $V_{DD}$ | supply voltage | | | 2.3 | - | 3.6 | V |
| $I_{DD}$ | supply current | operating mode; $V_{DD}$ = 3.6 V; no load; $V_I = V_{DD}$ or $V_{SS}$; $f_{SCL}$ = 100 kHz | | - | 30 | 50 | μA |
| $I_{stb}$ | standby current | standby mode; $V_{DD}$ = 3.6 V; no load; $V_I = V_{DD}$ or $V_{SS}$ | | - | 0.1 | 1 | μA |
| $V_{POR}$ | power-on reset voltage | no load; $V_I = V_{DD}$ or $V_{SS}$ | [2] | - | 1.6 | 2.1 | V |
| **Input SCL; input/output SDA** | | | | | | | |
| $V_{IL}$ | LOW-level input voltage | | | –0.5 | - | $+0.3V_{DD}$ | V |
| $V_{IH}$ | HIGH-level input voltage | | | $0.7V_{DD}$ | - | 6 | V |
| $I_{OL}$ | LOW-level output current | $V_{OL}$ = 0.4 V | | 3 | 6 | - | mA |
| | | $V_{OL}$ = 0.6 V | | 6 | 9 | - | mA |
| $I_L$ | leakage current | $V_I = V_{DD}$ or $V_{SS}$ | | –1 | - | +1 | μA |
| $C_i$ | input capacitance | $V_I = V_{SS}$ | | - | 15 | 21 | pF |
| **Select inputs A0 to A2, $\overline{RESET}$** | | | | | | | |
| $V_{IL}$ | LOW-level input voltage | | | –0.5 | - | $+0.3V_{DD}$ | V |
| $V_{IH}$ | HIGH-level input voltage | | | $0.7V_{DD}$ | - | 6 | V |
| $I_{LI}$ | input leakage current | pin at $V_{DD}$ or $V_{SS}$ | | –1 | - | +1 | μA |
| $C_i$ | input capacitance | $V_I = V_{SS}$ | | - | 2 | 5 | pF |
| **Pass gate** | | | | | | | |
| $R_{on}$ | ON-state resistance | $V_{DD}$ = 3.0 V to 3.6 V; $V_O$ = 0.4 V; $I_O$ = 15 mA | | 5 | 11 | 30 | Ω |
| | | $V_{DD}$ = 2.3 V to 2.7 V; $V_O$ = 0.4 V; $I_O$ = 10 mA | | 7 | 16 | 55 | Ω |
| $V_{o(sw)}$ | switch output voltage | $V_{i(sw)} = V_{DD}$ = 3.3 V; $I_{o(sw)}$ = –100 μA | | - | 1.9 | - | V |
| | | $V_{i(sw)} = V_{DD}$ = 3.0 V to 3.6 V; $I_{o(sw)}$ = –100 μA | | 1.6 | - | 2.8 | V |
| | | $V_{i(sw)} = V_{DD}$ = 2.5 V; $I_{o(sw)}$ = –100 μA | | - | 1.5 | - | V |
| | | $V_{i(sw)} = V_{DD}$ = 2.3 V to 2.7 V; $I_{o(sw)}$ = –100 μA | | 1.1 | - | 2.0 | V |
| $I_L$ | leakage current | $V_I = V_{DD}$ or $V_{SS}$ | | –1 | - | +1 | μA |
| $C_{io}$ | input/output capacitance | $V_I = V_{SS}$ | | - | 3 | 5 | pF |

[1] For operation between published voltage ranges, refer to the worst-case parameter in both ranges.

[2] $V_{DD}$ must be lowered to 0.2 V for at least 5 μs in order to reset part.

**Table 8. Static characteristics at $V_{DD}$ = 4.5 V to 5.5 V**

*$V_{SS}$ = 0 V; $T_{amb}$ = −40 °C to +85 °C; unless otherwise specified. See Table 7 on page 14 for $V_{DD}$ = 2.3 V to 3.6 V.*[1]

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **Supply** | | | | | | | |
| $V_{DD}$ | supply voltage | | | 4.5 | - | 5.5 | V |
| $I_{DD}$ | supply current | operating mode; $V_{DD}$ = 5.5 V; no load; $V_I$ = $V_{DD}$ or $V_{SS}$; $f_{SCL}$ = 100 kHz | | - | 65 | 100 | μA |
| $I_{stb}$ | standby current | standby mode; $V_{DD}$ = 5.5 V; no load; $V_I$ = $V_{DD}$ or $V_{SS}$ | | - | 0.2 | 1 | μA |
| $V_{POR}$ | power-on reset voltage | no load; $V_I$ = $V_{DD}$ or $V_{SS}$ | [2] | - | 1.7 | 2.1 | V |
| **Input SCL; input/output SDA** | | | | | | | |
| $V_{IL}$ | LOW-level input voltage | | | −0.5 | - | +0.3$V_{DD}$ | V |
| $V_{IH}$ | HIGH-level input voltage | | | 0.7$V_{DD}$ | - | 6 | V |
| $I_{OL}$ | LOW-level output current | $V_{OL}$ = 0.4 V | | 3 | - | - | mA |
| | | $V_{OL}$ = 0.6 V | | 6 | - | - | mA |
| $I_{IL}$ | LOW-level input current | $V_I$ = $V_{SS}$ | | −1 | - | +1 | μA |
| $I_{IH}$ | HIGH-level input current | $V_I$ = $V_{DD}$ | | −1 | - | +1 | μA |
| $C_i$ | input capacitance | $V_I$ = $V_{SS}$ | | - | 15 | 21 | pF |
| **Select inputs A0 to A2, $\overline{\text{RESET}}$** | | | | | | | |
| $V_{IL}$ | LOW-level input voltage | | | −0.5 | - | +0.3$V_{DD}$ | V |
| $V_{IH}$ | HIGH-level input voltage | | | 0.7$V_{DD}$ | - | 6 | V |
| $I_{LI}$ | input leakage current | pin at $V_{DD}$ or $V_{SS}$ | | −1 | - | +1 | μA |
| $C_i$ | input capacitance | $V_I$ = $V_{SS}$ | | - | 2 | 5 | pF |
| **Pass gate** | | | | | | | |
| $R_{on}$ | ON-state resistance | $V_{DD}$ = 4.5 V to 5.5 V; $V_O$ = 0.4 V; $I_O$ = 15 mA | | 4 | 9 | 24 | Ω |
| $V_{o(sw)}$ | switch output voltage | $V_{i(sw)}$ = $V_{DD}$ = 5.0 V; $I_{o(sw)}$ = −100 μA | | - | 3.6 | - | V |
| | | $V_{i(sw)}$ = $V_{DD}$ = 4.5 V to 5.5 V; $I_{o(sw)}$ = −100 μA | | 2.6 | - | 4.5 | V |
| $I_L$ | leakage current | $V_I$ = $V_{DD}$ or $V_{SS}$ | | −1 | - | +1 | μA |
| $C_{io}$ | input/output capacitance | $V_I$ = $V_{SS}$ | | - | 3 | 5 | pF |

[1] For operation between published voltage ranges, refer to the worst-case parameter in both ranges.

[2] $V_{DD}$ must be lowered to 0.2 V for at least 5 μs in order to reset part.

## 12. Dynamic characteristics

**Table 9. Dynamic characteristics**

| Symbol | Parameter | Conditions | | Standard-mode I²C-bus | | Fast-mode I²C-bus | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Max | Min | Max | |
| $t_{PD}$ | propagation delay | from SDA to SDx, or SCL to SCx | | - | 0.3[1] | - | 0.3[1] | ns |
| $f_{SCL}$ | SCL clock frequency | | | 0 | 100 | 0 | 400 | kHz |
| $t_{BUF}$ | bus free time between a STOP and START condition | | | 4.7 | - | 1.3 | - | µs |
| $t_{HD;STA}$ | hold time (repeated) START condition | | [2] | 4.0 | - | 0.6 | - | µs |
| $t_{LOW}$ | LOW period of the SCL clock | | | 4.7 | - | 1.3 | - | µs |
| $t_{HIGH}$ | HIGH period of the SCL clock | | | 4.0 | - | 0.6 | - | µs |
| $t_{SU;STA}$ | set-up time for a repeated START condition | | | 4.7 | - | 0.6 | - | µs |
| $t_{SU;STO}$ | set-up time for STOP condition | | | 4.0 | - | 0.6 | - | µs |
| $t_{HD;DAT}$ | data hold time | | | 0[3] | [4] | 0[3] | [4] | µs |
| $t_{SU;DAT}$ | data set-up time | | | 250 | - | 100 | - | ns |
| $t_r$ | rise time of both SDA and SCL signals | | | - | 1000 | $20 + 0.1C_b$[5] | 300 | ns |
| $t_f$ | fall time of both SDA and SCL signals | | | - | 300 | $20 + 0.1C_b$[5] | 300 | ns |
| $C_b$ | capacitive load for each bus line | | | - | 400 | - | 400 | pF |
| $t_{SP}$ | pulse width of spikes that must be suppressed by the input filter | | | - | 50 | - | 50 | ns |
| $t_{VD;DAT}$ | data valid time | HIGH-to-LOW | [6] | - | 1 | - | 1 | µs |
| | | LOW-to-HIGH | [6] | - | 0.6 | - | 0.6 | µs |
| $t_{VD;ACK}$ | data valid acknowledge time | | | - | 1 | - | 1 | µs |
| **RESET** | | | | | | | | |
| $t_{w(rst)L}$ | LOW-level reset time | | | 4 | - | 4 | - | ns |
| $t_{rst}$ | reset time | SDA clear | | - | 500 | - | 500 | ns |
| $t_{REC;STA}$ | recovery time to START condition | | | 0 | - | 0 | - | ns |

[1] Pass gate propagation delay is calculated from the 20 Ω typical $R_{on}$ and the 15 pF load capacitance.

[2] After this period, the first clock pulse is generated.

[3] A device must internally provide a hold time of at least 300 ns for the SDA signal (referred to the $V_{IH(min)}$ of the SCL signal) in order to bridge the undefined region of the falling edge of SCL.

[4] The maximum $t_{HD;DAT}$ could be 3.45 µs and 0.9 µs for Standard-mode and Fast-mode, but must be less than the maximum of $t_{VD;DAT}$ or $t_{VD;ACK}$ by a transition time. This maximum must only be met if the device does not stretch the LOW period ($t_{LOW}$) of the SCL signal. If the clock stretches the SCL, the data must be valid by the set-up time before it releases the clock.

[5] $C_b$ = total capacitance of one bus line in pF.

[6] Measurements taken with 1 kΩ pull-up resistor and 50 pF load.

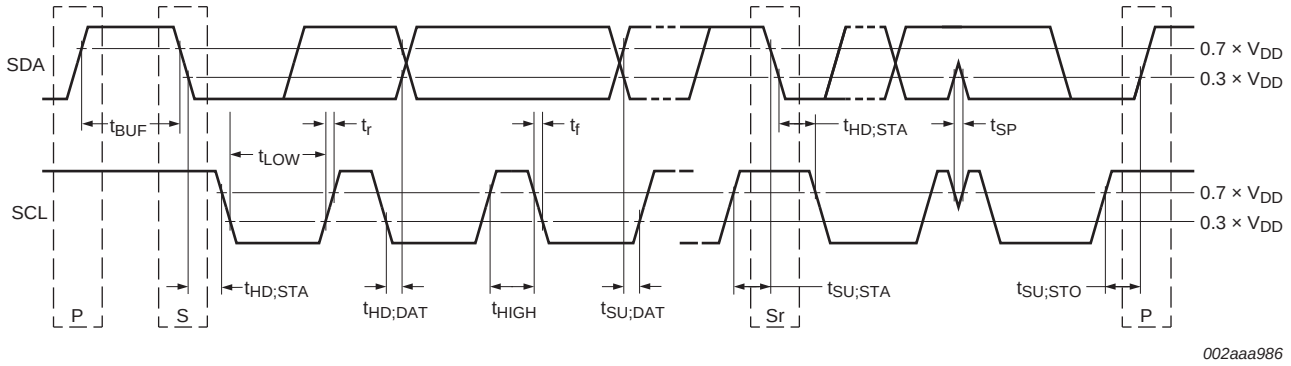



**Fig 15. Definition of timing on the I²C-bus**

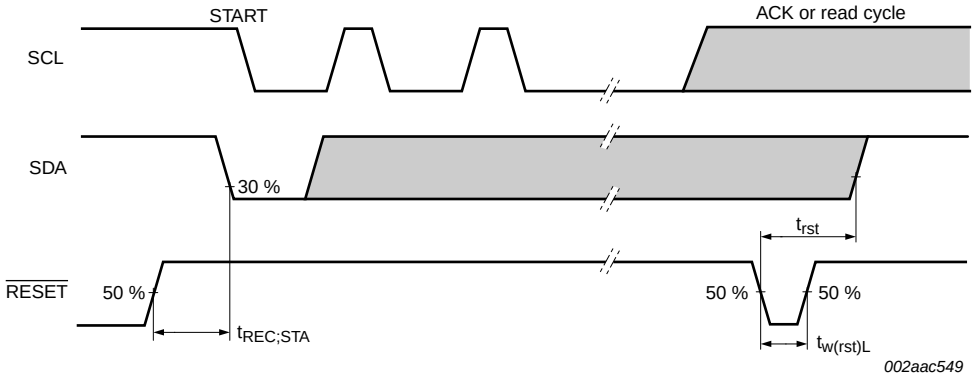



**Fig 16. Definition of $\overline{\text{RESET}}$ timing**

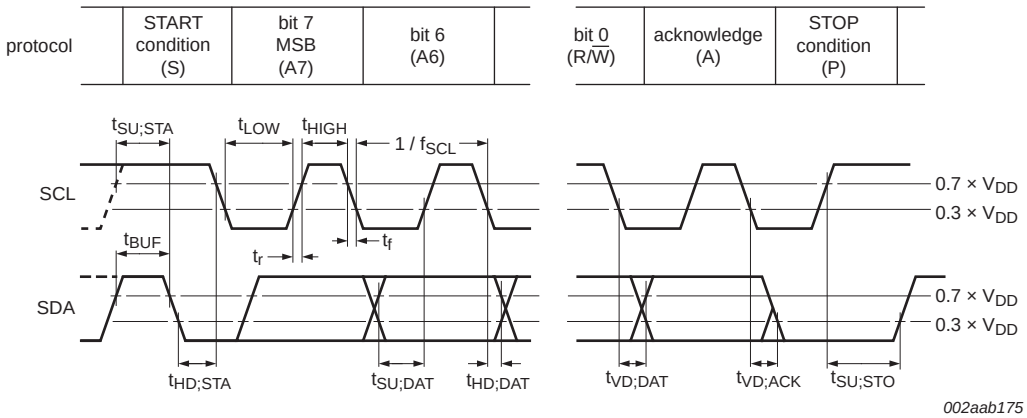
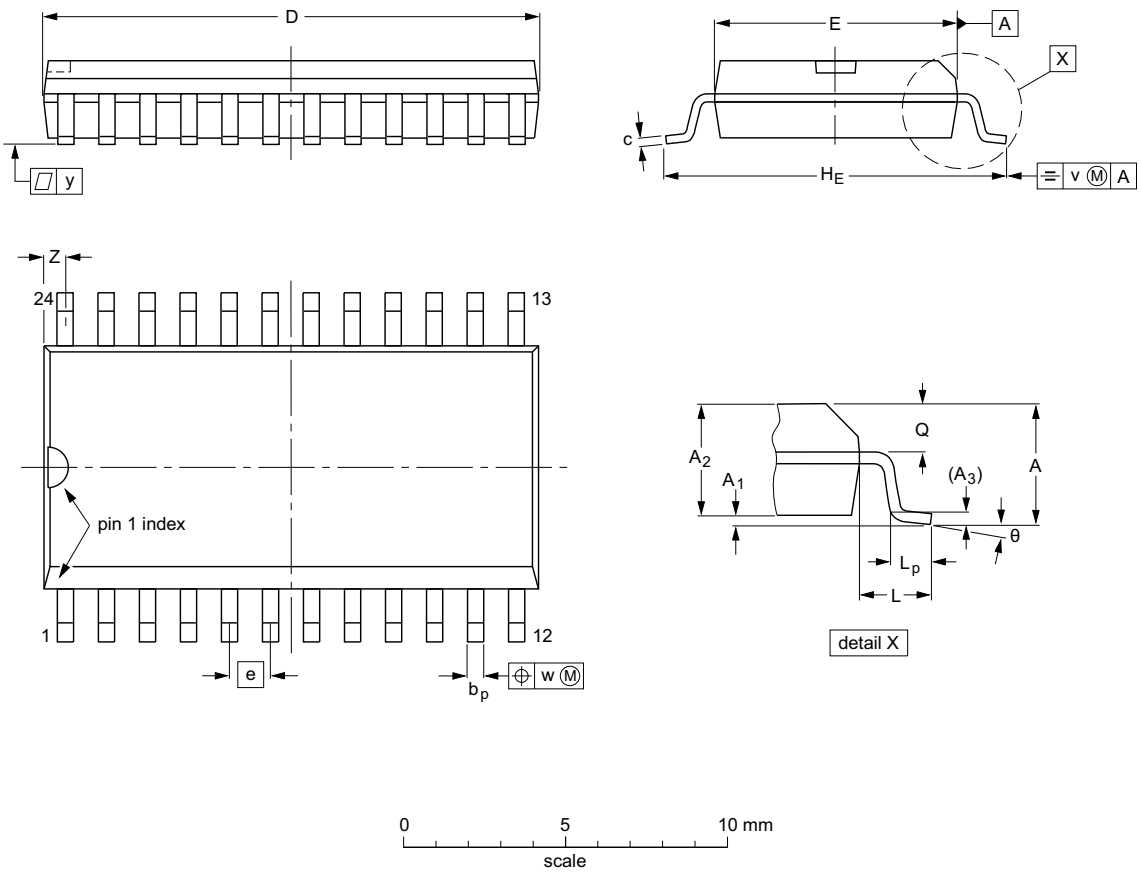



**Fig 17. I²C-bus timing diagram**

## 13. Package outline

**SO24: plastic small outline package; 24 leads; body width 7.5 mm** **SOT137-1**




**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

| UNIT | A max. | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | D (1) | E (1) | e | $H_E$ | L | $L_p$ | Q | v | w | y | Z (1) | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 2.65 | 0.3<br>0.1 | 2.45<br>2.25 | 0.25 | 0.49<br>0.36 | 0.32<br>0.23 | 15.6<br>15.2 | 7.6<br>7.4 | 1.27 | 10.65<br>10.00 | 1.4 | 1.1<br>0.4 | 1.1<br>1.0 | 0.25 | 0.25 | 0.1 | 0.9<br>0.4 | 8°<br>0° |
| inches | 0.1 | 0.012<br>0.004 | 0.096<br>0.089 | 0.01 | 0.019<br>0.014 | 0.013<br>0.009 | 0.61<br>0.60 | 0.30<br>0.29 | 0.05 | 0.419<br>0.394 | 0.055 | 0.043<br>0.016 | 0.043<br>0.039 | 0.01 | 0.01 | 0.004 | 0.035<br>0.016 | |

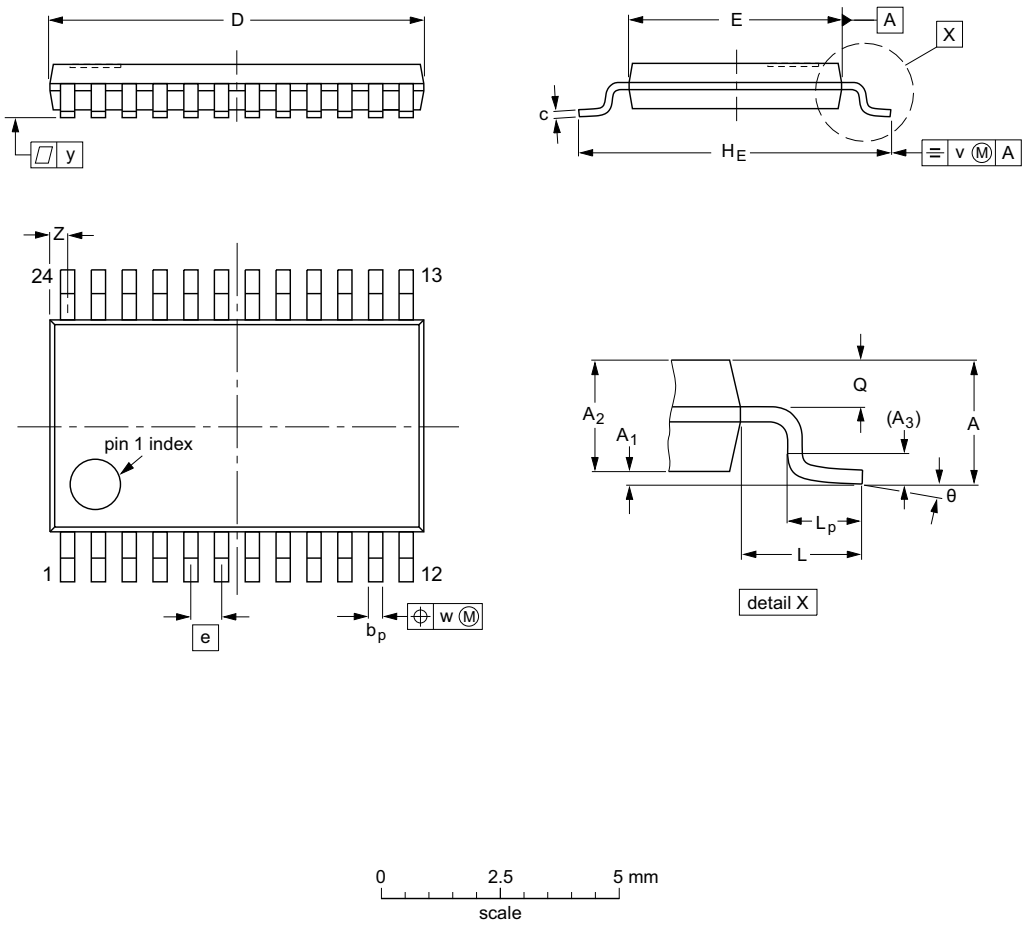
**Note**

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT137-1 | 075E05 | MS-013 | | | | ~~99-12-27~~<br>03-02-19 |

**Fig 18. Package outline SOT137-1 (SO24)**

**TSSOP24: plastic thin shrink small outline package; 24 leads; body width 4.4 mm** **SOT355-1**




**DIMENSIONS (mm are the original dimensions)**

| UNIT | A max. | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | $D^{(1)}$ | $E^{(2)}$ | e | $H_E$ | L | $L_p$ | Q | v | w | y | $Z^{(1)}$ | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1.1 | 0.15<br>0.05 | 0.95<br>0.80 | 0.25 | 0.30<br>0.19 | 0.2<br>0.1 | 7.9<br>7.7 | 4.5<br>4.3 | 0.65 | 6.6<br>6.2 | 1 | 0.75<br>0.50 | 0.4<br>0.3 | 0.2 | 0.13 | 0.1 | 0.5<br>0.2 | 8°<br>0° |

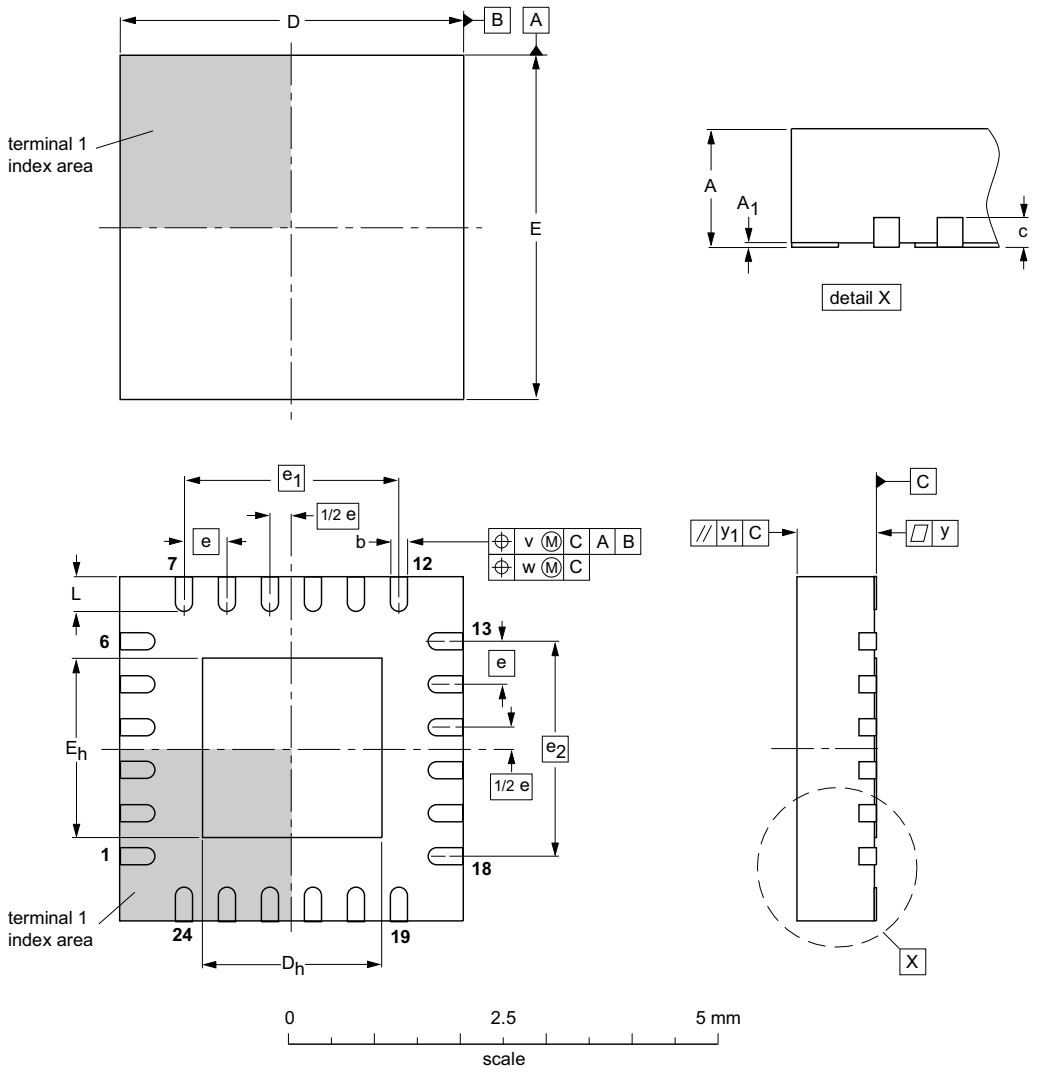
**Notes**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT355-1 | | MO-153 | | | | ~~99-12-27~~<br>03-02-19 |

**Fig 19. Package outline SOT355-1 (TSSOP24)**

**HVQFN24: plastic thermal enhanced very thin quad flat package; no leads; 24 terminals; body 4 x 4 x 0.85 mm** **SOT616-1**




**DIMENSIONS (mm are the original dimensions)**

| UNIT | A(1) max. | $A_1$ | b | c | D(1) | $D_h$ | E(1) | $E_h$ | e | $e_1$ | $e_2$ | L | v | w | y | $y_1$ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1 | 0.05<br>0.00 | 0.30<br>0.18 | 0.2 | 4.1<br>3.9 | 2.25<br>1.95 | 4.1<br>3.9 | 2.25<br>1.95 | 0.5 | 2.5 | 2.5 | 0.5<br>0.3 | 0.1 | 0.05 | 0.05 | 0.1 |

**Note**

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT616-1 | - - - | MO-220 | - - - | | | ~~01-08-08~~<br>02-10-22 |

**Fig 20. Package outline SOT616-1 (HVQFN24)**

# 14. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

## 14.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

## 14.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

## 14.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

## 14.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 21) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 10 and 11

**Table 10. SnPb eutectic process (from J-STD-020D)**

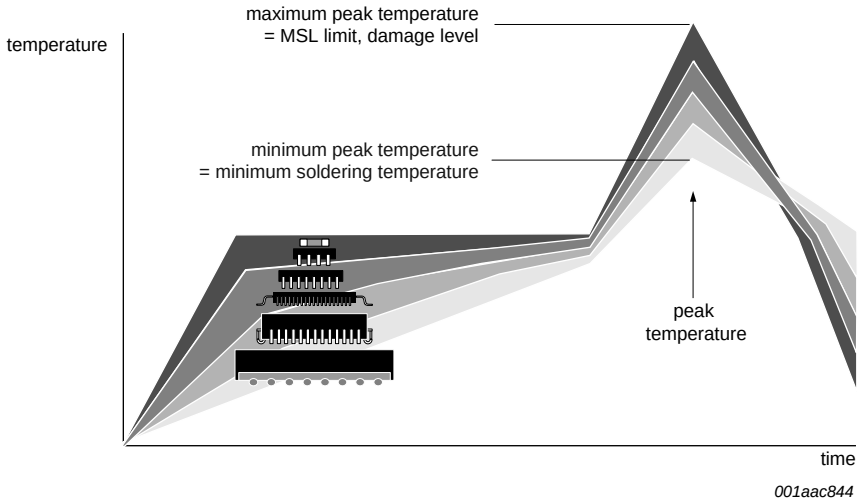
| Package thickness (mm) | Package reflow temperature (°C) | |
|---|---|---|
| | Volume (mm³) | |
| | < 350 | ≥ 350 |
| < 2.5 | 235 | 220 |
| ≥ 2.5 | 220 | 220 |

**Table 11. Lead-free process (from J-STD-020D)**

| Package thickness (mm) | Package reflow temperature (°C) | | |
|---|---|---|---|
| | Volume (mm³) | | |
| | < 350 | 350 to 2000 | > 2000 |
| < 1.6 | 260 | 260 | 260 |
| 1.6 to 2.5 | 260 | 250 | 245 |
| > 2.5 | 250 | 245 | 245 |

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 21.



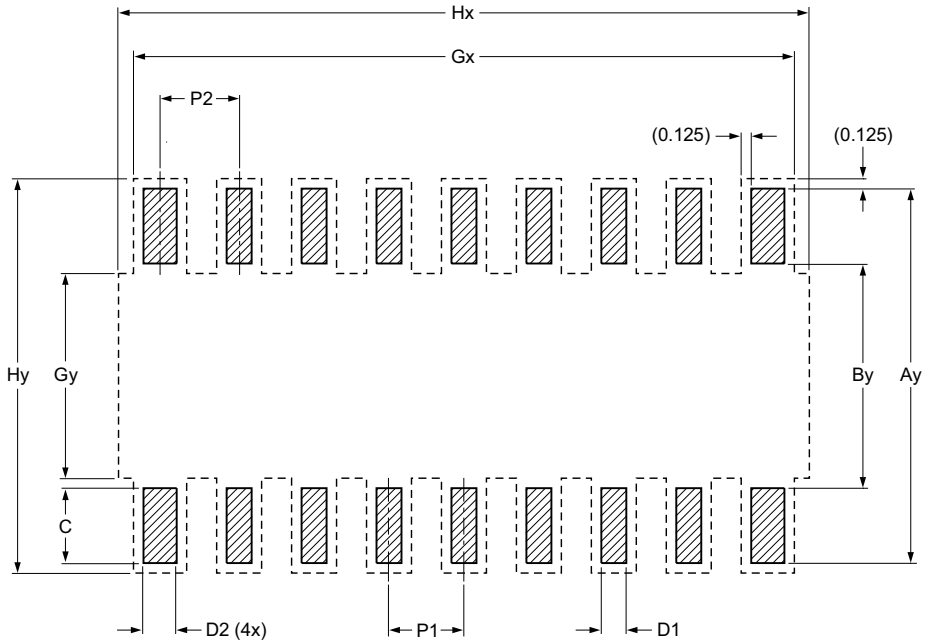

MSL: Moisture Sensitivity Level

**Fig 21. Temperature profiles for large and small components**

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

## 15. Soldering: PCB footprints

**Footprint information for reflow soldering of SO24 package** **SOT137-1**




Generic footprint pattern

Refer to the package outline drawing for actual layout

solder land

occupied area

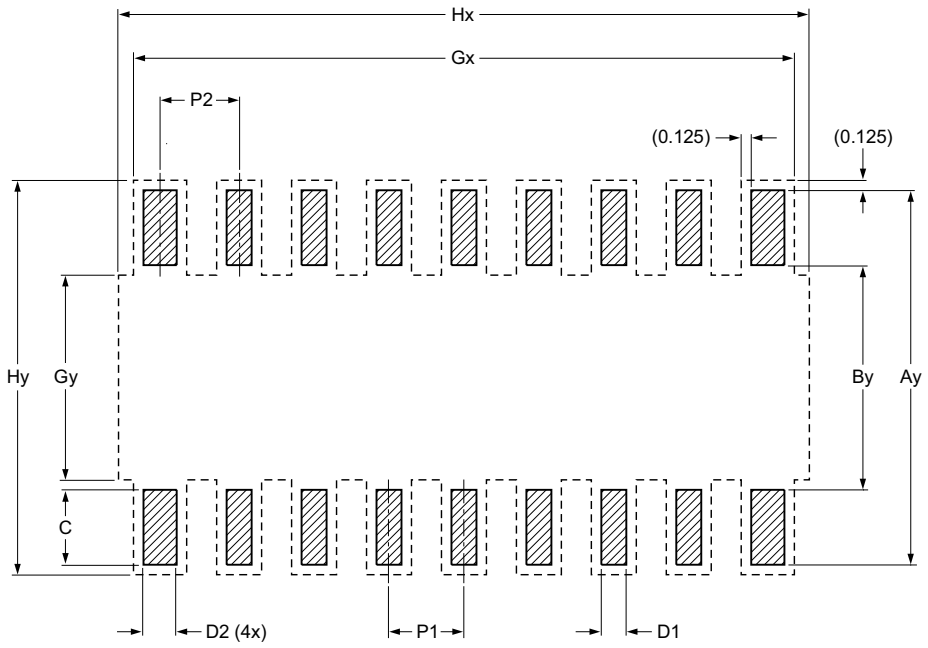
DIMENSIONS in mm

| P1 | P2 | Ay | By | C | D1 | D2 | Gx | Gy | Hx | Hy |
|---|---|---|---|---|---|---|---|---|---|---|
| 1.270 | 1.320 | 11.200 | 6.400 | 2.400 | 0.700 | 0.800 | 15.120 | 8.600 | 17.000 | 11.450 |

*sot137-1_fr*

**Fig 22. PCB footprint for SOT137-1 (SO24); reflow soldering**

**Footprint information for reflow soldering of TSSOP24 package** **SOT355-1**




Generic footprint pattern

Refer to the package outline drawing for actual layout

solder land

occupied area

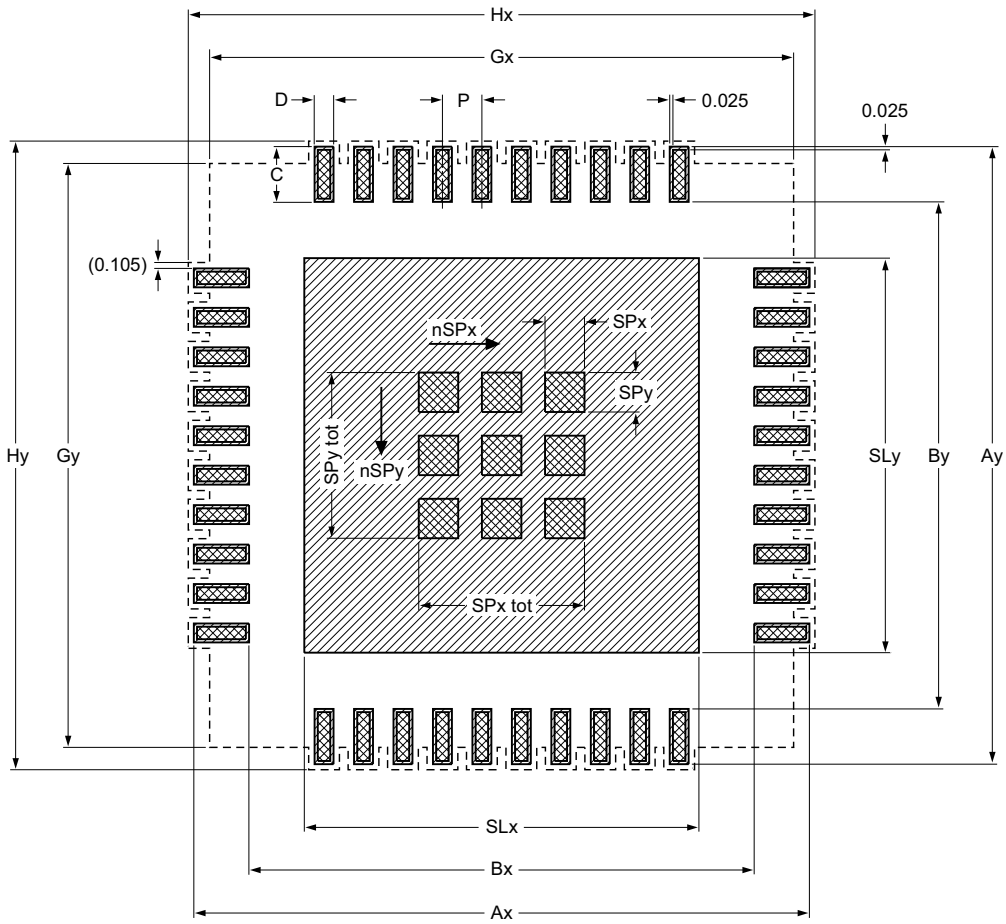
DIMENSIONS in mm

| P1 | P2 | Ay | By | C | D1 | D2 | Gx | Gy | Hx | Hy |
|---|---|---|---|---|---|---|---|---|---|---|
| 0.650 | 0.750 | 7.200 | 4.500 | 1.350 | 0.400 | 0.600 | 8.200 | 5.300 | 8.600 | 7.450 |

*sot355-1_fr*

**Fig 23. PCB footprint for SOT355-1 (TSSOP24); reflow soldering**

**Footprint information for reflow soldering of HVQFN24 package** **SOT616-1**




Generic footprint pattern

Refer to the package outline drawing for actual layout

solder land

solder paste deposit

solder land plus solder paste

occupied area

| nSPx | nSPy |
|---|---|
| 2 | 2 |

Dimensions in mm

| P | Ax | Ay | Bx | By | C | D | SLx | SLy | SPx tot | SPy tot | SPx | SPy | Gx | Gy | Hx | Hy |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0.500 | 5.000 | 5.000 | 3.200 | 3.200 | 0.900 | 0.240 | 2.100 | 2.100 | 1.200 | 1.200 | 0.450 | 0.450 | 4.300 | 4.300 | 5.250 | 5.250 |

Issue date ~~07-05-07~~ 09-06-15 *sot616-1_fr*

**Fig 24. PCB footprint for SOT616-1 (HVQFN24); reflow soldering**

## 16. Abbreviations

Table 12. Abbreviations

| Acronym | Description |
|---|---|
| CDM | Charged Device Model |
| ESD | ElectroStatic Discharge |
| HBM | Human Body Model |
| IC | Integrated Circuit |
| I²C-bus | Inter-Integrated Circuit bus |
| I/O | Input/Output |
| LSB | Least Significant Bit |
| MSB | Most Significant Bit |
| PCB | Printed-Circuit Board |
| POR | Power-On Reset |
| SMBus | System Management Bus |

## 17. Revision history

Table 13. Revision history

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|---|---|---|---|---|
| PCA9548A v.5.1 | 20151001 | Product data sheet | - | PCA9548A v.5 |
| Modifications: | • Section 6.2.1 “Control register definition”, first paragraph, third sentence: corrected from “The 2 LSBs of the control byte...” to “The contents of the control byte...”. | | | |
| PCA9548A v.5 | 20140331 | Product data sheet | - | PCA9548A v.4 |
| PCA9548A v.4 | 20130215 | Product data sheet | - | PCA9548A v.3 |
| PCA9548A v.3 | 20090707 | Product data sheet | - | PCA9548A v.2 |
| PCA9548A v.2 | 20060925 | Product data sheet | - | PCA9548A v.1 |
| PCA9548A v.1 | 20050415 | Product data sheet | - | - |

# 18. Legal information

## 18.1 Data sheet status

| Document status[1][2] | Product status[3] | Definition |
|---|---|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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## 20. Contents





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**Данный компонент на территории Российской Федерации**

**Вы можете приобрести в компании MosChip.**

Для оперативного оформления запроса Вам необходимо перейти по данной ссылке:

http://moschip.ru/get-element

Вы можете разместить у нас заказ для любого Вашего проекта, будь то серийное производство или разработка единичного прибора.

В нашем ассортименте представлены ведущие мировые производители активных и пассивных электронных компонентов.

Нашей специализацией является поставка электронной компонентной базы двойного назначения, продукции таких производителей как XILINX, Intel (ex.ALTERA), Vicor, Microchip, Texas Instruments, Analog Devices, Mini-Circuits, Amphenol, Glenair.

Сотрудничество с глобальными дистрибьюторами электронных компонентов, предоставляет возможность заказывать и получать с международных складов практически любой перечень компонентов в оптимальные для Вас сроки.

На всех этапах разработки и производства наши партнеры могут получить квалифицированную поддержку опытных инженеров.

Система менеджмента качества компании отвечает требованиям в соответствии с ГОСТ Р ИСО 9001, ГОСТ РВ 0015-002 и ЭС РД 009

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