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December 2010

### FDB14AN06LA0 F085

# N-Channel PowerTrench<sup>®</sup> MOSFET 60V, 60A, 14.6m $\Omega$

#### **Features**

- $r_{DS(ON)} = 12.8 \text{m}\Omega \text{ (Typ.)}, V_{GS} = 5 \text{V}, I_D = 60 \text{A}$
- $Q_q(tot) = 24nC$  (Typ.),  $V_{GS} = 5V$
- · Low Miller Charge
- Low Q<sub>RR</sub> Body Diode
- UIS Capability (Single Pulse and Repetitive Pulse)
- Qualified to AEC Q101
- · RoHS Compliant



#### **Applications**

- · Motor / Body Load Control
- · ABS Systems
- · Powertrain Management
- · Injection Systems
- DC-DC converters and Off-line UPS
- · Distributed Power Architectures and VRMs
- Primary Switch for 12V and 24V systems

Formerly developmental type 83557





### MOSFET Maximum Ratings $T_C = 25$ °C unless otherwise noted

Symbol	Parameter	Ratings	Units
V <sub>DSS</sub>	Drain to Source Voltage	60	V
V <sub>GS</sub>	Gate to Source Voltage	±20	V
	Drain Current	0.7	
	Continuous (T <sub>C</sub> = 25°C, V <sub>GS</sub> = 10V)	67	A
$I_D$	Continuous (T <sub>C</sub> = 25°C, V <sub>GS</sub> = 5V)	60	А
	Continuous ( $T_A = 25^{\circ}C$ , $V_{GS} = 5V$ , $R_{\theta JA} = 43^{\circ}C/W$ )	10	А
	Pulsed	Figure 4	А
E <sub>AS</sub>	Single Pulse Avalanche Energy (Note 1)	46	mJ
	Power dissipation	125	W
$P_{D}$	Derate above 25°C	0.83	W/°C
T <sub>J</sub> , T <sub>STG</sub>	Operating and Storage Temperature	-55 to 175	°C

#### **Thermal Characteristics**

$R_{\theta JC}$	Maximum Thermal Resistance Junction to Case TO-263	1.2	°C/W
$R_{\theta JA}$	Maximum Thermal Resistance Junction to Ambient TO-263, 1in <sup>2</sup>	43	°C/W
	copper pad area	43	

This product has been designed to meet the extreme test conditions and environment demanded by the automotive industry. For a copy of the requirements, see AEC Q101 at: http://www.aecouncil.com/

Reliability data can be found at: http://www.fairchildsemi.com/products/discrete/reliability/index.html.

All Fairchild Semiconductor products are manufactured, assembled and tested under ISO9000 and QS9000 quality systems certification.

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### **Package Marking and Ordering Information**

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDB14AN06LA0	FDB14AN06LA0_F085	TO-263AB	330mm	24mm	800 units

### **Electrical Characteristics** $T_C = 25^{\circ}C$ unless otherwise noted

Parameter	Test Co	onditions	Min	Тур	Max	Units
acteristics						
Drain to Source Breakdown Voltage	$I_D = 250 \mu A, V_C$	3S = 0V	60	-	-	V
Zoro Coto Voltago Drain Current	V <sub>DS</sub> = 50V		-	-	1	^
Zero Gate Voltage Drain Current	$V_{GS} = 0V$	$T_{\rm C} = 150^{\rm o}{\rm C}$	-	-	250	μΑ
Gate to Source Leakage Current	$V_{GS} = \pm 20V$		-	-	±100	nA
	acteristics  Drain to Source Breakdown Voltage  Zero Gate Voltage Drain Current	Drain to Source Breakdown Voltage $I_D = 250\mu A$ , $V_C$ Zero Gate Voltage Drain Current $V_{DS} = 50V$ $V_{GS} = 0V$	Drain to Source Breakdown Voltage $I_D = 250\mu$ A, $V_{GS} = 0$ V         Zero Gate Voltage Drain Current $V_{DS} = 50$ V $V_{GS} = 0$ V $V_{CS} = 150$ °C	Drain to Source Breakdown Voltage $I_D = 250\mu A$ , $V_{GS} = 0V$ 60         Zero Gate Voltage Drain Current $V_{DS} = 50V$ - $V_{GS} = 0V$ $V_{CS} = 150^{\circ}C$ -	acteristics    Drain to Source Breakdown Voltage   I <sub>D</sub> = 250μA, V <sub>GS</sub> = 0V   60   -     Zero Gate Voltage Drain Current   V <sub>DS</sub> = 50V   -   -     V <sub>GS</sub> = 0V   T <sub>C</sub> = 150°C   -	

#### **On Characteristics**

V <sub>GS(TH)</sub>	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$ , $I_D = 250 \mu A$	1	-	3	V
		I <sub>D</sub> = 67A, V <sub>GS</sub> = 10V	-	0.0102	0.0116	
r <sub>DS(ON)</sub>	Drain to Source On Resistance	I <sub>D</sub> = 60A, V <sub>GS</sub> = 5V	-	0.0128	0.0146	0
		$I_D = 60A, V_{GS} = 5V,$ $T_J = 175^{\circ}C$	-	0.028	0.033	32

#### **Dynamic Characteristics**

C <sub>ISS</sub>	Input Capacitance	V - 25V V - 0V		-	2900	-	pF
Coss	Output Capacitance	$V_{DS} = 25V, V_{GS} = 1MH_{7}$	$V_{DS} = 25V, V_{GS} = 0V,$ f = 1MHz		270	-	pF
C <sub>RSS</sub>	Reverse Transfer Capacitance	1 - 11VII 12		-	115	-	pF
$Q_{g(TOT)}$	Total Gate Charge at 5V	$V_{GS} = 0V \text{ to } 5V$			24	31	nC
$Q_{g(TH)}$	Threshold Gate Charge	$V_{GS} = 0V \text{ to } 1V$	V <sub>DD</sub> = 30V	-	3.0	3.9	nC
$Q_{gs}$	Gate to Source Gate Charge		I <sub>D</sub> = 60A	-	12	-	nC
Q <sub>gs2</sub>	Gate Charge Threshold to Plateau	1	$I_g = 1.0 \text{mA}$	-	9.1	-	nC
$Q_{gd}$	Gate to Drain "Miller" Charge			-	7.9	-	nC

#### **Switching Characteristics** (V<sub>GS</sub> = 5V)

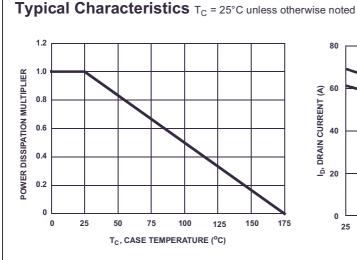
t <sub>ON</sub>	Turn-On Time	$V_{DD} = 30V, I_{D} = 60A$ $V_{GS} = 5V, R_{GS} = 5.1\Omega$	-	-	276	ns
t <sub>d(ON)</sub>	Turn-On Delay Time		-	15	-	ns
t <sub>r</sub>	Rise Time		-	169	-	ns
t <sub>d(OFF)</sub>	Turn-Off Delay Time		-	24	-	ns
t <sub>f</sub>	Fall Time		-	50	-	ns
t <sub>OFF</sub>	Turn-Off Time		-	-	109	ns

#### **Drain-Source Diode Characteristics**

$V_{SD}$	Source to Drain Diode Voltage	I <sub>SD</sub> = 60A	-	-	1.25	V
	Source to Drain blode voltage	I <sub>SD</sub> = 30A	-	-	1.0	V
t <sub>rr</sub>	Reverse Recovery Time	$I_{SD} = 60A$ , $dI_{SD}/dt = 100A/\mu s$	-	-	33	ns
Q <sub>RR</sub>	Reverse Recovered Charge	$I_{SD} = 60A$ , $dI_{SD}/dt = 100A/\mu s$	-	-	29	nC

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**Notes:** 1: Starting  $T_J = 25^{\circ}C$ ,  $L = 40\mu H$ ,  $I_{AS} = 48A$ .



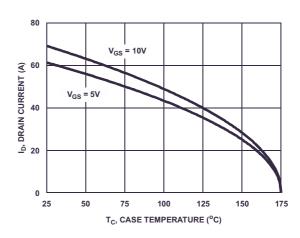


Figure 1. Normalized Power Dissipation vs
Ambient Temperature

Figure 2. Maximum Continuous Drain Current vs Case Temperature

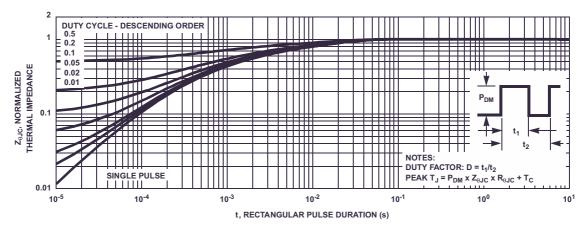


Figure 3. Normalized Maximum Transient Thermal Impedance

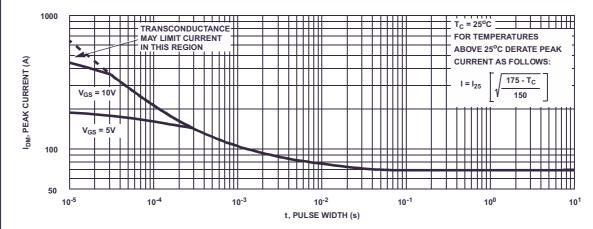


Figure 4. Peak Current Capability

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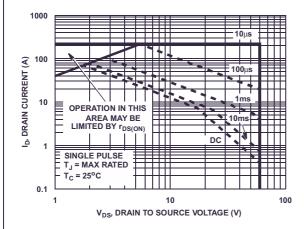
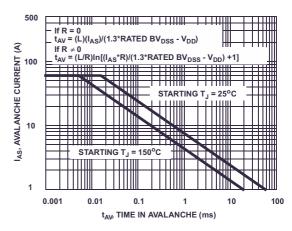


Figure 5. Forward Bias Safe Operating Area



NOTE: Refer to Fairchild Application Notes AN7514 and AN7515

Figure 6. Unclamped Inductive Switching

Capability

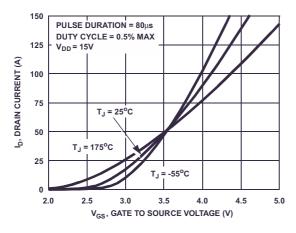


Figure 7. Transfer Characteristics

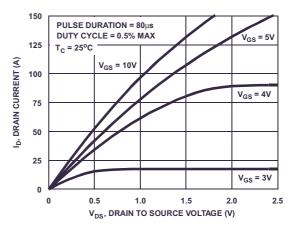


Figure 8. Saturation Characteristics

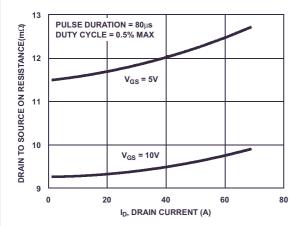


Figure 9. Drain to Source On Resistance vs Drain Current

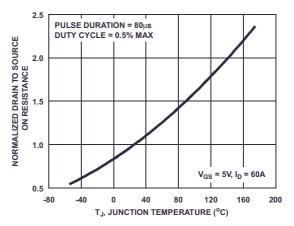


Figure 10. Normalized Drain to Source On Resistance vs Junction Temperature

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### Typical Characteristics T<sub>C</sub> = 25°C unless otherwise noted

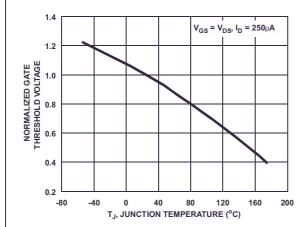


Figure 11. Normalized Gate Threshold Voltage vs Junction Temperature

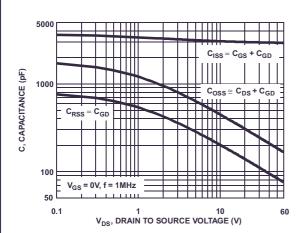


Figure 13. Capacitance vs Drain to Source Voltage

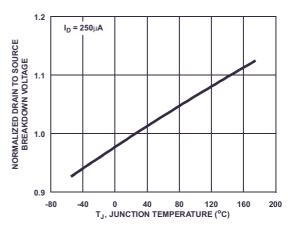


Figure 12. Normalized Drain to Source Breakdown Voltage vs Junction Temperature

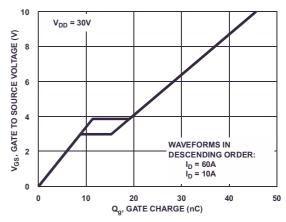


Figure 14. Gate Charge Waveforms for Constant Gate Currents

#### **Test Circuits and Waveforms**

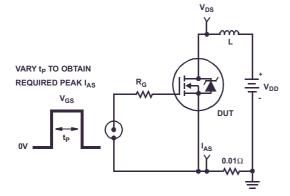


Figure 15. Unclamped Energy Test Circuit

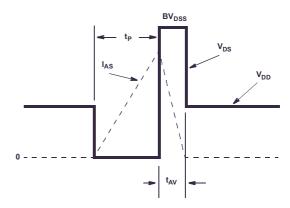


Figure 16. Unclamped Energy Waveforms

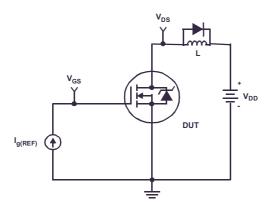


Figure 17. Gate Charge Test Circuit

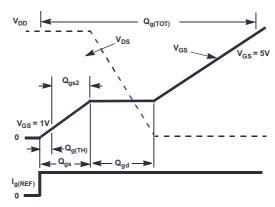


Figure 18. Gate Charge Waveforms

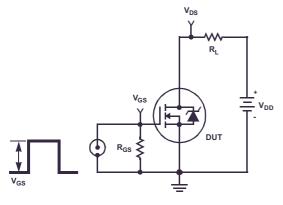


Figure 19. Switching Time Test Circuit

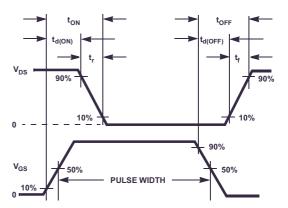


Figure 20. Switching Time Waveforms

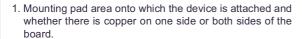
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#### Thermal Resistance vs. Mounting Pad Area

The maximum rated junction temperature,  $T_{JM}$ , and the thermal resistance of the heat dissipating path determines the maximum allowable device power dissipation,  $P_{DM}$ , in an application. Therefore the application's ambient temperature,  $T_A$  (°C), and thermal resistance  $R_{\theta JA}$  (°C/W) must be reviewed to ensure that  $T_{JM}$  is never exceeded. Equation 1 mathematically represents the relationship and serves as the basis for establishing the rating of the part.

$$P_{DM} = \frac{(T_{JM} - T_A)}{R_{\theta JA}} \tag{EQ. 1}$$

In using surface mount devices such as the TO-263 package, the environment in which it is applied will have a significant influence on the part's current and maximum power dissipation ratings. Precise determination of  $\mathsf{P}_{\mathsf{DM}}$  is complex and influenced by many factors:



- The number of copper layers and the thickness of the board.
- 3. The use of external heat sinks.
- 4. The use of thermal vias.
- 5. Air flow and board orientation.
- For non steady state applications, the pulse width, the duty cycle and the transient thermal response of the part, the board and the environment they are in.

Fairchild provides thermal information to assist the designer's preliminary application evaluation. Figure 21 defines the  $R_{\theta JA}$  for the device as a function of the top copper (component side) area. This is for a horizontally positioned FR-4 board with 1oz copper after 1000 seconds of steady state power with no air flow. This graph provides the necessary information for calculation of the steady state junction temperature or power dissipation. Pulse applications can be evaluated using the Fairchild device Spice thermal model or manually utilizing the normalized maximum transient thermal impedance curve.

Thermal resistances corresponding to other copper areas can be obtained from Figure 21 or by calculation using Equation 2 or 3. Equation 2 is used for copper area defined in inches square and equation 3 is for area in centimeters square. The area, in square inches or square centimeters is the top copper area including the gate and source pads.

$$R_{\theta JA} = 26.51 + \frac{19.84}{(0.262 + Area)}$$
 (EQ. 2)

Area in Inches Squared

$$R_{\theta JA} = 26.51 + \frac{128}{(1.69 + Area)}$$
 (EQ. 3)

Area in Centimeters Squared

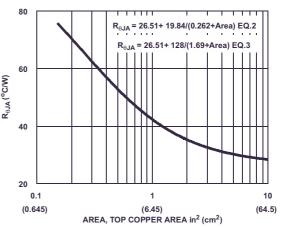
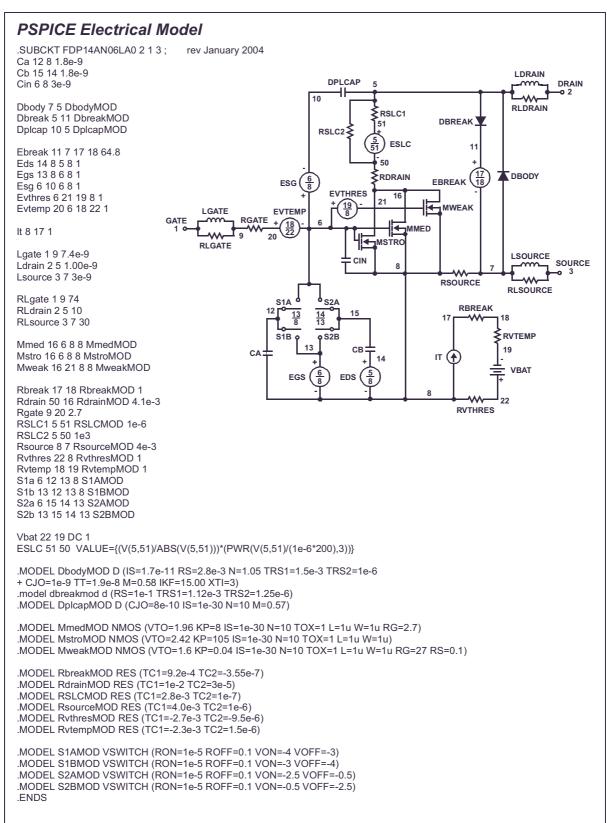


Figure 21. Thermal Resistance vs Mounting Pad Area

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Wheatley.

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Note: For further discussion of the PSPICE model, consult **A New PSPICE Sub-Circuit for the Power MOSFET Featuring Global Temperature Options**; IEEE Power Electronics Specialist Conference Records, 1991, written by William J. Hepp and C. Frank

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SABER Electrical Model
REV January 2004
template FDP14AN06LA0 n2,n1,n3
electrical n2,n1,n3
var i iscl
dp..model\ dbodymod=\ (isl=1.7e-11,rs=2.8e-3,nl=1.05,trs1=1.5e-3,trs2=1e-6,cjo=1e-9,tt=1.9e-8,m=0.58,ikf=15.00,xti=3)
dp..model dbreakmod = (rs=1e-1,trs1=1.12e-3,trs2=1.25e-6)
dp..model dplcapmod = (cjo=8e-10,isl=10e-30,nl=10,m=0.57)
m..model mmedmod = (type=_n,vto=1.96,kp=8,is=1e-30, tox=1)
m..model mstrongmod = (type=_n,vto=2.42,kp=105,is=1e-30, tox=1)
m..model mweakmod = (type=_n,vto=1.6,kp=0.04,is=1e-30, tox=1,rs=0.1)
                                                                                                           LDRAIN
sw_vcsp..model s1amod = (ron=1e-5,roff=0.1,von=-4,voff=-3)
                                                                                                                    DRAIN
sw_vcsp..model s1bmod = (ron=1e-5,roff=0.1,von=-3,voff=-4)
sw_vcsp..model s2amod = (ron=1e-5,roff=0.1,von=-2.5,voff=-0.5)
                                                                 10
                                                                                                          RLDRAIN
sw_vcsp..model s2bmod = (ron=1e-5,roff=0.1,von=-0.5,voff=-2.5)
                                                                             ≷RSLC1
c.ca n12 n8 = 1.8e-9
                                                                  RSLC2 ₹
c.cb n15 n14 = 1.8e-9
c.cin n6 n8 = 3e-9
                                                                                ISCL
                                                                                          DBREAK
                                                                               50
dp.dbody n7 n5 = model=dbodymod
                                                                               RDRAIN
                                                               8
dp.dbreak n5 n11 = model=dbreakmod
                                                          FSG
                                                                                                         DBODY
dp.dplcap n10 n5 = model=dplcapmod
                                                                    EVTHRES
                                                                       19
8
spe.ebreak n11 n7 n17 n18 = 64.8 <sub>GATE</sub>
                                                          (18)
22)
                                                                                            FRREAM
spe.eds n14 n8 n5 n8 = 1
                                                                                     MMED
spe.eqs n13 n8 n6 n8 = 1
                                         RLGATE
spe.esa n6 n10 n6 n8 = 1
                                                                                                          LSOURCE
                                                                         CIN
spe.evthres n6 n21 n19 n8 = 1
                                                                                                                   SOURCE
spe.evtemp n20 n6 n18 n22 = 1
                                                                                         RSOURCE
                                                                                                         RLSOURCE
i.it n8 n17 = 1
                                                                                               RBREAK
                                                                                            17
I.lgate n1 n9 = 7.4e-9
                                                                                                        18
I.ldrain n2 n5 = 1.00e-9
                                                                                                       ≨RVTFMP
I.Isource n3 n7 = 3e-9
                                                                                                         19
                                                                                          IT
                                                                              14
res.rlgate n1 n9 = 74
                                                                                                          VBAT
res.rldrain n2 n5 = 10
res.rlsource n3 n7 = 30
                                                                                               RVTHRES
m.mmed n16 n6 n8 n8 = model=mmedmod, I=1u, w=1u
m.mstrong n16 n6 n8 n8 = model=mstrongmod, l=1u, w=1u
m.mweak n16 n21 n8 n8 = model=mweakmod, l=1u, w=1u
res.rbreak n17 n18 = 1, tc1=9.2e-4,tc2=-3.5e-7
res.rdrain n50 n16 = 4.1e-3, tc1=1e-2,tc2=3e-5
res.rgate n9 n20 = 2.7
res.rslc1 n5 n51 = 1e-6, tc1=2.8e-3,tc2=1e-7
res.rslc2 n5 n50 = 1e3
res.rsource n8 n7 = 4e-3, tc1=4.0e-3,tc2=1e-6
res.rvthres n22 n8 = 1, tc1=-2.7e-3,tc2=-9.5e-6
res.rvtemp n18 n19 = 1, tc1=-2.3e-3,tc2=1.5e-6
sw_vcsp.s1a n6 n12 n13 n8 = model=s1amod
sw vcsp.s1b n13 n12 n13 n8 = model=s1bmod
sw_vcsp.s2a n6 n15 n14 n13 = model=s2amod
sw_vcsp.s2b n13 n15 n14 n13 = model=s2bmod
v.vbat n22 n19 = dc=1
equations {
iscl: v(n51,n50) = ((v(n5,n51)/(1e-9+abs(v(n5,n51))))*((abs(v(n5,n51)*1e6/200))**3))
```

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#### SPICE Thermal Model

REV January 2004 FDP14AN06LA0T

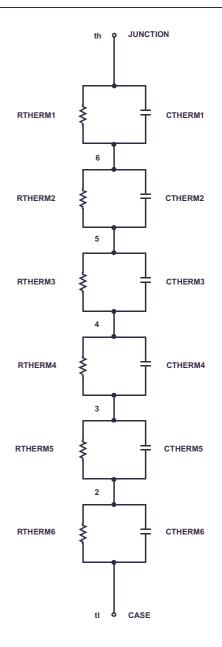
CTHERM1 TH 6 2.5e-3 CTHERM2 6 5 3e-3 CTHERM3 5 4 4e-3 CTHERM4 4 3 7e-3 CTHERM5 3 2 8.2e-3 CTHERM6 2 TL 5e-2

RTHERM1 TH 6 4.2e-2 RTHERM2 6 5 8.4e-2 RTHERM3 5 4 1.04e-1 RTHERM4 4 3 1.14e-1 RTHERM5 3 2 2.74e-1 RTHERM6 2 TL 3.44e-1

#### SABER Thermal Model

SABER thermal model FDP14AN06LA0T template thermal\_model th tI thermal\_c th, tI  $\{$  ctherm.ctherm1 th 6 =2.5e-3 ctherm.ctherm2 6 5 =3e-3 ctherm.ctherm3 5 4 =4e-3 ctherm.ctherm4 4 3 =7e-3 ctherm.ctherm5 3 2 =8.2e-3 ctherm.ctherm6 2 tI =5e-2  $\{$  therm.rtherm1 th 6 =4.2e-2  $\{$  therm.rtherm2 6 5 =8.4e-2  $\{$  therm.rtherm3 5 4 =1.04e-1

rtherm.rtherm4 4 3 =1.14e-1 rtherm.rtherm5 3 2 =2.74e-1 rtherm.rtherm6 2 tl =3.44e-1



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